General-Purpose I/O Board: Make the Connection

There are times when I've wanted to connect a simple LED (light-emitting diode) display to my TRS-80, or to interface a TTL (transistor-to-transistor logic) device to it. Some readers have also asked for a general-purpose input/output (I/O) board that interfaces with CMOS devices. I decided to kill two birds with one stone in this month's column by building a board you can use for either application.

The board's main component is an 8255A parallel peripheral interface (PPI), with an 8253/8254 programmable interval timer (PIT) also included (see the Photo). You can use the MOS versions of these components (available from Intel and other manufacturers) or you can use the new CMOS versions available from Harris and OKI Semiconductor (see the addresses at the end of this column).

In addition to a connecting cable for your TRS-80, you'll need one for I/O. The 50-pin socket connector I use has 16 general-purpose I/O lines, as well as counter inputs and outputs. It also provides a seven-segment display to display the digits from zero through nine. I'll describe the features and operation of the entire board in more detail later.

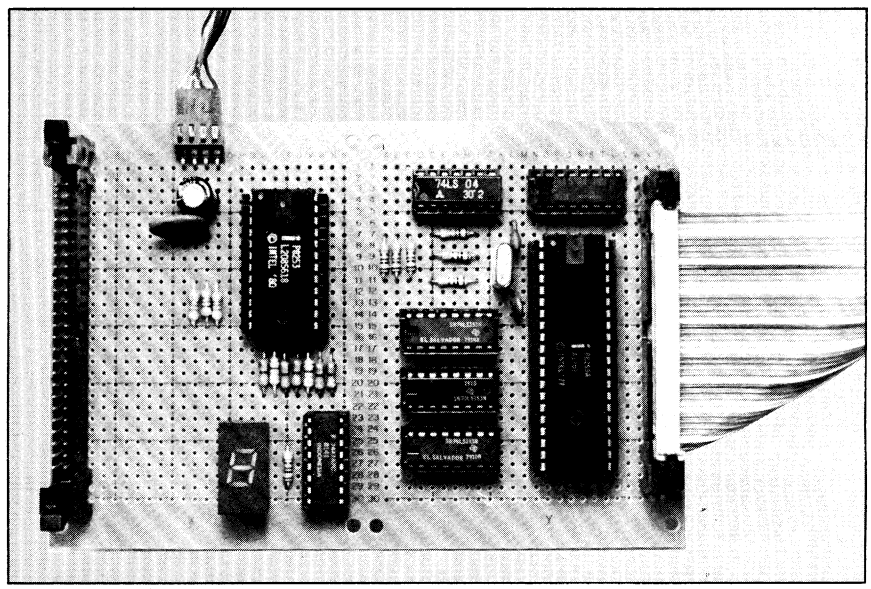

Photo. Completed input/output board.

CMOS versus TTL

CMOS is the up-and-coming logic family because it offers low power and fast speeds. The new high-speed CMOS logic family—the 74HC00 series—offers performance matching that of low-power Schottky (74LS00 series), with a fraction of the power consumption. Other CMOS advantages include excellent noise immunity, high immunity to alpha particle attack, wider possible supply voltages, reduced system cooling requirements, reduced IC packaging requirements, and lower busing and regulating requirements.

While CMOS chips have many uses, you can't easily connect them with TTL devices. CMOS outputs tend to stay close to the power supply "rails" (ground and +5V in most systems). The guaranteed minimum high-level output voltage for a typical CMOS IC is generally within 1 percent of the supply voltage, here at least 4.95V using a +5V supply. Likewise, the guaranteed maximum low-level output voltage is 0.05V when using a +5V supply.

The outputs of TTL devices do not stay so close to the power rails. The minimum high-level output voltage for a TTL device is generally specified at 2.4V, while the maximum low-level output voltage is 0.4V.

The input voltage requirements for CMOS devices are generally within 20 percent of the supply voltage for each rail. Using a +5V power supply, the minimum high-level input voltage is 4V, while the maximum low-level input voltage is 1V. Comparatively, the minimum high-level input voltage requirement for TTL devices is 2V, while the maximum low-level input voltage is 0.8V.

You can see by looking at the specs that CMOS outputs can drive TTL inputs, since the guaranteed output voltage falls within the requirements of the TTL inputs. Also, TTL low-level outputs can drive CMOS inputs, since the TTL output (0.4V maximum) is lower than the CMOS input requirement of 0.8V. A problem arises, however, when you try to drive a CMOS input with a high-level TTL output. The minimum guaranteed high-level TTL output voltage of 2.4V doesn't meet

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the minimum 4.0V input requirement of the CMOS device.

You can overcome this in several ways. A simple pull-up resistor on the TTL output will raise the voltage enough to accommodate the CMOS device. Or, a number of converter chips are available that convert TTL to CMOS levels (and back when you use other than +5V on the CMOS device). A third alternative is to use CMOS devices that accept TTL-level inputs. The new 74HCT00 family does this, as well as the CMOS chips I will consider shortly (the 82C53, 82C54, and 82C55A). The TTL interface on these chips is identical to that of the TRS-80 MOS-equivalent devices, the 8255A and the 8254 (or 8253).

The TTL-level interface isn't without a trade-off, however. The reduced input requirements also reduce the devices' noise immunity.

A Look at the 8255A (82C55A) PPI

The 8255A parallel peripheral interface requires four locations in I/O addressing space: one for the control register and one for each of three I/O ports (ports A, B, and C). The control register is write-only, while the other three registers are read/write. The read/write registers have slightly different functions depending on the 8255A's operating mode.

The 8255A has two primary ports, A and B. They're 8-bit ports, and the 8 bits of either port are all inputs or all outputs; you can't assign the input/output configuration on a bit-by-bit basis as with some other I/O chips.

A third 8-bit port, port C, is actually two half-size (4-bit) ports. When you're in the Basic I/O mode (described below), you can set the directions of the upper and lower halves of port C independently. When you're in any other mode, most of the bits take on special handshaking functions, leaving only a couple of bits left for I/O purposes. The general structure of the 8255A is shown in Fig. 1.

The 8255A has three operating modes: Basic I/O (mode zero), strobed I/O (mode 1), and bidirectional bus (mode 2). Each is useful for different types of applications.

Mode zero is probably the 8255A's most commonly used mode. It provides 24 I/O lines as basic input or output lines, and it's useful to turn devices on or off, configure them, or read their status.

When either port A or port B (or both) is programmed as an output, the port internally latches the binary value written to it and it goes to that port's eight output lines.

Port C is slightly different in that you can individually program each half (4 bits) as input or output. If you write to Port C, it internally latches all of the bits (if any) pertaining to output lines, and the values go to the respective output lines. You can also read back bits written to ports configured as outputs.

Port C has another feature unavailable with port A or B: By sending a special command byte to the 8255A command register, you can set or clear any of the output bits individually (without affecting any of the other bits).

When you configure any of the above ports (or half-ports) as inputs, the computer gets the current bit values simply by reading the respective port. The bits aren't latched in the 8255A, so the computer reads only the current state of the bits.

Mode 1 (strobed input/output) uses several port C lines for handshaking and interrupt functions, leaving only two lines free for general-purpose I/O. I used this mode in my printer buffer project (September and October, p. 102 and p. 146), and it's useful for transferring information between two devices.

Data input to the 8255A is latched internally using the handshaking lines and can optionally cause an interrupt to the processor to occur. Likewise, output data to another device is latched, with the appropriate handshaking taking place. The 8255A can optionally interrupt the processor when the remote device accepts the output value.

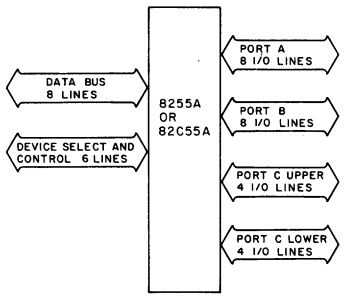

Figure 1. General structure of the 8255A/PPI.

The 8255A lets you select the modes for ports A and B separately. If port A is in mode 1, for example, you could put port B in mode zero, but you'd lose the respective port C handshaking signals.

Which port C lines are available for basic I/O depends on the direction you choose for port A. If port A is an output, PC4 and PC5 will be free. If port A is an input, PC6 and PC7 will be free. In either case, you can assign the free port C pins as both inputs or both outputs. (The printer buffer project has a timing diagram showing the mode 1 timing.)

Mode 2 (bidirectional bus) is permitted for port A only, and also uses several port C bits for handshaking (PC3–PC7). You use this mode to communicate with another device over a common 8-bit bus. Using the handshaking lines, two devices can send information back and forth, with the bus direction changing as needed. Like mode 1, interrupt lines are available, which you can use to notify the processor of certain communication conditions.

When port A is in mode 2, you can specify port B as mode zero or mode 1. When specified as mode zero, you can use port C bits 0–2 as basic I/O lines (all inputs or all outputs). When specified as mode 1, you can use PC0–PC2 as handshaking lines for port B.

Configuring the 8255A

Figure 2 shows the mode control-word format. You must set the high-order bit (bit 7) to indicate a mode set-up; otherwise, a port C bit set/reset function takes place.

Bits 5 and 6 select the mode—zero, 1, or 2—for port A. Bit 4 determines the direction of port A (1 = input, 0 = output). Bit 3 determines the direction for the upper half of port C (or the free port C bits when in mode 1). Bit 2 selects the mode—zero or 1—for port B. Bit 1 selects the direction of port B, and bit zero selects the direction of the lower half of port C (or the lower 3 bits when in mode 2). For more information on the operation of the 8255A, see the manufacturer's data book (see the reference list at the end of this column).

The 8253/8254 (82C53/82C54) PIT

The 8254 programmable interval timer is essentially an improved 8253, providing higher clock speeds and status register read-back. You may notice in the photograph that I used the 8253 instead of the improved 8254. That's because I had several 8253s on hand and didn't need the 8254's extra features.

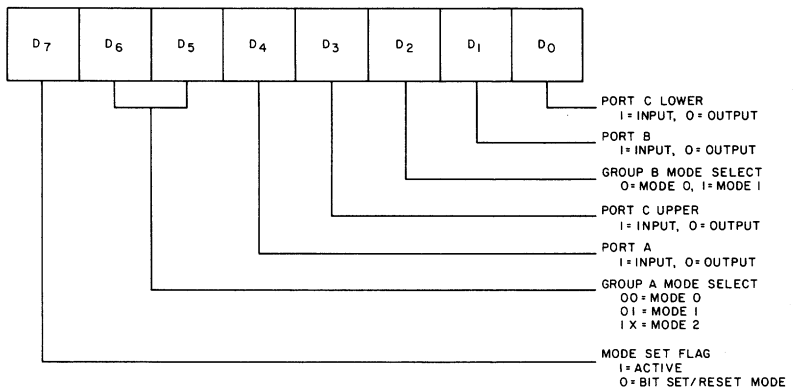

Figure 2. 8255A control word format.

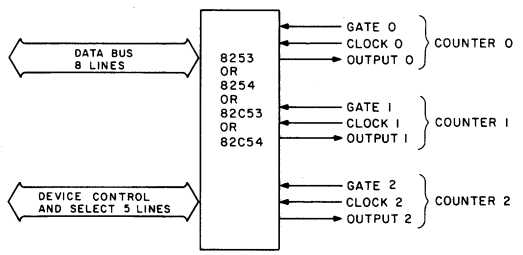

Figure 3. Basic structure of 8253/8254.

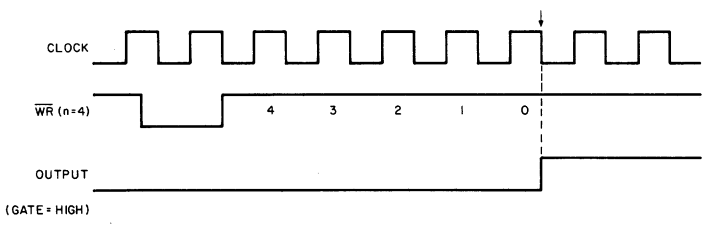

Figure 4. 8254 mode zero timing example.

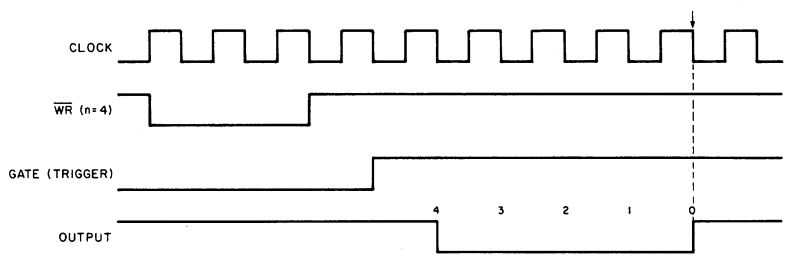

Figure 5. 8254 mode 1 timing example.

Like the 8255A, the 8254 requires four locations in the Z80's I/O addressing space: one for the control register and one for each of the three 16-bit counters on the chip. Unlike the 8253, the 8254 has a control register to and from which you can both write and read.

The 8253's control register is write-only. The 8254's read-back feature gives the processor status information about the chip that would otherwise be unavailable or, at least, would require additional external hardware. The three counter registers are read/write registers, although they should latch time values before reading (as described below).

As mentioned, the 8254 has three 16-bit counter/timers. These are countdown counters: They count down from an initial value and perform a particular operation when they reach zero. Their operation varies depending on the mode you're in. Each counter has an associated clock input, gate input (for on/off control), and output.

The basic structure of the 8254 is shown in Fig. 3. It has six possible operation modes, and you can set each counter individually to operate in any of them. The modes are interrupt on terminal count (mode zero), hardware retriggerable one-shot (mode 1), rate generator (mode 2), square wave (mode 3), software-triggered strobe (mode 4), and hardware-triggered strobe (mode 5).

In mode zero (interrupt on terminal count), the counter goes low when you initially write the count value to it. The chip then decrements the count value for each pulse of the clock input to the counter, as long as the gate signal is high. Counting doesn't take place when the gate is low. When the count value reaches zero, the output goes high. You could use the high output to interrupt the processor or to trigger an external event. A timing diagram for mode zero is shown in Fig. 4.

In mode 1 (hardware retriggerable one-shot), the output initially goes high when you set the mode. When the chip receives a trigger pulse on the gate input, the count value is put into the counter and the output goes low on the next clock pulse. The output then remains low until the counter reaches zero. At that time, the output returns high and the counter waits for another trigger pulse, which makes it restart

the process. The gate signal doesn't affect the counter output in this mode. Figure 5 shows a sample timing diagram for mode 1 operation.

Mode 2 (a programmable rate generator) is a divide-by-N counter. The chip divides the input clock frequency by the count value sent to the counter, with the output pulsing at the divided frequency. The output goes low for one clock period, then high again. The gate input must be high to enable counting. This mode is often used to generate a periodic interrupt or timing for a regular, periodic event. A sample timing diagram for mode 2 operation is shown in Fig. 6.

Mode 3 (square wave mode) is typically used for baud-rate generation. Unlike mode 2, the output changes (toggles) at each half-count of the counter. For example, if the count value is 100, the output goes high for 50 counts, then low for 50 counts. If the count value is odd, the output goes high for one count longer than it is low. The gate input must be high for counting to take place. Figure 7 shows a sample mode 3 timing diagram.

In mode 4 (software triggered strobe), the chip's output initially goes high when it loads the counter. When the counter reaches zero, the output goes low for one clock cycle, then goes high again. To retrigger the counter, you must write a new count value to it. Counting is enabled only when the gate goes high, but the gate has no effect on the output. Figure 8 shows a sample timing diagram for mode 4 operation.

Mode 5 is similar to mode 4, except that the rising edge of the gate input triggers the counting, instead of a software write of the count value. When the count value reaches zero, the output goes low for one clock cycle, then returns high, awaiting another gate trigger. Thus the counter is retriggerable. If the gate input has another rising edge, the chip automatically loads the initial count value into the counter on the next clock, thereby starting the countdown all over. A sample timing diagram for mode 5 is shown in Fig. 9.

Configuring and Operating The 8253/8254

The control-word format for the 8254 is shown in Fig. 10. The high-order 2 bits (bits 6 and 7) specify which of the three counter/timers you're set-

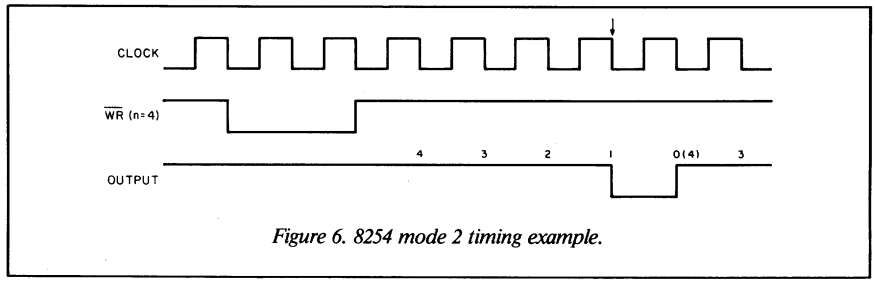

Figure 6. 8254 mode 2 timing example.

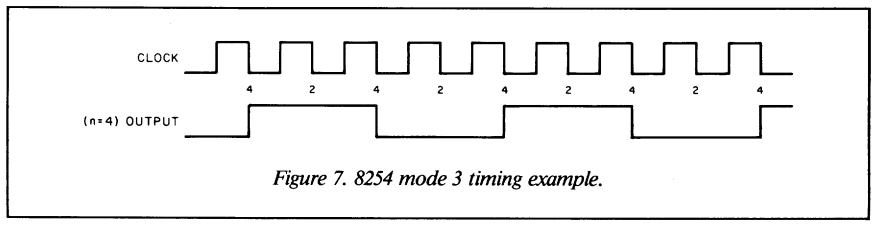

Figure 7. 8254 mode 3 timing example.

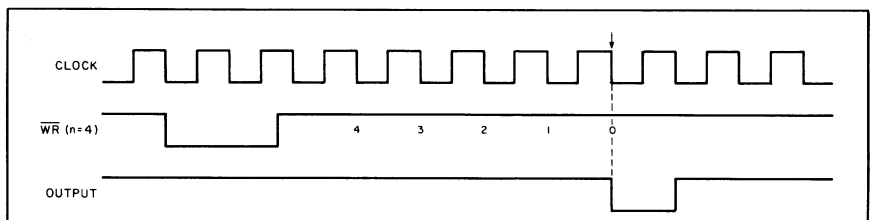

Figure 8. 8254 mode 4 timing example.

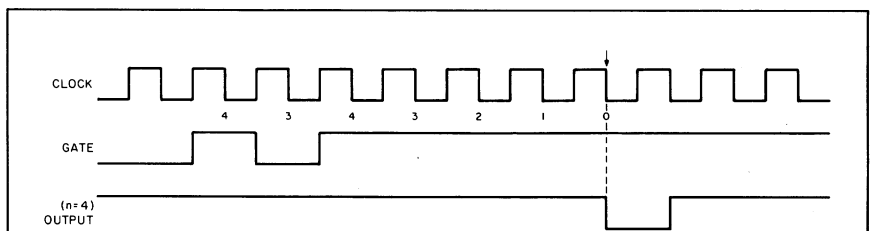

Figure 9. 8254 mode 5 timing example.

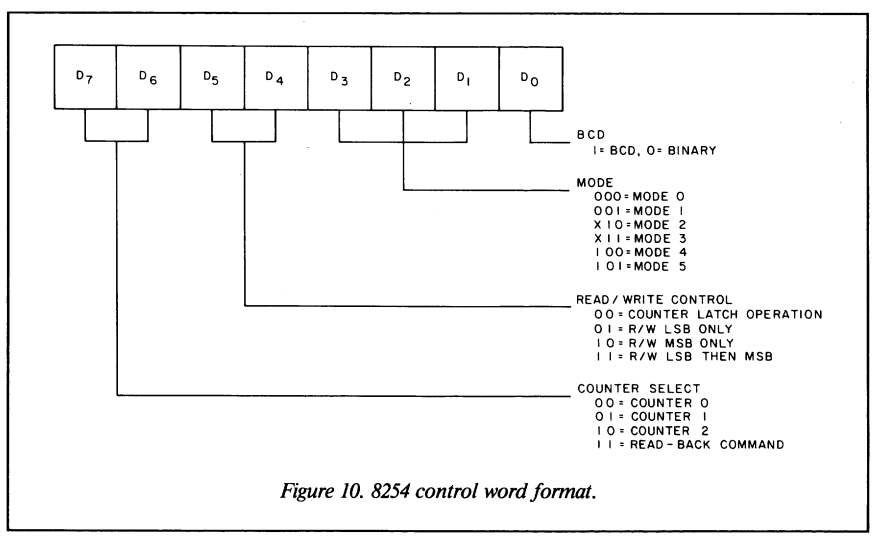

Figure 10. 8254 control word format.

ting up. In the 8254, these bits may also specify a "read-back command" mode, which is unavailable on the 8253. Bits 4 and 5 determine the count-value read/write mode. You have the option to read or write the most significant byte only, the least significant byte only, or the least significant byte followed by the most significant byte. Bits 1, 2, and 3 specify the timer operation mode (zero to 5), and bit zero specifies either straight binary or binary-coded decimal (BCD) counting.

You may want to read the value of a particular counter. Since the counter is a dynamic register, it may change as the processor reads it. To prevent this, a read latch option is available. If bits 4 and 5 of the control byte are both zeros, the 8253/8254 latches the current count value of the specified counter into a temporary register, letting you read it without the count value changing. You should use this approach when you read a counter.

Address selection takes place at the two inverters at the 74LS138 inputs.

Building the I/O Board

Figure 11 shows the I/O board schematics (see Table 1 for a parts list). Address selection takes place at the two inverters at the 74LS138 inputs. The dotted lines show the configuration I used (*** shown below). The possible addresses are as follows:

A6/	A5/	40–47 hexadecimal
A6/	A5	60–67 hexadecimal
A6	A5/	00–07 hexadecimal
A6	A5	20–27 hexadecimal ***

The first four addresses of the range (20–23 hexadecimal [hex]) belong to the 8255A, while the remaining four addresses (24–27 hex) belong to the 8253/8254.

A 50-pin header connector is used as the I/O connector, letting you connect this board to other boards as needed. The connector has 16 I/O signals from the 8255A going to it—all of ports A and C—as well as the three counter outputs, the three gate inputs, and one clock input (to counter 2). The gate input signals are pulled up with resistors so you can still use the respective counters without connecting a device to the expansion connec-

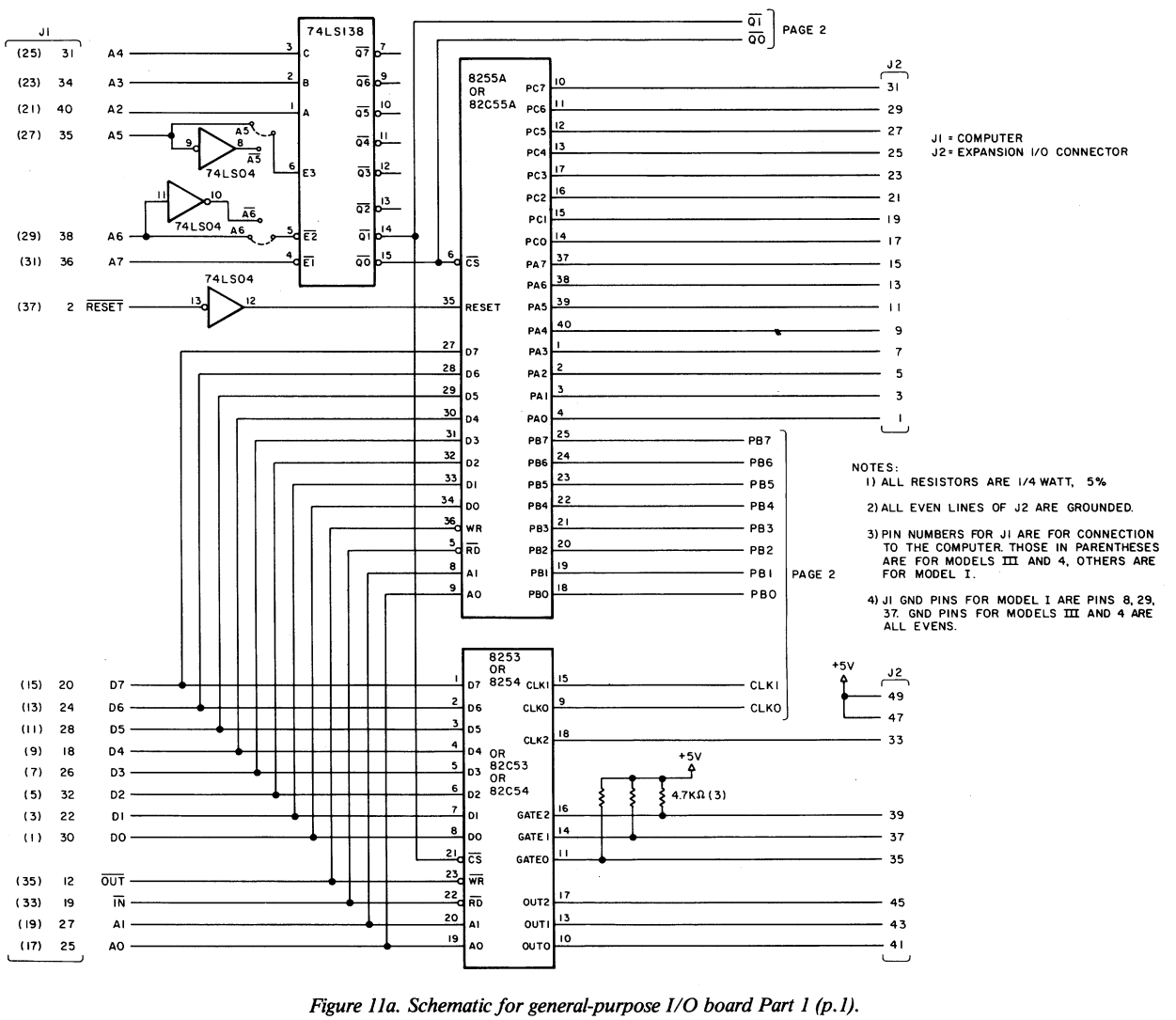

Figure 11a. Schematic for general-purpose I/O board Part 1 (p.1).

tor. Two lines also go to +5V, so an external board can have a logic supply. The chips should draw no more than 50mA of current from each line, and the external board should have a local filtering capacitor to reduce noise if you used the +5V supply.

The crystal oscillator generates a reference frequency for counters zero and 1 of the 8254, which the 74LS193 divides down to shunt various frequencies to the 8254 counters. With the 4 MHz crystal shown, the 8254 receives a maximum frequency of 2 MHz. While this is the maximum allowed by the 8253, the 8254 permits up to 8 MHz. You can lower or raise the crystal frequency as necessary to meet your own requirements.

The 2 MHz clock seems to give a good general-purpose set of frequencies, since this makes available to the 8254 counters four "average" frequencies: 2 MHz, 1 MHz, 500 kHz, and 250 kHz.

The I/O board also has a single-digit seven-segment display. This lets you display a one-digit status indicator, if needed. Between the counter frequency selection and the seven-segment display, the 8 bits from the 8255A port B are used.

In addition to the parts shown in the schematic, you will also need a power supply. The current requirement depends upon whether you use CMOS devices and whether an external board draws current from the I/O board. Worst-case current draw is around 500mA.

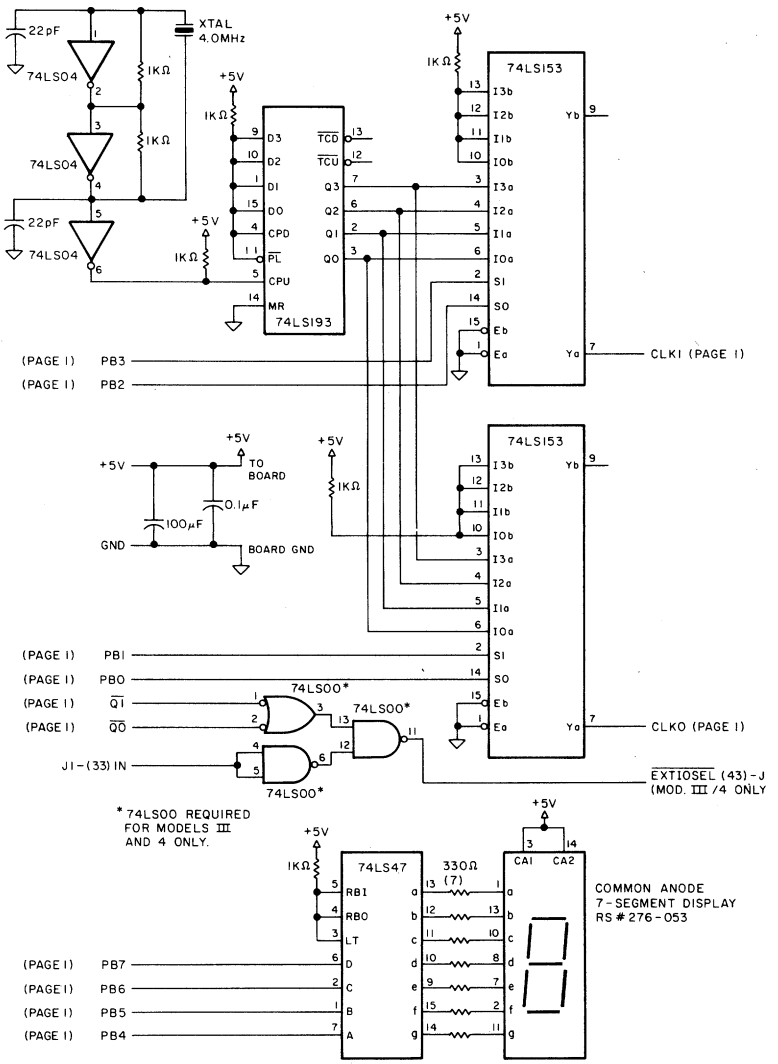

Figure 11b. Schematic for general-purpose I/O board Part 2 (p.2).

The parts list specifies the standard MOS parts. The 82C55A and 82C54 are made by both Harris and OKI Semiconductor, while the 82C53 is made only by OKI. For information on availability, distributors, and price, contact the respective companies.

Using the I/O Board

As indicated, the port A and port C bits are available at the 50-pin I/O connector. This lets you use any of the three possible 8255A operation modes. Also, the I/O board uses all 8 bits of port B on the 8255A to control on-board functions and options.

The four high-order bits (bits 4–7) control the seven-segment display. These go to the input of a 74LS47 BCD-to-seven-segment decoder chip. The 74LS47 converts the BCD value at its inputs into proper segment-on/-off conditions at its outputs, thus displaying the appropriate digit.

Since the board requires BCD digits in the decimal range zero to 9, binary values outside this range (10–15 decimal) cause other, predetermined, patterns to appear on the display. These patterns are described in the data sheet for the 74LS47.

Don't be alarmed if the digit doesn't light up when you apply power to the board. When the board is first initialized, the 8255A places all of its I/O lines into the input mode. The inputs to the 74LS47 float high (all 1's) and the 74LS47 causes all segments to be off when all four inputs are high.

Only one of the three counter clock inputs goes to the I/O connector, with the remaining two used on-board. You can change this if necessary for a particular application. For added versatility, I designed the board to give counters zero and 1 a choice of four possible clock input frequencies, all under software control. Using the 4 MHz crystal shown in the schematics, the four frequencies are 2 MHz, 1 MHz, 500 kHz, and 250 kHz.

The 8255A uses port B to choose the frequency for each counter. Bits zero and 1 select the frequency for counter zero, while bits 2 and 3 select the frequency for counter 1. The 74LS193 is a 4-bit binary counter, which divides the 4 MHz input frequency into the four possible counter frequencies. Each 74LS153 then selects one of the four available frequencies (based on the 2-bit select code at its S0 and S1 in-

puts from the respective port B bits) to transfer to the appropriate 8254 clock input. The select codes and the corresponding output frequencies are:

0	0	2 MHz
0	1	1 MHz
1	0	500 kHz
1	1	250 kHz

By programming the proper port B output values, you can individually set the frequency input to counters zero and 1 at any of these four frequencies.

You can use both the 8255A and the 8254 to interrupt the processor. If you have an application requiring interrupts, you can wire the appropriate interrupt signal to the TRS-80 interrupt line through an open-collector gate, such as the 7406 (inverting). Make sure the interrupt polarity is correct so that an active interrupt signal is low.

You could connect any of a multitude of different application boards to the I/O connector for your computer to control. One simple board might have terminal blocks with the 16 I/O lines connected for easy input and output to TTL-type (or CMOS-type) devices. This type of board is particularly useful for prototyping circuits, where I/O is needed. I think I'll build such a board for myself.

Quantity	Description	Distributor	Part Number	Price (each)
1	8255A programmable peripheral interface IC *	JDR	8255	4.49
1	8253 programmable interval timer IC * †	JDR	8253	6.95
1	74LS138 3-to-8 decoder IC	JDR	74LS138	.55
1	74LS04 hex inverter (LS TTL) IC	JDR	74LS04	.24
1	74LS193 binary up/down counter (LS TTL) IC	JDR	74LS193	.79
2	74LS153 dual 4-line to 1-line MUX (LS TTL) IC	JDR	74LS153	.55
1	74LS00 quad two-input nand gate (LS TTL) IC ‡	JDR	74LS00	.24
1	.3 inch seven-segment red LED display (com. anode)	RS	276-053	1.79
7	330 ohm resistor (¼ watt)	RS	271-1315	.08
7	1k ohm resistor (¼ watt)	RS	271-1321	.08
2	22 pF capacitors	JDR		.05
3	4.7k ohm resistor (¼ watt)	RS	271-1330	.08
1	50-pos. cable header (w/w)	DK	R247-ND	6.93
1	4.0 MHz crystal	DK	X006	2.95
1	100 μF/35V electrolytic capacitor (PC mount)	RS	272-1028	.79
1	.1 μF/50V disk capacitor	RS	272-135	.25
1	.1 inch matrix grid proto board (dual size)	RS	276-161	2.95
1	40-position cable header (w/w) §	DK	R241-ND	5.58
1	40-position ribbon cable edge connector §	DK	R503-ND	3.80
1	40-position ribbon cable socket connector §	DK	R306-ND	3.73
1 ft.	40-conductor ribbon cable §	DK	R007-ND	0.00
1	50-position cable header (w/w) ‡	DK	R247-ND	6.93
1	50-position ribbon cable edge connector ‡	RS	276-1566	4.95
1	50-position ribbon cable socket connector ‡	DK	R307-ND	4.65
1 ft.	50-conductor ribbon cable ‡	DK	R008-ND	0.00

* CMOS parts also available
† 8254 part also available (see text).
‡ Models III/4 only.
§ Model I only.

Addresses

JDR Microdevices, 1224 S. Bascom Avenue, San Jose, CA 95128, 800-538-5000 or 408-995-5430 outside California; 800-662-6279 inside California

Radio Shack (RS), National Parts Division, 900 East Northside Drive, Fort Worth, TX 76102, 817-870-5662

Digi-Key Corp. (DK), Highway 32 S., P.O. Box 677, Thief River Falls, MN 56701, 800-346-5144 or 218-681-6674

Table 1. Parts list and ordering information.

Controlling Software

Models III and 4 users must be particularly careful to write a 10 hex value (16 decimal) to I/O port 0EC hex (236 decimal) to enable access to the external TRS-80 I/O port.

While most applications will have specific set-up commands for the board within the controlling software, I've written a general program that sets up all the devices and options on the I/O board (see the Program Listing).

First you select the desired 8255A mode. The program then asks you for the input/output configuration of the 8255A ports. After the 8255A is configured, you're prompted for the digit you want to appear on the seven-segment display, which the program then sets up.

Once the board completes the processing, you enter the counter/timer portion of the program. You can set any or none of the 8253/8254 counters. If you configure any counters, you enter the counter mode as well as the initial count value. For counter zero or 1, you also enter the input frequency to the timer.

Power Consumption

If you're interested in the power consumption difference between the MOS and CMOS parts, here are the specs: The maximum power consumption for the 8255A and the 8254 are 600 mWs and 700 mWs, respectively. The maximum power consumption for both the 82C55A and the 82C54 is roughly 55 milliamps, with each having a 55 microwatt maximum standby power consumption. ■

IC	Ground	+5V
74LS04	7	14
74LS138	8	16
74LS47	8	16
74LS153	8	16
74LS193	8	16
74LS00	7	14
8253	12	24
8255	7	26

Table 2. Power and ground connections for the I/O board.

REFERENCES

1983 Intel Microprocessor and Peripheral Handbook
Intel Corporation
3065 Bowers Ave.
Santa Clara, CA 95051

1984 Harris CMOS Digital Data Book
Harris CMOS Digital Products Division
Mail Stop 53-035
P.O. Box 883
Melbourne, FL 32902-0883

The TTL Data Book for Design Engineers
Texas Instruments Inc.
6000 Denton Drive
P.O. Box 5012
Mail Stop 366
Dallas, TX 75222

OKI Semiconductor
Suite 401
1333 Lawrence Expy.
Santa Clara, CA 95051

Program Listing. Controlling software.

```
10 '*********************************************************
20 '     This program allows the user to easily configure the *
30 ' general-purpose I/O card for many applications. The      *
40 ' program will prompt the user first for the mode and      *
50 ' configuration of the 8255A (or 82C55A) and will set up   *
60 ' the 8255A accordingly. The program will then allow the   *
70 ' user to optionally set up any or all of the three timers *
80 ' in the 8253. When selecting timers zero or one, the user *
90 ' is also asked which of the four possible frequencies he  *
100 ' wishes to go into the timer's clock input line. The     *
110 ' program will then set up the respective 8253 timers, as *
120 ' appropriate.                                            *
130 '                                                         *
140 '     Created by Roger C. Alford                          *
150 '*********************************************************
160 '
170 '
200 '*========== MAIN CONTROLLING CODE SECTION ==========*
210 GOSUB 1000                    'CONFIGURE THE 8255A PPI
215 CLS
220 INPUT "DO YOU WISH TO SET UP ANY OF THE TIMERS (Y/N) ";A$
230 IF A$="N" THEN 260
240 IF A$<>"Y" THEN 220
250 GOSUB 5000                    'CONFIGURE THE 8253 PIT
260 END
270 '-----------------------------------------------------
280 '
1000 '*========= 8255A CONFIGURATION CODE ==========*
1010 CLS:PRINT "THE 8255A MODE OPTIONS ARE:"
1020 PRINT "    0) MODE 0 - BASIC INPUT/OUTPUT"
1030 PRINT "    1) MODE 1 - STROBED INPUT/OUTPUT"
1040 PRINT "    2) MODE 2 - BI-DIRECTIONAL BUS"
1050 INPUT "SELECT DESIRED (PORT A) MODE ";M
1060 M=M+1
1070 IF M<1 OR M>3 THEN 1010
1080 ON M GOSUB 2000,3000,4000
1085 GOSUB 12000                  'SET-UP 7-SEGMENT DISPLAY
1090 RETURN
1100 '-----------------------------------------------
1110 '
2000 '*=========== 8255A MODE 0 CONFIGURATION CODE ===========*
2010 CLS:PRINT "8255A MODE 0 CONFIGURATION"
2015 PRINT "   (PORT B IS AUTOMATICALLY MADE OUTPUT)"
2020 PRINT:PRINT
2030 INPUT "WOULD YOU LIKE PORT A TO BE INPUT OR OUTPUT (I/O) ";I$
2040 IF I$<>"I" AND I$<>"O" THEN 2030
2050 INPUT "WOULD YOU LIKE PORT CL TO BE INPUT OR OUTPUT (I/O) ";J$
2060 IF J$<>"I" AND J$<>"O" THEN 2050
2070 INPUT "WOULD YOU LIKE PORT CH TO BE INPUT OR OUTPUT (I/O) ";K$
2080 IF K$<>"I" AND K$<>"O" THEN 2070
2090 CW=128
2100 IF I$="I" THEN CW=CW+16
2110 IF J$="I" THEN CW=CW+1
2120 IF K$="I" THEN CW=CW+8
2130 OUT 35,CW                    'SEND THE 8255A CONTROL WORD
2140 RETURN
2150 '-----------------------------------------------------
2160 '
3000 '*=========== 8255A MODE 1 CONFIGURATION CODE ==========*
3010 CLS:PRINT "8255A MODE 1 CONFIGURATION"
3013 PRINT "    (PORT B IS AUTOMATICALLY MADE MODE 0 OUTPUT)"
3015 PRINT "    (PORT C BITS 4&5 OR 6&7 WILL BE FREE FOR G.P. I/O)"
3020 PRINT:PRINT
3030 INPUT "WOULD YOU LIKE PORT A TO BE INPUT OR OUTPUT (I/O) ";I$
3040 IF I$<>"I" AND I$<>"O" THEN 3030
3050 IF I$="O" THEN T$=" 4&5 " ELSE T$=" 6&7 "
3060 PRINT "WOULD YOU LIKE PORT C BITS";T$;"TO BE INPUT OR OUTPUT (I/O) ";
3065 INPUT J$
3070 IF J$<>"I" AND J$<>"O" THEN 3060
3080 CW=160
3090 IF I$="I" THEN CW=CW+16
3100 IF J$="I" THEN CW=CW+8
3110 OUT 35,CW                    'SEND THE 8255A CONTROL WORD
3120 RETURN
3130 '-----------------------------------------------------
3140 '
4000 '*========== 8255A MODE 2 CONFIGURATION CODE ==========*
```

Listing continued

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```
4010 CLS:PRINT "8255A MODE 2 CONFIGURATION"
4020 PRINT "    (PORT B IS AUTOMATICALLY MADE OUTPUT)"
4030 PRINT "    (PORT C BITS 0-2 WILL BE FREE FOR G.P. I/O)"
4040 PRINT:PRINT
4050 INPUT "WOULD YOU LIKE PORT C BITS 0-2 TO BE INPUT
     OR OUTPUT (I/O) ";I$
4060 IF I$<>"I" AND I$<>"O" THEN 4050
4070 IF I$="I" THEN CW=193 ELSE CW=192
4080 OUT 35,CW                  'SEND THE 8255A CONTROL WORD
4090 RETURN
4100 '-------------------------------------------------------
4110 '
5000 '*========== 8253 CONFIGURATION CODE ==========*
5010 CLS:PRINT "YOUR OPTIONS ARE:"
5020 PRINT "    0) SET TIMER 0"
5030 PRINT "    1) SET TIMER 1"
5040 PRINT "    2) SET TIMER 2"
5050 PRINT "    3) EXIT"
5060 INPUT "ENTER YOUR SELECTION ";M
5070 M=M+1
5080 IF M<1 OR M>4 THEN 5060
5090 IF M=4 THEN 5120
5100 ON M GOSUB 6000,7000,8000
5110 GOTO 5010
5120 RETURN
5130 '-------------------------------------------------
5140 '
6000 '*========== 8253 TIMER 0 CONFIGURATION CODE ==========*
6010 T=0:T$="0"
6020 GOSUB 9000                 'SET TIMER MODE
6025 GOSUB 13000                'SET TIMER INPUT FREQUENCY
6030 GOSUB 10000                'SET INITIAL TIMER COUNT
6040 RETURN
6050 '-------------------------------------------------------
6060 '
7000 '*========== 8253 TIMER 1 CONFIGURATION CODE ==========*
7010 T=1:T$="1"
7020 GOSUB 9000                 'SET TIMER MODE
7025 GOSUB 13000                'SET TIMER INPUT FREQUENCY
7030 GOSUB 10000                'SET INITIAL TIMER COUNT
7040 RETURN
7050 '-------------------------------------------------------
7060 '
8000 '*========== 8253 TIMER 2 CONFIGURATION CODE ==========*
8010 T=2:T$="2"
8020 GOSUB 9000                 'SET TIMER MODE
8030 GOSUB 10000                'SET INITIAL TIMER COUNT
8040 RETURN
8050 '-------------------------------------------------------
8060 '
9000 '*========== 8253 TIMER MODE SELECTION CODE ==========*
9003 CLS:PRINT "8253 TIMER ";T$;" CONFIGURATION"
9005 PRINT:PRINT
9010 PRINT "THE AVAILABLE TIMER MODES ARE:"
9020 PRINT "    0) MODE 0 - INTERRUPT ON TERMINAL COUNT"
9030 PRINT "    1) MODE 1 - PROGRAMMABLE ONE-SHOT"
9040 PRINT "    2) MODE 2 - RATE GENERATOR"
9050 PRINT "    3) MODE 3 - SQUARE WAVE RATE GENERATOR"
9060 PRINT "    4) MODE 4 - SOFTWARE TRIGGERED STROBE"
9070 PRINT "    5) MODE 5 - HARDWARE TRIGGERED STROBE"
9080 INPUT "ENTER THE DESIRED MODE ";MD
9090 IF MD<0 OR MD>5 THEN 9080
9100 GOSUB 11000                'GET READ/LOAD MODE
9110 CW=T*64+RL*16+MD*2
9120 OUT 39,CW                  'SEND THE TIMER CONTROL WORD
9130 RETURN
9140 '-------------------------------------------------------
9150 '
10000 '*========== 8253 INITIAL COUNT CODE ==========*
10010 CLS:PRINT "8253 TIMER ";T$;" CONFIGURATION"
10020 PRINT:PRINT
10030 INPUT "ENTER INITIAL TIMER COUNT VALUE (-1 FOR NONE) ";IC
10040 IF IC=-1 THEN 10150
10050 IF IC<0 THEN 10030
10060 IF RL<>3 AND IC>255 THEN 10030
10070 IF IC>65535 THEN 10030
10080 IF RL=3 THEN 10110
10090 OUT 36+T,IC               'SEND INITIAL TIMER COUNT
10100 GOTO 10150
10110 IH=INT(IC/256)            'GET HIGH BYTE OF COUNT VALUE
10120 IL=IC-(IH*256)            'GET LOW BYTE OF COUNT VALUE
10130 OUT 36+T,IL               'SEND LOW BYTE OF INITIAL COUNT
10140 OUT 36+T,IH               'SEND HIGH BYTE OF INIT. COUNT
10150 RETURN
10160 '-------------------------------------------------------
10170 '
11000 '*========== 8253 READ/LOAD MODE CODE ==========*
11010 CLS:PRINT "8253 TIMER ";T$;" CONFIGURATION"
11020 PRINT:PRINT
11030 PRINT "THE AVAILABLE READ/LOAD MODES ARE:"
11040 PRINT "    1) READ/LOAD LSB ONLY"
11050 PRINT "    2) READ/LOAD MSB ONLY"
11060 PRINT "    3) READ/LOAD LSB FIRST, THEN MSB"
11070 INPUT "ENTER DESIRED READ/LOAD MODE ";RL
11080 IF RL<1 OR RL>3 THEN 10170
11090 RETURN
11100 '-------------------------------------------------------
11110 '
12000 '*========== SET 7-SEGMENT DISPLAY CODE ==========*
12010 CLS:PRINT "7-SEGMENT DISPLAY SET-UP"
12020 PRINT:PRINT
12030 INPUT "ENTER DIGIT TO APPEAR ON THE DISPLAY (0-9) ";DG
12040 IF DG<0 OR DG>9 THEN 12030
12050 OUT 33,DG*16              'SET DISPLAY DIGIT
12060 RETURN
12070 '-------------------------------------------------------
12080 '
13000 '*========== SET TIMER INPUT FREQUENCY CODE ==========*
13010 CLS:PRINT "8253 TIMER ";T$;" CONFIGURATION"
13020 PRINT:PRINT
13030 PRINT "THE AVAILABLE TIMER INPUT FREQUENCIES ARE:"
13040 PRINT "    1) 2 MHZ"
13050 PRINT "    2) 1 MHZ"
13060 PRINT "    3) 500 KHZ"
13070 PRINT "    4) 250 KHZ"
13080 INPUT "ENTER THE DESIRED TIMER INPUT FREQUENCY ";TF
13090 IF TF<1 OR TF>4 THEN 13080
13100 TF=TF-1
13105 IF T=1 THEN AV=243 ELSE AV=252
13110 TM=INP(33) AND AV
13120 IF T=1 THEN TF=TF*4
13130 OUT 33,TM+TF
13140 RETURN
13150 '-------------------------------------------------------
```

End