

CHAPTER 8 FLOPPY DISK DRIVE SD-321

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8.1 General

Double sided, double density type of 5-1/4" floppy disk drive SD-321 has the features as described below:

- 1) SD-321 produces an ultra thin structure of 1/2 – 1/3 the conventional models.
- 2) The VCM (Voice coil motor) type linear actuator which is developed originally is adopted to the head drive mechanism, so it is of high reliability.
- 3) In order to miniaturize the circuit board and get high reliability, most of the control circuit is integrated to two LSIs.

8.2 General Specifications

| | |
|---|--|
| 8.2.1 Memory capacity | |
| (1) Unformatted | : 250k byte (Single density recording) 500k byte (Double density recording) |
| (2) Formatted (16 sectors/track) | : 164k byte (Single density recording) 328k byte (Double density recording) |
| 8.2.2 Recording density (side 1, trk 39): | 2938 BPI (Single density recording) 5876 BPI (Double density recording) |
| 8.2.3 Transmission speed | 125k bit/sec (Single density recording) 250k bit/sec (Double density recording) |
| 8.2.4 Track mean speed waiting time | 100 msec |
| 8.2.5 Access time | |
| (1) Between tracks | : 15 msec |
| (2) Between tracks moving average | : 220 msec |
| (3) Settling time | : 15 msec |
| 8.2.6 Motor starting time | 0.5 sec |
| 8.2.7 Motor speed | 300 rpm |
| 8.2.8 Track density | 48 TPI |
| 8.2.9 Total number of tracks | 80 |
| 8.2.10 Inner circumference track radius | 36.52 mm (trk 39, side 0) 34.40 mm (trk 39, side 1) |
| 8.2.11 Outer circumference track radius | 57.15 mm (trk 00, side 0) 55.03 mm (trk 00, side 1) |
| 8.2.12 Recording system | MFM |
| 8.2.13 R/W head positioning | Voice coil motor |
| 8.2.14 Main axis motor | Outer rotor-type brushless transistor motor |
| 8.2.15 Power supply | |
| (1) +12V ($\pm 5\%$): | 0.7A (typ) (at reading/writing) 1.9A (max) (at motor starting) |
| (2) +5V ($\pm 5\%$): | 0.25A (typ) 0.4A (max) |
| 8.2.16 Power consumption: | 9.7W (typ) |

8.3 Outline of Mechanisms

The SD-321 is an ultra thin 5.25-inch floppy disk device and comprises the following nine elements:

- 1) Read/write head
- 2) Head access mechanism
- 3) Head loading mechanism
- 4) Disk drive mechanism
- 5) Disk protection mechanism
- 6) Disk eject mechanism
- 7) Index detector
- 8) Write protection detector
- 9) Control circuit

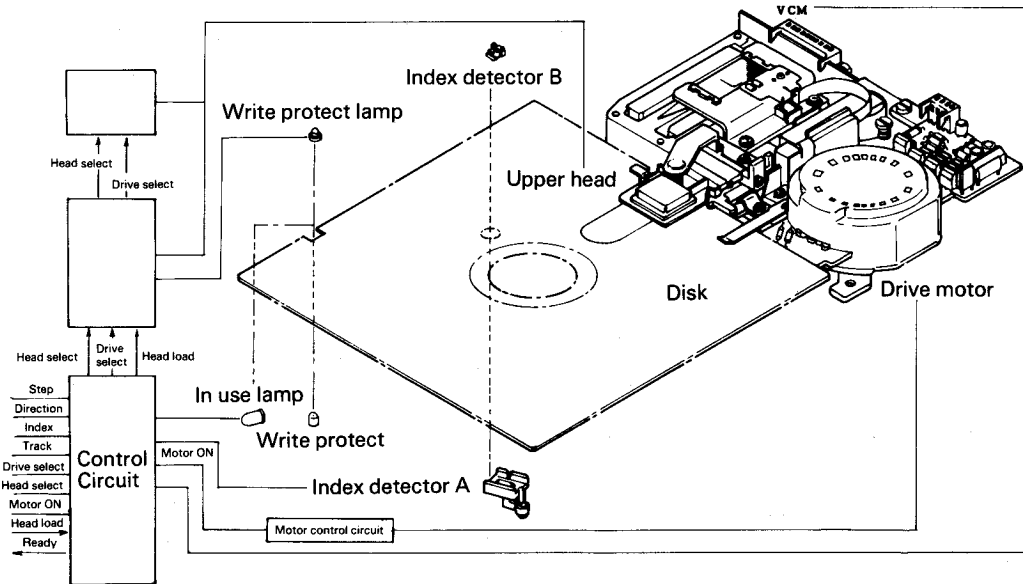


Fig. 8-1 General Block Diagram

8.3.1 Read/Write head

The read/write head uses a reliable tunnel-erase type ferrite ceramic head with erase gaps on both sides of the read/write gap. Upper and lower read/write heads are supported by upper and lower head holders by thimbles. This makes head touch to media good and minimizes the influence on the media at loading and unloading.

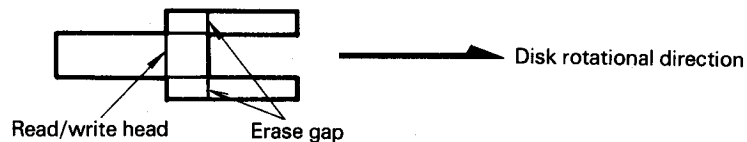


Fig. 8-2 Read/Write Head

8.3.2 Head access mechanism

The read/write head track is positioned highly accurately and delicately by the voice coil motor by directly moving it. The moving direction is selected by the host system. The voice coil motor can be moved by the distance equivalent to the specified number of tracks if one pulse is entered for one track.

8.3.3 Head loading mechanism

When the disk is inserted and the pushbutton is pressed, the collet lever gets down. At the same instant, the read/write head makes contact with the disk and the pad holds the disk. Data transmission is made in this state.

8.3.4 Disk drive mechanism

The disk drive pulley is connected to the disk drive motor via a belt and rotates at a speed of 300 rpm. When the disk is inserted and the pushbutton switch is pressed, the disk drive pull rotation is transmitted to the disk. The disk drive motor is a brushless DC motor, and has an FG coil inside so that it is controlled to rotate at a constant speed by the speed detection signal of the FG coil.

8.3.5 Disk protection mechanism

To protect the disk center hole, the pushbutton can not be pressed unless the disk is inserted in the correct position.

8.3.6 Disk eject mechanism

When the pushbutton switch is pressed to remove the disk, the disk is automatically ejected and pops out from the front panel.

8.3.7 Index detector

This detects the index hole on the disk to determine the data start point in the track, and comprises a pair of light emitting diodes and a phototransistor.

8.3.8 Write protection detector

This detects the disk's write protection notch, and comprises a pair of light emitting diodes and a phototransistor.

When the disk with the write protection label pasted is inserted, the control circuit inhibits writing onto the disk.

8.3.9 Control circuit

The circuit which electrically controls each mechanism's operation is divided into a main PCB, a drive motor PCB and a voice coil motor PCB. The control circuit is largely divided into the following sections. Most of these sections are constructed in the custom LSI as shown below.

- | | |
|-------------------------------------|--------------------------------|
| 1) Read/write logic and amplifier | 5) Side selector |
| 2) Voice coil motor control circuit | 6) Write protection detector |
| 3) Track 00 detector | 7) Drive selector |
| 4) Index detector | 8) Drive motor control circuit |

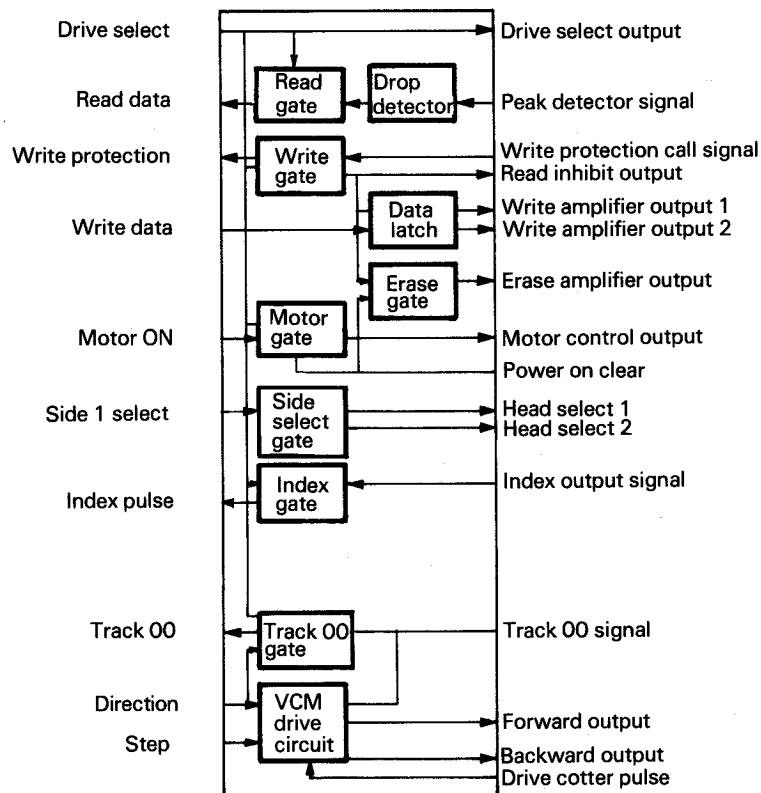


Fig. 8-3 LSI Block Diagram

8.4 Operating Principles

8.4.1 Disk drive motor

The SD-321 uses a long-life outer rotor type DC motor for disk driving. As shown in Fig. 8-4., the motor mechanism comprises a motor unit containing the frequency generator (FG) which can take out the frequency proportional to the rotor rotation, and a circuit section.

The circuit section comprises the following circuits:

- Motor speed control circuit
- Start/stop control circuit
- Motor drive circuit

When a low-level motor drive signal is entered into the start/stop control circuit, the motor drive circuit drive transistor turns on and the disk drive motor starts operation. By applying the output of the built-in FG to the motor speed control circuit, the motor drive circuit drive transistor is controlled to keep the disk drive motor speed constant. When a high-level motor drive signal is entered into the start/stop control circuit, the motor drive circuit drive transistor turns off and the disk drive motor stops.

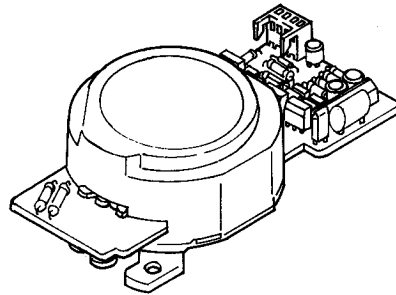


Fig. 8-4 Disk Drive Motor

8.4.2 Head access mechanism

Use of a voice coil motor in the head access mechanism improves positioning accuracy and delicacy and produces an ultra thin structure of 1/3 the conventional models. The voice coil motor (VCM) construction is shown in Fig. 8-5. The drive circuit generates a drive signal of aimed direction from a step signal and a direction signal, and moves the voice coil motor through the adder and power amplifier.

In this step, the intermediate position between the tracks adjacent to the position detector connected to the voice coil motor is detected, and the drive signal is reset. Since the position detector continuously generates a control signal except for each track position, the voice coil motor is moved to the adjacent track and stopped there. The voice coil motor speed is maximum at the intermediate position, and needs to be rapidly reduced after passing the intermediate position. The voice coil motor is thus braked using the speed detector.

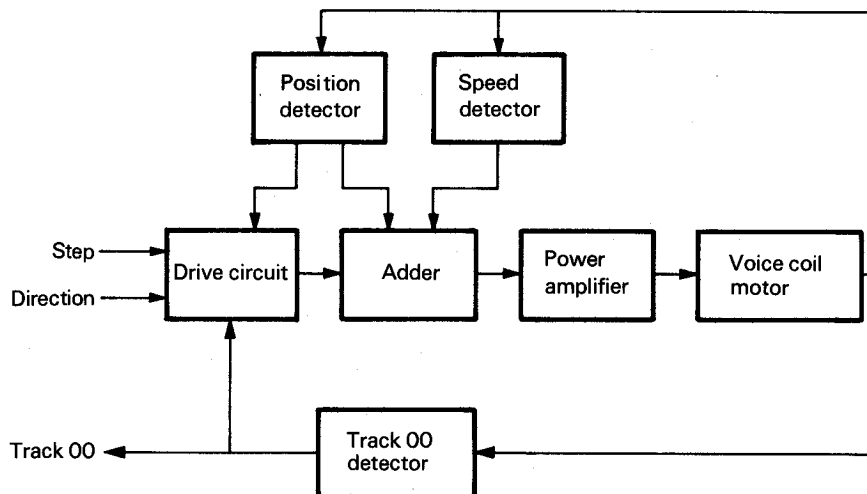


Fig. 8-5 VCM Block Diagram

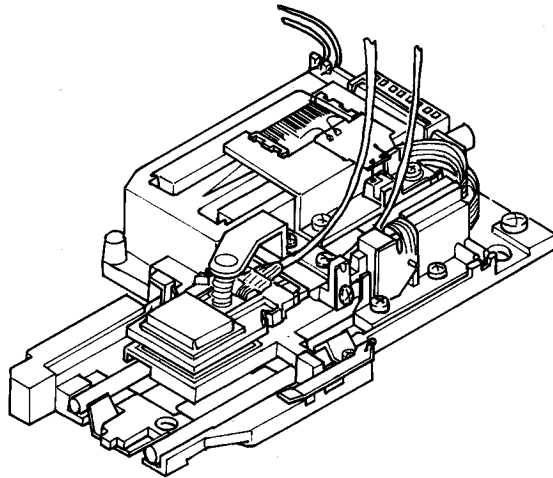


Fig. 8-6 VCM External View

8.4.3 Head loading mechanism

When the disk is inserted and the pushbutton is pressed, the collet lever gets down by being transmitted mechanically. Then, the upper head holder is released and presses the upper head to the lower head through the disk with a constant pressure, by using the upper head spring.

At the same time, the pad attached to the pad lever holds the disk between the pad and the pad receiver, the disk is rotated smoothly and the dust on the disk surface is eliminated by the liner provided inside the envelope.

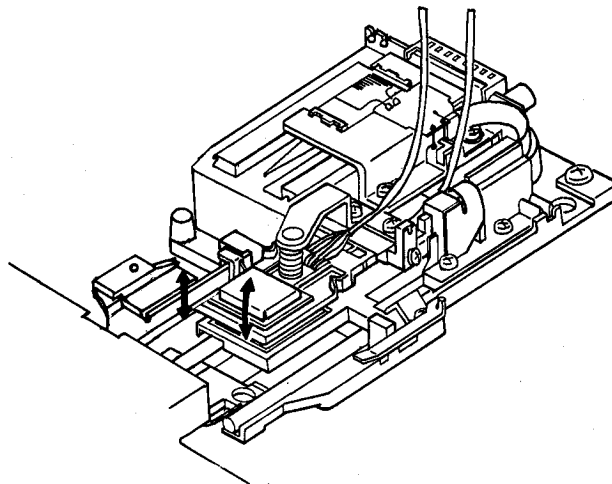


Fig. 8-7 Head Loading Mechanism

8.4.4 Operation channel

A) At disk insertion

When the disk is inserted through the front panel, the disk pushes the ejector and when the disk reaches the specified position, the eject lock pin attached to the eject lock lever falls into the groove of the ejector. At this time the eject lock lever locks the front panel cover, determining the position of the inserted disk and preventing insertion of the next disk.

Further, the eject lock lever rotates the safety lever to release the slide lever to allow it to be freely pushed. When the pushbutton switch is pressed, the collet is pushed down to clamp the disk between it and the disk drive pulley, bringing it to the position where the disk drive motor rotation can be transmitted to the disk.

As soon as the collet is pushed down, the upper head lowers to a position about 0.7 mm above the lower head, and the slide lever engages with the latch in this position and holds it.

B) At disk ejection

When the pushbutton switch is pressed, the slide lever is disengaged from the latch, the eject operation lever rotates the eject transmission lever, and the eject transmission lever disengages the eject lock pin from the ejector groove. At the same time the front panel entrance held by the eject lock lever is released, and the ejector is set free in the entrance direction.

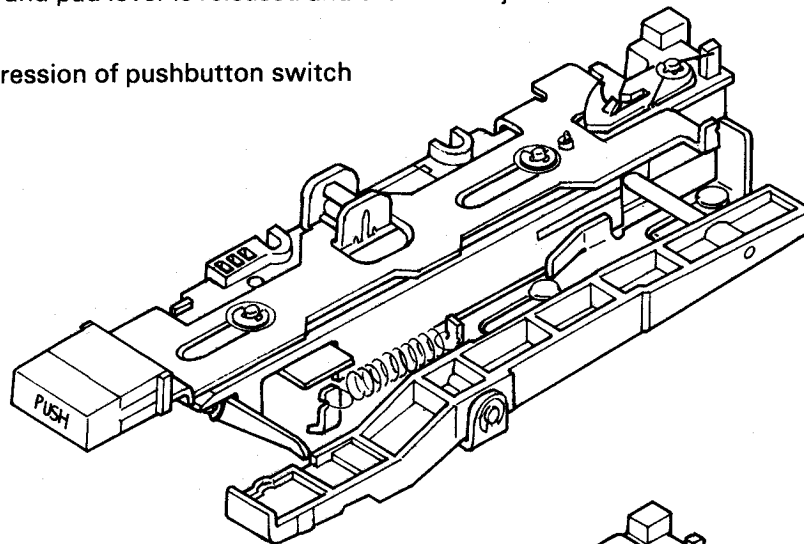
After disengaging from the eject lock pin, the ejector attempts to push out the disk, but fails as its motion is restricted by the pad lever.

As the slide lever disengaged from the latch approaches the disk setting position, the pad lever and the head rise together.

At the same time the collet also rises to set the disk free.

When the pad lever and the upper head rise to the specified position, the engagement between the ejector and pad lever is released and the disk is ejected.

Before depression of pushbutton switch



After depression of pushbutton switch

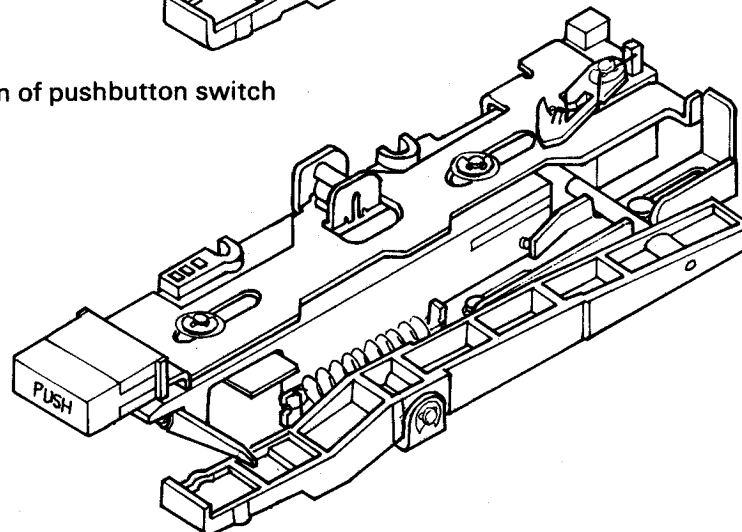


Fig. 8-8 Operation Channel Mechanism

8.4.5 Disk protection mechanism

To protect the disk, one end of the safety lever is usually engaged with the eject lock lever. When the disk is not in the correct position, the safety lever tip projects into the path of the slide lever to restrict the slide lever motion, so that the collet does not fall.

The eject lock lever also lifts the disk from the lower head surface to protect the head either at insertion or ejection of the disk.

8.5 Interface

Up to four SD-321s can be connected in a daisy chain. Input/output of all signals is compatible with TTL level. +12V and +5V are required as a power supply interface.

8.5.1 Signal Interface (Main PCB J2)

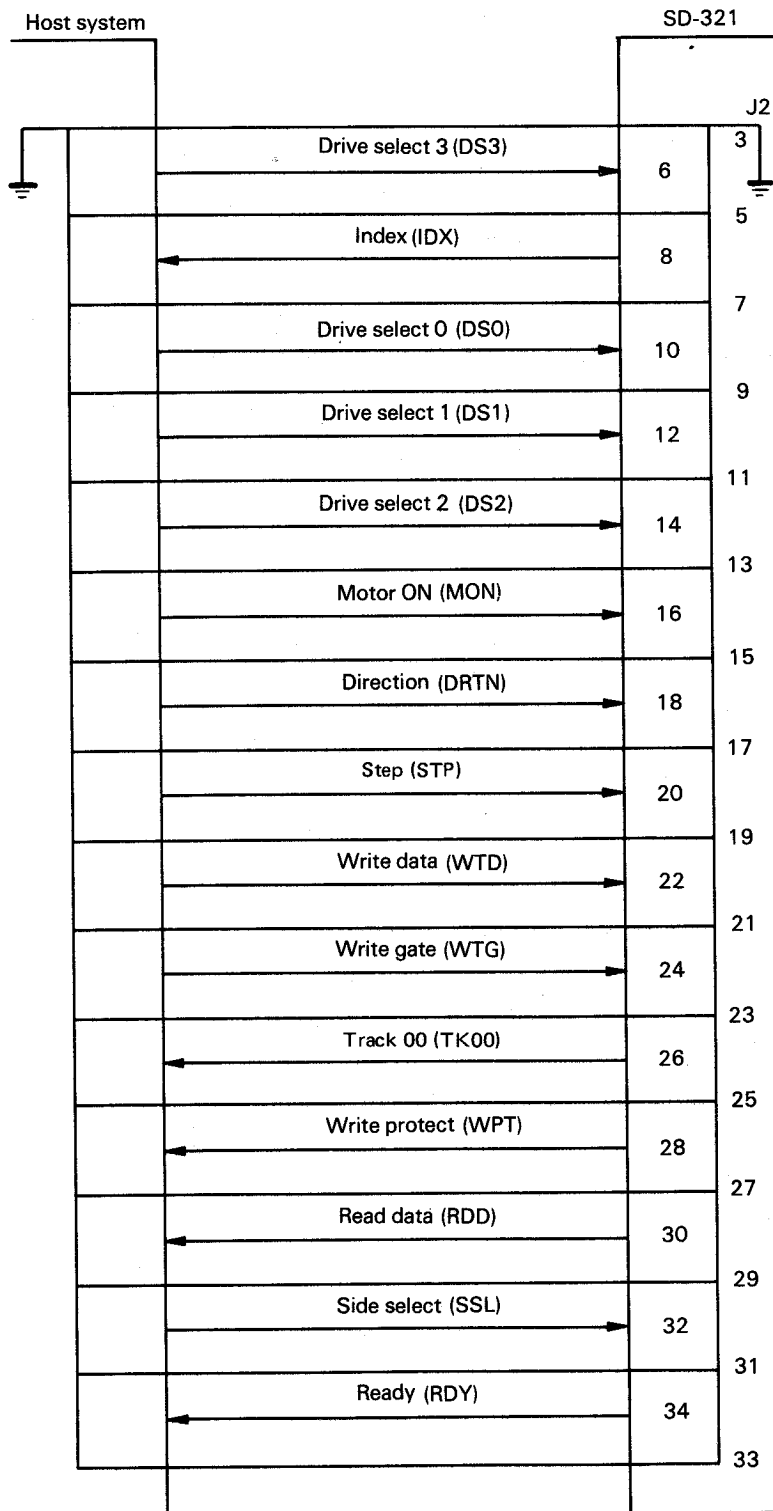


Fig. 8-9 Signal Interface

8.5.2 Electrical specifications of input and output signals

| | |
|--------------|---------------------------|
| LOW = TRUE | (V_{IN} : 0V – +0.4V) |
| | (I_{IN} : 40 mA max.) |
| HIGH = FALSE | (V_{IN} : 2.5 – 5.25V) |
| | (I_{IN} : 0 mA Open) |

The SD-321 uses SN7406 (or equivalent) as an output driver. Each input terminal is pulled up at 5V with 150Ω , and connected to LSI through a resistor of $10\text{ k}\Omega$.

8.5.3 Functions of input signals

1) Drive select 0 – 3 (DS0 – DS3)

The SD-321 can be connected to up to four sets in a daisy chain. Connected sets are selected by the dip switch located on the main PCB. (The SD-321 has been set to operate at drive select 0 before shipment.) Transmission/reception of input and output signals is permitted only for the drive selected by this switch.

2) Motor ON (MON)

When the motor ON signal is set to logic 0, the disk drive motor starts operation. However, seek, write and read operations should be performed after the ready signal is set to logic 0. The ready signal is set to logic 0 within one second after the motor ON signal is entered.

3) Direction (DRTN)

The direction signal determines the voice coil motor moving direction. The voice coil motor moves from track 00 to 39 when this signal is set to logic 0, and vice versa when the signal is set to logic 1.

4) Step (STP)

By entering a pulse into the step signal, the voice coil motor for positioning the read/write head can be moved in the direction specified by the DRTN signal.

The maximum response step cycle is 15 mS/track.

Step is inhibited when the write gate signal is at logic 0.

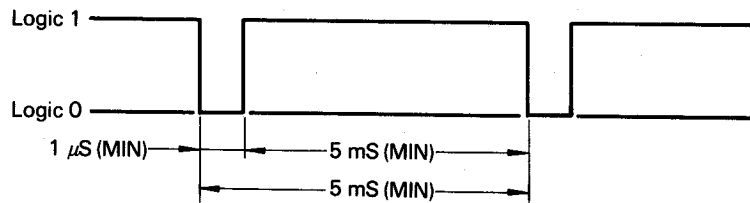


Fig. 8-10 Step Signal

5) Write gate (WTG)

The write gate signal controls write data and read data signals, makes the write data signal valid at logic 0 and the read data signal valid at logic 1. For a disk with the write protect label pasted on, the write operation is inhibited in LSI.

6) Write data (WTD)

The write data signal inverses the read/write head writing current and allows it to flow to generate a change in the magnetic flux when the input pulse changes from logic 1 to 0 in the signal line of the data to be written onto the disk. The write data signal is valid only when the write gate signal is at logic 0.

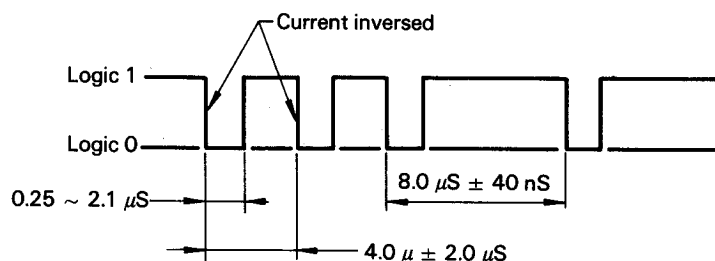


Fig. 8-11 Write Data Signal (In Case of FM Recording)

7) Side select (SSL)

The side select signal selects two upper and lower read/write heads to be used for operation.

Logic 0: SIDE 1 (Upper head)

Logic 1: SIDE 0 (Lower head)

When the head loading signal is at logic 0, the read/write head is loaded on the disk.

8.5.4 Functions of output signals

1) Ready (RDY)

The ready signal is set to logic 0 when the power is turned on, the disk is inserted or the disk rotates normally.

2) Track 00 (TK00)

The track 00 signal is set to logic 0 when the read/write head is in the position of track 00.

3) Index (IDX)

The index signal generates a pulse of logic 0 once per disk rotation.

The position where the index signal changes from logic 1 to 0 indicates the beginning of data on the track.

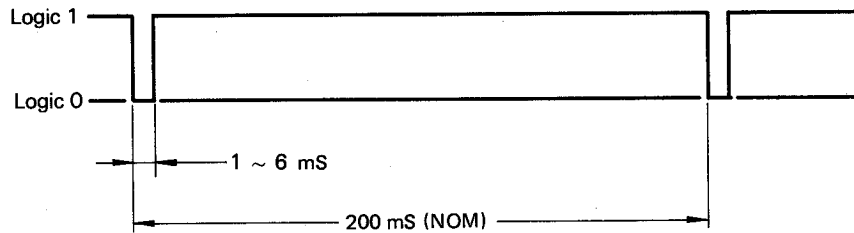


Fig. 8-12 Index Signal

4) Read data (RDD)

The read data signal outputs the raw data pulse train read by the read circuit. It is usually at logic 1 and turns to 0 when magnetization is inverted on media.

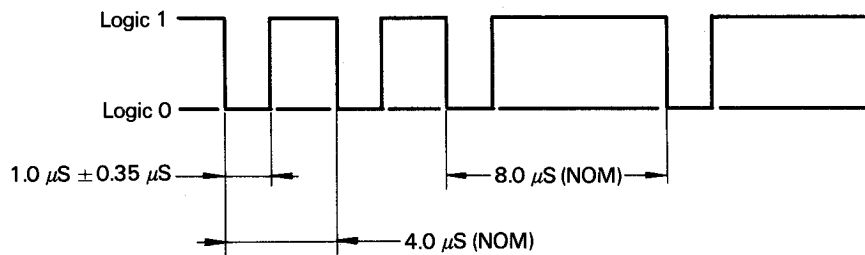


Fig. 8-13 Read Data Signal

5) Write protect

The write protect signal is set to logic 0 for a disk with the write protect label pasted on.

8.5.5 Timing

The track initial position is 00.

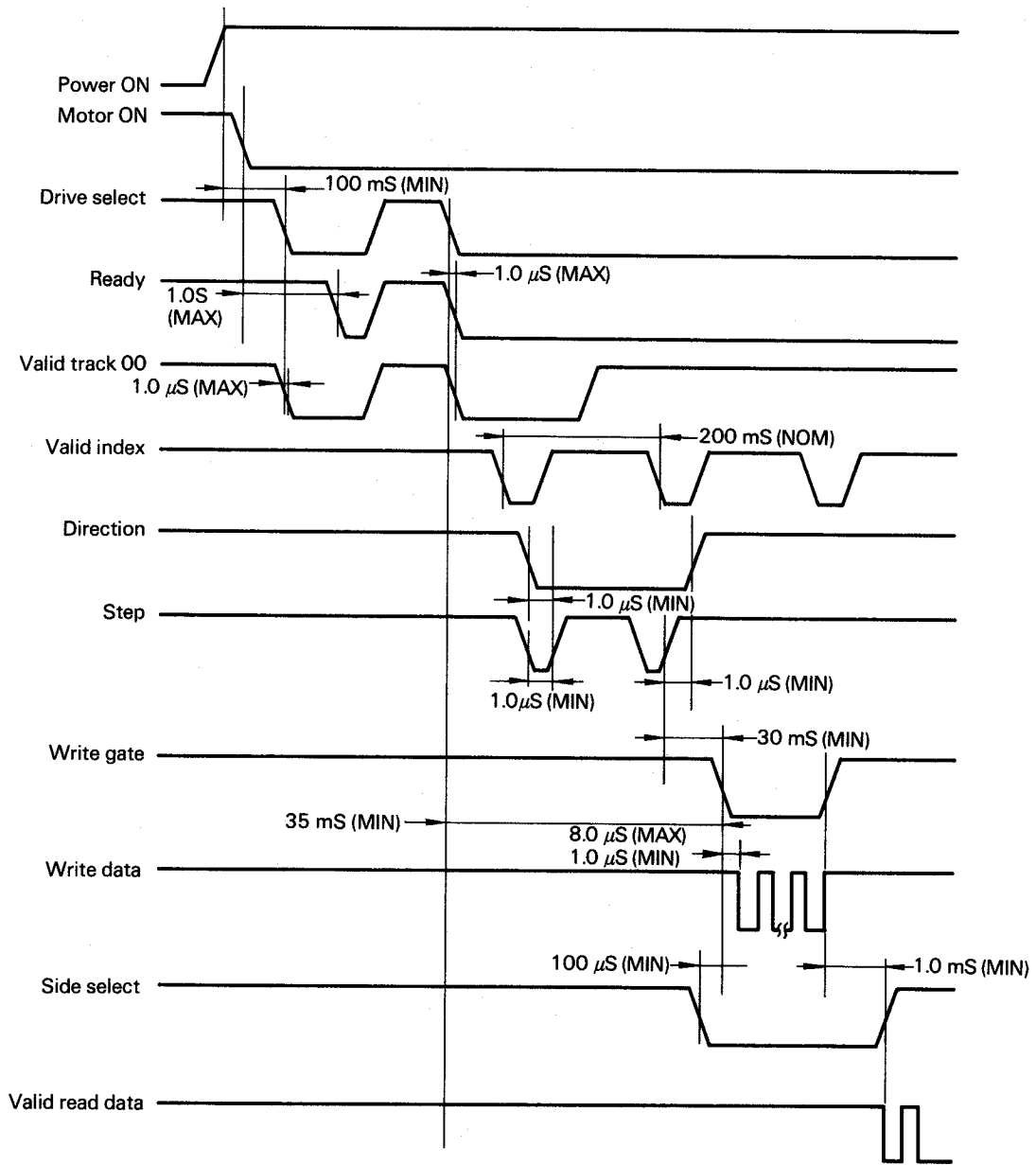


Fig. 8-14 Timing

8.5.6 Connectors

1) Power connector (J1/P1)

The DC power supply connector is located on the main PCB and uses a 4-pin AMPP/ N1-450426-0.

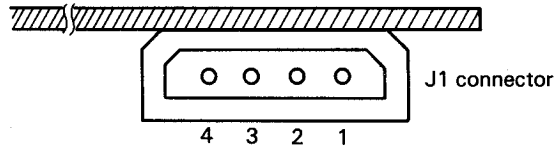


Fig. 8-15 Connector

2) Signal connector (J2/P2)

The connection of the J2 connector is a 34-pin card edge connector, and patterns 1 and 2 are omitted. The parts mounting surface is an odd number, and the soldering surface is an even number. There is a key slot between 4 and 6. The connector dimensions are given below. The following connector is recommended for the user.

- Connector : 3M P/N 3463-0001
- Polarity key : 3M P/N 3479-0000
- Flat cable : 3M P/N 3365134

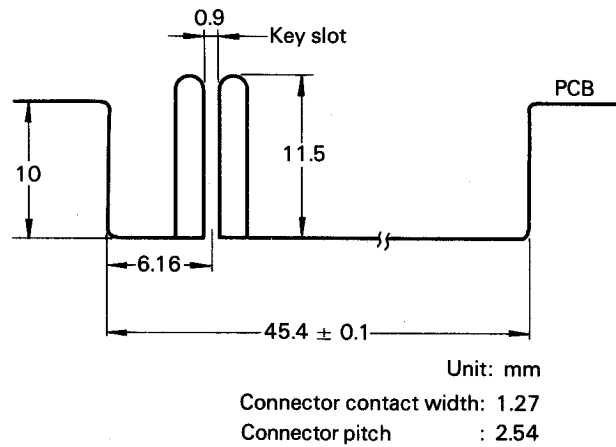


Fig. 8-16 Signal Connector

CHAPTER 9 GENERAL SPECIFICATIONS FOR QX-10 OPTION CARD

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9.1 Option Connector Signal Assignment Diagram

The following signals are assigned to the option slots:

| Signal | Pin No. | Pin No. | Signal |
|-----------------------------|---------|---------|-----------------------------|
| GND | 1 | 2 | GND |
| DTB 0 | 3 | 4 | DTB 1 |
| 2 | 5 | 6 | 3 |
| 4 | 7 | 8 | 5 |
| 6 | 9 | 10 | 7 |
| -12V | 11 | 12 | -12V |
| ADR 0 | 13 | 14 | ADR 1 |
| 2 | 15 | 16 | 3 |
| 4 | 17 | 18 | 5 |
| 6 | 19 | 20 | 7 |
| 8 | 21 | 22 | 9 |
| 10 | 23 | 24 | 11 |
| 12 | 25 | 26 | 13 |
| 14 | 27 | 28 | 15 |
| GND | 29 | 30 | GND |
| CLK | 31 | 32 | GND |
| $\overline{\text{BSAK}}$ | 33 | 34 | $\overline{\text{MEMX}}$ |
| $\overline{\text{IRD}}$ | 35 | 36 | $\overline{\text{IWR}}$ |
| $\overline{\text{MRD}}$ | 37 | 38 | $\overline{\text{MWR}}$ |
| RSIN | 39 | 40 | INT (H) 1 |
| INT (H) 2 | 41 | 42 | INT (L) |
| + 5V | 43 | 44 | $\overline{\text{RSET}}$ |
| + 5V | 45 | 46 | + 5V |
| $\overline{\text{DRQ (F)}}$ | 47 | 48 | $\overline{\text{DRQ (S)}}$ |
| $\overline{\text{RDY (F)}}$ | 49 | 50 | $\overline{\text{RDY (S)}}$ |
| $\overline{\text{WAIT}}$ | 51 | 52 | $\overline{\text{IWS}}$ |
| $\overline{\text{DAK (F)}}$ | 53 | 54 | $\overline{\text{DAK (S)}}$ |
| $\overline{\text{EOP (F)}}$ | 55 | 56 | $\overline{\text{EOP (S)}}$ |
| + 12V | 57 | 58 | + 12V |
| GND | 59 | 60 | GND |

9.2 Description of Signals

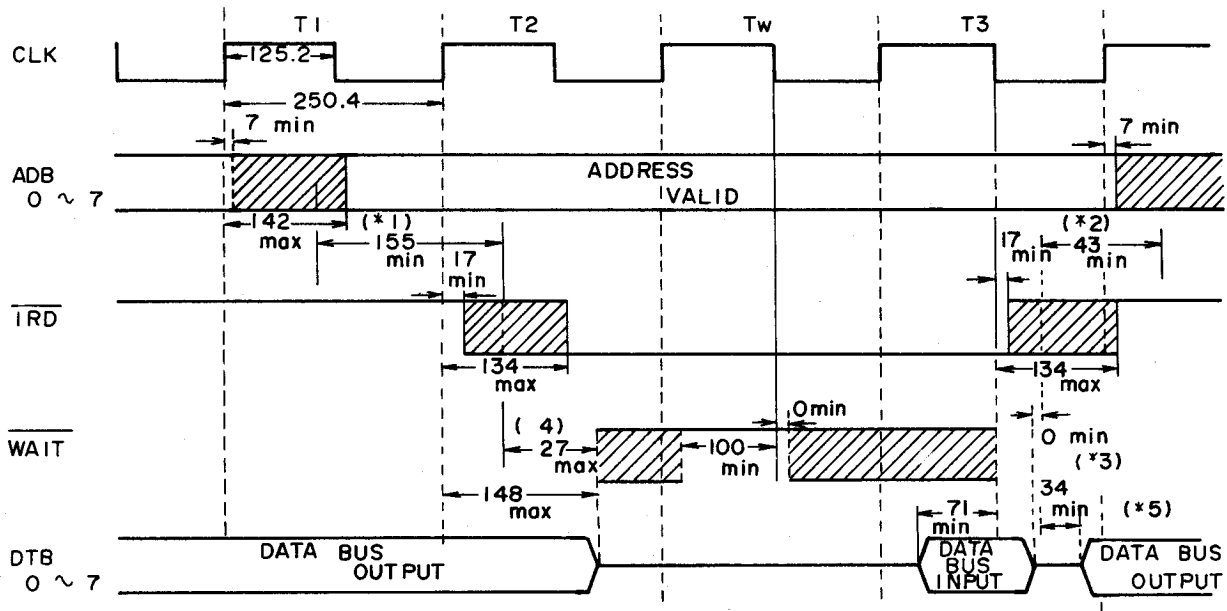
| Signal | Pin No. | Description |
|--|---------------------------------|---|
| GND | 1, 2, 29, 30, 32, 59, 60 | Potential OV. Return lines of respective power supplies (+ 5, + 12, - 12). All pins are connected to the signal ground on the main board. |
| DTB 0 DTB 7 ADR 0 ADR 15 CLK | 3 ~ 10 13 ~ 28 31 | DATA BUS. Input/Output signals. These are buffered by the bidirectional buffer on the main board. All of these are output signals except for data input from the option slot. ADDRESS BUS. Output signals. These signals designate memory addresses and an input/output device. SYSTEM CLOCK. Output signal. It is the main system clock (3.9936 MHz). The phase is the same as that supplied to the CPU. |
| $\overline{\text{BSAK}}$ | 33 | BUS ACKNOWLEDGE. Output signal. This is a bus acknowledgement signal for CPU. When LOW, this signal indicates that the DMA is operating. |
| $\overline{\text{MEMX}}$ | 34 | EXTERNAL MEMORY SELECT. Output signal. When Low, this signal indicates that memory at the option slot has been selected. |
| $\overline{\text{IRD}}$ | 35 | I/O READ. Output signal. Set to LOW for data input from an I/O device; the CPU receives data at the rising edge of the signal. |
| $\overline{\text{IWR}}$ | 36 | I/O WRITE. Output signal. Set to LOW for data output to an I/O device. |
| $\overline{\text{MRD}}$ | 37 | MEMORY READ. Output signal. Set to LOW for data input from memory; the CPU receives data at rising edge of the signal. |
| $\overline{\text{MWR}}$ | 38 | MEMORY WRITE. Output signal. Set to LOW level for data output to memory. |
| $\overline{\text{RSIN}}$ | 39 | RESET IN. Input signal. Input of this signal from the option side resets the CPU when the signal goes LOW, while the reset operation ends when the signal is set to HIGH. |
| INT (H) 1 INT (H) 2 | 40 41 | HIGH PRIORITY EXTERNAL INTERRUPT. Input signals. High priority interrupts applied when signals are set to HIGH. These signals are connected to the 8259 on the main board. |
| INT (L) | 42 | LOW PRIORITY EXTERNAL INTERRUPT. Input signal. This signal is used in the same manner as INT (H), but the priority of the interrupt is low. |

| Signal | Pin No. | Description |
|-----------------------------|------------|---|
| $\overline{\text{RSET}}$ | 44 | RESET. Output signal. This signal initializes the device at the option slot. When the system is in the reset condition, this signal is set to LOW. |
| $\overline{\text{DRQ (F)}}$ | 47 | DMA REQUEST. Input signals. These signals are set to LOW to request DMA transfer from a device at the option slot. DRQ (F) has a higher DMA request level than DRQ (S). |
| $\overline{\text{DRQ (S)}}$ | 48 | |
| $\overline{\text{RDY (F)}}$ | 49 | DMA READY. Input signals. WAIT can be applied to the DMA controller by setting these signals to LOW. RDY (F) and RDY (S) correspond to DRQ (F) and DRQ (S), respectively. |
| $\overline{\text{RDY (S)}}$ | 50 | |
| $\overline{\text{WAIT}}$ | 51 | WAIT. Input signal. CPU operation can be interrupted by setting this signal to LOW. |
| $\overline{\text{IWS}}$ | 52 | I/O WRITE SHORT. output signal. Used when the IWR signal does not provide sufficient time to write data from an external memory to an I/O device during a DMA transfer. |
| $\overline{\text{DAK (F)}}$ | 53 | DMA ACKNOWLEDGE. Output signals. When the DMA controller receives DRQ, these signals are set to LOW when the DMA is started. DAK (F) and DAK (S) correspond to DRQ (F) and DRQ (S), respectively. |
| $\overline{\text{DAK (S)}}$ | 54 | |
| $\overline{\text{EOP (F)}}$ | 55 | END OF PROCESS. Output signals. These signals indicate the end of 1 block during a DMA transfer. They are set to LOW together with DAK when the last byte is sent. EOP (F) and EOP (S) correspond to DRQ (F) and DRQ (S), respectively. |
| $\overline{\text{EOP (S)}}$ | 56 | |
| + 5V | 43, 45, 46 | + 5V power supply lines. (Up to 2.5A.) |
| + 12V | 57, 58 | + 12V power supply lines. (Up to 0.5A.) |
| - 12V | 11, 12 | - 12V power supply lines. (Up to 0.5A.) |

9.3 I/O Port Access Timing

① I/O Read Timing

[Unit: nsec]

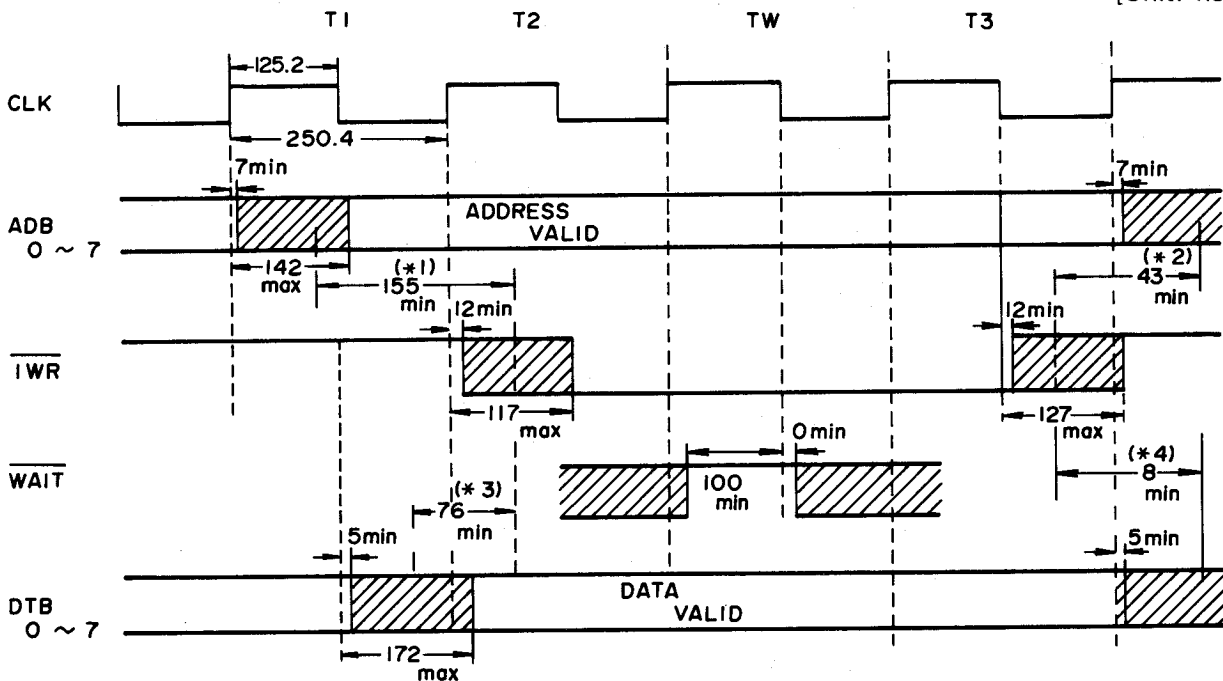


- (*1) Address stabilization prior to $\overline{\text{IRD}}$.
- (*2) Address holding time after $\overline{\text{IRD}}$.
- (*3) Data holding time after $\overline{\text{IRD}}$.
- (*4) Delay before float after $\overline{\text{IRD}}$.
- (*5) Floating hold time after $\overline{\text{IRD}}$.

Note: The data bus is normally in the output state, and serves as an input terminal only when data is output from the option side.

② I/O Write Timing

[Unit: nsec]

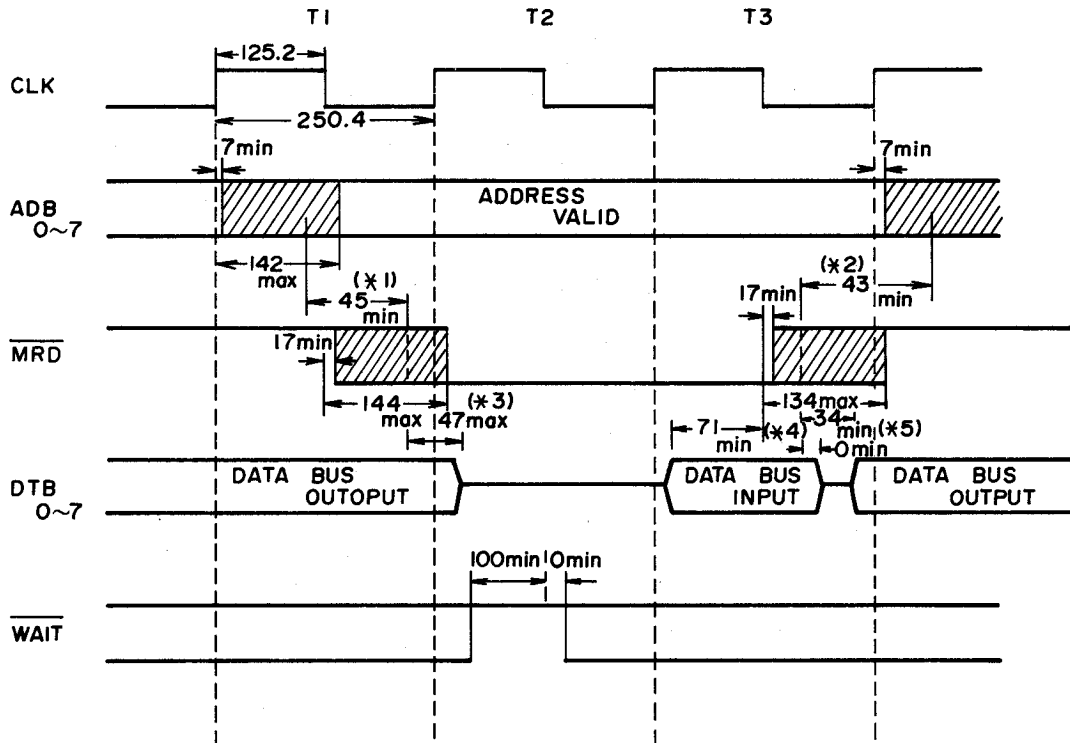


- (*1) Address stabilization prior to $\overline{\text{IWR}}$.
- (*2) Address holding time after $\overline{\text{IWR}}$.
- (*3) Data stabilization after $\overline{\text{IWR}}$.
- (*4) Data holding timing prior to $\overline{\text{IWR}}$.

9.4 Memory Access Timing

① Memory read timing

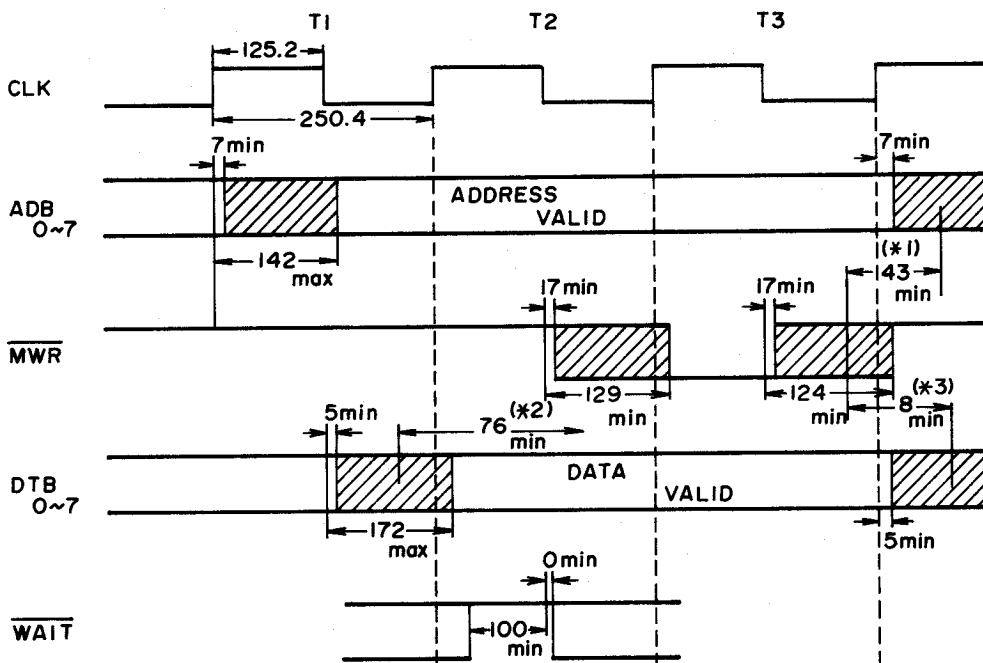
[Unit: nsec]



- (*1) Address bus stabilization time preceding the falling edge of $\overline{\text{MRD}}$.
- (*2) Address bus holding time following the rising edge of $\overline{\text{MRD}}$.
- (*3) Time following the falling edge of $\overline{\text{MRD}}$ before the data bus starts floating.
- (*4) Data bus holding time following the rising edge of $\overline{\text{MRD}}$.
- (*5) Data bus floating time following the rising edge of $\overline{\text{MRD}}$.

② Memory write timing

[Unit: nsec]

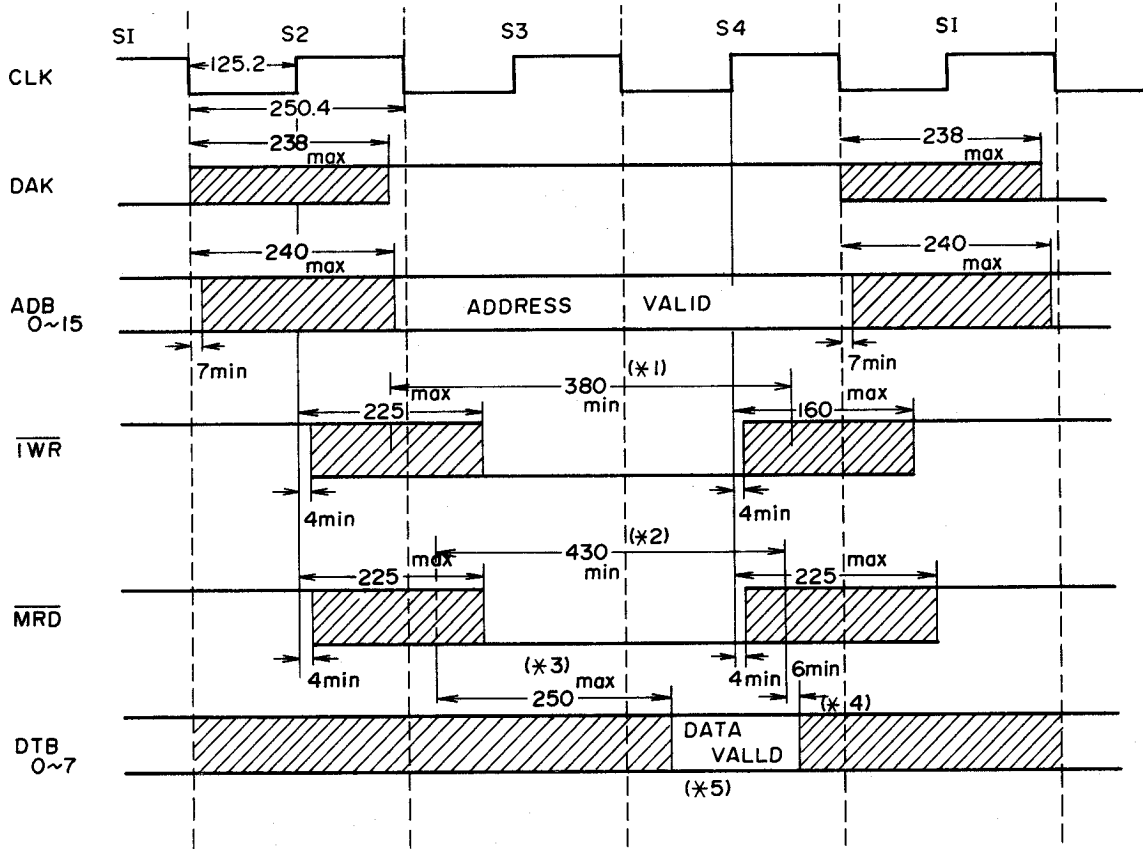


- (*1) Address bus holding time following the rising edge of $\overline{\text{MWR}}$.
- (*2) Data bus stabilization time preceding the falling edge of $\overline{\text{MWR}}$.
- (*3) Data bus holding time following the rising edge of $\overline{\text{MWR}}$.

9.5 DMA Access Timing

① Memory read, I/O write timing

[Unit: nsec]



(*1) Low level pulse width of IWR

(*2) Low level pulse width of MWR

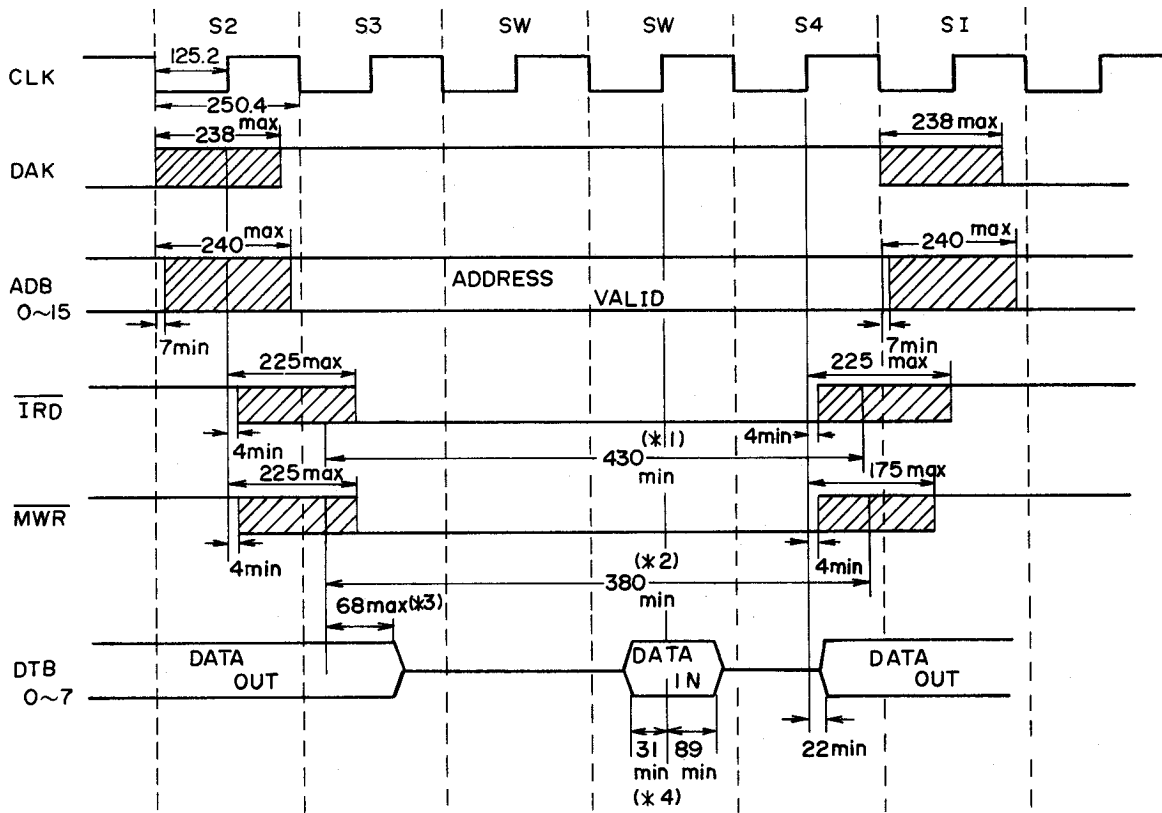
(*3) Data bus stabilization time following the falling edge of MRD

(*4) Data bus holding time following the rising edge of MRD

(*5) Data from internal memory to I/O in DMA

② I/O read, memory write timing

[Unit: nsec]



(*1) Low level pulse width of IRD

(*2) Low level pulse width of MWR

(*3) Time following the falling edge of MWR before the data bus starts floating

(*4) Limitation of input data from I/O to internal memory

9.6 I/O Port Address Map for Options

The addresses of I/O ports allocated for options are from 80H to FFH. Of these, some are already assigned to existing interface cards. Therefore, when other option cards are prepared, contact the Electronic Instruments Design Dept. of the EPSON Corporation for confirmation that the addresses are free. (This precaution must be observed to prevent the same port from being allocated to more than one option.)

| Port address | 0 | 1 | 2 | 3 |
|----------------------|--------------------------------------|---|-----------------------|-------|
| 80 84 | | | | |
| 88 8C | GPIB interface | | | |
| 90 | | | | Q10IE |
| 94 98 | Memory box (optical fiber) interface | | | Q100F |
| 9C | Pulse transformer interface | | | Q10PT |
| A0 | AD/DA interface | | | Q10AD |
| A4 A8 AC | RS 232C interface | | | Q10RS |
| B0 B4 | Direct modem interface | | | Q10DM |
| B8 BC | | | | |
| C0 | Bar code, drawer interface | | | |
| C4 C8 CC | | | | |
| D0 D4 D8 DC | | | | |
| E0 E4 E8 EC | | | | |
| F0 F4 | | | | |
| F8 | 1st level kanji Q10K1 | | 2nd level kanji Q10K2 | |
| FC | Multifont Q10 MF | | | |

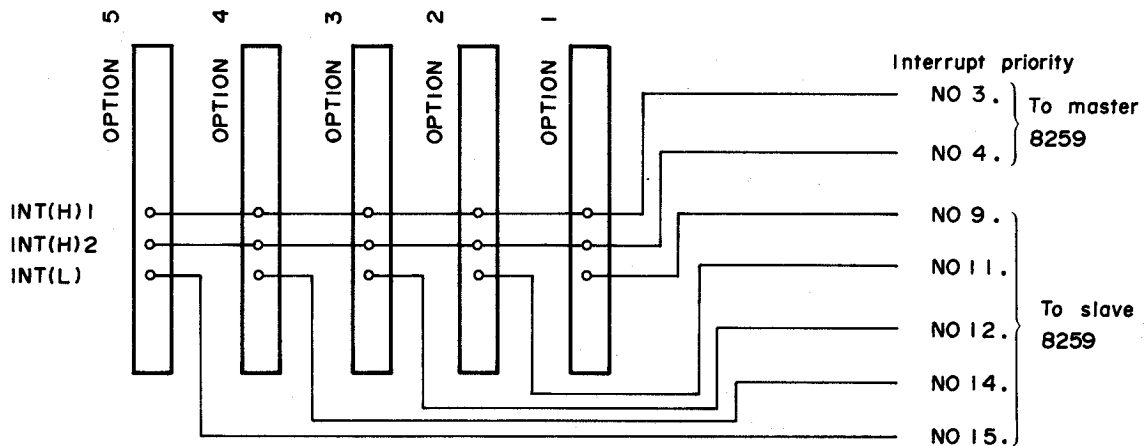
9.7 Cautions for Interface Preparation

Take note of the following when preparing option cards.

- ① \overline{RSIN} is the input signal for system reset. Since this signal is directly input to the CPU reset terminals with no particular synchronization, it is recommended that it be synchronized with the rising edge of the read/write pulse and that the pulse width be held to less than 1 mS when D-RAM data is to be saved, however, note that the pulse width must be greater than three clocks.

- ② Difference between INT(H) and INT(L)

Although there are three types of interrupt request signals (INT(H)1, INT(H)2, and INT(L)) for each option connector, INT(H)1 and INT(H)2 are common to all of the connectors. Therefore, only one card which utilizes INT(H)1 or 2 can be used at any given time. However, since INT(L) is assigned to the various connectors individually, it can be used with several cards simultaneously. Connection of the INT(H) and INT(L) interrupts on the main board is shown below.



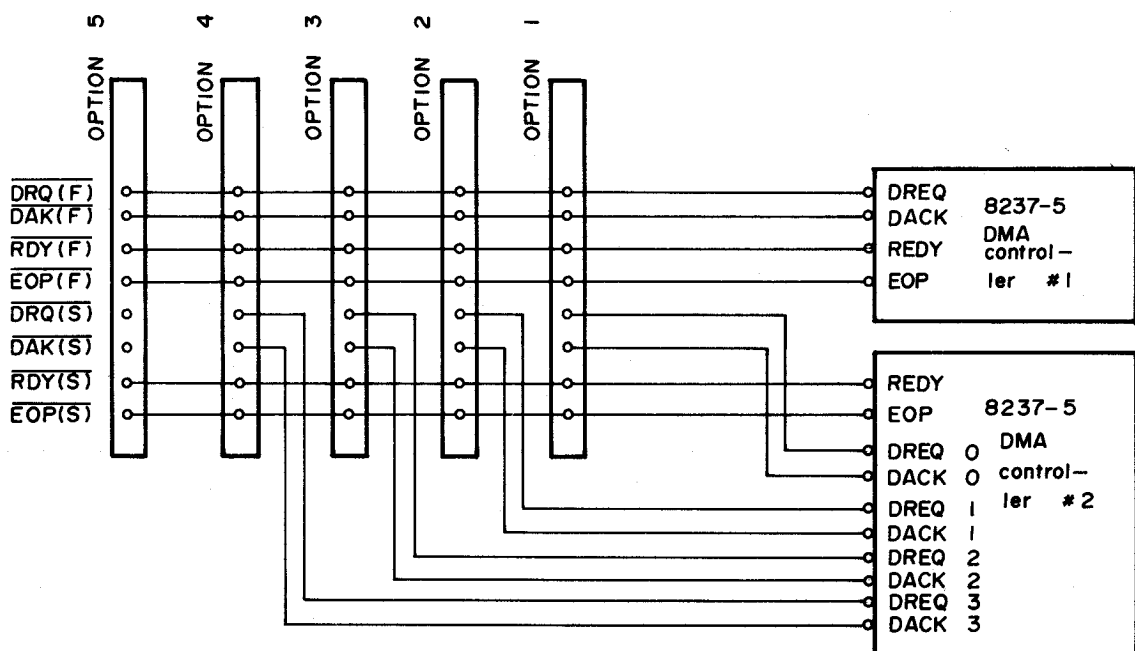
- ③ Difference between $\overline{DRQ(F)}$ and $\overline{DRQ(S)}$

There are also two types of DMA request signals for each option connector, $\overline{DRQ(F)}$ and $\overline{DRQ(S)}$. $\overline{DRQ(F)}$ is common to all of the connectors, while $\overline{DRQ(S)}$ is assigned individually. However, $\overline{DRQ(S)}$ and $\overline{DAK(S)}$ are not connected to option connector 5.

Also, $\overline{RDY(F)}$ and $\overline{EOP(F)}$ corresponding to $\overline{DRQ(F)}$ and $\overline{DRQ(S)}$ are common to all of the connectors, as are $\overline{RDY(S)}$ and $\overline{EOP(S)}$.

This is because all the $\overline{DRQ(S)}$ signals use the same DMA controller. Finally, $\overline{DAK(S)}$ is individually assigned to all of the connectors in the same manner as $\overline{DRQ(S)}$.

These relationships are shown in the figure below.



④ Difference between $\overline{\text{BSAK}}$ and $\overline{\text{DAK}}$

Both of these signals are active during DMA operation, but whereas $\overline{\text{BSAK}}$ is active during all DMA operations (i.e., the signal is output even when the CPU is stopped), $\overline{\text{DAK}}$ ($\overline{\text{DAK(F)}}$ or $\overline{\text{DAK(S)}}$) becomes active only when the corresponding $\overline{\text{DRQ}}$ is accepted and that DMA is operating. For this reason, it is recommended that these two signal types be used as follows.

- a. $\overline{\text{BSAK}}$ should be ANDed upon I/O port address decoding and the I/O port non-selected when it is LOW. (This is because the address bus contains a memory address when $\overline{\text{BSAK}}$ is LOW.)
- b. Use $\overline{\text{DAK}}$ for chip selection of the I/O port outputting the corresponding $\overline{\text{DRQ}}$.

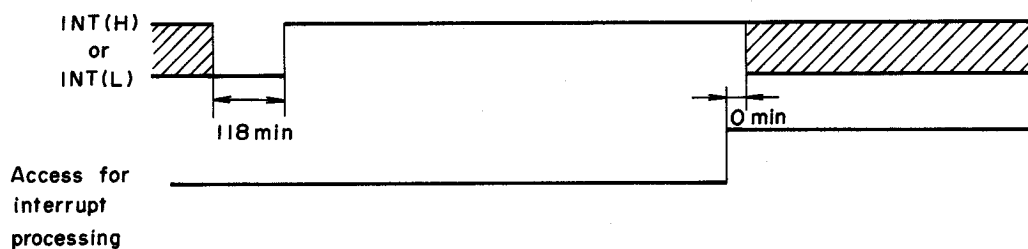
It is particularly important that $\overline{\text{BSAK}}$ is used as described, since incorrect operation will result (regardless of whether the DMA is used) if this processing is not performed.

⑤ $\overline{\text{MEMX}}$ is required when the option card includes memory. This signal becomes LOW when bit 3 in the memory bank register is 1 and neither P-ROM, C-MOS RAM, nor the common area are selected. Thus, programming considerations are necessary when external memory (on the option card) is to be used. In other words, when external memory is to be selected, bit 3 in the memory bank register must be set to 1 and bits 7-4 (the internal memory bank) must be set to 0 so that memory on the main board is not selected. Note must also be taken of the fact that the resident RAM area cannot be placed on external memory.

⑥ Interrupt processing

Interrupts from the option slots are controlled by the INT(H) or INT(L) signals. An 8259A is used as the interrupt controller in the main system, and the INT signals are connected directly to the IR terminal of this 8259A. When the INT signal goes from LOW to HIGH, it must be kept HIGH from its rising edge until the $\overline{\text{INTA}}$ from the CPU has been accepted by the 8259A; however, since the $\overline{\text{INTA}}$ signal is not output to the option connector, the INT signal must also be kept HIGH until interrupt processing is started for that device. Finally, since a rising edge is necessary, be sure to observe the rules concerning the duration of the LOW level for the INT signal. These considerations are outlined in the figure below

[Unit: nsec]



⑦ Notes concerning inclusion of options in the OS

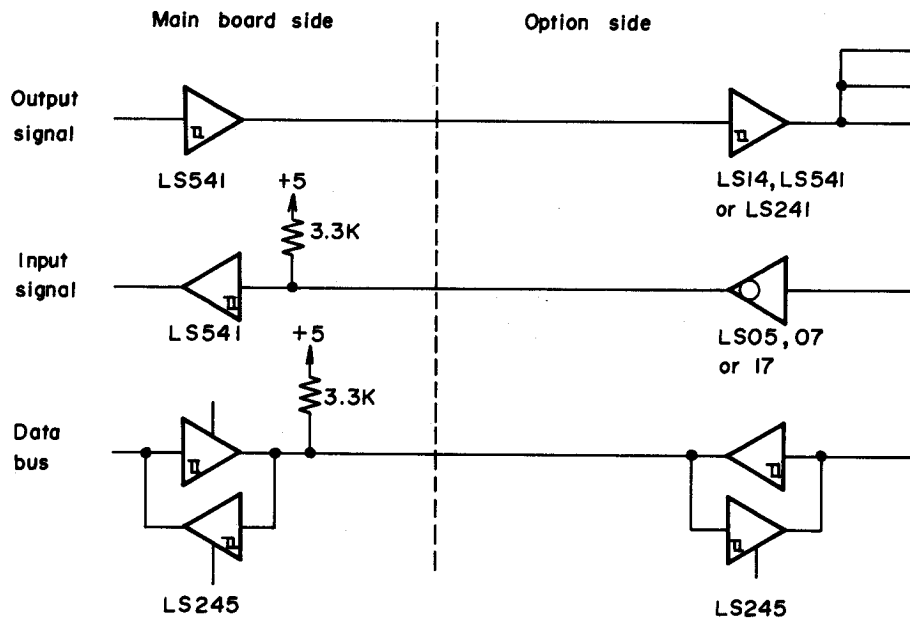
When option cards are prepared, some additional circuits must be provided to make it possible for the OS to determine whether previously reserved options are present, and to allow it to automatically control interrupt tables and so forth. The OS must use the following sequence to determine whether the various options are connected to the option connectors.

First, data is output to the ports designated for each option (with a different port for each option); depending on the option, the content of the data may also be designated. If the applicable option is connected, an interrupt is generated, causing INT(H) or INT(L) to go HIGH. In the case of an INT(L) interrupt, the main system is able to determine the slot to which the card is connected from the interruption address, which differs according to slot number. If the option card is not connected, the OS recognizes the fact because no interrupt is generated.

Therefore, a circuit must be provided so that an interrupt is applied when data is written into one of the port addresses assigned to options controlled by the OS, and to clear the interrupt when that same port is read out.

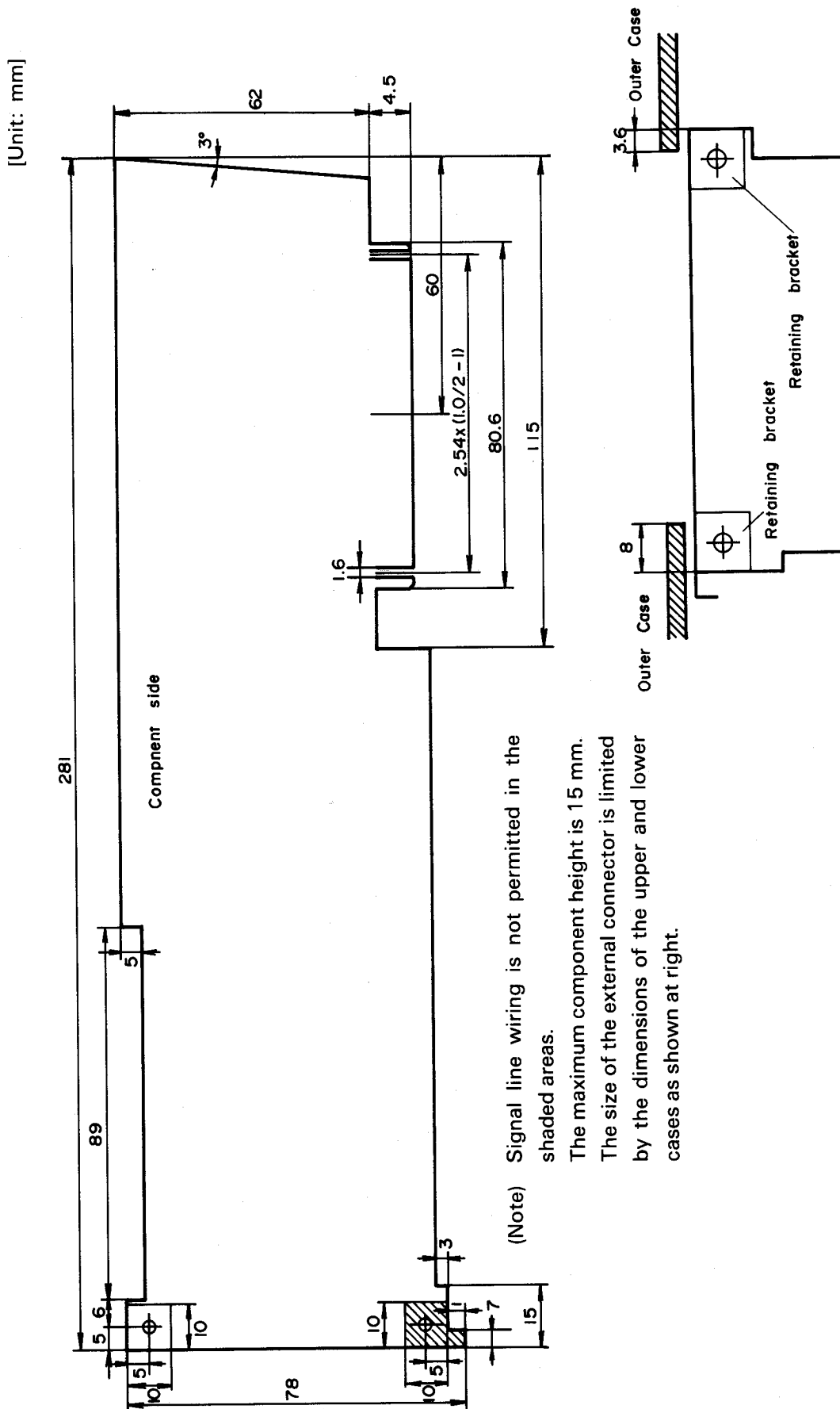
⑧ I/O signal interface

All input signals fed to the main board from the option side are pulled up by 3.3k ohm resistors. These signals (other than bidirectional data bus signals) are received by the 74LS541, and therefore should be controlled by an open collector circuit. The 74LS541 is also used for driving output signals (other than data bus signals) which are fed to the option side from the main board. The option side should be provided with a one-stage buffer for connection of multiple options. I/O switching for the data bus must be controlled by the 74LS245 bidirectional bus buffer on the main board, as well as on the option side. This is to prevent data conflicts. Signal lines which are not used must be left open. The recommended I/O interface circuit is shown below:



9.8 Dimensions

Dimensions of the option card are as follows:



9.9 Requirements for Compliance with FCC (or FTZ) Rules

9.9.1 According to FCC (or FTZ) Rules, certain types of option cards for computers must comply with the limits prescribed in the specifications of FCC (or FTZ) Rules when type tested with each card incorporated in a computer system. Thus, option cards to be fabricated may be subject to approval by the FCC (or FTZ).

For the above reason, those who fabricates the option cards are required to submit to EPSON a sample of any type of option card for any computer of EPSON brand to obtain the consent of our Electronic Instruments Design Department prior to its production. EPSON will in turn determine whether or not the sample of the option card submitted by those is subject to application for approval by the FCC (or FTZ), and if application for approval is required, the application will be filed by EPSON CORPORATION (Japan) or its overseas branch.

9.9.2 Cautions in designing option cards to readily pass FCC (or FTZ) type tests

- (1) CMOS IC's should be used for option cards whenever possible. When use of any CMOS IC is difficult, use LS-TTL or normal TTL design. Never use S- or ALS-TTL.
- (2) GND line and power line patterns on the PC board should be wide enough to minimize power supply impedance.
- (3) The clock frequency should preferably be low with the pulse waveform of as slow rise and fall times as possible.
- (4) When a connector to an external device is required, use a connector of the type with a metallic enclosure and connect the FG (Frame Ground) terminal of the connector firmly to the rear frame of the EPSON QX-10.