FOREWORD

This manual provides an outline of the HX-20 hardware configuration and explains the MONITOR program and its use. The information, drawings, diagrams and data contained in this manual are both accurate and reliable. However, the circuits related to the products not manufactured by EPSON, sample programs, etc. have been inserted merely to facilitate the understanding of the general applications of the HX-20, and thus they are not complete for practical use.

EPSON assumes no responsibility for the infringement of third party's patents resulting from the incorporation of or use of the EPSON HX-20, nor for the infringement of any other rights related thereto.

SECTION 1 HARDWARE

CHAPTER 1 GENERAL

1.1 System Overview

The HX-20 is an all-in type computer which incorporates a liquid crystal display (LCD) and a microprinter in addition to other essential components. It was designed as a portable computer which operates on a built-in battery. As the HX-20 has a great choice of options, the HX-20 system can be configured or expanded with ease according to your specific application.

1.1.1 System configuration

The HX-20 incorporates the following standard equipment:

1. 24-column microprinter
2. Liquid crystal display [20 characters x 4 lines (80 characters)]
3. Typewriter type keyboard (68 keys)
4. RS-232C interface
5. Serial interface
6. Cartridge (ROM or microcassette drive) interface
7. External audio cassette interface
8. Barcode reader interface
9. ROM (32K bytes)
10. RAM (16K bytes)

The HX-20 is thus capable of system configuration with expansibility as shown below.

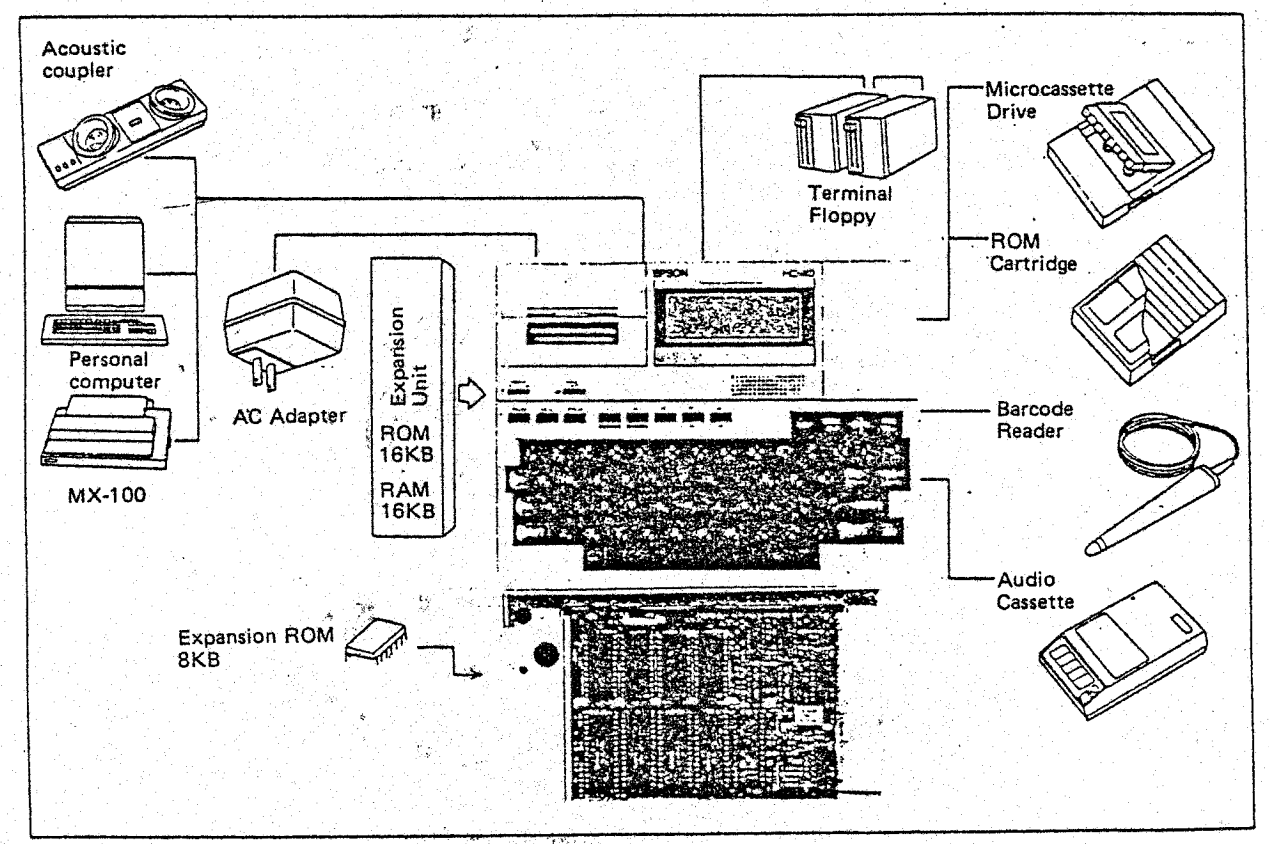


Fig. 1-1 System Configuration

Fig. 1-1 System Configuration

1.1.2 System block diagram

An (8K) ROM can be added to the internal 32K ROM of the HX-20. Other options, however, are connected to the HX-20 via the appropriate interface connectors located inside the portable computer as shown in Figs. 1-3 and 1-4 below.

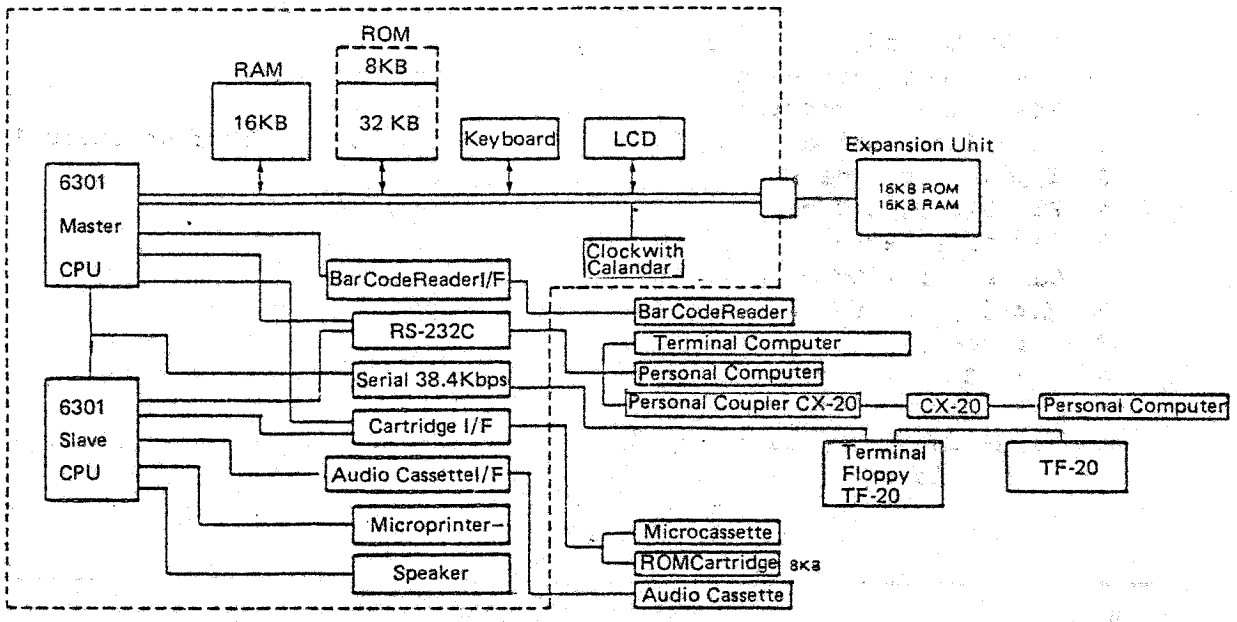


Fig. 1-2 System Block Diagram

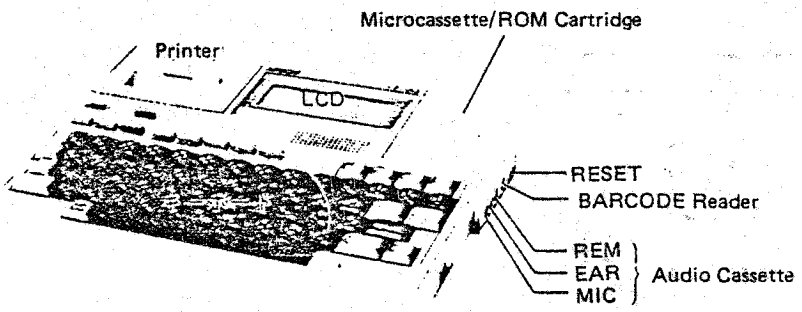


Fig. 1-3 Interface Connectors

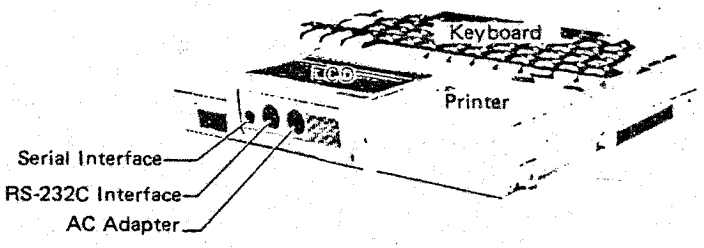


Fig. 1-4 Interface Connectors

1.1.3 Major components

The HX-20 consists of the following 7 major components:

1 MOSU control circuit board (MOSU board)
2 Keyboard unit
3 Liquid crystal display (LCD) panel
4 Microprinter
5 Ni-Cd battery
6 Speaker
7 Case

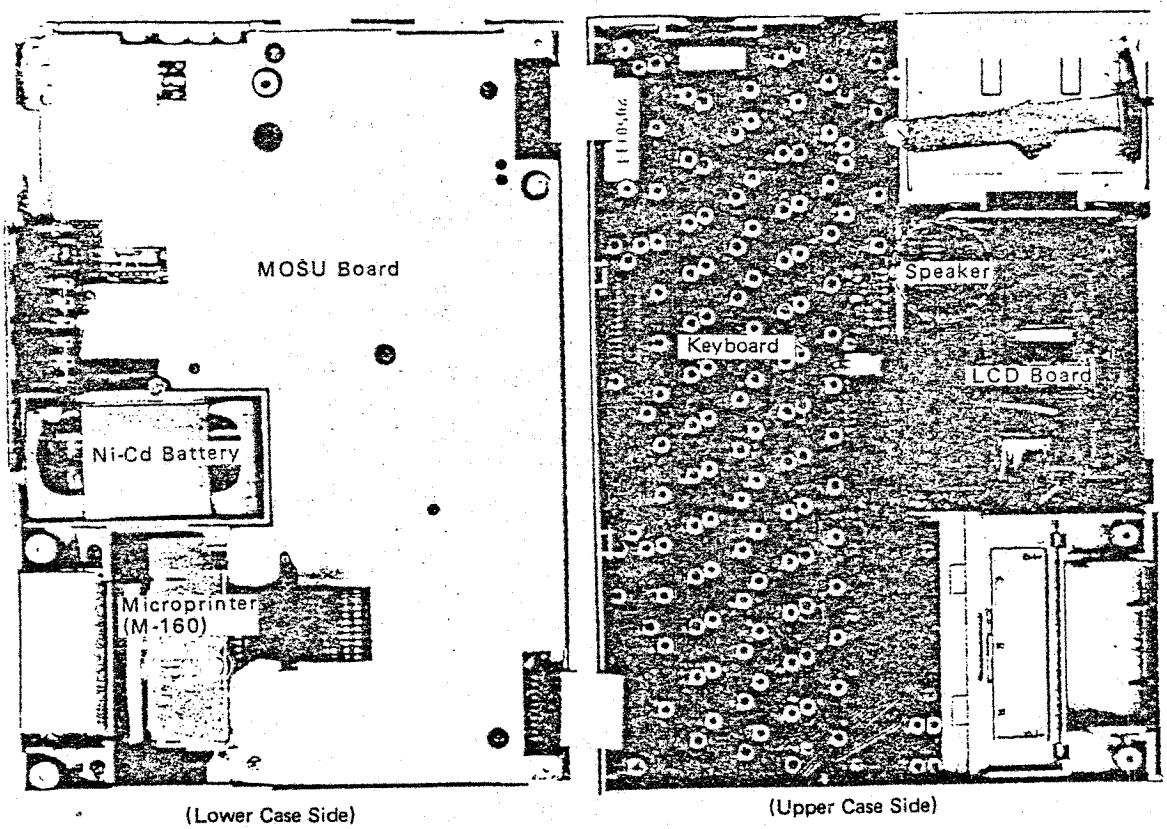


Fig. 1-5 Major Components

(1) On the MOSU board are mounted the connectors for various interfaces such as the RS-232C interface, the serial interface, the external audio cassette interface, the barcode reader interface, the expansion unit interface, and the optional cartridge interface and the AC adapter inlet. The HX-20 controls its components by a dual CPU system which employs two CMOS 6301 CPUs. This enables distributed processing of inputs and outputs and provides upgraded system performance.

(2) On the keyboard unit are mounted the power switch and the view angle control knob for the LCD. The LCD control circuit is located inside the keyboard unit.

1.1.4 Hardware configuration of HX-20

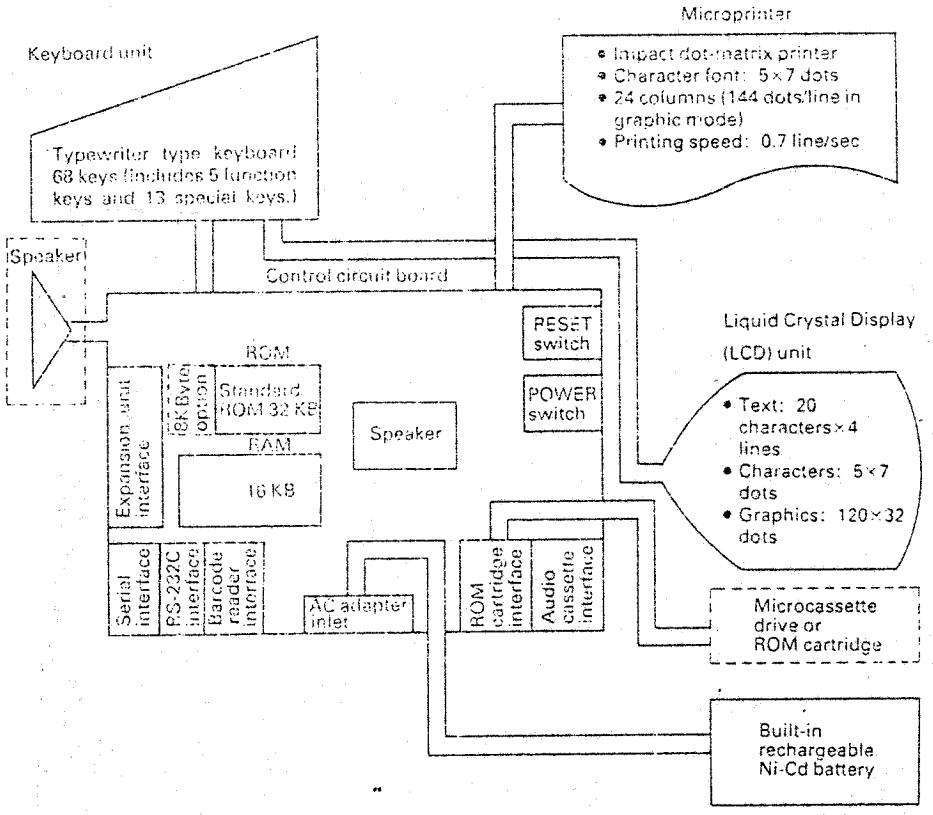


Fig. 1-6 Block Diagram of HX-20

The HX-20 comprises 6 major blocks as shown in the block diagram above; namely, an MOSU control circuit board, a keyboard unit, a microprinter, an LCD unit, a speaker, and a battery power supply. Each block is connected to the control circuit board and housed in the HX-20. A block diagram of the MOSU control circuit board is shown in Fig. 1-7 on the next page.

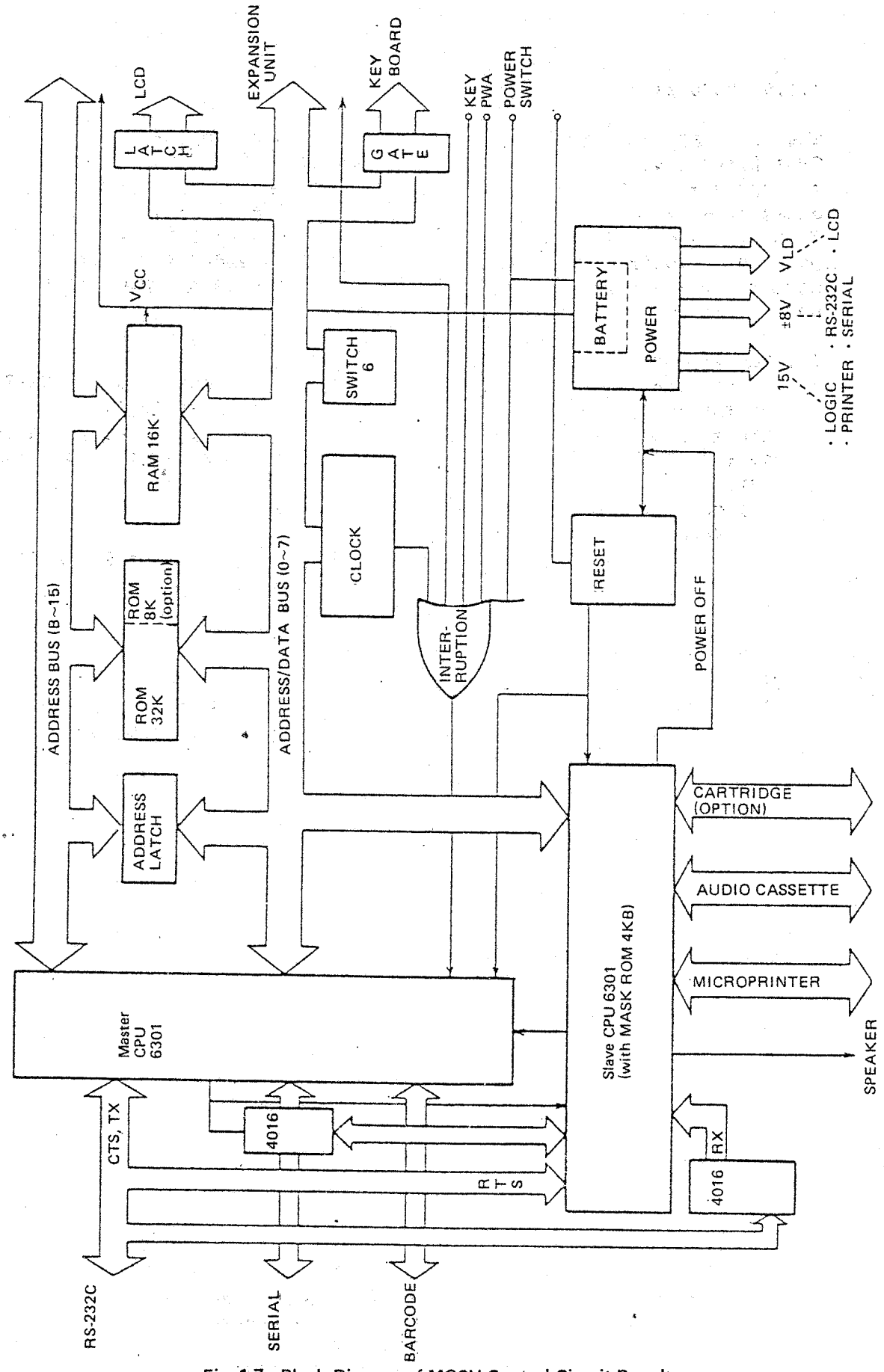


Fig. 1-7 Block Diagram of MOSU Control Circuit Board

1.1.5 MOSU board

The HX-20 adopts a dual CPU system which consists of two CMOS 6301 CPUs located on the MOSU board. Input/output units such as the microprinter, keyboard unit, LCD, etc., are thus controlled by distributed processing between the master CPU and the slave CPU.
Each CPU, the master and the slave, has its own oscillator and control program to control inputs and outputs. Data transfers between the master CPU and the slave CPU are performed through the high-speed serial interface (38,400 BPS).

(1) Master CPU 6301

The master CPU 6301 is a main processor which controls the HX-20 by the program stored in the external ROM (15E to 12E).
The system clock of the master CPU is approx. 1.63 µsec which is generated by an externally connected 2.4576 MHz crystal oscillator.
The master CPU mainly controls the following:

(a) Keyboard
(b) Liquid crystal display (the buffer for display is incorporated in the LCD control circuit board)
(c) Addressing of the built-in ROM and RAM
(d) Barcode reader
(e) Clock function
(f) Serial interface

Note: The master CPU does not use the built-in mask ROM.
The master CPU operates in Expanded Multiplex mode.

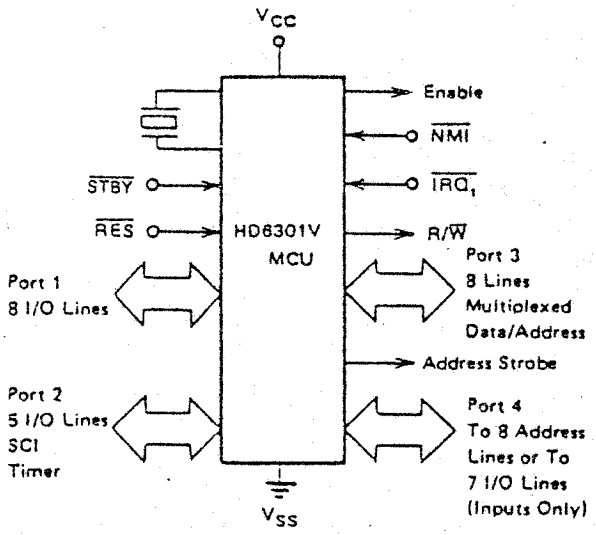


Fig. 1-8 Expanded Multiplex Mode of HD6301V MCU

(2) Slave CPU

The slave CPU has a control program in the built-in mask ROM (4K bytes) and controls input/output units independent of the master CPU.
The slave CPU mainly controls the following:

(a) External audio cassette
(b) Microprinter (M-160)

(c) Barcode reader
(d) RS-232C interface
(e) Optional cartridge (ROM or microcassette drive)
(f) Power ON/OFF

The system clock of the slave CPU is approx. 1.63 μsec. The slave CPU operates in Single Chip Mode:

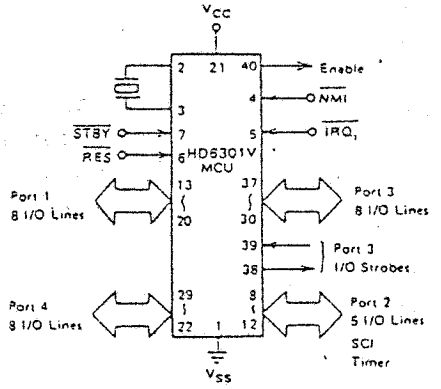


Fig. 1-9 Single Chip Mode of HD6301V MCU

(3) Power Supply Unit

The power supply unit consists of a charging circuit with built-in battery and the AC adapter, a voltage detection circuit, an LCD voltage circuit, an RS-232C voltage circuit, and a backup circuit, all designed to minimize power consumption.

(a) Fuse: 5A fuse for protection against faults by overcurrent.
(b) Charging circuit: This circuit consists of a noise filter, a diode for reverse current protection and a resistor. A zener diode is also connected to the output side of the fuse circuit for overvoltage protection.
(c) Voltage detection circuit: Normally, this circuit monitors the battery voltage after the power has been turned on. When the battery voltage falls below 4.5 volts the circuit outputs a POWER ABNORMAL signal to notify the master CPU of the low voltage condition.
(d) LCD voltage circuit: This circuit generates approx. +7V by DC-DC conversion of the battery voltage to drive the liquid crystal display.
(e) RS-232C voltage circuit: This circuit generates approx. ±8V from the battery voltage which meet the voltage requirements of the EIA Interface Standard RS-232C. This circuit is designed so that ±8V is output only when the RS-232C interface is used. Power on/off control of the circuit is performed by the slave CPU.
(f) Backup circuit: This circuit supplies from the built-in battery, the minimum current required to operate the clock and the components to be used when power is turned on, and also protects the data stored in the RAM while the power switch is being turned off.

(4) Clock

The HX-20 employs a real-time clock (146818RTC) which has clock and calendar functions and is connected directly to the master CPU through the data bus. It uses a 32.768 KHz oscillator as the basic clock.

(5) RAMs

The HX-20 incorporates a total of 8 CMOS RAM chips each with a capacity of 16,384 bits. (2K bytes). The total RAM capacity is thus 16K bytes. The RAMs are backed up by the built-in battery for data retention even when the power is turned OFF.

(6) ROMs

The HX-20 incorporates 4 8K-byte mask ROM chips. The ROM chips contain the BASIC interpreter, OS (Operating System) and machine language monitor.

(7) Switch (SW6)

A 4-pin DIP switch is mounted on the control circuit board. Pin Nos. 1 to 3 are used for selecting character sets. Pin No. 4 is used to specify whether or not the terminal floppy unit is connected (ON: connected, OFF: not connected).

(8) Interrupts

There are two types of interrupts: NMI (non-maskable interrupts) and IRQ (Interrupt request). The NMI interrupts are not used. An IRQ is generated under one of the following conditions.

(a) Keyboard input
(b) Low voltage detection (PWA)
(c) Power switch (PWSW)
(d) External interrupt (INT EXT)
(e) Clock interrupt

(9) System Bus

The system bus consists of an address bus and a data bus. The address bus consists of 16 address lines (0 ~ 15) and a maximum of 64K bytes of addresses are thus accessible directly. Since the 8 low-order address lines (0 ~ 7) are also used as data lines, an address latch is provided to switch between the address and data buses by the appropriate timing.

(10) RS-232C Interface

The USART (Universal Synchronous/Asynchronous Receiver/Transmitter) IC's (75188 and 75189) are used for the RS-232C interface. +8V and -8V are used as the signal levels of the RS-232C interface. The operation of the interface is controlled by both the master CPU and the slave CPU. Through this interface, data can be transferred at bit rates ranging from 110 BPS to 4,800 BPS.

(11) Serial Interface

The Serial Communication Interface (SCI) is used to connect the master CPU with the slave CPU. Interfacing between the master CPU and the slave CPU or between the master CPU and an external unit is switched under software control.
Through the serial interface, data can be transferred at bit rates ranging from 38,400 BPS to 150 BPS.
The operation of this interface is controlled by the master CPU.
The serial interface is not supported by BASIC.

(12) Connector Locations

There are 12 connectors in the HX-20: 9 on the MOSU board 2 on the keyboard, and 1 at the optional cartridge section. The location and description of each connector is given in the figure and table below.

Table 1-1 Connectors on the MOSU Board

Connector	No. of pins	Connection
CN1	5	Serial interface
CN2	8	RS-232C
CN3	2	AC adapter
CN4	20	Keyboard
CN5	20	Keyboard
CN6	20	Microprinter
CN7	40	Expansion unit
CN8	14	Optional cartridge
CN9	2	Built-in battery

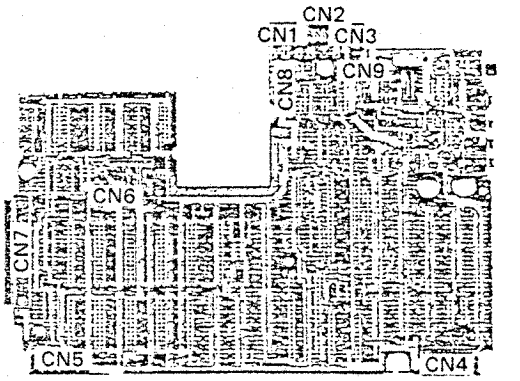


Fig. 1-10 Rear View of MOSU Board

1.2 Input/Output Interfaces

1.2.1 Interface control

The input/output interfaces are controlled by the master CPU and the slave CPU as shown in Fig. 1-11.

(1) Control by the master CPU: LCD and keyboard

(2) Control by the slave CPU: Speaker, external audio cassette and M-160 microprinter

(3) Control by both CPUs: High-speed serial interface, RS-232C interface, cartridge interface (option) and barcode reader interface

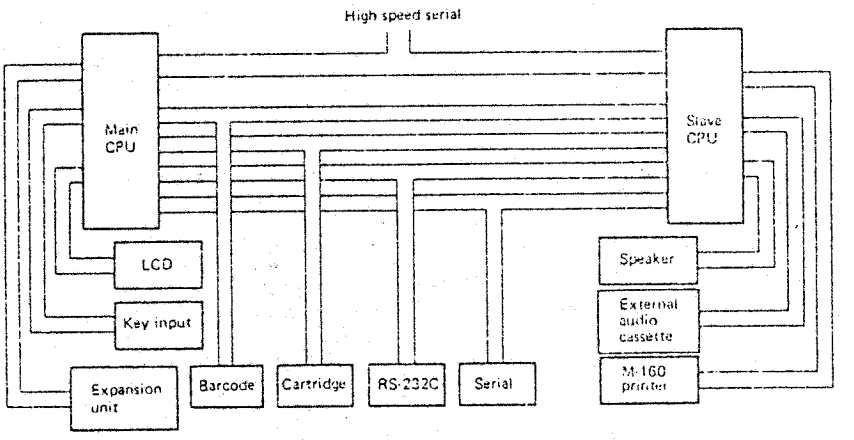


Fig. 1-11 Relationship between CPUs and I/O Operations

The following 6 interfaces are open to external units.

Table 1-2 External Interfaces

Interface	Connector Type	Specification of Connector	No. of Signal Lines (including Voltage and GND Lines
Barcode Reader	Jack 3.50 (x1) 3-position		3
Optional cartridge	Plug-in connector		14
RS-232C	8-pin DIN	TCS4480	8
Serial	5-pin DIN	TCS4450	5
External Audio Cassette	Jack 3.50 (x2) 2.50 (x1)		6
Expansion Unit	F/C		40

1.2.2 Interface cables

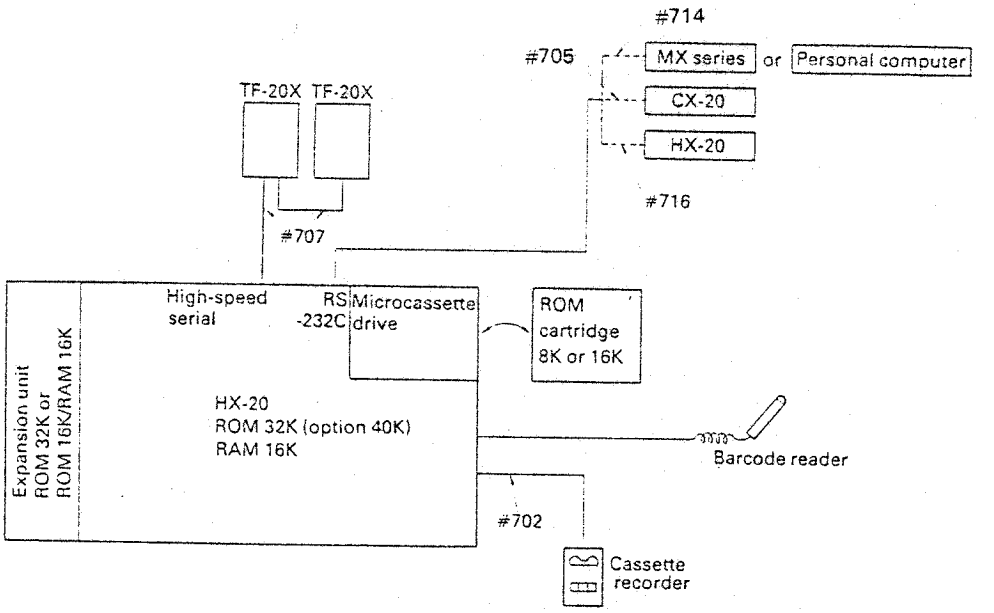


Fig. 1-12 Cable Connection Diagram

Table 1-3 Interface Cables

Cable Set Number	Connection between	Part Number	Connector
#702	HX-20 and External audio cassette	Y201302000	Two 3.5mm dia. plugs and one 2.5mm dia. plug
#705	HX-20 and acoustic coupler	Y201305000	One 8-pin DIN connector and one DB-25 connector
#707	HX-20 and TF-20	Y201307000	One 5-pin DIN connector and one 6-pin DIN connector
#714	HX-20 and Terminal printer (MX series)	Y201309000	One 8-pin DIN connector and one DB-25 connector
#716	HX-20 and HX-20	Y201311000	Two 8-pin DIN connectors

(1) Cable Set #702 (with two 2.5mm dia. jack adapters)

(a) Use: To connect the HX-20 to an external cassette tape recorder

(b) Plugs: 3.5mm dia. (white and red), and 2.5mm dia. (black)

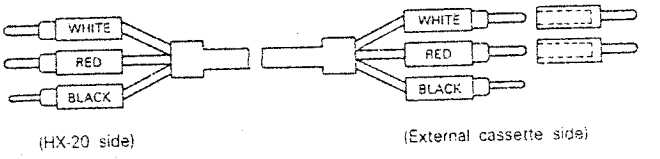


Fig. 1-13

(c) Connection
Connect the HX-20 to the external cassette tape recorder as shown below.
If the diameter of the input jack of the external audio cassette is 2.5mm, connect the plugs using the supplied jack adapter.

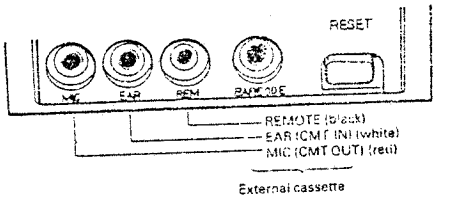


Fig. 1-14

(d) Signal names

Color	Pin No.	Signal Name
Black	1	Shield
	2	Input
Red	1	Shield
	2	Output
Black	1	Remote
	2	Remote

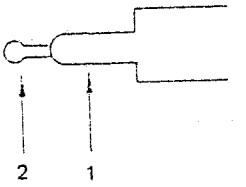


Fig. 1-15

(2) Cable Set #705

(a) Use: To connect the HX-20 to the acoustic coupler.

(b) Connectors:
HX-20 side: 8-pin DIN connector
Coupler side: DB-25 connector (male)

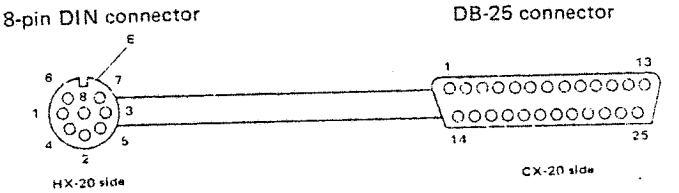


Fig. 1-16

(c) Connection
Plug the DIN connector into the RS-232C interface connector on the rear panel of the HX-20 and the DB-25 connector into the CX-20 interface connector. Then, tighten the two mounting screws with a screwdriver to secure the DB-25 connector to the CX-20.

Fig. 1-17

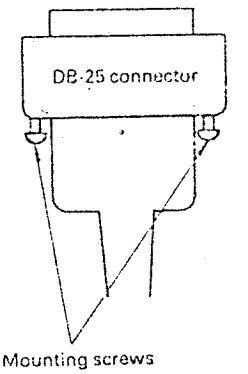


Fig. 1-18

(d) Signal names

8-Pin DIN Connector

Pin No.	Signal Name	Color
1	GND	Black
2	TX	Red
3	RX	Gray
4	RTS	Yellow
5	CTS	Green
6	DSR	Brown
7	DTR	Blue
8	CD	White
E	FG (CG)	(Shield)

DB-25 Connector

Pin No.	Signal Name	Color
1	CG	(Shield)
2	TX	Red
3	RX	Gray
4	RTS	Yellow
5	CTS	Green
6	DSR	Brown
7	GND	Black
8	CD	White
9-19	Unused	-
20	DTR	Blue
21-25	Unused	-

(3) Cable Set #707

(a) Use: To connect the HX-20 to the floppy disk unit.

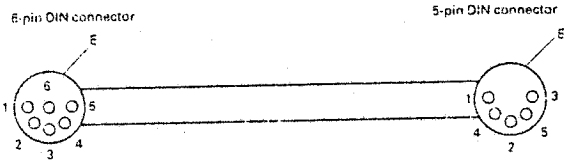
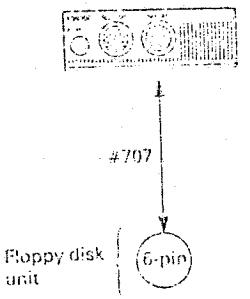


Fig. 1-19

(b) Connectors:

HX-20	Floppy disk unit
(5-pin DIN)	(6-pin DIN)



(c) Connection

Plug the DIN connectors on both sides into the corresponding interface connectors.

Fig. 1-20

(d) Signal names

6-Pin DIN connector

Pin No.	Signal Name	Color
1	PRX	White
2	PIN	Green
3	PTX	Red
4	POUT	Yellow
5	SG (Signal Ground)	Black
6	Unused	-
E	FG (CG)	(Shield)

5-Pin DIN connector

Pin No.	Signal Name	Color
1	SG (Signal Ground)	Black
2	PTX	Red
3	PRX	White
4	POUT	Yellow
5	PIN	Green
E	FG (CG)	(Shield)

(4) Cable Set #714

(a) Use: To connect the HX-20 to the MX-series terminal printer.

(b) Connectors
HX-20 side: 8-pin DIN connector
Printer side: DB-25 connector (male)

(c) Connection
Plug the DIN connector into the RS-232C interface connector and the DB-25 connector into the interface connector of the terminal printer.

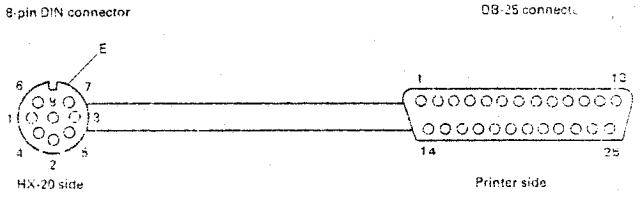


Fig. 1-21

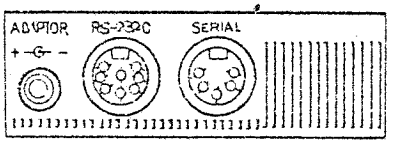


Fig. 1-22

(d) Signal names

8-Pin DIN

Pin No.	Signal Name	Color
1	SG (Signal Ground)	Black
2	$\overline{TX}$	Red
3	$\overline{RX}$	White
4	RTS	Brown
5	CTS	Brown
6	DSR	Yellow
7	DTR	Green
8	CD	Blue
E	CG	(Shield)

DB-25 Connector

Pin No.	Signal Name	Color
1	CG	(Shield)
2	$\overline{TX}$	White
3	$\overline{RX}$	Red
4	Not used	Blue
5	Not used	Blue
6	DSR	Green
7	SG (Signal Ground)	Black
8	Unused	Brown
9-19	Unused	-
20	DTR	Yellow
21-25	Unused	-

NOTE: Pin Nos. 4 and 5 are connected within each connector and then connected to the pin No. 8 of the mating connectors.

(5) Cable Set #716

(a) Use: To connect two HX-20 units through the RS-232C interface.

(b) Connectors: Two 8-pin DIN connectors

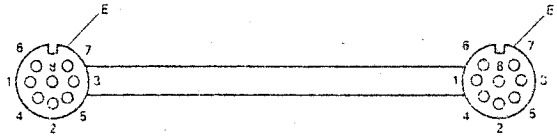


Fig. 1-23

(c) Connection

Plug the DIN connector into the RS-232C interface connector on the rear panel of each HX-20 unit.

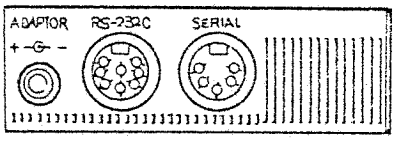


Fig. 1-24

(d) Signal Names

Pin No.	Signal Name	Color
1	SG (Signal Ground)	Black
2	TXD	Red
3	RXD	White
4	RTS	Brown
5	CTS	Brown
6	DSR	Yellow
7	DTR	Green
8	CD	Blue
E	FG (CG)	(Shield)

Pin No.	Signal Name	Color
1	SG (Signal Ground)	Black
2	TXD	White
3	RXD	Red
4	RTS	Blue
5	CTS	Blue
6	DSR	Green
7	DTR	Yellow
8	CD	Brown
E	FG (CG)	(Shield)

Note: Pin Nos. 4 and 5 are connected within each connector and then connected to the pin No. 8 of the mating connectors.

CHAPTER 2 PRINCIPLE OF OPERATION

2.1 Power Supplies

The power supply circuit of the HX-20 is located in the MOSU board. From the battery voltage this circuit generates all the voltages required for various operations in the HX-20.

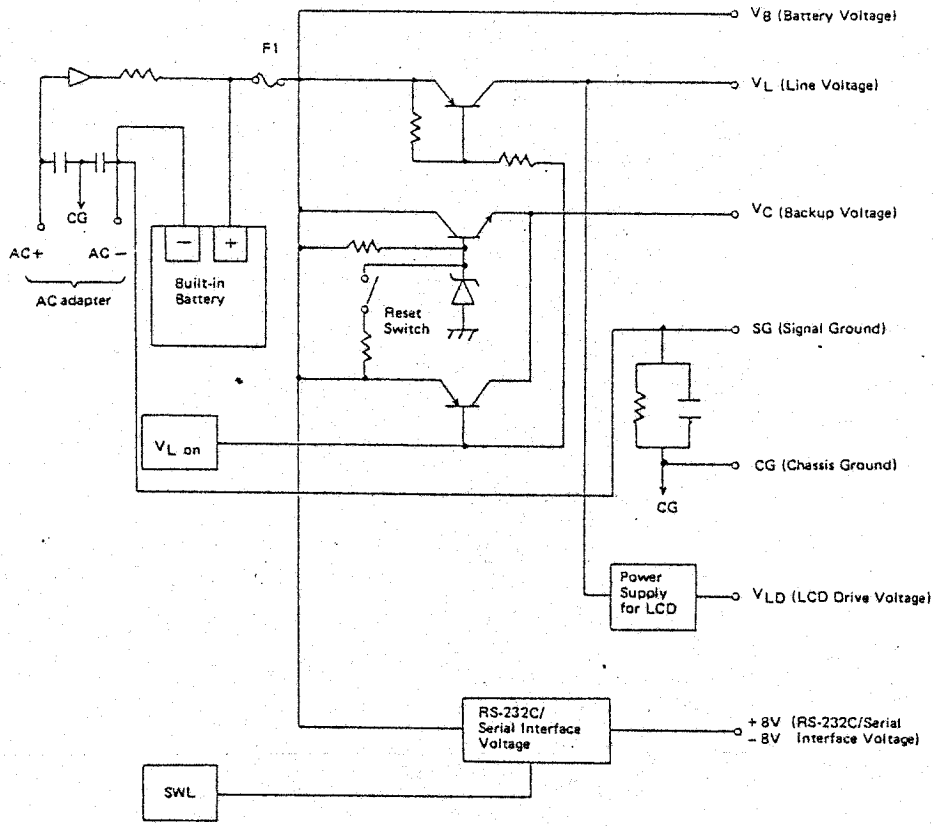


Fig. 2-1 Power Supply Circuit

Table 2-1 Output Voltages

Name	Description	Use
V_B	Output voltage of built-in battery (positive terminal of the built-in battery).	Power supply for built-in printer, expansion unit, V_L, V_C, or ±8V.
V_L	Line voltage. This voltage is generated from V_B when the power switch is turned on.	Voltage for circuit elements or barcode reader.
V_C	Backup voltage. Approx. 3V when the power is turned off and approx. 4.5V when the power is turned on.	Power supply for CMOS RAM, power ON/OFF circuit or reset circuit.
V_{LD}	LCD drive voltage. Approx. 7V is generated from VL when the power switch is turned on.	Power supply for LCD panel
+8V -8V	RS-232C level voltage (-3 to -27V, +3 to +27V). Voltage output starts upon input of an SWL signal.	Power supply for RS-232C or high-speed serial interface.
SG	Signal ground (negative terminal of the built-in battery).	
CG	Protective ground.	

2.1.1 Output voltages

(1) Built-In Battery (SUB C Type)
This battery is a rechargable type battery which is used within a range of 6.0V to 4.0V. The effective output capacity is approximately 1,100 mAH.

(2) V_B (Battery Voltage)
Voltage V_B is a battery voltage which is supplied from the built-in battery via fuse F1 and serves as the power supply for the various voltages to be used within the HX-20. When using the HX-20 with an external interface, this voltage can be output at up to 1.0A.

(3) V_L (Line Voltage)
Voltage V_L is supplied from V_B through the internal transistor Q8 (2SB808G) which is turned on when the power is turned on.
This voltage is used by all the circuit elements except the backed-up elements listed in Table 2-2 below.
When using the HX-20 with an external interface, this voltage can be output at up to 50mA.

(4) V_C (Backup Voltage)
Voltage V_C is used to protect the data stored in the RAM when the power is turned off and to keep the reset circuit in the operating state when the power is turned on.
Approx. 3V is supplied as V_C from V_B through transistor Q7 (2SA1048), when the power is turned off, and approx. 4.5V when the power is turned on.
When using the HX-20 with an external interface, this voltage can be output at up to 40mA.

Table 2-2 Elements Backed Up by V_C

Location	In type	Use
4F	TC40H002	Reset and Enable
5D	TC40H000	RAM R/W and CE
5E	TC40H004	Interrupt circuit
5F	TC4011UBP	Clock and reset circuits
13C~16C	HM6117	2K RAM x 4
12G~15G	HM6117	2K RAM x 4
16D	TC40H138	CE2 output for RAM
6G	HD146818	Real-time clock

(5) V_{LD} (LCD Drive Voltage)
Voltage V_{LD} is generated from line voltage V_L when the power is turned on.

(6) +8V, -8V (RS-232C/Serial Interface Voltage)
This voltage is activated by the slave CPU only when the RS-232C or serial interface (external interface) is to be operated.

2.1.2 Low voltage detection circuit
After the power switch has been turned on, the voltage detecting comparator operates to constantly check the built-in battery for proper voltage while the power switch is in the ON state.

This circuit prevents the HX-20 from operating abnormaly due to a decrease in the battery voltage. When the battery voltage drops below 4.5V, the low voltage detection circuit is activated and an interrupt is applied to the master CPU by an IRQ.

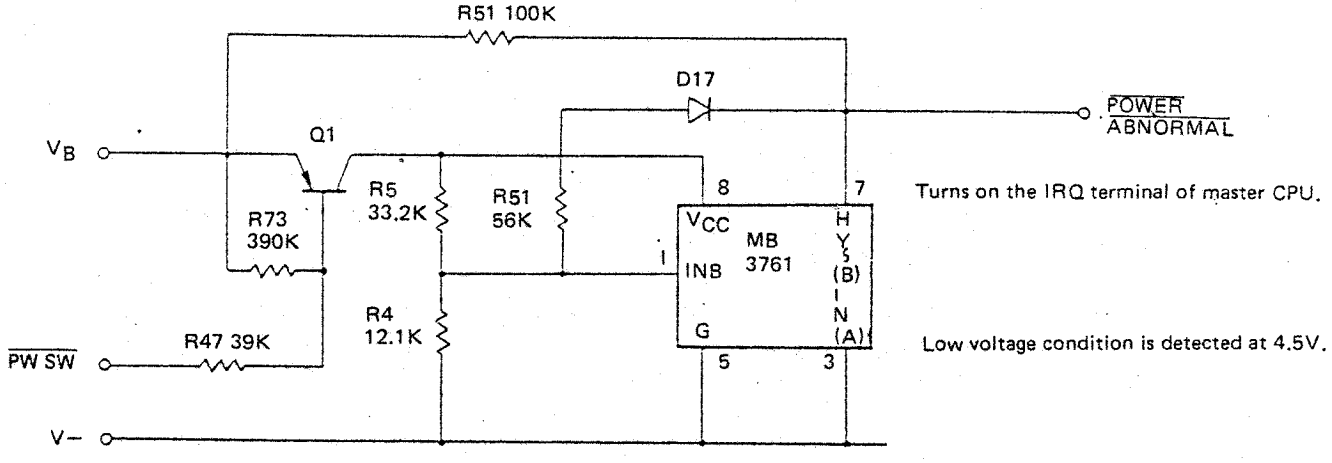


Fig. 2-2 Low Voltage Detection Circuit

2.1.3 Reset circuit
The reset circuit functions to prevent the respective circuit elements (master CPU, etc.) from overruning when power is applied to the HX-20, as well as to initialize the respective circuit elements while the reset circuit is operating.
The reset circuit operates only under the following conditions.

(1) When power is applied.
A $\overline{\text{RESET}}$ signal is output for approx. 30msec after the power switch has been turned on.

(2) When the Reset Switch is pressed.
A $\overline{\text{RESET}}$ signal is output for approx. 30msec while the Reset switch is being pressed and after it has been released.

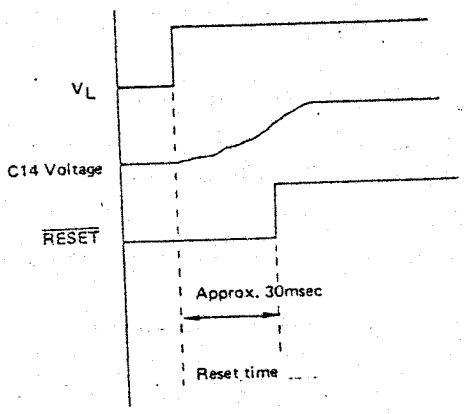


Fig. 2-3 Reset Timing

2.2 CPU Operation
2.2.1 Master CPU and slave CPU

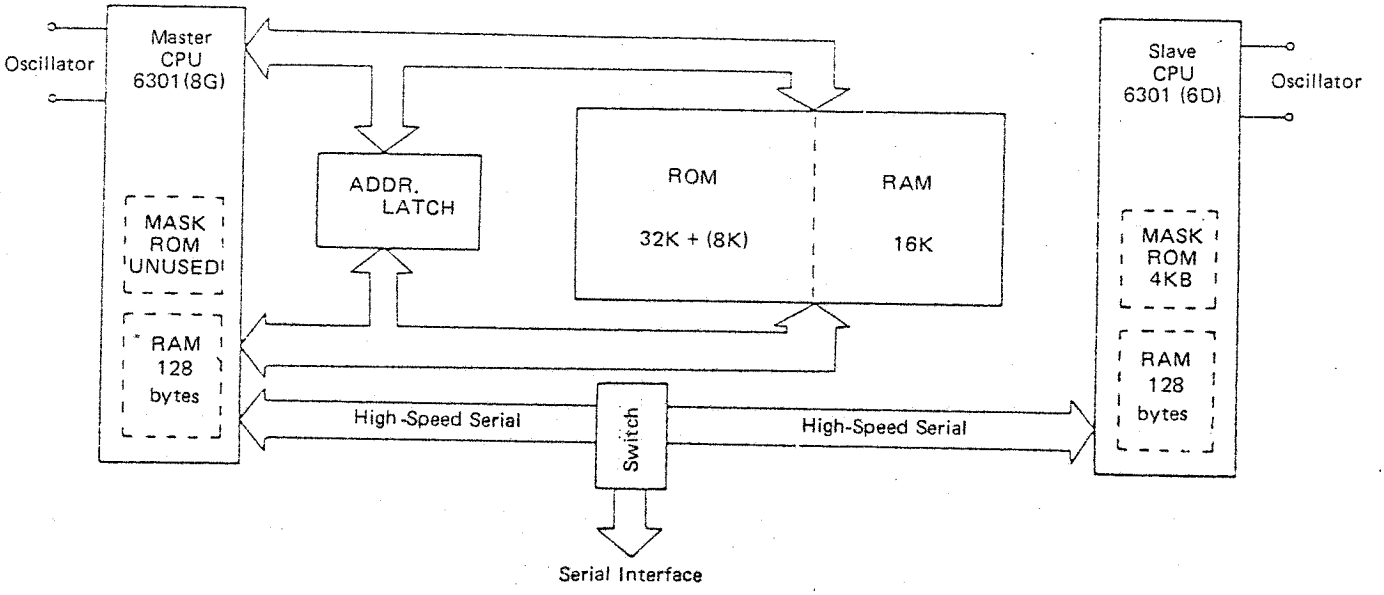


Fig. 2-4 CPU Operation

The HX-20 adopts a dual CPU system in which two 6301 CPUs are used to permit the distributed processing of inputs/outputs.

The master CPU is operated by a control program which is stored in an external ROM. The master CPU controls: (1) keyboard, (2) LCD, (3) ROM/RAM addressing, (4) barcode reader, (5) clock function, etc. The master CPU does not use the built-in mask ROM, but it only uses the program contained in the external ROM to perform the various controls described above.

The slave CPU has a control program in the built-in mask ROM (4KB). The slave CPU operates independently of the master CPU to control: (1) external audio cassette, (2) microprinter, (3) barcode reader, (4) RS-232C interface, (5) high-speed serial interface, (6) optional cartridge, (7) power off, etc. Connected to the master CPU via the high-speed 38,400 BPS serial interface, the slave CPU transmits and receives commands and data which are necessary in performing its control functions.

2.2.2 Operation modes (Memory Allocation)
The operation mode of each CPU must be set by hardware. For this reason, the operation mode of the CPU cannot be changed by software. The operation mode of each CPU is determined by the logic level (high or low) of each signal input to the pin Nos. 8, 9 and 10 of the CPU. The addresses of these pin numbers correspond to the bits 5, 6 and 7 of internal register 0003.

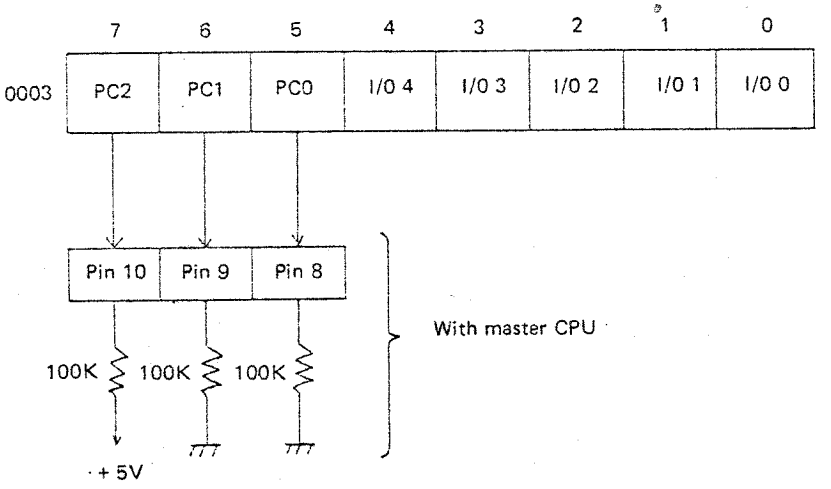


Fig. 2-5 Operation Mode

Notes:

1. Since the master CPU is connected so that pin Nos. 8 and 9 become low and pin No. 10 becomes high, it operates in Mode 4, i.e., Multiplexed/RAM mode.
2. With the slave CPU, pin Nos. 8, 9 and 10 are all connected to +5V through a 100 KΩ resistor. The slave CPU thus operates in Mode 7, i.e., Single Chip mode.

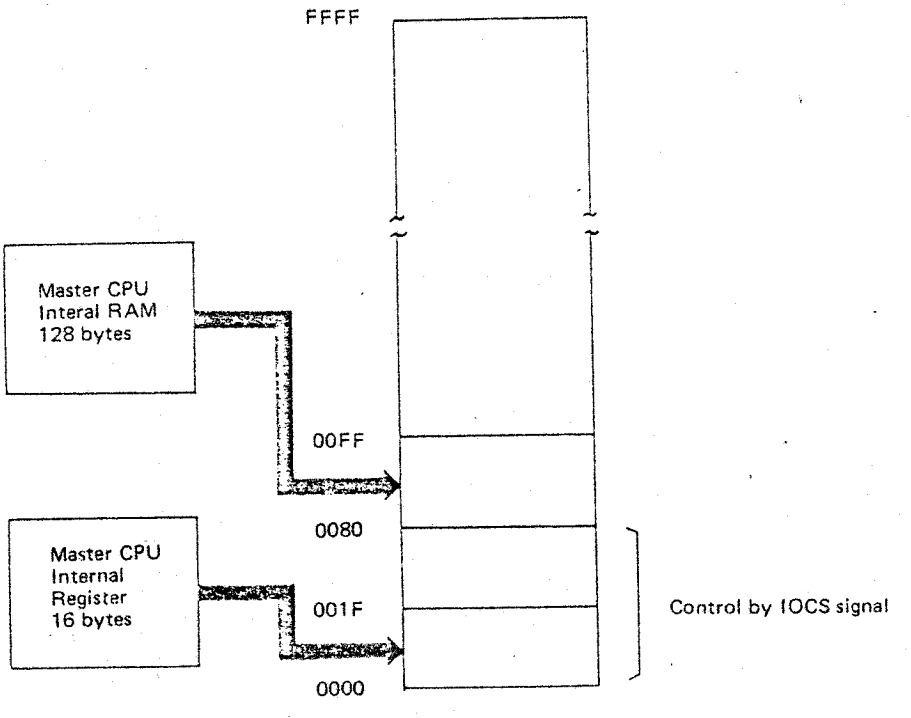
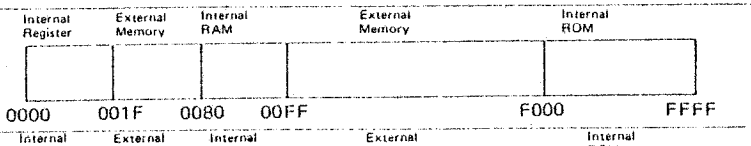
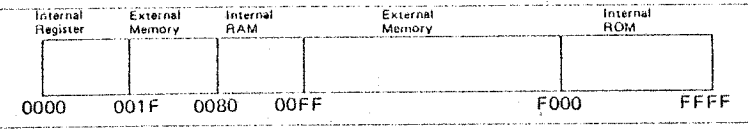
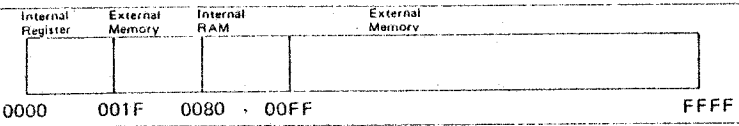
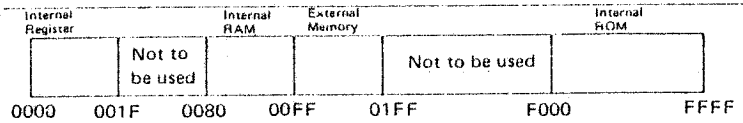
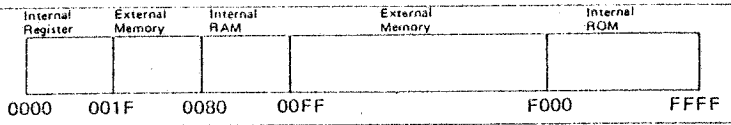
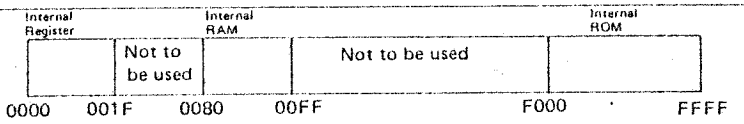


Fig. 2-6 Memory Map of Master CPU
(Multiplexed/RAM Mode 4)

Table 2-3 Operation Modes

Mode	Port			ROM	RAM	Interrupt Vector	Operation Mode	Memory Map	
0	L	L	L	Internal	Internal	Internal (external for 3 cycles after RES goes high)	MULTIPLEXED TEST		This mode is used for testing only. · Does not include addresses 04, 05, 06, 07, and 0F which can be used externally. · Must be free of any overlapped area in internal and external memory spaces.
1	H	L	L	Internal	Internal	Internal	NON-MULTIPLEXED/PARTIAL DECODE		Does not include addresses 00, 02, 04, 06, and 0F which can be used externally.
2	L	H	L	—	—	—	UNUSED		
3	H	H	L	—	—	—	UNUSED		
4	L	L	H	External	Internal	External	MULTIPLEXED/RAM		Does not include addresses 04, 05, 06, 07, and 0F which can be used externally.
5	H	L	H	Internal	Internal	Internal	NON-MULTIPLEXED/PARTIAL DECODE		Does not include addresses 04, 06, and 0F (cannot be used externally).
6	L	H	H	Internal	Internal	Internal	MULTIPLEXED/PARTIAL DECODE		Does not include addresses 04, 05, and 0F which can be used externally.
7	H	H	H	Internal	Internal	Internal	SINGLE CHIP		

2.2.3 Operation timing
The operation timing of the CPU is outlined in Fig. 2-7. For details, see Appendix on "6301V".

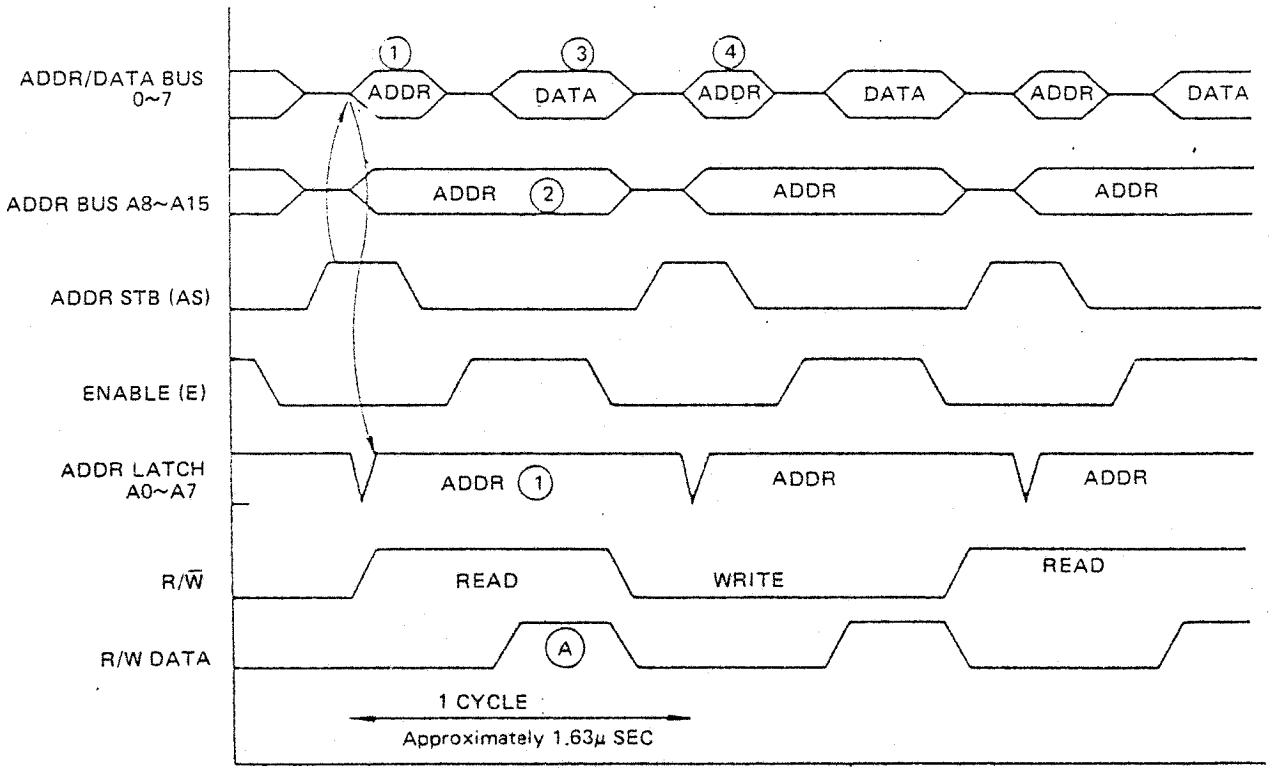


Fig. 2-7 Operation Timing

As an external oscillator is connected to the pin Nos. 2 and 3 of each CPU, the clock frequency (2.4576MHz) obtained from this external oscillator is divided by 4 in the CPU to generate a system clock of approx 1.63μsec. During a read cycle, when address 1 is output to the address/data bus following the output of ADDRESS STROBE signal (AS), the contents of that address are held in the address latch until address 4 is output. When the next address 2 is output, the address of a required data in the ROM will be specified. By outputting ENABLE signal (E) at this point, one byte of data (program) A in the ROM is output on the data bus, which can then be fetched into the 6301 CPU.

To write data, the RAM address must at first be specified in the same way as a data read. Then, if data is output with R/W signal held at Low level, the data can be written into the specified I/O or RAM.

The master CPU has 16 address lines (DA0~A15) and 8 data lines (DA0~DA7). It can thus directly address up to 64K bytes of memory locations. The bus lines are connected to the CPUs and ROM as described in the following section.

2.3 Address Control

2.3.1 Memory addressing

The internal RAM can be addressed by the CE2 (Chip Enable) signal which is output from IC "16D", the address lines (A0~A10: max. 2K bytes can be used) supplied to each RAM chip and CE1 signal. The external RAM can also be addressed by using address lines A0~15 (a maximum of 64K bytes can be used). However, the HX-20 has another RAM or buffer (for master CPU, real-time clock IC146818, LCD μPD7227), which uses the same addresses as the external RAM. For this reason, control signals are required to indicate which RAM is to be used, external or internal.

2.3.2 Address control signals

(1) The basic control signal is an $\overline{\text{IOCS}}$ signal, which must be output to the pin No. 8 of IC "2E". The $\overline{\text{IOCS}}$ signal is output when the address lines used are $\overline{\text{A7}}$ to $\overline{\text{A15}}$. When the signal is output, it indicates that addresses 0000 to 007F are specified.

(2) Auxiliary control signals include IC "9E" and associated I/O address control signals.

(3) Address control CPU

(a) With master CPU

The internal RAM or external RAM of the CPU is controlled by the bit 6 (address 0014) of the RAM control register located in the master CPU. When bit 6 is on, the internal RAM is selected. In this case, the master CPU performs neither data write nor read to or from the external RAM.

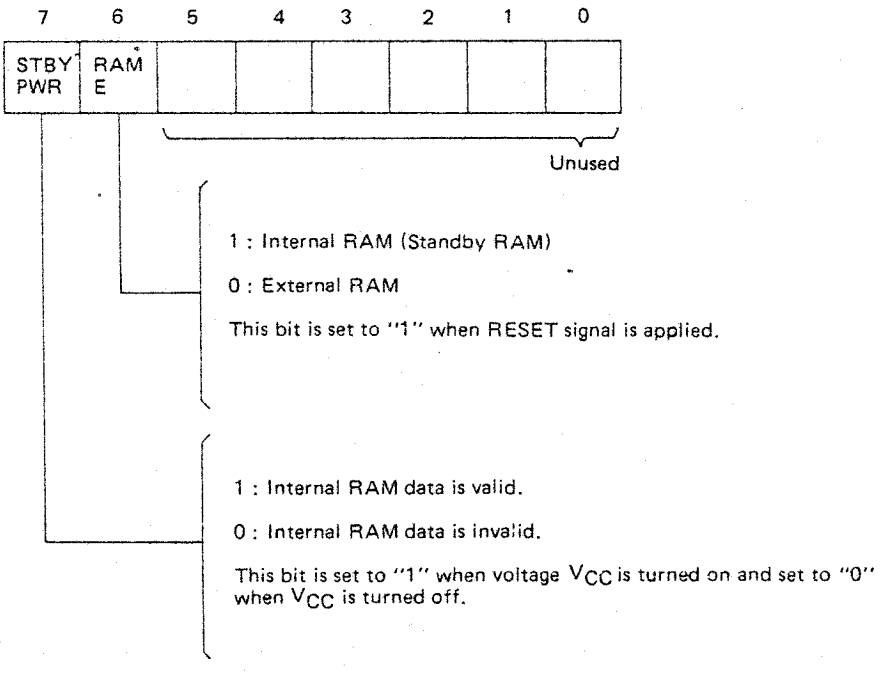


Fig. 2-8 RAM Control Register

(b) With internal RAM or expansion RAM

When IOCS ($\overline{\text{A7}}$~$\overline{\text{A15}}$) is output, it is supplied to the pin No. 9 of IC "4E" and then its inverted signal is output to the pin

No. 8. At this point, under the condition $\overline{A11}$~$\overline{A15}$, the pin No. 15 of IC "16D" for RAM Chip Select is set at Low level, but the pin No. 11 of IC "4F" is set at High level (i.e., the ON state of $\overline{IOCS}$). Therefore, the pin No. 13 goes low and the pin No. 4 of IC "5E" goes high. As a result, the CE2 terminal of RAM "13C" will not be activated and the RAM cannot be specified.

Since the IOCS signal is also supplied from connector CN7 to the expansion unit, the built-in RAM is protected from being specified erroneously.

For the above reasons, addresses 0000 to 007F indicate the RAM in the CPU, LCD buffers, or the built-in RAM for the real-time clock.

(c) With LCD buffers

The LCD has a total of 6 buffers (for 480 bytes), each of which is specified by addresses 0000 to 00F4 (80 bytes). However, these addresses are designated by setting the data pointer (of 7-bit configuration) within the LCD using the CID (LOAD IMMEDIATE TO DATA POINTER) command. Since each of the six 80-byte buffers is specified by the CS (Ship Select) signal, the master CPU does not address the LCD buffers directly. For this reason, addressing of the LCD buffers is done by the master CPU using only two addresses "0026" and "002A" as the LCD addresses, as shown in Fig. 2-9.

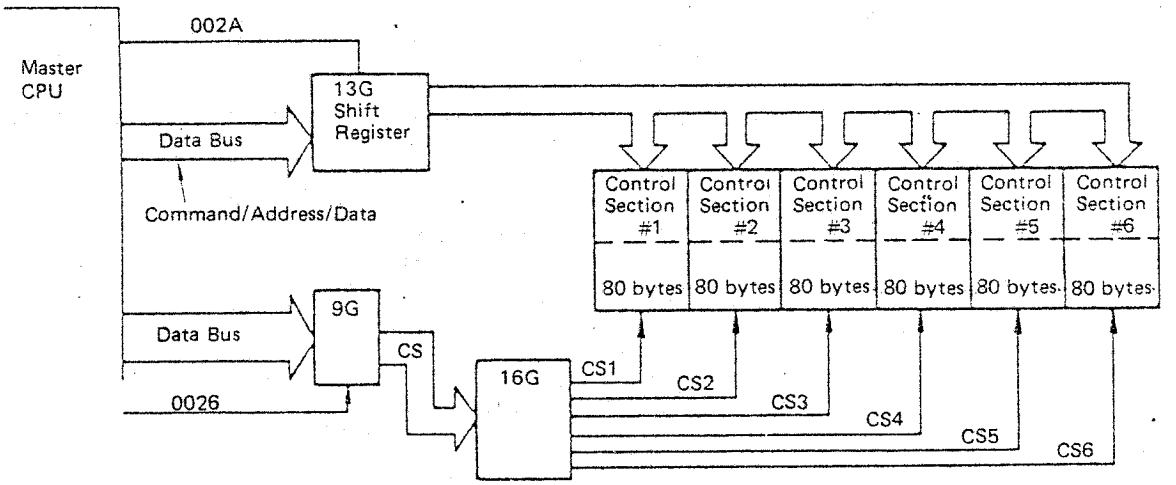


Fig. 2-9 Addressing of LCD Buffers

(d) With Clock RAM

Accessing the clock RAM is controlled by the pin No. 13 (E) of IC "6G", to which a control signal is supplied via the pin No. 8 of IC "1E", pin No. 1 of IC "4F", and pin No. 8 of IC "5E" only when both $\overline{IOCS}$ ($\overline{A7}$~$\overline{15}$) signal and DA6 signal (address 0040 or greater) are ON. Here, the addresses of the clock RAM are 0040 to 007F. Therefore, while this address space is being selected, the pin No. 13 of IC "6G" is at Low level, thus enabling the read/write of the clock RAM.

Bit / Address	7	6	5	4	3	2	1	0
XX40	0	1	0	0	0	0	0	0
XX7F	0	1	1	1	1	1	1	1

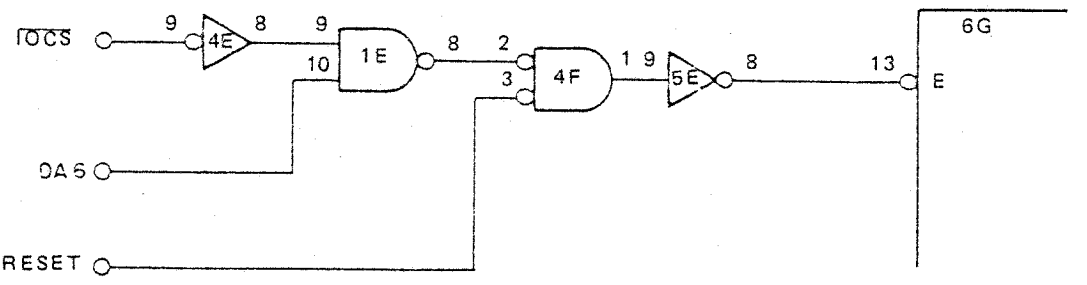


Fig. 2-10 Addressing of Clock RAM

2.3.3 $\overline{\text{IOCS}}$ signal

The $\overline{\text{IOCS}}$ signal is output under the condition of $\overline{\text{A7}}$~$\overline{\text{15}}$ (i.e., address lines $\overline{\text{A7}}$~$\overline{\text{A15}}$ all are at Low level). This signal is used for switching addresses in the low-order area of a memory.

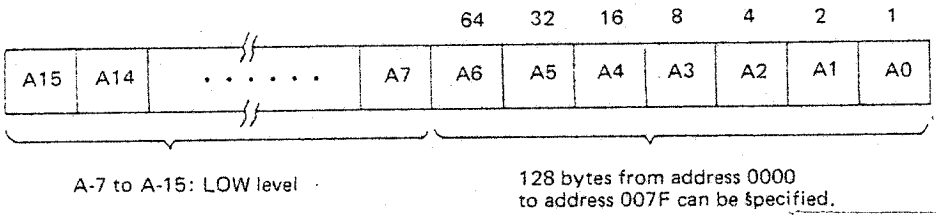


Fig. 2-11 $\overline{\text{IOCS}}$ Signal

Function	Operation
External RAM Control ($\overline{\text{IOCS}}$)	Chip Enable output to the external RAM corresponding to addresses 0000 to 07FF (2KB) is disabled.
Real-time Clock IC accessing ($\overline{\text{IOCS}}$)	According to the AND condition with address bit 6 (addresses 0040 to 007F), ENABLE signal (E) is output to the real-time clock IC so that accessing the real-time clock is enabled.
I/O Select Control ($\overline{\text{IOCS}}$)	According to the AND condition with address bits 5 and $\overline{4}$ (addresses 0020 to 002F), GATE signal is output to the I/O select IC to enable I/O address selection. (By this signal, I/O addresses 0020, 0022, 0026, 0028, 002A, and 002C can be output.)
Bank Switching ($\overline{\text{IOCS}}$)	Using address bits $\overline{2}$, $\overline{3}$, $\overline{6}$, 4 and 5 and with address bits 1 and 0 in the ON or OFF state, the memory banks in the expansion unit are selectable. Note: Bit 0 is insignificant, and may be either ON or OFF.

2.3.4 RAM select circuit

Fig. 2-12 shows a schematic of the RAM select circuit.

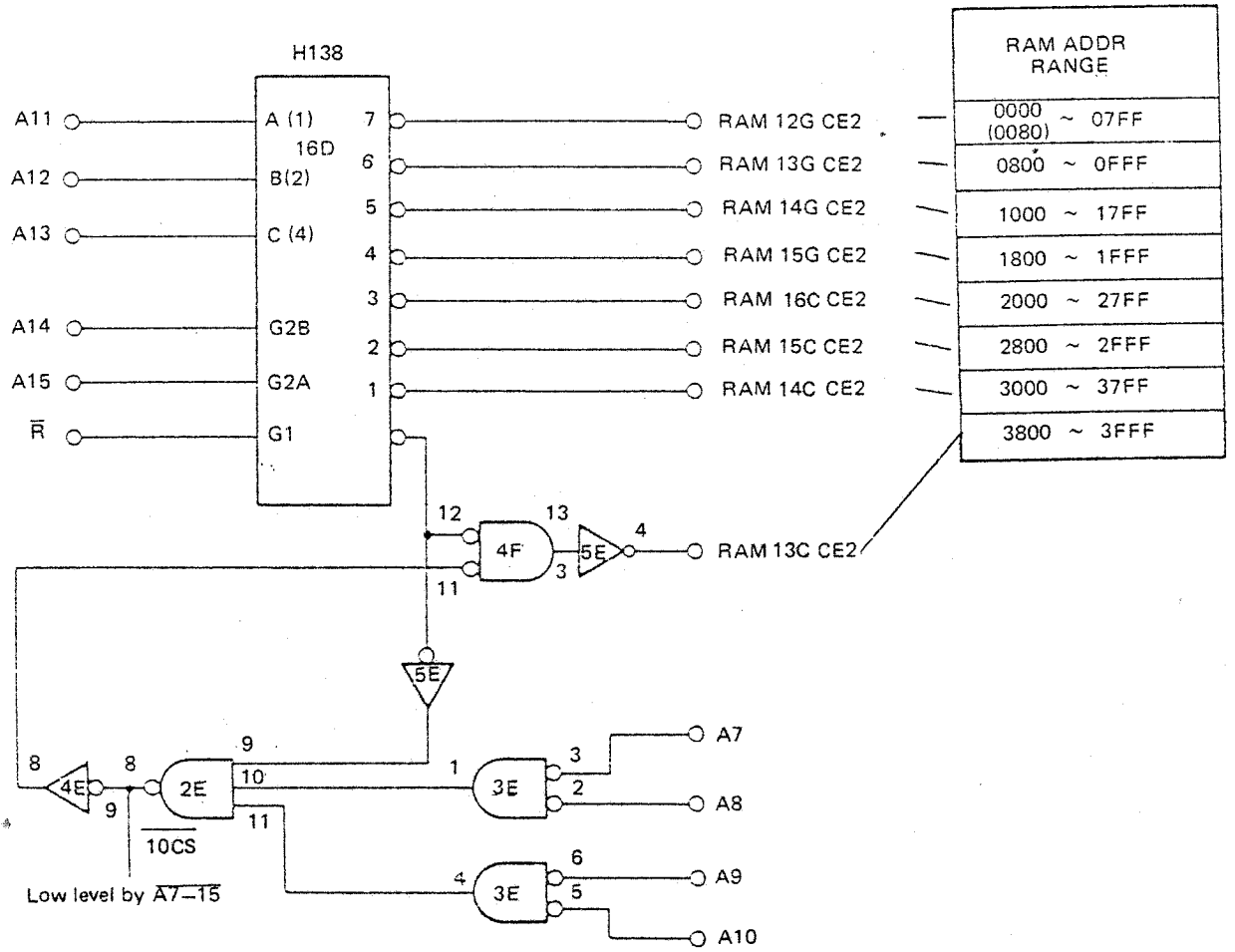


Fig. 2-12 RAM Select Circuit

2.3.5 I/O select circuit

When using any of the I/O addresses (I/O units) specified by the memory map, the I/O select circuit functions to output the gate signals corresponding to the respective I/O interfaces from IC "9E" as shown in Fig. 2-13.

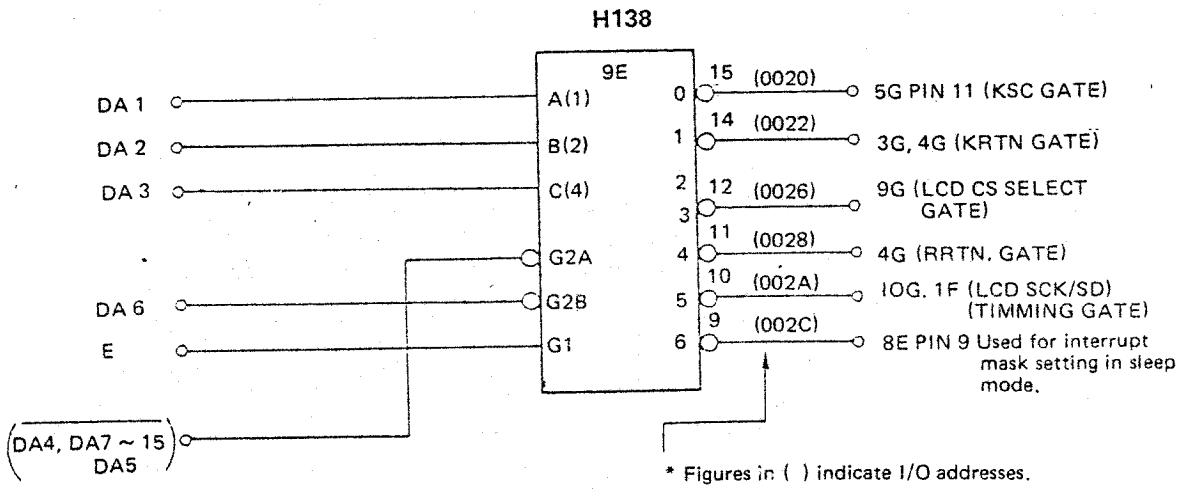


Fig. 2-13 I/O Select Circuit

0020: Used to output KSC GATE signal, to scan the keyboard data and the ON/OFF setting status of SW6.
0022: Used to input KRTN 0~7 signals to read out the keyboard data scanned by the KSC GATE signal onto the data bus.
0026: Used to mask an interrupt from the keyboard by changing the output level to Low at the pin No. 12 of IC "9G" in LCD chip select, ROM cartridge control, or interrupt mask reset in sleep mode.
0028: Used to read out KRTN signals 8 and 9, PW SW and BUSY (SO) signal onto the data bus.
002A: Used to output the SCK signal and SD (serial data) to the LCD.
002C Used for interrupt masking in sleep mode through IC "8E".

2.3.6 ROM select circuit
Fig. 2-14 shows a schematic of the ROM Select Circuit.

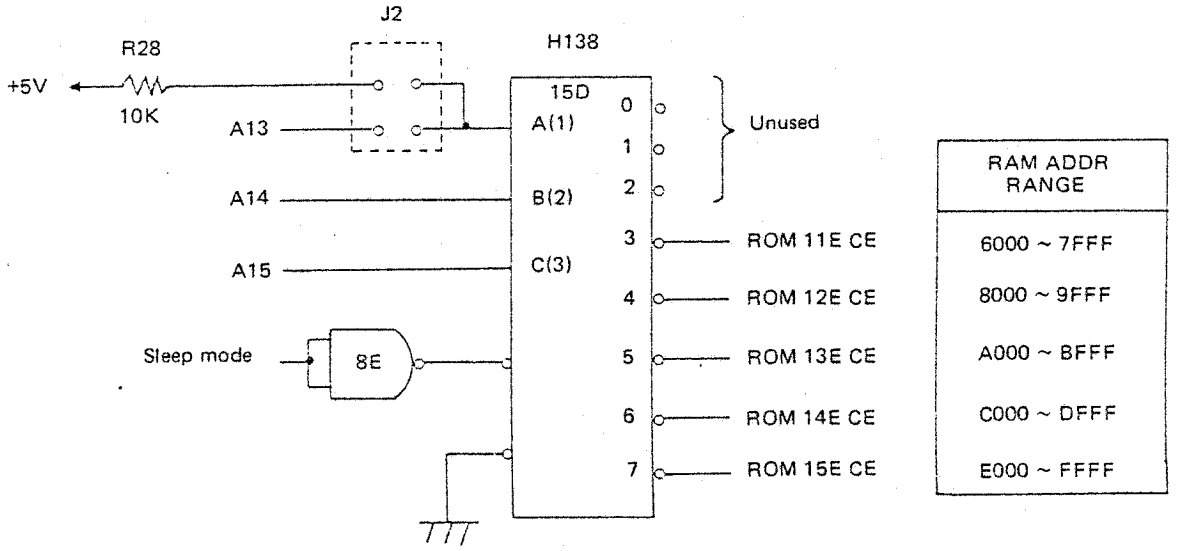


Fig. 2-14 ROM Select Circuit

2.4 Address Map
Since the master CPU operates in Expanded Multiplex mode (i.e., mode 4), addresses 0000 to 001F are used for the internal registers of the CPU and addresses 0020 to 007F for an external memory (I/O addresses, clock registers and RAM area).

Addresses 0080 to 00FF are assigned to the internal RAM of the CPU and addresses 0100 to FFFF to an external memory.

The slave CPU operates in Single Chip mode and thus addresses 0020 to 007F and 0100 to EFFF cannot be used.

2.4.1 Division of master CPU addresses (Low-order Area)
The addresses of the master CPU are divided by the RAM control bit 6 (address 0014) and IOCS signal as shown below.

Note: Addresses from 0080 to 00FF are selectable between the external RAM and internal RAM by the RAM control bit 6.

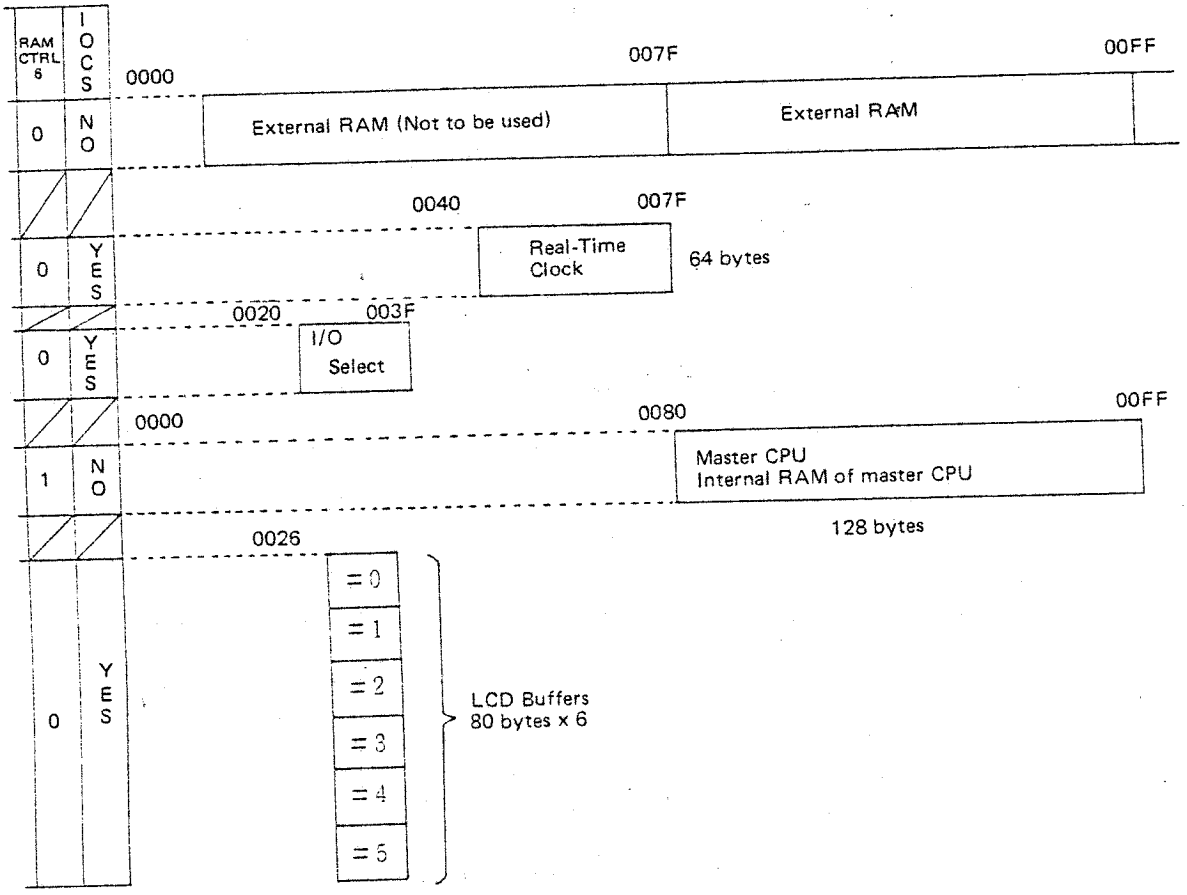


Fig. 2-15 Division of Master CPU Address

2.4.2 Memory map of master CPU (in Expanded Multiplex Mode 4)
Addresses 0000 to 00FF exist in the master CPU and addresses from 0100 and higher are assigned to an external RAM (ICs 13C~16C and 12G~15G and the expansion unit).

Address	Description
0000 ∫ 0007	Port control and registers PORT / PORT ADDR / DIRECTION REG. 1 / 0002 / 0000 (RS-232C I/F and others) 2 / 0003 / 0001 (Serial I/F, RS-232C I/F, barcode reader) 3 / 0006 / 0004 (A0~A7 and D0~D7) 4 / 0007 / 0005 (A8~A15)
0008 ∫ 000F	Timer control and data registers 0008 : Timer control 0009 ~ 000A : Free running counter ..... CPU R/W 000B ~ 000C : Output compare register ... R/W 000D ~ 000E : Input capture register .... READ 000F : P3 control register
0010 ∫ 0013	Serial control and registers 0010 : Serial bit rate 0011 : Serial control and status 0012 : Receive data register 0013 : Transmit data register
0014	RAM control : Switching between external RAM and internal RAM
0015 ∫ 001F	Unused
0020	Keyboard scan : KSC0~7 output or SW6 status read
0022	Keyboard input: KRTN0~7
0026	Cartridge interface, interrupt mask reset, LCD chip select or key masking
0028	Keyboard input : KRTN 8-9, $\overline{\text{PW SW}}$, BUSY
002A	Generates the clock for serial data transfer by ANDing with $\overline{\text{R/W}}$ signal.
0040 ∫ 004D	Clock registers 0040 : Second 0041 : Second (alarm) 0042 : Minute 0043 : Minute (alarm) 0044 : Hour 0045 : Hour (alarm) 0046 : Day of week 0047 : Date 0048 : Month 0049 : Year 004A ~ 004D : Control registers 1 ~ 4

Address	Description
004E ∫ 007F	RAM area for RAM system (50 bytes)
0080 ∫ 00FF	Internal RAM of CPU (128 bytes)
0100 ∫ FFFF	External RAM

2.4.3 Memory map of slave CPU (in Single Chip Mode)
The slave CPU controls input/output units such as microprinter, etc. by the control program stored in the built-in mask RAM (4KB).

Address	Description
0000 ∫ 0007	Port control and registers PORT / PORT ADDR / DIRECTION REG. 1 / 0002 / 0000 (microprinter and speaker) 2 / 0003 / 0001 (SCI and others) 3 / 0006 / 0004 (RS-232C I/F, external cassette and others) 4 / 0007 / 0005 (RS-232C I/F, and ROM cartridge)
0008 ∫ 000F	Timer control and data registers 0008 : 0009 ~ 000A : 000B ~ 000C : Refer to the master CPU. 000D ~ 000E : 000F :
0010 ∫ 0013	Serial control and registers 0010 : 0011 : Refer to the master CPU. 0012 : 0013 :
0014	RAM control : Switching between external RAM and internal RAM

Address	Description
0015 ∫ 007F	Unused
0080 ∫ 00FF	Internal RAM (128 bytes)
0100 ∫ EFFF	Unused (These addresses do not exist physically.)
F000 ∫ FFFF	Internal ROM (4KB)

2.5 Interrupt Control

When an input/output unit etc., make a request for processing by the CPU, it must send an interrupt signal to the CPU.

According to the type of interrupt shown in the interrupt table below, each class of interrupts is assigned a priority. In each vector address, the starting address of the program required for the processing of an interrupt request (i.e., interrupt handling routine) is stored. When an interrupt request occurs and the CPU is ready to accept the interrupt request, the contents of the program counter and index register, etc., are saved to the stack area and the CPU processes the interrupt request.

2.5.1 Interrupt priority table of master CPU

Interrupt level	Vector address	Interruption source
HIGHEST	FFFE FFFF	° Immediately after power on ° After reset
	FFFF FFFF	° Address error or operation code error (TRAP) ... Used by the MONITOR.
	FFFC FFFD	° $\overline{\text{NMI}}$ signal (Unused)
	FFFA FFFB	° Software interrupt (Unused)
	FFF8 FFF9	° Key input ($\overline{\text{K.B REQUEST}}$ signal) ° Power on (PW SW signal) ° Power off ($\overline{\text{PW SW}}$ signal) ° Clock ($\overline{\text{CLOCK IRQ}}$ signal) ° External interrupt ($\overline{\text{INT EX}}$ signal)
	FFF6 FFF7	° Timer Input Capture (Unused)
	FFF4 FFF5	° Timer Output Compare (Keyboard)
	FFF2 FFF3	° Timer overflow (Microcassette)
LOWEST	FFF0 FFF1	° Interrupt from SCI (serial communication interface) (PIN signal) (CTS signal)

2.5.2 Interrupt priority table of slave CPU

Interrupt level	Vector address	Interruption Source
HIGHEST	FFFE FFFF	° Immediately after power on ° After reset
	FFFE FFFF	° Address error or operation code error (TRAP)
	FFFC FFFD	° $\overline{\text{NMI}}$ signal (Unused)
	FFFA FFFB	° Software interrupt
	FFF8 FFF9	° Unused
	FFF6 FFF7	° Timer Input Capture
	FFF4 FFF5	° Timer Output Compare
	FFF2 FFF3	° Timer Overflow (Microcassette)
LOWEST	FFF0 FFF1	° Interrupt from SCI