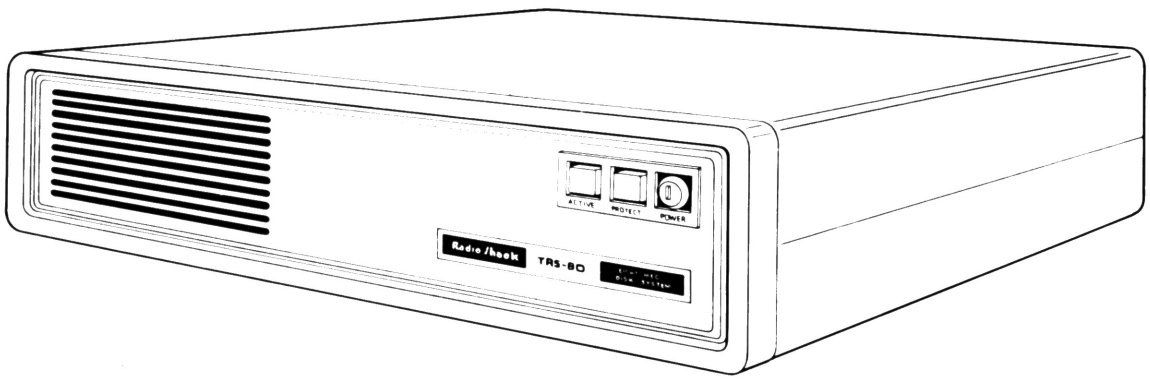
Radio Shack®

Service Manual

26-4150/4151

TRS-80®

Hard Disk Drive



CUSTOM MANUFACTURED IN THE U.S.A. BY RADIO SHACK, A DIVISION OF TANDY CORPORATION

Table of Contents

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* *

W A R N I N G S

* *

Do not move the Hard Disk Drive Unit unless the Spindle Lock on the bottom of the unit is in the locked position. Moving the unit even two feet without locking the Spindle Lock could result in damage to the disk media.

Before operation of the Hard Disk Drive, the Spindle Lock must be put in the unlocked position. To do this, carefully tilt up the unit and loosen the screw which holds the locking bracket. Position the bracket to the side in the indented area and tighten the screw.
DO NOT TURN THE DISK DRIVE UNIT UPSIDE DOWN.

The spindle on the bottom of the unit must only be rotated clockwise as viewed from the bottom of the unit. If the spindle is rotated in the incorrect direction, media scoring and head damage could result.

Do not move the Hard Disk Drive unit while the drive is running. Permanent damage to the drive may occur resulting in the loss of information or replacement of the disk.

DO NOT USE THE INIT COMMAND EXCEPT AS A LAST RESORT OR UNLESS THE DATA ON DRIVE 4 IS SAVED ON A FLOPPY DISKETTE.
If the Hard Disk system will not boot up, try to find the cause of the problem before using the INIT command. When INIT is used, Drive 4 is reformatted and all data is lost.

When the unit is opened:

1. Never rotate the damper located on the bubble unit without AC power applied.

2. DO NOT OPEN THE BUBBLE UNIT. IT IS NOT FIELD SERVICEABLE.

1/ SPECIFICATIONS

POWER REQUIREMENTS

AC Power Requirements
- 50/60 Hz +/- 0.5 Hz
- 100/115 VAC installations (90 to 127 V at 1.1A typical)
- 200/230 VAC installations (100 to 253 V at 0.6A typical)
- Fuse - 6 amp, fast-blow

DC Power Requirments
- +24 VDC +/- 10%, 2.8A typical during stepping (0.2A typical stepping steady state, non-stepping)
- +5 VDC +/- 5%, 2.0A typical during stepping (3.6A typical non-stepping)

DIMENSIONS

Height	6 inches (15.24 cm)
Width	18.5 inches (47 cm)
Depth	19.25 inches (48.9 cm)
Weight	17 lbs. (7.73 kg)

ENVIRONMENT

Ambient Temperature	50 to 115 degrees F. (10 to 46 degrees C.)
Relative Humidity	8% to 80%
Maximum Wet Bulb	78% non-condensing
Heat Dissipation	150 watts (511 BTU/hr) Max.
Altitude	operating: 0 to 6000 feet (0 to 1829 meters) storage: -1000 to 12000 feet (-305 to 3656 meters)

WARM-UP PERIOD

Minimum On Power-Up	2 minutes
Minimum to Turn System On After Turning System Off	15 seconds

HARD DISK DRIVE

Disk Organization

Tracks per Unit	1024
Tracks per Platter	512
Sectors per Track	34
Bytes per Sector	256
Cylinders per Disk	256
Average Latency	9.6 msec
Rotational Speed	3125 rpm

SPECIFICATIONS (cont'd)

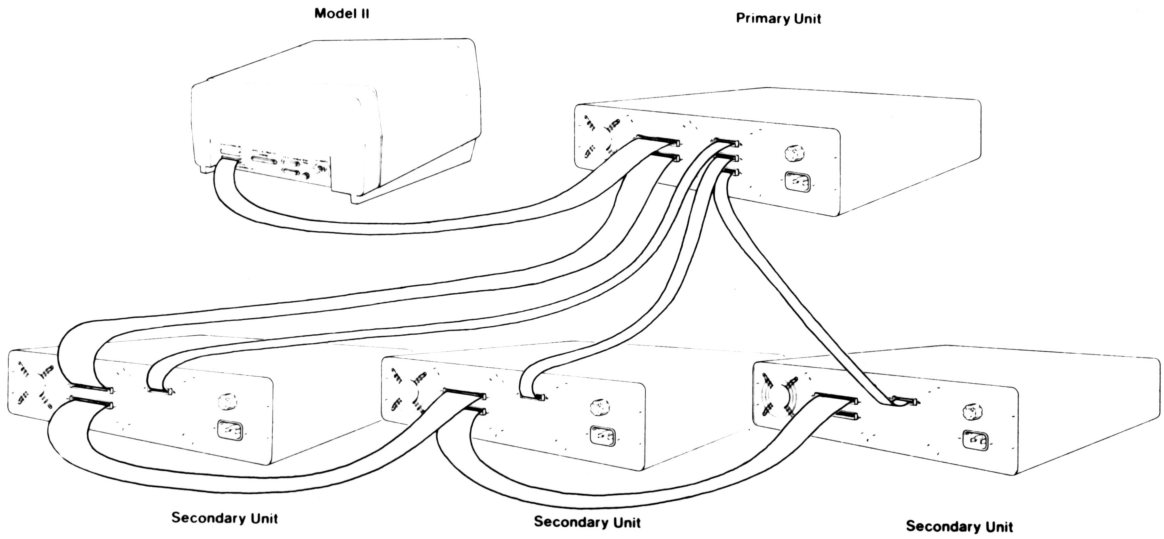
Recording Density	6270 bpi
Flux Density	6270 fci
Track Density	172 tpi
Storage Capacity (Hard Disk)	
Unformatted	
Bytes per Track	8704
Bytes per Surface	2.23M
Bytes per Drive	10M
Formatted	
Bytes per Drive	8.5M (primary drive) 8.9M (secondary drive)

TRSDOS-HD FORMATTED FLOPPY DISKETTE

Storage Capacity	
Bytes per Sectors	256
Sectors per Track	32
Tracks (single-side)	76
Bytes per Diskette	622,592

2/ CONNECTIONS AND POWER-UP

The primary and secondary units should be connected as illustrated below. Don't forget to connect the power cord for the computer and each Hard Disk Drive Unit.



Power-Up

1. Be sure all floppy diskette drives are empty and all components are turned off.

2. Turn Drive 4 (the Primary Drive) ON.

   Be sure Drive 4 is turned ON first or data may be lost or destroyed.

3. Turn all Secondary Drives ON. Allow 1 minute warm-up for the Disk Drives.

4. Turn the Computer ON.

5. Turn all peripherals (including Floppy Disk Expansion Unit) ON.

   If the operating system is stored on Hard Disk (TRSDOS-HD), the Computer will go to Drive 4 and automatically load the operating system. Refer to the Hard Disk Owner's Manual and the TRS-80 Model II Owner's Manual for operating instructions.

When turning OFF the system . . .

1. Turn all peripherals (including Floppy Disk Drives) OFF.
2. Turn all Secondary Hard Disk Drives (Drives 5-7) OFF.
3. Turn the Primary Drive (Drive 4) OFF.
4. Turn the Computer OFF.

Always be sure Drive 4 (the Primary Drive) is the last disk drive turned OFF. If Drive 4 is not the last drive turned off, data could be damaged or destroyed.

3/ REPLACEMENT PROCEDURES

Replacement procedures contained in this manual are limited to case disassembly, removal and replacement of subassemblies, and case assembly.

Before beginning repair, disconnect all external cables from the rear connector panel and BE SURE that the Spindle Lock is in the locked position.

DISASSEMBLY

1. Remove the top row of screws (5) from the rear panel and lift off the case top.

2. To remove the hard disk controller board, remove all cables from the board (data cables, hard disk expansion cable, controller connecting cables, power harness). Remove the five screws and split washers from the controller board.

3. To remove the hard disk power supply, remove the six small black screws which secure the power supply cover to the bottom of the unit and lift off the cover. Loosen all cables. Remove the six screws and washers which hold the power supply board.

4. To remove the bubble unit, perform the following steps:
   a. Remove all cables from the bubble unit controller board and remove the screws which secure the board. Twist the nylon retaining clips 90 degrees and carefully lift off the controller board.

REASSEMBLY

1. Replace stepper board, bubble unit, and bubble controller board. Be sure that the wire connector on the Index Sensor goes to pins 1 and 2 on the PCB.

2. Fasten the power supply in the bottom of the unit by using six #6 screws and washers and also reconnect the power cables.

3. Replace the power supply cover and fasten it using six #6 black screws.

4. Position the hard disk controller board on top of the power supply cover with the edge connector toward the rear of the unit. Fasten the board using five #6 screws.

5. Reconnect all cables (data, hard disk expansion, controller, power harness). Be sure that the data cables are connected so that the cable comes from the left-hand side of the plug when looking from the front of the unit.

6. Replace the case top and five #6 screws in the rear panel.

4/ OVERVIEW

The TRS-80 Hard Disk Unit consists of two non-removable 8-inch disks spaced approximately 1 inch apart. There are four Read/Write heads (one on each side of each platter) which move towards or away from the center of the disk as needed.

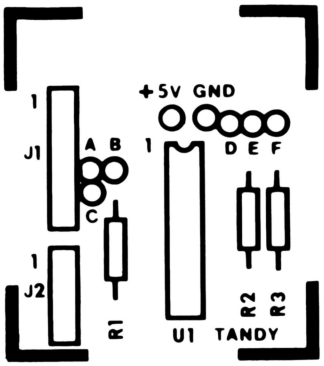
The Disks and Read/Write heads are fully enclosed in a sealed chamber. A special air filteration system prevents dust and other particles which destroy data from reaching the disks. Another filtering system allows pressure equalization with the "outside" air pressure.

UNDER NO CIRCUMSTANCES MUST THE CHAMBER BE UNSEALED IN THE FIELD. A CLASS 100 CLEAN ROOM ENVIRONMENT IS NEEDED FOR UNDER-THE-BUBBLE REPAIR.

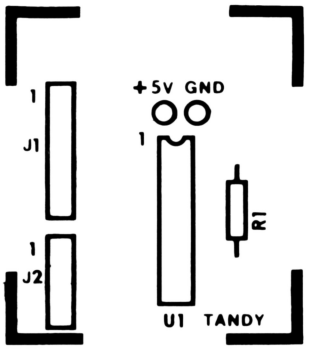
The Hard Disks have their own built-in error detection and correction scheme. These errors are due to minor defects in the media as well as signals from external sources. There will be no more than 12 tracks per head with defects. Of these 12 tracks, no more than 4 tracks will contain multiple errors.

On all Hard Disk Units, flaws in the media are identified at the factory before the disk drives are delivered to the customer. Attached to the bottom of each disk drive unit is a "Media Error Map". This map identifies the flawed tracks on that particular unit.

5/ PRINTED CIRCUIT BOARDS

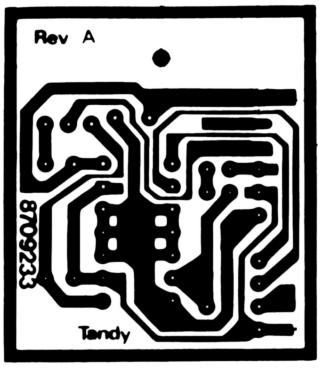


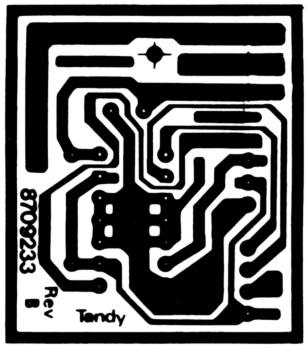
Revision A board



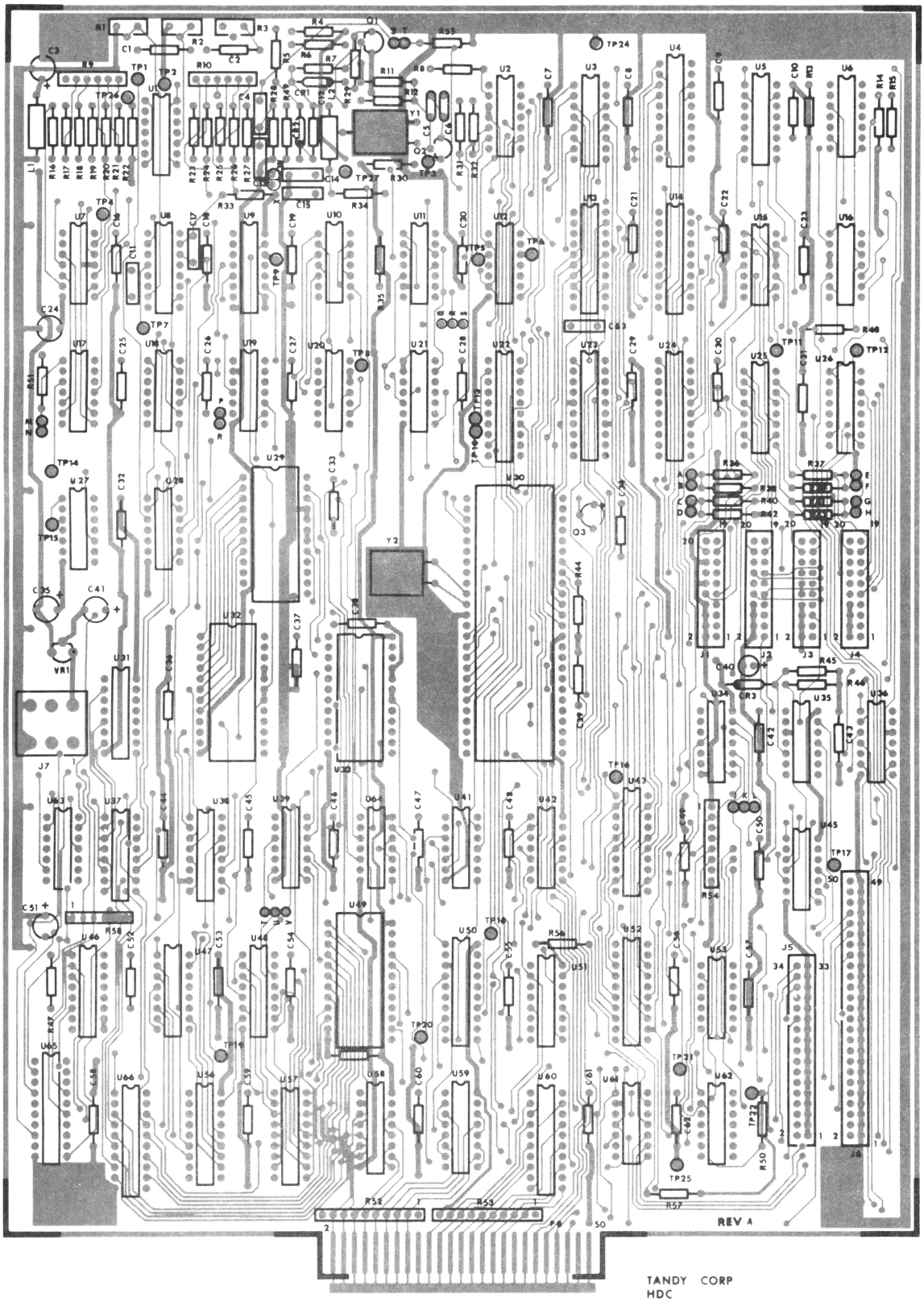
Revision B board

Front Panel Driver Printed Circuit Board - Component Side

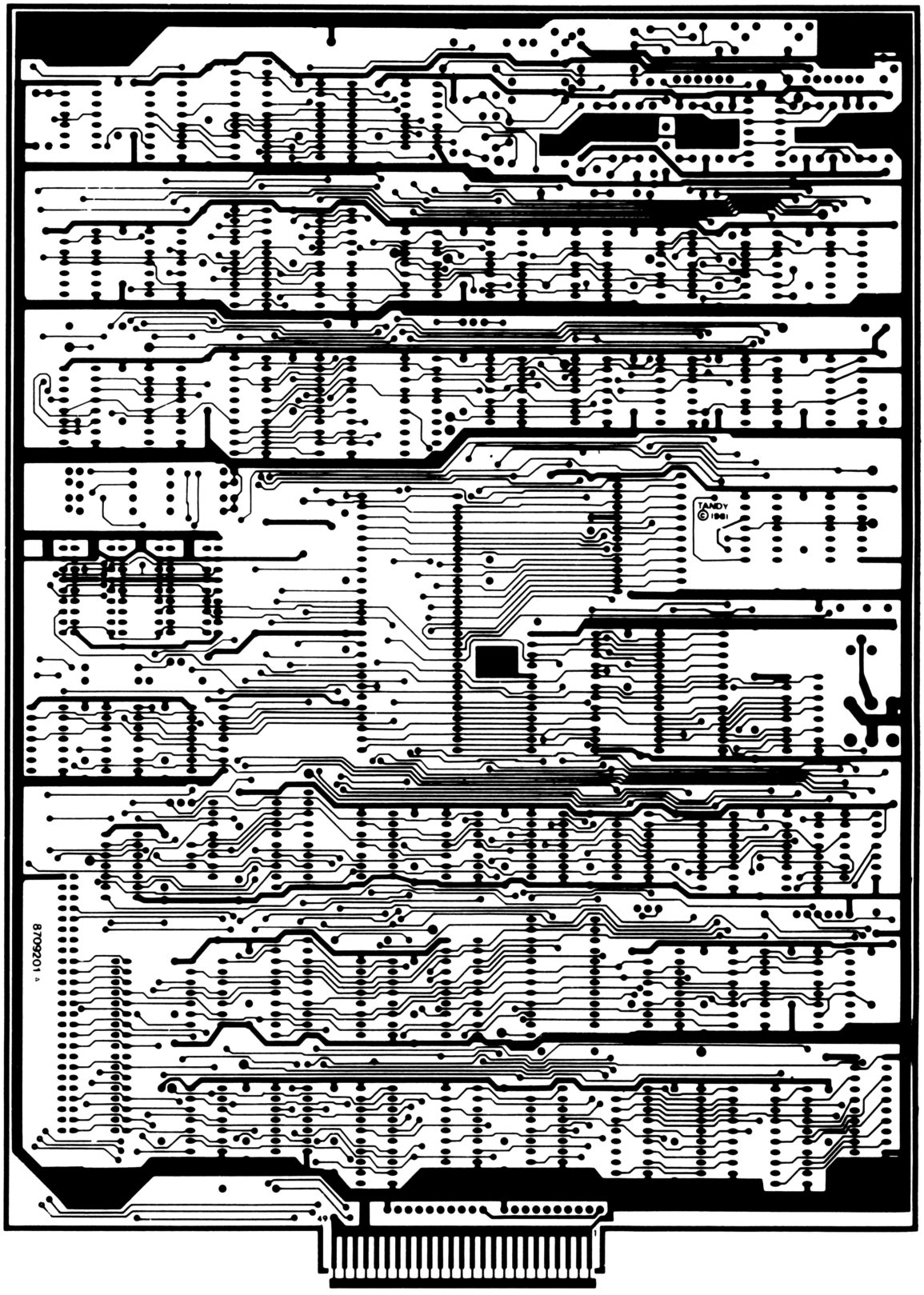




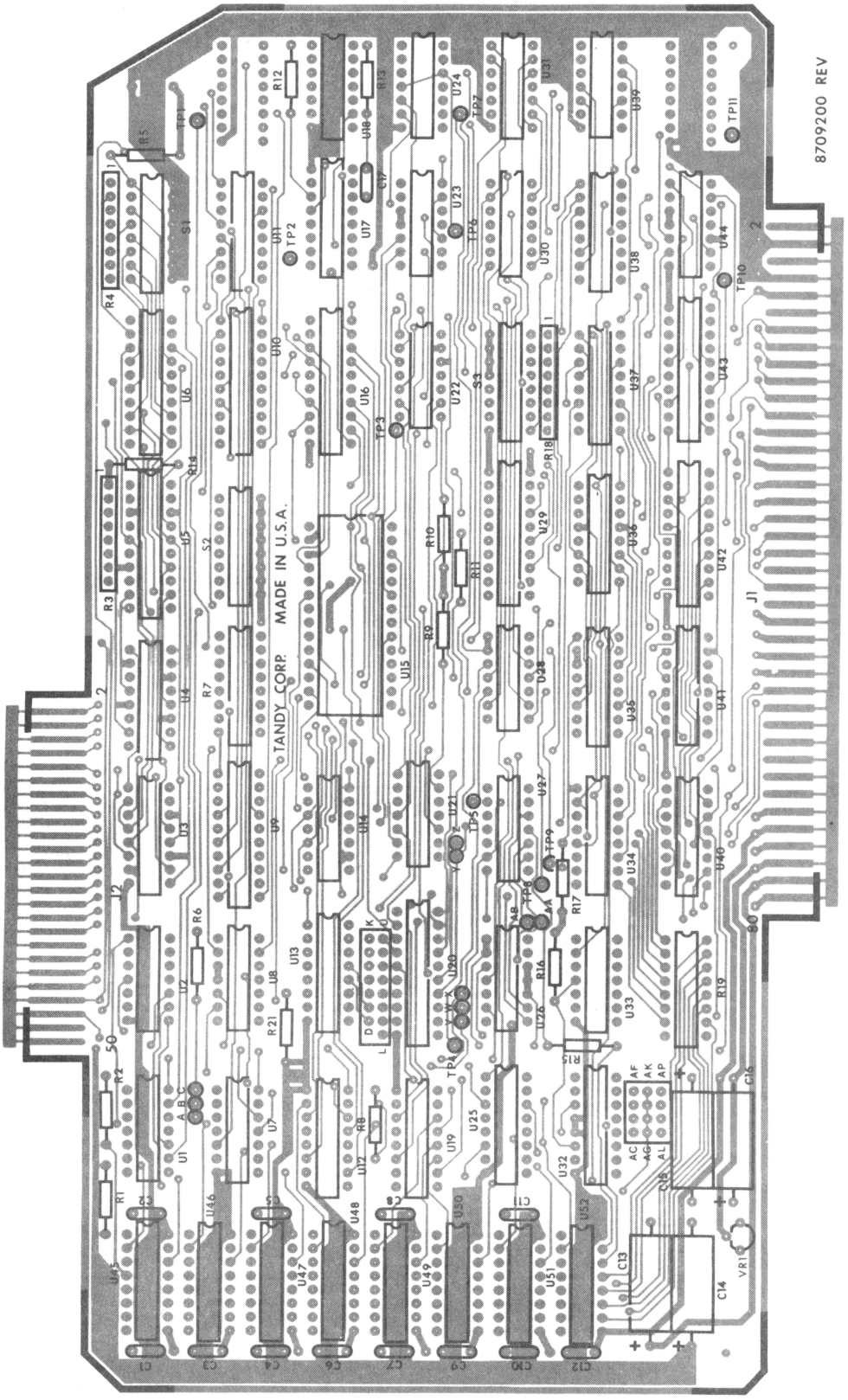
Front Panel Driver Printed Circuit Board - Circuit Side



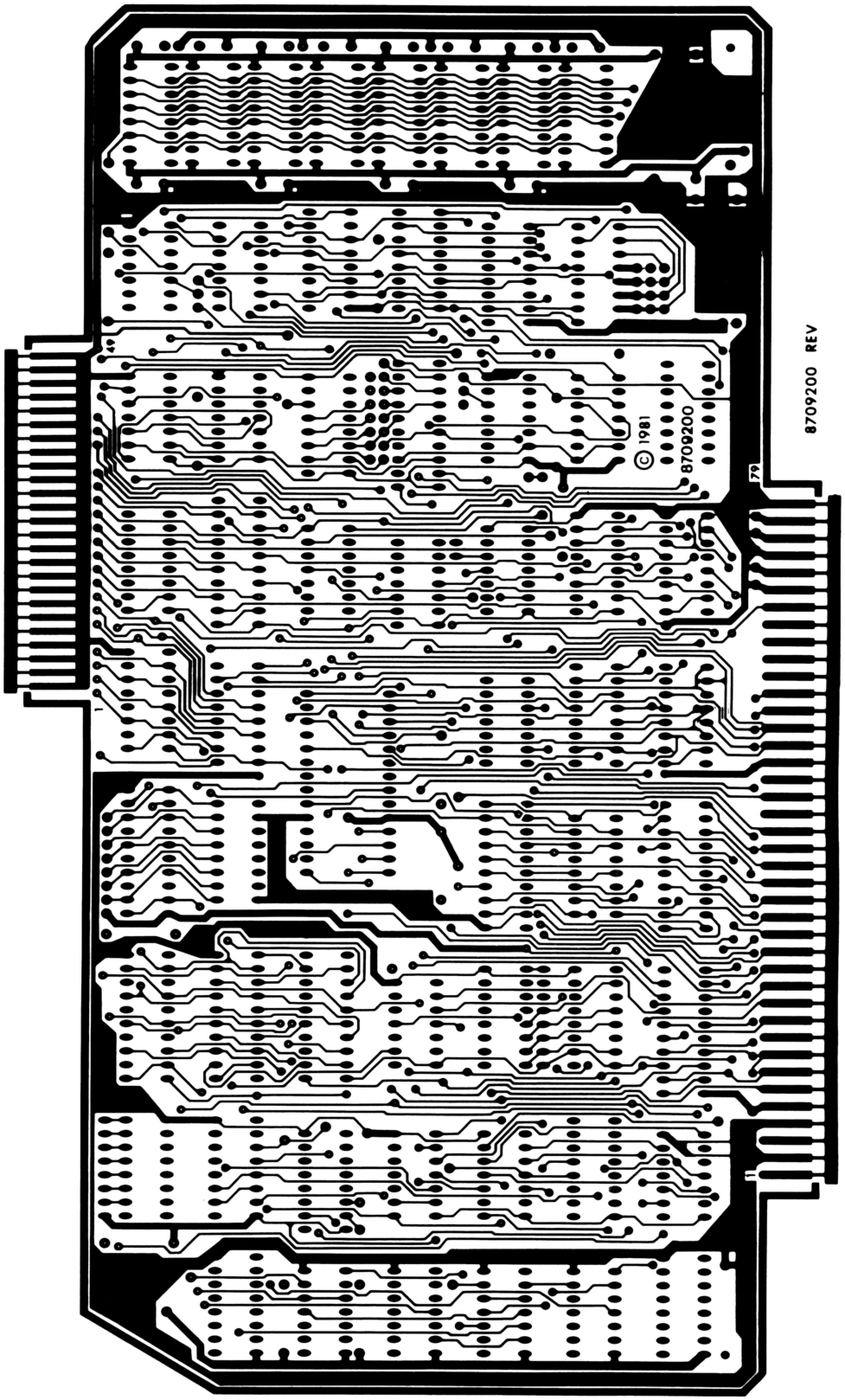
Hard Disk Controller Printed Circuit Board - Component Side



Hard Disk Controller Printed Circuit Board - Circuit Side

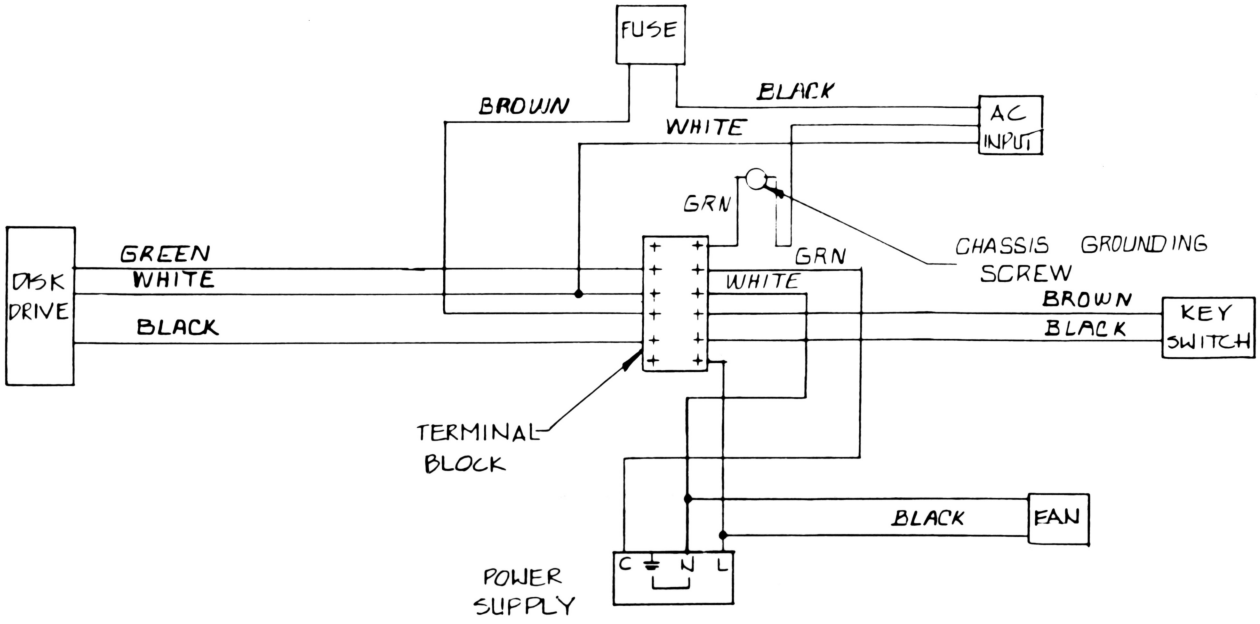


Hard Disk Interface Printed Circuit Board - Component Side

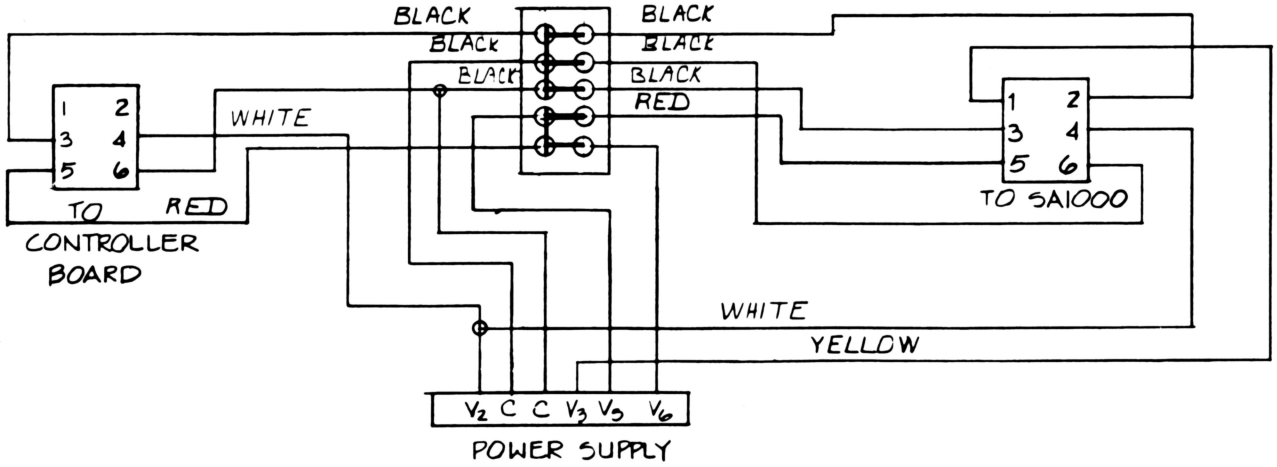


Hard Disk Interface Printed Circuit Board - Circuit Side

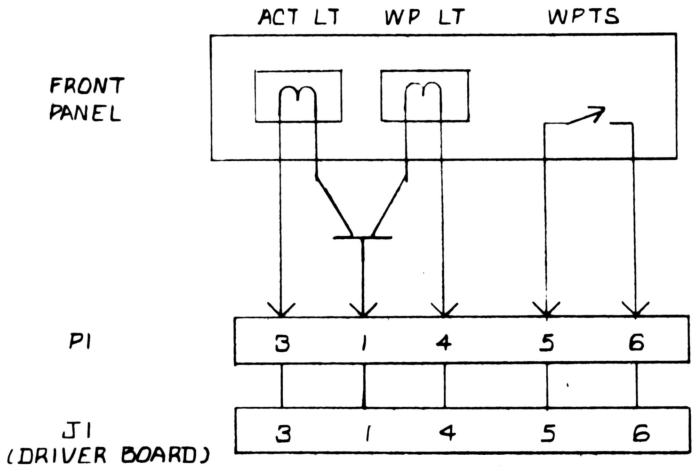
6/ WIRING DIAGRAMS



AC Wiring Harness



DC Wiring Harness



Front Panel Driver Board Wiring Diagram

Front Panel Driver Board Wiring Charts

J1	P1	Front Panel Lights
1	1	Active/WP
2	2	N.C.
3	3	Active
4	4	Write Protect
5	5	Write Protect
6	6	Write Protect

J2	P2	Bubble Controller
1	1	6C-8
		8A-1*
2	2	7E-1
		5B-11*
3	3	N.C.
4	4	J2-5

*may appear at these designations on some boards.

7/ ELECTRICAL PARTS LISTS

Hard Disk Controller Printed Circuit Board

Symbol	Description	Manufacturer's Part Number
	PC Board Assembly	8896002
	Staking Pins	8529014
	Integrated Circuits	
U4	WD1100-02, pre-comp. generator	8040112
U6	Delay line, 60ns	8429009
U13	WD1100-05, parallel/serial parser	8040115
U14	WD1100-04, CRC checker generator	8040114
U22	WD1100-03, AM detecter	8040113
U24	WD1100-01, serial/parallel parser	8040111
U27	Delay line, 100ns	8429008
U29	1024 x 8, BiPROM	8040086
U30	8 x 300, micro-controller	8040300
U32	1024 x 8, BiPROM	8040086
U33	1024 x 8, BiPROM	8040086
U49	8T31, 8-bit bidirectional port	9060031
U56	1024 x 4, static RAM	8042114
U57	1024 x 4, static RAM	8042114
U58	8T26A, 4-bit transceiver	9060026
U59	8T26A, 4-bit transceiver	9060026
	Resistor Paks	
R52	220/330 ohm, 10-pin	8290020
R53	220/330 ohm, 10-pin	8290020
R54	220/330 ohm, 10-pin	8290020
R58	4.7K, 6-pin, SIP	8293247

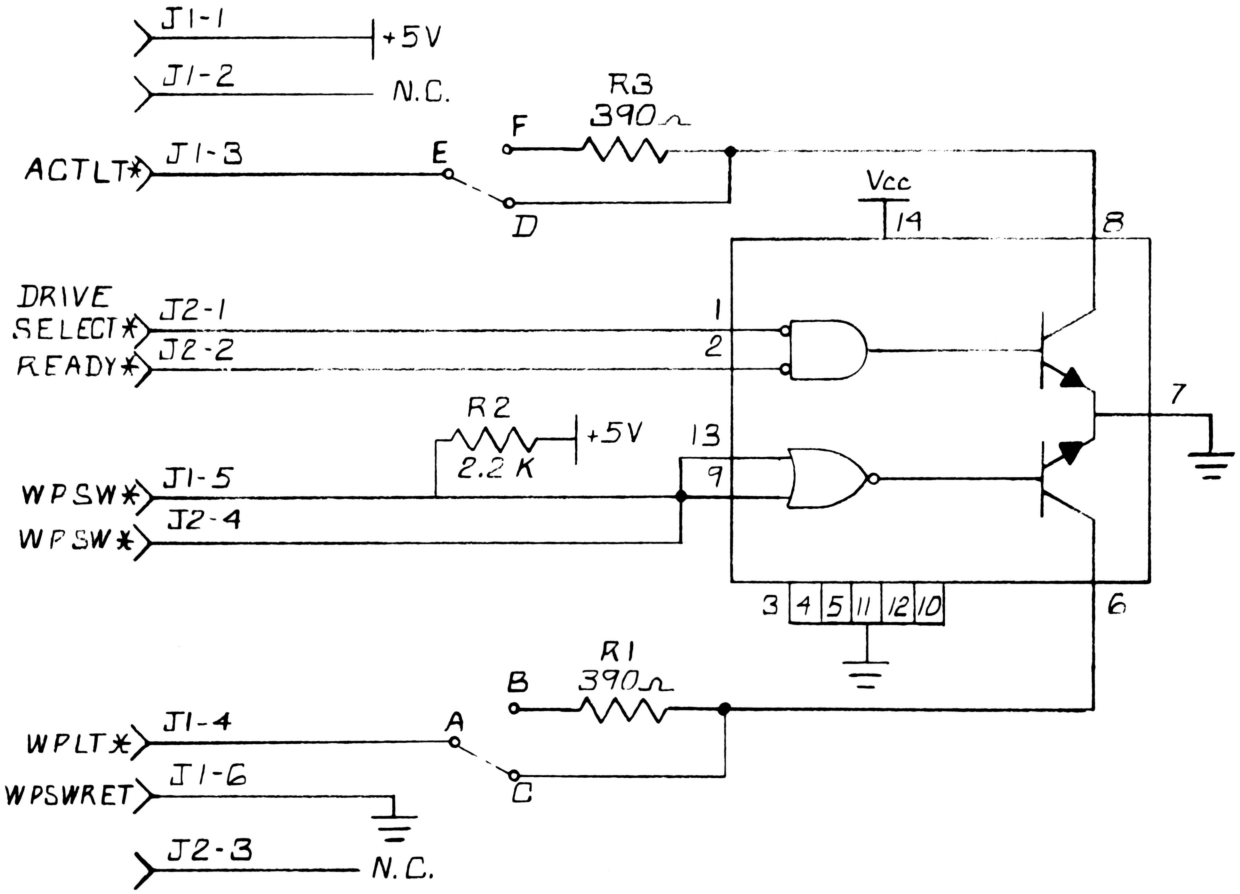
Front Panel Driver Printed Circuit Board

Symbol	Description	Manufacturer's Part Number
	PC Board Assembly	8896001
	Connector, 6-pin SIP	8519103
	Harness, power	8709263
	Harness, power	8709080
U1	75413, PE driver	8050413
R1	4.7K, 1.4W, 5%	8207247
R2	4.7K, 1/4W, 5%	8207247

Hard Disk Interface Printed Circuit Board

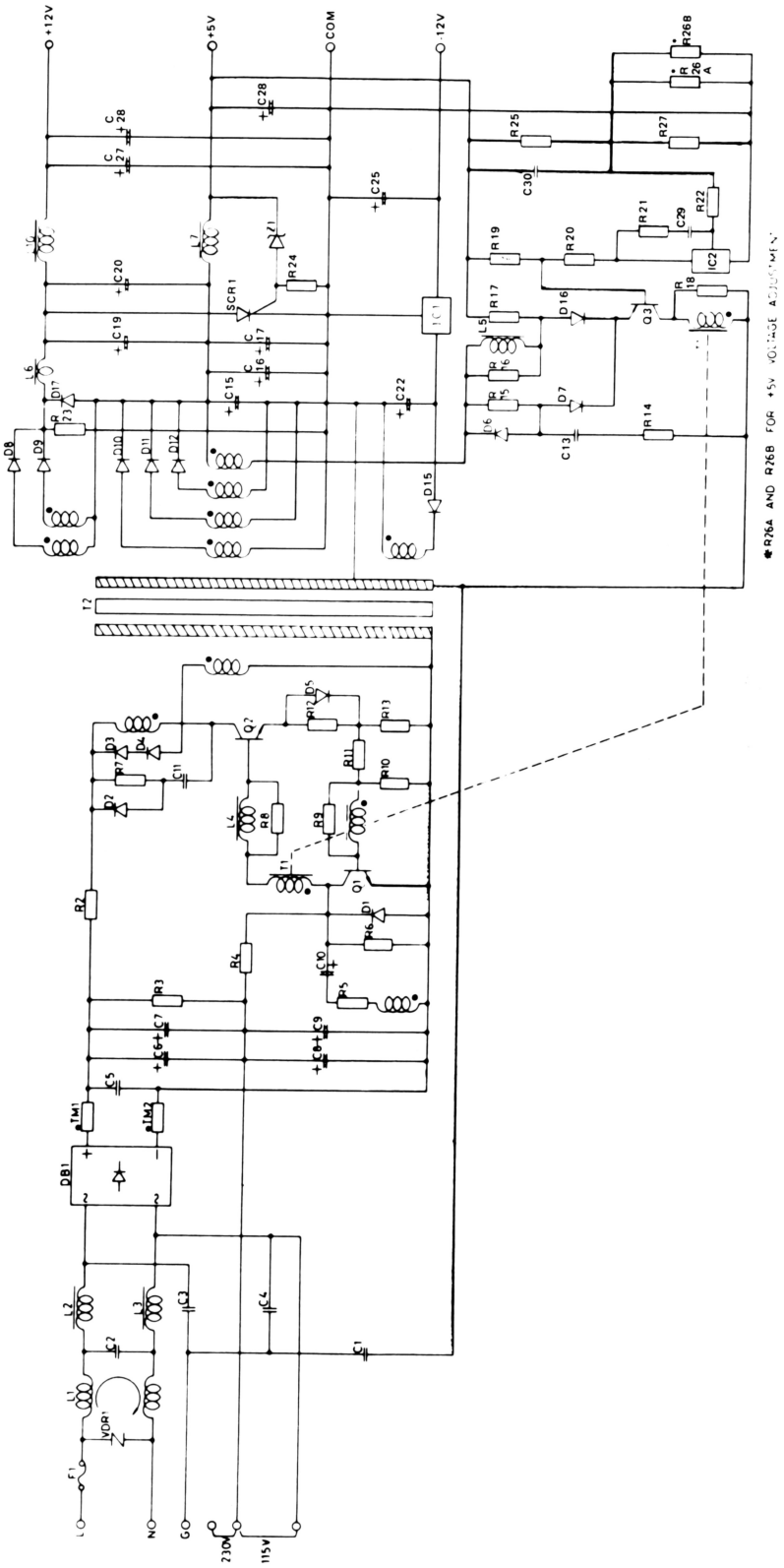
Symbol	Description	Manufacturer's Part Number
	PC Board Assembly	8896001
	Staking Pins	8529014
	Integrated Circuits	
U3	8T26, quad transceiver, 16-pin	9060026
U4	8T26, quad transceiver, 16-pin	9060026
U12	8T26, quad transceiver, 16-pin	9060026
U13	1519-200B, 200ns delay, 16-pin	8429004
U19	8T26, quad transceiver, 16-pin	9060026
U40	8T26, quad transceiver, 16-pin	9060026
U41	8T26, quad transceiver, 16-pin	9060026
U44	74S64, 2-3-3-4, AOI, 14-pin	9010064
U45	MK4116, 16K RAM, 200ns, 16-pin	8041016
U46	MK4116, 16K RAM, 200ns, 16-pin	8041016
U47	MK4116, 16K RAM, 200ns, 16-pin	8041016
U48	MK4116, 16K RAM, 200ns, 16-pin	8041016
U49	MK4116, 16K RAM, 200ns, 16-pin	8041016
U50	MK4116, 16K RAM, 200ns, 16-pin	8041016
U51	MK4116, 16K RAM, 200ns, 16-pin	8041016
	Resistor Paks	
R3	4.7K, 8-pin, SIP	8292246
R4	4.7K, 8-pin, SIP	8292246
R7	220/330 ohm, 16-pin DIP	8290003
R18	4.7K, 8-pin SIP	8292246
R19	39 ohm, DIP	8290002
	Switches	
S1	DIP, 16-pin	8489004
S2	DIP, 16-pin	8489004
S3	DIP, 16-pin	8489004

8/ SCHEMATICS

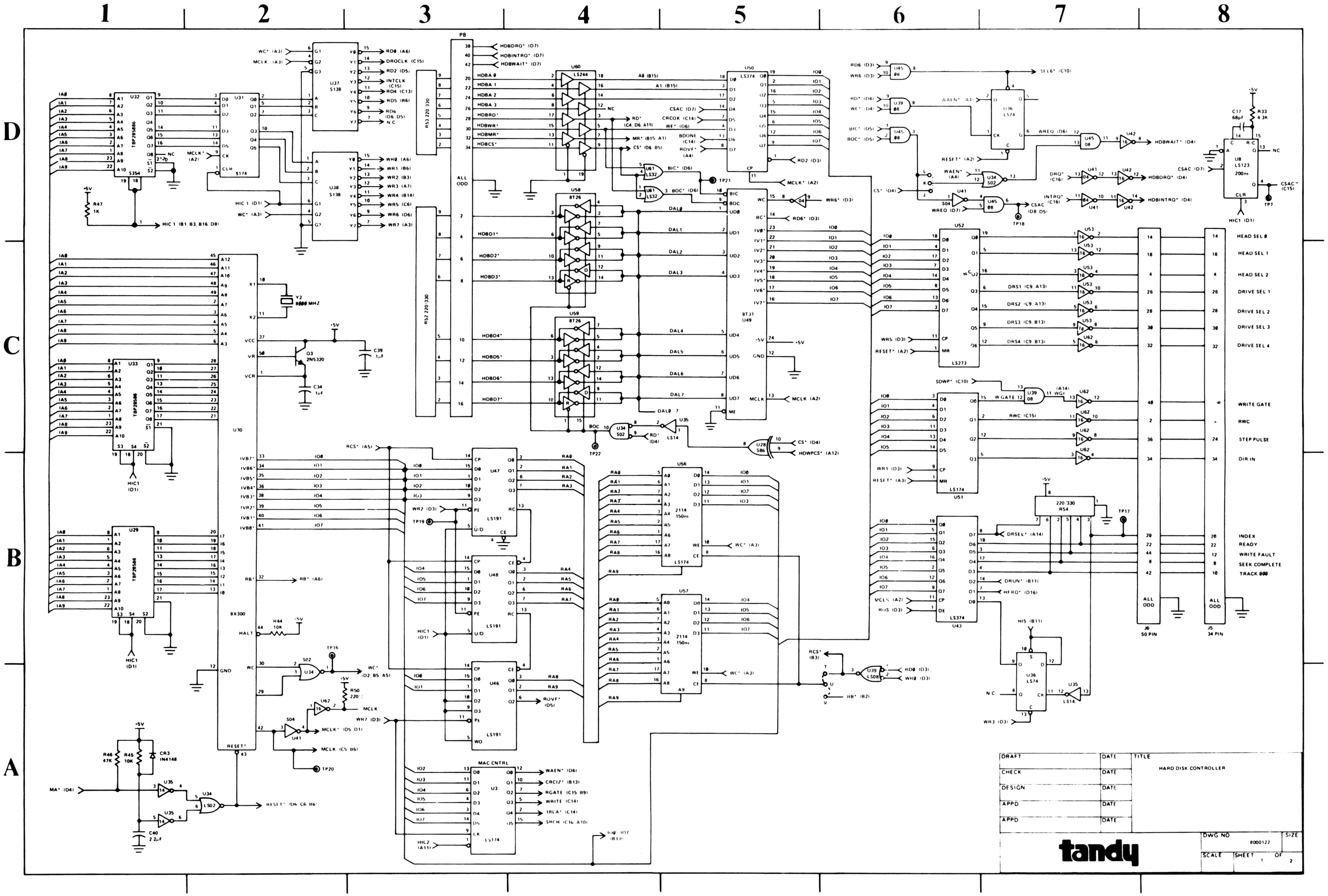


NOTE:
Jumper options E-F and A-B and resistors R3 and R1 are not needed and may be disregarded.

Front Panel Driver Board Schematic

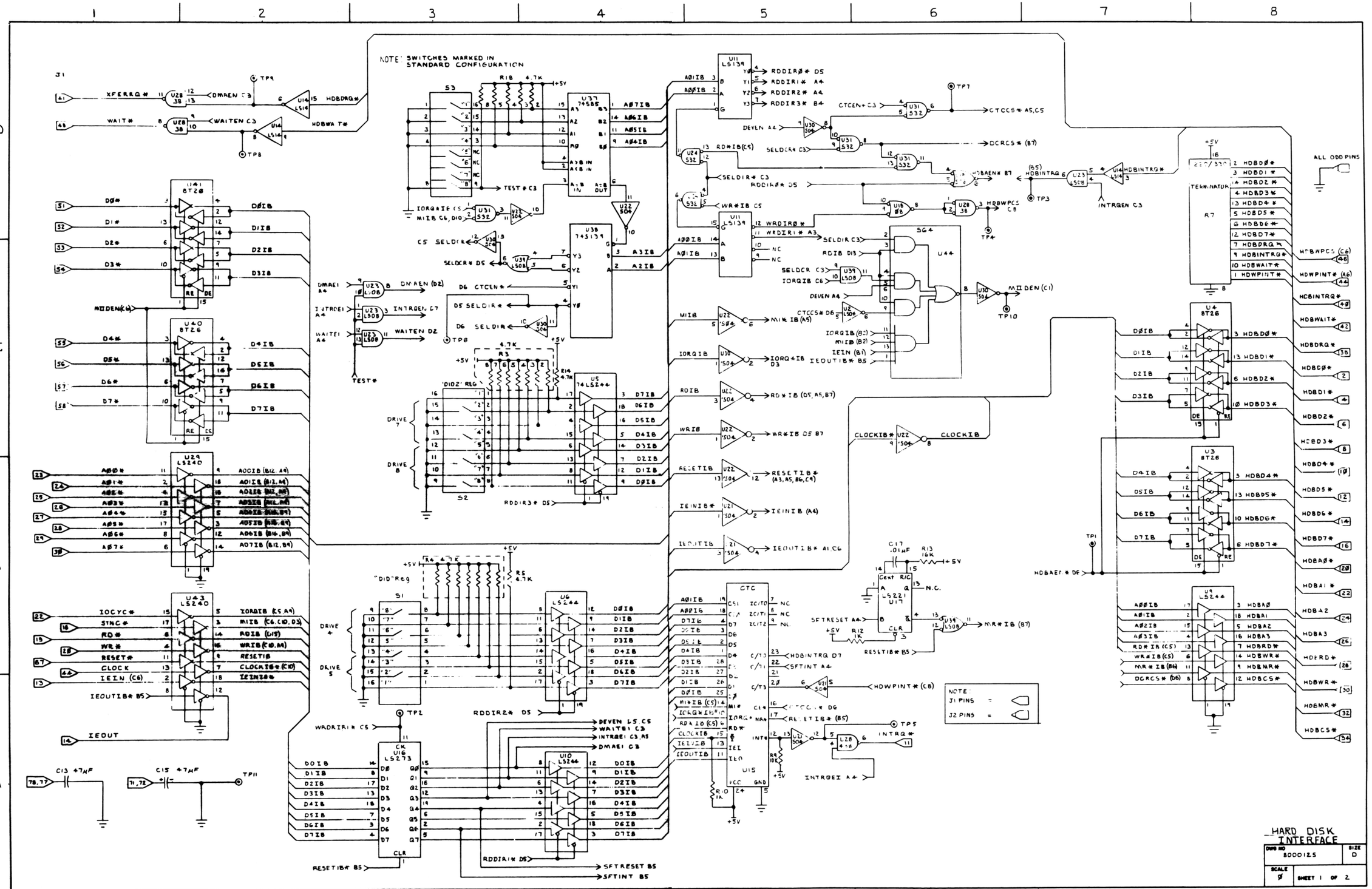


Hard Disk Power Supply Schematic

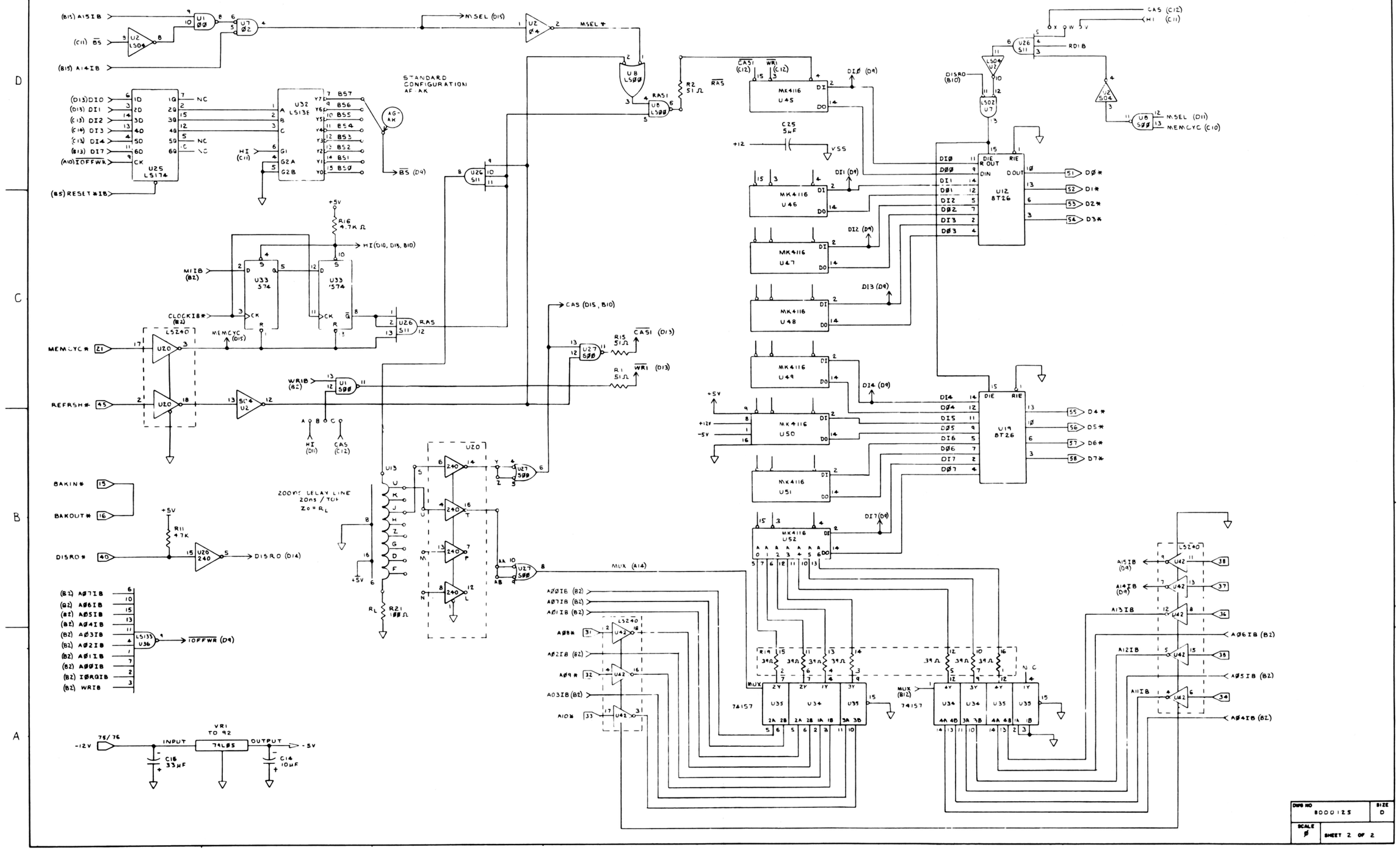


Hard Disk Controller Schematic (Sheet 1)

Hard Disk Controller Schematic (Sheet 2)



Hard Disk Interface Schematic (Sheet 1)



Hard Disk Interface Schematic (Sheet 2)

9/ THEORY OF OPERATION

POWER SUPPLY

Operating Characteristics

		Min	Typ	Max	Units
Vin Range					
Input Select 115V		90	115	135	Vrms
Input Select 230V		180	230	270	Vrms
Line Frequency		47	55	63	Hz
Output Voltages	+5V	4.9	5	5.1	Volts
	+24V	21.6	24	29	Volts
	-12V	11.4	12	12.6	Volts
Output Current	+5V	0.75	2.4	3	Amps
	+24V	0	2.2	3	Amps
	-12V	0.042	0.12	0.17	Amps
Line Regulation (measured at full-rated output power)					
	+5V	----	----	0.5	%
	+24V	----	----	0.5	%
	-12V	----	----	0.5	%
Load Regulation (measured by varing load on considered output from typ to either min or max rated load)					
	+5V	-2	----	+2	%
	+24V	-10	----	+20	%
	-12V	-5	----	+5	%
Ripple Voltages	+5V	----	----	50	mV
	+24V	----	----	100	mV
	-12V	----	----	50	mV
Efficiency		70	----	----	%
Hold Up Time					
Full Load, Low Line		10	----	----	mSec
Full Load, Nom Line		16	----	----	mSec
Over-Voltage Protection		5.94	----	6.82	Volts

Short Circuit Protection				
+5V	----	----	2	ADC
+24V	----	----	1	ADC
-12V	----	----	0.6	ADC
Transient Response at load change on any output from min to max and max to min within regulation limit	----	----	4.5	mSec
Insulation				
Input to GND	50	----	----	KVDC
Input to Outputs	50	----	----	KVDC
Output to GND	50	----	----	KVDC
Isolation				
Input to GND	4.5	----	----	KVDC
Input to Outputs	4.5	----	----	KVDC

Troubleshooting

Equipment for Test Set-up

1. Isolation Transformer (minimum of 500VA rating)

*** * * * C A U T I O N * * * ***

Dangerously high voltages are present in this power supply. For the safety of the person doing the testing, please use an isolation transformer. The 500VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

2. 0 - 140 volt Variable Transformer (Variac) - Used to vary input voltage. Recommend 10 amp, 1.4 KVA rating, mainimum

3. Voltmeter - Needed to measure DC voltages to 50V and AC voltages to 200 V. Recommend two digital multimeters.

4. Oscilloscope - Need X10 and X100 probes.

5. Load board with connectors - See Table 1 for values of loads required. The entry on the table for Safe Load power is the minimum port ratings for the resistors used.

6. Ohmmeter

7. Wattmeter - 150 watt rating minimum.

TABLE 1. LOAD BOARD VALUES

Output	Min Load	Load R	Safe Load Power	Max Load	Load R	Safe Load Power
+5V	0.75A	6.67ohm	8W	3A	1.67ohm	30W
+24V	0	0	- - - -	3A	8ohm	140W
-12V	0.042A	286ohm	1W	0.17A	7.06ohm	4W

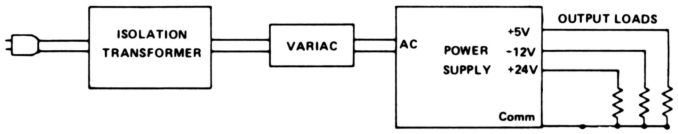


Figure 1. Test Set-Up

Set-Up Procedure

Set up test equipment as shown in Figure 1. You will want to monitor the input voltage and the input power and also the +5V output with DVM's. Also monitor the +5V output with an oscilloscope using 50 mV/div sensitivity. The DVM monitoring the +5V output can also be used to check the other outputs. See the No Output section for test points within the power supply.

Visual Inspection

Check the power supply for any broken, burned, or obviously damaged componets. Visually check the fuse; check with the ohmmeter if there is any doubt.

Start-Up

Load the power supply with the minimum load specified in Table One. Bring power up slowly with the Variable Transformer while monitoring the +5V output with the scope and DVM and the input with the wattmeter. If the watttmeter registers high input power with low AC voltage applied, shut down power immediately and refer to the No Output section. Supply should start with approximately 50 to 70 VAC applied and should regulate by the time 95 VAC is reached. If the output has reached 5 volts, do a performance test as shown in the Performance Test section. If there is no output, refer to the No Output section.

No Output

1. Check the fuse. If the fuse is blown, replace it. Do not apply power until the cause of the failure is found.

2. Check the diode bridge (DB1), power transistor (Q2), catch diodes (D3, D4), turn-off transistor (Q1), emitter resistor (R13), D1, and R2.

3. Use the ohmmeter from output common to each output with output loads disconnected and check for shorted rectifiers or capacitors. If +24V output seems shorted, check crowbar SCR (SCR1) and zener (Z1).

4. Check for B+. Set up power supply and attach X100 scope probe ground to the point common to R10, D1, and R6; this point is between the large black input capacitors and the control transformer (T1). Slowly turn up power and check for B+ on the side of R2 nearest to R3. With input at 95 VAC, this point should be between 250 and 300 VDC. If it is not, check fuse, DB1, and if necessary, TM1 and TM2 (4 ohms each), D3, and D4, and input capacitors C6 through C9. If B+ is present at this point, but the power supply still does not run, check the other side of R2. Replace R2 if B+ does not read almost the same value.

5. Check the Q2 waveforms. Use the X100 probe on the To-3 package of Q2 and check the collector waveform. The transistor should be switching. The correct waveform is shown in Figure 2. If this waveform is not present, check for a shorted junction on Q2. If there is not one, check the base waveform. The base of Q2 is the transistor pin nearest the bolt attaching the hestsink to the PCB. The correct waveform is shown in Figure 3. If the waveform is not there, read what DC voltage is present. If there is not at least 0.5V on the base, check continuity of L4, Q1, D1, R3, R4, R5, and C10.

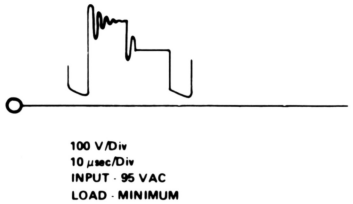


Figure 2. Q2 Collector Waveforms

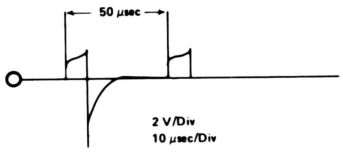


Figure 3. Q2 Base Waveforms

Performance Test

Each of these test conditions should be set up and noted to be within the limits specified in Table 2.

Test	Input	+5 Load	+24 Load	-12 Load
1	95VAC	Max	Max	Max
2	135VAC	Max	Max	Max
3	135VAC	Max	No Load	Max
4	135VAC	Min	No Load	Min
5	95VAC	Min	No Load	Min

Table 2. Voltage and Ripple Specifications

Output	Min	Max	No Load	Ripple
+5V	4.90V	5.10V	----	50mV P-P
+24V	21.20V	26.40V	30V	250mV P-P
-12V	-11.40V	-12.60V	----	50mV P-P

HARD DISK CONTROLLER BOARD

General

The hard disk controller board is a discrete implementation of all functions required to control the eight-inch hard disk drive via a standard data and control bus. The controller is fabricated using a mix of high-speed bipolar and NMOS devices contained on a single two-sided PC board. The design of the circuitry makes use of a high-speed microcontroller, the 8X300, newly developed NMOS support devices, Schottky and low power Schottky devices. All I/O connections are made using standard ribbon cable connectors. Standard pin-out configurations for disk interface connectors permit direct pin-for-pin connections to the drives. All power for the board is supplied by a single 5-volt power supply. All host to disk data transfers are buffered by onboard RAM to achieve totally asynchronous transfers to and from the disk by the host.

The disk controller is built around five basic sections:

1. Processor functions
2. Serial data separation
3. Data conversion and checking
4. Serial data generation
5. Host interface functions

Processor Functions

All functions of the controller are ultimately desciplined by the onboard processor. Due to the high data rates associated with hard disk drives, a processor capable of extremely fast execution speed is required for processing of data and controlling machine functions within the circuitry. The processor used is the 8X300, a bipolar micro-controller particularly well suited for handling data efficiently at high rates.

The 8X300 operates at a basic clock rate of 8 MHz and performs all operations within two clock cycles giving it a speed of 4 MIPS (Million Instructions Per Second) or one instruction executed every 250 nanoseconds. The architecture of the processor is different from most popular microprocessors in that no common data or address bus is provided to be shared by RAM, ROM, or peripheral devices.

Instructions are fetched from ROM via a dedicated instruction address and data bus. The Instruction Address bus (IA0 - IA13)

is capable of directly accessing 8K words of program storage, however, the controller uses only the first ten address lines, IA0 through IA9, limiting onboard program storage to 1K words.

Program data is input to the 8X300 (U30) on the Instruction Data bus (ID0 - ID15) as 16-bit words which are decoded to perform the desired operation. All bus designations utilized by the 8X300 are reversed from the traditional LSB (Least Significant Bit) to MSB (Most Significant Bit) weighting.

Fast IO Select

An extension byte has been added onto the instruction data memory to provide port access decoding on an instruction-by-instruction basis. This "Fast IO Select" byte is not processed by the 8X300, but rather it is decoded by auxiliary hardware (U31, U37, U38) to provide eight read strobes and eight write strobes which route data to the various devices distributed along the interface vector bus.

The Fast IO byte is latched into a 6-bit latch (U31) on the trailing edge of MCLK to ensure that the data remains stable during the entire instruction. This data selects a read strobe and a write strobe through two 1-of-8 decoders (U37 and U38) which are alternately enabled by the WC* control strobe produced by the 8X300. The read strobe decoder (U37) is always disqualified at the end of instructions by MCLK' (MCLK prime), a delayed copy of MCLK, to provide edges on read strobes during sequential read operations from various ports. This delay compensates for timing races through the Fast IO latch (U31) and the control signals.

Because each decoder has a unique input, it is possible to select any read port with any write port during each instruction. Data is transferred between the processor and its ports on a separate 8-bit bus called the IO bus. This bus is active low. It must be noted that this bus is in no way related to the instruction data bus and should be thought of as simply an 8-bit bidirectional IO bus of the 8X300. In fact, it has been renamed as IO0 - IO7 to reflect this distinction.

Internal Bus Control

Several bus control signals are produced by the 8X300 to identify and strobe the data on the IO bus. Write Control (WC) is a signal which determines the direction of the data to and from peripherals. When WC is false (during the first half cycle), data is being input to the 8X300 from the IO bus. When WC is true (during the second half cycle), data is being output to the IO bus from the 8X300. Select Control (SC) is

becomes active during the second half cycle instead of WC if the IO bus contains an 8-bit IO address. The WC and SC signals are combined by a NOR gate (U24) to indicate all accesses to any port. This arrangement allows immediate data moves from the 8X300 to any output port within one instruction instead of the normal 5-bit immediate moves provided for by the instruction set.

All instruciton fetches occur late in the second cycle of the preceeding instruction. This time is marked by the generation of a 65 ns (nominal) active high pulse called MCLK which occurs every instruction. MCLK is used to latch data prior to being input on the IO bus to ensure stability during reads. MCLK is also used to disqualify read strobes which would otherwise remain true into the second clock cycle of any instruction which does not write to a port.

There are two more bus control signals produced by the 8X300, Left Bank select (LB*) and Right Bank select (RB*). However, due to the implementation of the Fast IO Select logic, only RB* which is used as the chief enable signal for U56 and U57 is needed.

Reset Circuit

The 8X300 is held reset for approximately 40 milliseconds after initial power on. This is accomplished by an RC network (R45, C40, and CR3) which drives a Schmitt trigger (U35) to provide a proper rise/fall time on the RESET* line of the 8X300. Alternate reset of the processor can be accomplished by dropping MR* (J1 pin 32) whenever the host wishes to reset the controller. A Schmitt trigger (U35) is provided with a 4.7K pull-up resistor (R46) to buffer the MR* input from the host. RESET* also propagates to the drive control latches (U52 and U51), host interface WAIT (U36), and DRQ* and INTRQ* latches (U4), ensuring proper initialization of these functions during power up and subsequent resets from the host.

Processor Power Supply

Power is supplied to the 8X300 from the +5 volt (Vcc) power bus. Due to the internal operation of the 8X300, an on-chip voltage reference is provided to produce bias to an external pass transistor (Q3) which drops Vcc to the 8X300 to approximately +3 volts. All signals into and out of the 8X300 are internally level shifted to be TTL compatible.
Read and Write Ports

Throughout the circuit, output ports are formed by "D" type latches using write strobes (WR0 - WR7) to latch data into the

ports. Reading of ports is universally accomplished by using read strobes (RD0, RD2, RD4 - RD6) that enable selected tri-state output devices on the IO bus. Additionally, two read strobes are used to clock the host DRQ* and INTRQ* latches (U4) and one read strobe is left unused as a "dummy" port for instructions not requiring data from a port. This ensures glitch-free operation of the Fast IO port decoders.

Read/Write Memory

Since the 8X300 does not permit data to be saved or retrieved from dedicated program storage, RAM must be installed on the IO bus. RAM must be accessed just like other port accesses via the IO bus by IO instructions. To provide for addressing the RAM, three latch/counters (U48, U47, and U46) are connected to the IO bus to receive and store addresses required to access the RAM (U56 and U57).

RAM Addressing

The RAM address bus (RA0 - RA9) uniquely addresses one of 1024 memory locations. As each counter chip reaches a count of 0, it will set a borrow condition to the next higher counter which will be decremented at the end of the next access to RAM. When all bits of the address have been reset, the ROVF* bit on the last counter (U46) will be reset providing an overflow status which can be read by the processor on U50. By setting various beginning address values, ROVF* can be used to mark the end of any RAM access loop from 1 to 1024 bytes in length. The controller board uses this function to set sector buffer lengths of 128, 256, or 512 bytes.

Sector Buffering

All data read from or written to the disk is passed through the RAM to provide buffering required for asynchronous data transfer between the host and disk. The counters are post-decremented, which means that the effective addresses are stable to the RAM by at least the instruction prior to the actual access. This pre-selection feature effectively reduces RAM access time to the output enable and propagation time of the RAM for read operations. This feature also reduces the width of the minimum WR* strobe pulse for write operations.
RAM Accessing

RAM access is initiated by RCS* which is the logical OR (by U39) of RD0* and WR0* which are generated by the Fast IO decoders (U37 and U38). Data to be read from RAM will be placed on the IO bus whenever RCS* is low and WC* is high. Data is written into a selected RAM cell on the trailing edge

of WC* if RCS* is low. During writes, both WC* and RCS* will be low for at least 120 nanoseconds so that data setup time requirements are met.

Scratchpad Operations

Because the RAM address counters are pre-settable, direct reads and writes to a specific address are possible. This function is used for scratchpad storage during program execution. This mode of RAM access requires two or three instruction cycles for each random access to the RAM as opposed to one for sequential access using the post-decrement feature.

MAC Control Port

Basic control of the various functional sections of the controller is accomplished by a dedicated 6-bit control port called MAC CNTRL (U3). MAC CNTRL enables CRC generation (CRCIZ*), functions of the WAIT control circutiry (WAEN*), gating of read data into data separation circuitry (RGATE), selection of read or write functions (WRITE*), control of CRC check word output (1BLA*), and AM detection (SRCH). MAC CNTRL output states are latched into the port by a write strobe (WR7). Additionally, any time MAC CNTRL is loaded with a new byte, the lower two data bits (IO0 and IO1) are strobed into the upper two address counter/latch bits (RA8 and RA9). All remaining ports are distributed among the basic functional sections of the controller and will be described in detail within the discussion of those functions.

Serial Data Separation

The controller board contains circuitry which processes incoming MFM data from the drive by a method called data separation. Here, some background information may be helpful:

> In order to provide maximum data recording density and therefore maximum storage efficiency, data is recorded on the disk using a Modified Frequency Modulation (MFM) technique. This technique requires clock bits to be recorded only when two successive data bits are missing in the serial data stream. This reduces the total number of bits required to record a given amount of information on the disk. This results in an effective doubling of the amount of data capacity, hence the term "double density".

Because clock bits are not recorded with every data bit cell, circuitry that can remain in sync with data during the absence of clock bits is required. Synchronous decoding of MFM data streams requires the decoder circuitry to synthesize clock bits when they are present. This is accomplished by using a phase-locked oscillator employing an error amplifier/filter to sync onto and hold a specific phase relationship at the data and clock bits in the data stream. The synthesized clock called RCLK can then be used to separate data bits from clock bits and to shift the resultant serial data into registers for parallelization into bytes.

Incoming Data Selection

Serial data is input from up to four radially connected drives via a quad RS-422 differential receiver (U25). The receiver converts differential input data to TTL levels for use by the controller. The data from the selected drive is then routed to the data separation circuitry by a four-section AND/OR/INVERT gate (U15). At this point, data and clocks are still combined and appear as 50 nanoseconds (nominal) active high pulses spaced at intervals of one, one and a half, or two times the RCLK period. This data is presented to the input of another AND/OR/INVERT gate (U18) which will gate either MFM data or a reference clock into the first stage of the VCO error amplifier circuitry.

Reference Clock

The reference clock is derived from the write clock crystal oscillator (Q2, U12, and associated circuitry). This oscillator uses a fundamental cut crystal to oscillate at four times the RCLK frequency. The 4X output is then divided by U12 to produce both a 2X clock (2XDR*), which is used as a refence, and a 1X clock (WCLK) which is used to produce MFM write data for the disk. The crystal (Y1) frequency is 17.360 MHz for compatible drives.

Clock Gating

The gating of the reference and MFM data into the data separator is dependent upon the condition of the Read Gate signal (RGATE) and the spacing of the data on the serial stream after RGATE is brought true. Due to the techniques which are employed to separate data from clocks, it is necessary to run the VCO at a rate twice the data clock (RCLK) rate. The VCO is therefore set to an open-loop frequency of 2 times RCLK. Any variations in this rate due to variations in disk rotational speed must be compensated for by the VCO, but instantaneous shifts in data due to the effects of adjacent

bit cells on the disk and minor noise must be ignored. Also, the response of the VCO must be adjusted to effectively ride over missing clock bits which occur as a result of the MFM recording technique. The resultant compromise between response and reject requirements of the VCO cause the VCO to have a tendency to become locked onto harmonics of the data rate rather easily. This is likely to occur if the VCO is connected to a data stream over a field of data which has data bits spaced at one and a half or two times the actual RCLK time intervals.

To provide protection against this undesirable condition, the VCO is always held locked onto a stable clock running at two times the RCLK frequency whenever the controller is not actually reading data. Furthermore, great care is taken to switch in read data to the VCO error detector only when it is known that the data stream frequency is equal to the RCLK frequency. This can occur only when the data is a solid stream of all ones or all zeros.

High Frequency Detector

The switching function is initiated immediately after RGATE goes true and will only switch read data into the VCO after 16 consecutive ones or zeros (high frequency) are detected by a one-shot (U8) and counter (U9) connected directly to the raw MFM data. The one-shot is adjusted for a pulse width of one and one fourth times the RCLK period. This is 287 nanoseconds, +/- 10 ns. These adjustments of the DRUN one-shot (U8) provide tolerences of up to one fourth the RCLK period in jitter on the MFM data bits while still being able to distinguish MFM zeros or ones from other data patterns.

Each clock or data bit on the serial stream triggers the one-shot. If the time between sucessive triggers is less than the one-shot time constant, the one-shot remains retriggered. As the one-shot is triggered by data stream bits, so is the up/down counter (U9) whose count mode is controlled by the state of the one-shot outputs. While the one-shot is being retriggered, the counter counts up. When any data bit fails to reach the one-shot before its time constant is over, the one-shot resets and in turn clears the counter. Only when 16 sucessive retriggers occur, can the counter reach its terminal count. At this time, the counter overflow goes true and sets the DRUN* latch output (U10 pin 8) low which switches read data in and reference clock out. An AND-OR-INVERT gate (U18) performs the switching. DRUN* is read through U43 by the 8X300 to determine the condition of the MFM data stream.

VCO

RCLK is produced by the VCO through a divide-by-two counter (U11). The VCO is a discrete LC oscillator with a shunt capacitor formed by a hyper-abrupt tuning diode (CR2). The diode varies its capacitance as a function of the amount of reverse DC bias applied to its PN junction. As bias decreases, the capacitance increases which pulls the oscillator down in frequency. Conversely, as the bias increases, the oscillator frequency rises.

The VCO performs conventionally with one interesting exception. To help the VCO lock onto the incoming signals more quickly, a provision has been made to allow an external timing signal to freeze the output of the VCO in the high state. This is accomplished by disqualifying U2 in the VCO feedback circuit and by removing bias from the transistor (Q1) which provides loop gain in the oscillator. PHASEUP* performs this function and is present just after the switch over from reference clock to MFM data is made.

The width of PHASEUP* is directly related to the difference in timing between the positive-going transition of the VCO output and the positive transition of the second data/clock bit of the MFM data stream. PHASEUP* causes the output of the VCO to rise in phase with the MFM data from the drive. This eliminates the need for the VCO to perform a frequency acquisition to lock onto the data stream. The VCO need only adjust its phase slightly to center data/clocks within the RCLK. The phase acquisition is much faster and easier to achieve and results in vastly improved performance.

Error Amplifier

Control of the VCO is accomplished by the error amplifier and filter. The error amplifier is a balanced differential amplifier whose output sources or sinks current to the filter stage. The output of the error amplifier is pulse-width modulated by the phase detector (U7, U17). Whenever the VCO is running too slow, the error amplifier receives pulses from data bits before it receives pulses from the VCO clock. This causes the error amplifier to produce pump-up pulses to the filter. The filter integrates these pulses producing an average increase in the voltage to the cathode of the hyper-abrupt tuning diode (CR2). This effectively increases the reverse bias on the diode which reduces its capacitance and therefore increases the VCO frequency slightly to match the phase of the incoming data. Whenever the VCO is running too fast, the error amplifier produces pump-down pulses to the filter. The diode then receives decreased reverse bias and,

therefore, more capacitance and lower VCO frequency.

The operating point of the tuning diode (CR2) is initially set for an open-loop VCO frequency of two times RCLK by setting OSC ADJUST* and monitoring the VCO output. This adjustment places the initial bias through the bias divider (R3-R6, C1 and C2) at approximately -2.8 volts to -3.2 volts. At this setting, the most responsive region of the diode is being used giving higher gain in the VCO. To keep the initial bias voltage close to 3 volts with varying disk data rates, the VCO incuctor (L2) is 3.9uH.

The VCO is forced to match the phase of the incoming data. Once the VCO is close to the phase of the incoming data, the pump pulses will become very small or be missing completely. It must be noted that some slight error will always be present because without pumps, the filter will float and the VCO will drift. However, the overall gain of the error amplifier and the VCO will maintain this error very small, resulting in very close tracking between the VCO output phase and the incoming data phase.

Previously, we said that great care is taken to ensure that the VCO starts on the same phase as the incoming data. If this were not the case, the error amplifier would produce very large pumps in an attempt to pull the VCO onto frequency and phase. Due to the gain of the error amplifier and the required characteristics of the filter, the integrated pump pulses would overcompensate, causing the VCO to overshoot in its attempt to lock-on. This action would continue in a diminshing fashion until lock-on occurred. Unfortunately, the data sync fields it was trying to accquire would be over by the time the VCO finally acquired lock-on. Therefore, PHASEUP* is extremely important to the overall ability of the data separator to function reliably.

Sample on Phase Detector

The circuitry which feeds the error amplifier is called the Sample on Phase Detector. This circuit consists of several "D" latches (U17) and a delay line (DL1). The function of the circuit is to provide time windows during which the leading edges of the incoming MFM data can be compared to the leading edges of the VCO clock. These windows are approximately 50 nanoseconds in length and are initiated by the leading edge of any data bit as it enters the detector. The windows are terminated by the same data bit, edge-delayed by a net 50 nanoseconds (60 ns in the delay line minus approximately 10 ns in propagation delays).

When both the delayed data bit and the nearest VCO edge arrive at the detector, the detector is reset until the next data bit arrives on the MFM data stream. The delayed data bit sets its half of the detector latches to produce a pump-up condition at the error amplifier. The VCO clock edge sets its half of the detector to produce a pump-down condition. When the circuit is balanced, both pumps are either on or both pumps are off, producing no net pump-up or pump-down.

Window Extension

Once the VCO has been locked onto the phase of the incoming data, the actual separation of data and clocks can occur. This is accomplished by using a technique called window extension. This technique causes data bits to first have their leading edges shifted into the center of the RCLK half cycles then to have them latched or extended until the next rising edge of the RCLK. The shift is accomplished by tapping the data of the Sample on Phase Detector delay line at the 60 nanosecnd tap, and inverting the VCO clock to the RCLK divider (U11). The delayed data clocks a pair of latches (U20 and U21). The "data" latch has its "D" input and CLEAR connected to RCLK* and the "clock" latch has its "D" input and CLEAR connected to RCLK*.

If a MFM data bit enters the latches while RCLK is high, it will be extended as a data bit. If RCLK* is high, it will be extended as a clock bit. Due to this extension technique, bits can jitter approximately one-fourth the RCLK period without being lost. The output of each latch is then further extended by being fed directly into the second half of the latches and clocked on alternate edges of RCLK. The final outputs of the data extension/separation stage are two separate signals; one signal consists solely of NRZ (non-return to zero) data and the other of NRZ (non-return to zero) clocks. The NRZ data and clocks are finally in a form suitable for processing by subsequenct circuitry on the Controller board.

Clock Detection

Due to the nature of MFM data encoding, it is impossible to know exactly if MFM bits are data or clocks. This ambiguity results in having to create circuitry to assume that bits on RCLK* are actually data bits until the VCO is locked on and a unique data/clock pattern is detected. This is accomplished by holding the VCO to RCLK divider (U11) reset until it is fairly certain that bits on the data stream are actually clocks belonging to a field of zero data.

Once this assessment has been made, the processor releases the

AM detector (U22) by raising the SRCH signal. This signal releases a latch (U11) which will remove DHOLD from the RCLK divider (U11) on the next rising edge of a MFM data bit so that CLOCKS will be on the RCLK* phase and DATA will be on the RCLK phase. The processor makes its assessment of the state of the data stream solely on the occurrence of a significant run of zeros which is detected by the one-shot (U8) in the DRUN circuit. Once released, the phase of RCLK vs. data and clocks will remain stable throughout the read of an ID field or data field. Whenever SRCH is dropped, the VCO to RCLK divider is once again reset and no RCLKS are produced.

Data Conversion and Checking

MFM data which has been separated to form NRZ data and clocks is processed through specialized circuitry to prepare it for parallel processing by the 8X300. This processing consists of three functional circuits.

1. AM detection (U22)
2. Serial-to-Parallel conversion (U24)
3. CRC checking circuit (U14)

Each function will be discussed separately but bear in mind that many interdependencies exist.

AM Detection

As previously stated, it is impossible to know whether serial data bits are actually data or clock bits by just looking at the data stream. Furthermore, it is equally impossible to determine byte boundaries. The problem is solved by a uniquely recorded data/clock pattern called an Address Mark (AM). The AM consists of a data pattern of HEX 'A1' with a missing clock pattern of HEX '0A'. Normally a data byte of HEX 'A1' requires a clocking pattern of HEX '0E'. In fact, due to the rules of MFM data encoding, an alternating clock pattern such as HEX 'A' or HEX '5' cannot exist legally.

The AM is used to uniquely identify the start of a field of information (data or ID field) within each sector. A long run of zero data always precedes each AM on the disk. Zeros have a clock bit for every RCLK. When attempting to read information from the disk, the Controller first acquires phase lock over a field of zeros. When this acquistion is achieved, the processor releases the AM detector (U22) by raising the Search control line (SRCH) on the MAC CNTRL port (U3).

Due to the circuitry associated with the VCO to RCLK divider, the RDAT* output of the data separator (U20 pin 6) will be high and the CLKS* output (U21 pin 8) will be low. RCLK* will be the shifting clock for RDAT* and RCLK will be the shifting clock for CLKS*. These four signals are routed into the AM detector. Inside the AM detector, RDAT* is shifted into an 8-bit synchronous serial shift register and clocked on the falling edge of RCLK*. CLKS* is shifted into a similar shift register on the falling edge of RCLK. The output stage of the RDAT* register is dumped into an 'A1' comparator and the output stage of the CLKS* register is dumped into a '0A' comparator. AM detection occurs when both detectors are true, thereby setting the AMDET* latch. At the instant AM occurs, the exact relationship between data and clocks is known. It is also known that data is being clocked by RCLK* so CLKS* can actually be discarded; their purpose was in detecting AM. The AMDET* signal is used as a synchronization signal to start subsequenct conversion circuity. The AMDET* signal remains true until the processor again de-asserts the Search control line.

Serial to Parallel Conversion

After an AM has been detected, the serial-to-parallel converter (U24) takes over. NRZ data and RCLK are used to shift data bits into an 8-bit serial-to-parallel shift register. As each bit is shifted, a divide-by-8 counter circuit is incremented. After every eighth bit of data is shifted, the counter produces an overflow pulse marking byte boundaries in the serial data stream. The overflow bit from the counter resets the counter, clocks the data from the shift register into an 8-bit parallel latch, and sets a tri-state flag register called BDONE. The flag can be read by the processor to see if any converted data is ready to be read from the latches.

When the processor sees BDONE in the true state, it services the device by gating data onto the IO bus using read strobe 4 (RD4*) in conjunction with a tri-state buffer (U23). The act of reading the latches also clears off the pending BDONE flag. As successive bytes are processed, the BDONE is serviced by the processor as data becomes available.

Outputs from the serial-to-parallel device also include SHFCLK* and DOUT. SHFTCLK* is actually RCLK* propagated through the device. DOUT is the Q output of the last stage of the shift register string. DOUT and SHFTCLK* are routed to the CRC generator checker device and also are tri-stated along with BDONE. These signals are active only when WRITE* is high which indicates a read mode of operation.

CRC Checking Circuit

Data recorded on magnetic media is prone to several types of errors which could render data unusable if some form of error detection were not employed. Therefore, a cyclic redundancy check (CRC) is performed on all data transfers from the disk. The CRC is an error detection code consisting of 16 additional bits which are appended to every ID field and data field on the disk. These bits are produced by dividing the data stream serially with a large polynomial. This division produces a unique 16-bit value for any information passed through the CRC generator.

As data is being read from the disk, the CRC generator (U14) re-computes the original CRC bits. The value in the CRC generator must always be zero after the last two bytes (which contain the original recorded CRC) are read. When this happens, the data was correctly read and the controller will not flag an error. If, however, the CRC generator is not zeroed after it has checked all bytes of the recorded data, the controller will flag the data as erroneous and enter into a re-try condition. If the controller cannot get correct data after attempting to read it 16 times, the read will be aborted and the host informed that the data in the buffer is questionable.

The Controller board uses the same device to generate and check CRC's for data being written to or read from the disk. The polynomial used is:

$$X^{16} + X^{12} + X^{5} + 1$$ (commonly called the CRC-CCITT polynomial)

The processor polls the condition of the DRUN circuitry during read operations. When DRUN is true, it begins to search for an address mark. Once the AM is located, the processor will start to read parallel data which has been converted from NRZ data by the serial-to-parallel device. The processor will terminate this activity when it has received the information it is looking for or if an error is detected.

While the processor is reading the parallel data, the CRC generator is reconstructing the CRC check value. The CRC generator is initialized by the processor setting CRCIZ* low for at least 250 nanoseconds during the search for the AM. CRCIZ* is originated on the MAC CNTRL port (U3). Upon receiving the CRCIZ* signal, the CRC generator/checker will preset all 16 of its internal polynomial division shift registers to logic ones and arm an internal latch which will

enable the checking function on the leading edge of the first non-zero data to enter the device. It should be remembered that prior to an AM there is always a field of zeros (all data bits low) so the first non-zero data bit into the device will always be the most significant bit of the AM (HEX A1).

The CRC device, when enabled by the first non-zero data bit, will shift succeeding data bits into a feedback shift register string with Exculusive OR gates tied to the feedback nodes on the first, fifth, twelfth, and sixteenth registers. As each RCLK occurs, the registers will divide the incoming data and a unique pattern of ones and zeros will appear across the registers.

When the last bit of an ID or data field is processed, the pattern in the registers should be equivalent to the 16 bits appended to the fields during original recording. The appended bits are also entered into the CRC device. If all of the bits in the appended field are identical to the bits in the registers, then the Exclusive OR gates in the register string will have flipped all of the ones to zeros and the CRC will have been satisfied.

The output of each register stage is tied to a 16-bit comparator which goes true when all of its inputs are zeros. The output of the comparator is retimed to remove any decoding slivers and is output as CRCOK. The processor can read CRCOK through U50 to see if a CRC error has occurred.

After the CRC bits are processed, the data stream will contain at least one more byte of zeros. It is the nature of the CRC polynomial that if no bits are set to ones in the registers and if a constant input of zeros is shifted into the registers, no bits will be flipped. This provides a convenient latching function for the CRCOK flag which will remain true for at least one byte after the last CRC check byte, giving the processor time to read the flag.

The data, clock, and BDONE are supplied to the CRC device on a 3-bit mini bus. During read operations, the serial-to-parallel device (U24) will be sourcing these lines since the WRITE control line from MAC CNTRL (U3) is low and this enables tri-state drivers on these lines. The Parallel-to-Serial device (U13) will have its tri-state drivers disabled.

Serial Data Generation

The Controller records data on the disk in MFM format. In order to produce the proper data format, the Controller uses

several specialized devices to process the parallel data supplied by the host into a serial MFM data stream. The data supplied by the host is temporarily stored in the buffer RAM until the correct sector is located for the data to be written.

The process of writing is essentially the opposite of reading except that the data separator circuitry is not required and the generation of the MFM data stream is produced by synchronous clocking techniques.

The functional sections of the serial data genration section are listed below:

1. Parallel-to-Serial conversion (U13)
2. CRC generation (U14)
3. MFM and precompensation (U4)

Parallel to Serial Conversion

Parallel data is converted into a serial NRZ data stream by the parallel-to-serial device (U13). The processor enables this conversion by lowering the WRITE* signal on MAC CNTRL (U3). WRITE* causes the tri-state buffers present on the parallel-to-serial device to become active, supplying the CRC device with data, clocks, and BDONE strobes.

The processor presents parallel data on the IO bus along with the WR4* write strobe which latches the data into the parallel port on the BDONE. Inside the parallel-to-serial device, the parallel latches are loaded into a serial shift register on every eighth WCLK transition. As the data is transferred to the shift registers, the BDONE status flag is set. The processor reads this flag through U50 to determine when to write the next parallel byte to the device. The timing of the parallel accesses is at a rate one-eighth that of the bit rate of the NRZ data stream.

The output of the last register in the shift string is brought out of the device as a NRZ serial data stream. The shifting clock is also brought out as SHFCLK to be used as the clock for the CRC device.

Whenever it is desired to write a repetitive string of identical data bytes, the processor can simply ignore the BDONE flag and permit the device to reload the data from its latches over and over again for as long as required to generate the field. This feature of the device is used in writing certain fields used in formatting.

CRC Generation

The CTC generator/checker (U14) is used to generate the CRC bits and to append them to the end of the data being written to the disk. This is the complementary function to that performed during reads. The operation of the polynomial generator is identical to read operations except that at the end of the data field, the processor sets a signal which causes the device to output the computed CRC after the data instead of reading the CRC and checking it.

The initial state of the shift registers within the device is forced to all ones by the processor pulsing CRCIZ* for approximately 250 nanoseconds while the parallel-to-serial device is outputting all zeros on the NRZ data line. At that time, a latch is set which holds the registers at ones until the first non-zero data bit enters the device. The first non-zero bit will be the MSB of the AM (HEX A1) of the data field to be written. When the processor decides that enough zeros have been written to satisfy the sync field requirements, it will store a HEX A1 in the parallel-to-serial device. At the proper time (in sync with BDONE) the parallel-to-serial device will begin to send the MSB of the AM to the CRC device. This will start the CRC polynomial generator and the CRC will be computed.

As the processor writes the last byte of data to the parallel-to-serial device, it will drop the 1BLA* (1 Byte Look Ahead) signal on MAC CNTRL port (U3). This signal will cause the CRC generator (U14) to begin dumping the computed CRC onto the NRZ data stream at the conclusion of the last data byte (synchronized with the BDONE signal). In this fashion, the device is able to append the proper CRC information to the end of a field of data. 1BLA* is maintained at a low state for the duration of the unloading process which lasts for 16 bit times.

During the unloading process, the CRC registers back-fill with zeros. This feature is handy because by leaving 1BLA* low ;for additional time, zeros will always be written after the CRC which is a requirement for the proper operation of the CRC device during read operations. The NRZ data with CRC appended is then sent to the MFM generator device (U4).

MFM Generation

The conversion from NRZ write data to MFM write data takes place in the MFM/Precompensation device (U4). This device accepts NRZ data and a complimentary WCLK and produces MFM data and clocks by sending the data through circuitry which

decides when and where to write clocks on the data stream under the MFM encoding rules. The proper encoding of the data into MFM requires the device to apply three rules to the data.

1. If the current data cell contains a data bit, no clock bit will be generated.

2. If the previous data cell contained a data bit, no clock bit will be generated.

3. If the previous data cell and the present data cell are vacant, a clock bit will be produced in the current clock cell.

The terms "data cell" and "clock cell" are defined by the state of the WCLK. While WCLK is low it, is a data cell and while high, it is a clock cell. It can be seen then that both clock and data cells are one-half the period of WCLK or 115 nanoseconds. Also note that by the rules started above, a clock and data bit can never occur within the same WCLK period and legal spacings for bits can be one, one and a half , or two times the WCLK period only. The rules are implemented within the device by shift registers that hold the next two, last, and present data bits and combinational logic. The state of WCLK is considered and the approopriate bit cells are filled and combined on the MFMW output line of the device. This line is subject to decoding slivers, so it is run through a re-timing latch (U5) to clean it up.

Write Precompensation

The MFM data stream is now totally compatible with the recording rules and may be sent to suitable line drivers for transmission to the drive except for one modification. Due to the decreasing radius on the physical surface of the disk, the inside tracks have less circumference and therefore exhibit an increase in recording flux density over the outside tracks. This increase in flux density aggravates a problem in magnetic recording know as dynamic bit shift.

Dynamic bit shift comes about as the result of one bit on the disk (a flux reversal) influencing an adjacent bit. The effect is to shift the leading edge of both bits closer together or further apart than recorded. The net result is that enough jitter is added to the data recorded on the inside tracks to make them harder to recover without error. In any event, there is a method called write precompensation which can be applied to reduce the effect of this shift on the data.

Write Precompensation is a way of predicting which direction a

particular bit will be shifted and intentionally writing that bit out of position in the opposite direction to the expected shift. This is done by examining the next two data bits, the last bits, and the present bits to be written and producing three signals depending on what these bits are. The three signals are EARLY, LATE, and NOM. They are used in conjuction with a delay line to cause the leading edge of a data/clock bit to be written early, late, or on time. As with MFMW, these signals are subject to decoding slivers and must be retimed by U5.

The processor can enable or disable the generation of these signals by controlling the RWC (Reduce Write Current) line from U51. When RWC is high, precompensation is in effect. When RWC is low, no precompensation is generated and the NOM output of the device is held true.

The delay line, U6, actually performs the precompensation with the help of an AND-OR-INVERT gate (U16). The MFMW pulses are applied to the input of the delay line and, depending on which of the three precompensation signals is present, the U16 selects a different tap on the delay line. Nominal data is actually tapped from the second tap, early data from the first, and late data from the third. From U16, the MFMW data is sent to the input of a quad driver (U26) where it is converted to a differential form and then sent to the disk drive. The AND-OR-INVERT gate (U16) has one other function. If the controller is not writing, the WGI (Write Gate Internal) signal will be low. This is inverted by U35 and applied to the fourth section of U16. This resulting high input effectively inhibits the gate from accepting MFMW data.

Host Interface

All data transfers between the host and the Controller take place over an 8-bit bidirectional bus consisting of eight Data Access Lines (DAL0-DAL7) between U49, U58 and U59. The source or destination register is selected by three address lines HDBA0 through HDB2. All accesses are controlled by Card Select (CS*), Read Enable (RE*), or Write Enable (WE*). Since the access time for any particular read or write operation will vary, the Controller provides a not-ready signal (WAIT*). For systems using interrupts and/or DMA, the Controller provides Interrupt Request (INTRQ) and Data Request (DRQ).

Accessing the Controller is essentially like accessing variable speed RAM. The host must provide a valid address in HDBD0* through HDBD2* along with a CS*. The host may assert RE* or WE* either immediately or after a short set-up time. If

access time will be over 100 nanoseconds, WAIT* will be asserted. The host must keep all address lines and strobes stable while WAIT* is true. When the Controller de-asserts WAIT*, the data has been accepted on a write or the data is on the DAL bus on a read.

Wait Enable

Since most of the registers in the Controller are not implemented in hardware, it takes the 8X300 a finite amount of time to fetch the requested data on a Read or store data on a Write. This time varies depending on the amount of processing the 8X300 must do to access the desired register. After the data has been written or read, the WAIT* line de-asserted allowing the host to terminate the current bus cycle.

The generation of the WAIT* signal is controlled by a bit in the MAC latch (U3) called Wait Enable (WAEN*). If the Controller is ready to accept random accesses to its task file, WAEN* will be asserted. The host must drop the Card Select (CS*) line on J5 upon each bus access. The leading edge of CS* clocks the wait control latch (U32), transferring the WAEN* state through the latch, qualifying the wait drivers (U45, U42). This clocking action is required to insure that WAIT* will not be asserted in the middle of any bus access already in progress. After the wait latch has been clocked, CS* (BIC* or BOC* in some installations) causes WAIT* to be asserted to the host.

The WAIT* line is released on the trailing edge of any read or write strobe to the communications latch (U49). This release is caused by the logical OR of RD6* and WR6* on U45 which presets the wait latch (U36) to a non-wait request condition.

Bus Gating

During all accesses by the host, one of two signals will be produced to gate the bus. During read operations, CS* and RD* are ANDed, producing Bus Output Control (BOC*). This signal gates the contents of the communication latch (U49) onto the DAL bus. During write operations, CS* and WE* produce Bus Input Control (BIC*). This signal latches the state of the DAL lines into an internal R/S latch.

Register Selection

The combination of a host read or write operation along with the WREQ* signal being asserted causes a signal, Card Select Access (CSAC), to be generated. The 8X300 samples this signal at U50 every 250 nanoseconds and, if asserted, reads the

status of A0 through A2 and WE* (U60). The state of A0 through A2 and WE* determine which register is to be accessed and in what direction that access will take place.

Interrupts and DRQ's

The Controller produces Interrupt Requests (INTRQ) to signal the end of all disk operations and Data Requests (DRQ) to signal data ready to DMA controllers. INTRQ* and DRQ* originate on the MFM generator (U4) as an auxillary function of the chip. The INTRQ* signal is set using INTCLK and the DRQ signal is set using DRQCLK, both of which are produced by U37. Interrupts are cleared by CSAC'* (a 200 nanosecond version of the CSAC signal) and A0 and A1 whenever the host reads the Status register, issures a command, or accesses the sector number register. DRQ's are cleared when the host accesses the Data or Cylinder Low registers. DRQs will be re-issued for each byte to be transferred. During Power On Reset or Master Reset (MR*), INTRQ is set and DRQ is reset.

HARD DISK INTERFACE BOARD

Signal Interfacing to the Model II Bus

Data is passed between the Hard Disk Interface Board and the Model II system bus via two 8T26 transceivers, U40 and U41. Address and control signals are taken from the system bus and are buffered by two LS240 inverting drivers, U29 and U43. U29 carries the address lines and U43 carries the control signals. The WAIT* and XFERRQ* signals are driven to the system bus by one-half of U28, a 7438 open-collector NAND gate. Connection of these signals is made via J1, an 80-pin edge connector which plugs into a standard Model II motherboard.

Signal Interfacing to the Hard Disk Controller Bus

Two 8T26 devices, U3 and U4, transfer data to the hard disk controller bus (the HDC bus). Address lines A0 through A3 and four control signals are driven to the HDC bus by U9, an LS244 inverting buffer. The INTRQ* and HDBWPCS signals are driven to the HDC bus by one-half of U28. All data lines are connected to a 220/330 terminator, R7, on the HDC bus side of U3 and U4. These signals are taken from the interface board at J2, a 50-pin edge connector. A ribbon cable connects the board to a 50-pin I/O header mounted on the Model II back panel.

Port Decoding Logic

The hard disk has 16 port mapped addresses for control and ID registers. The first four positions of an eight position DIP switch, S3, are used to determine the four most signaificant addresses to be decoded as an access to the HDC. The hard disk system for the Model II is mapped from C0 to CF Hex. This corresponds to a setting of S3 as follows:

positions 1, 2, 8 - OFF
positions 3, 4, - ON
positions 5, 6, 7 - Not Used

A 74S85 4-bit comparator, U37, checks address lines A4 through A7 for an address that matches the setting of S3 which, in this case, is C0 to CF Hex. Upon an address in this range, the signal at the A=B output, pin 6, will be the inverted output of IORQ* ANDed with M1. This signal is inverted by U21 and is the enable for one-half of U38, a 74S139 two-into-four decoder. U38 uses address lines A2 and A3 to give the outputs SELDCR* (Seclect Device Control Register), or CTCEN* (CTC Enable), or SELDIR* (Select Device ID Register).

SELDCR* is ANDed by U32 with the inverted signal DEVEN which originates from U16 pin 12 and U10 pin 13. This ANDed signal becomes DCRCS* which is fed to U9 and buffered for the HDC bus. This buffered signal is called HDBCS*.

CTCEN* is gated with the inverted signal DEVEN to form the signal CTCCS*. When this signal is active low, an access of the on-board CTC is present.

SELDIR* is gated with RD* by U24 to generate an enable for one-half of U11. The outputs of this 74LS139 correspond to read operations from ports C0, C1, C2, and C3. The outputs are labeled RDDIR0* through RDDIR3*. SELDIR* is also gated with WR* by U24. The resulting signal is tied to the enable of the other half of U11. Only two of the four outputs of this half are used. These are WRDIR0* and WRDIR1* which correspond to WRITE operations to ports C0 and C1. WRDIR1* writes to port C1 and sets the outputs of U16, a 74LS273. U16 provides the following signals to the interface board:
DEVEN, WAITEI, INTRQEI, DMAEI, SFTRESET, and SFTINT.

U44, a 74S64, is a multiple input And-Or-Invert gate. The output of this gate is inverted by one-sixth of U30 to become the signal MIIDEN. This signal enables the bus transceivers, U41 and U40, to either write data to or read data from the Model II system bus. When MIIDEN is true (or high), data is written to the system bus. When MIIDEN is false (or low), data is read from the system bus.

DID Registers and Switches

Two Device ID registers are located at ports C2 and C3. These registers can only be read and are set by means of two eight position DIP switches, S1 and S2. Each switch and register is used for identifying the two drives which they represent. S1 is read from port C2 and is used for drives four and five. S2 is read from port C3 and is used for drives six and seven. Each drive is defined by a 4-bit number, 0 to F, and each switch position stands for one bit of that number. When using four 8-inch hard disk drives, S1 and S2 are set as follows:

positions 1, 3, 5, and 7 - ON
positions 2, 4, 6, and 8 - OFF

CTC

The Z-80 CTC chip (U15) on the interface board provides the Model II with an interrupt vector for up to four interrupting conditions from the Hard Disk Controller. CTC channels 0 to 3 are port mapped from location C4 to C7 respectively. The CTC

uses the standard Z-80 system interrupt protocol where interrupt priority is determined by a peripheral device's location in the daisy chain. Because of this, there cannot be an open card slot on the Model II motherboard between the CPU board and the Interface board.

16K Dynamic RAM

The interface to the Model II system bus consists of:

a. data bus buffers
b. address buffers
c. control line buffers

The data bus buffer-drivers buffer input data from the output data to the CPU. They are chips U12 and U19. Gating logic consists of U7, U8, U26, and U2.

The address buffers buffer and invert the address signals and present them to the multiplexers (U34 and U35), to the port select logic (U36), and to the memory select logic (U1, U7, and U26).

The control line buffers provide the following signals to the memory board - SYNC* (M1), CLOCK, MEMCYC*, RD*, REFRSH*, WR*, IOCYC*, and RESET*. These signals are used by the RAS precharge extender circuit, U33 and U26. This circuit ensures that the minimum precharge time will be provided by the 4 MHz CPU to the memory chips. RD* is used by U26 to gate data onto the bus. REFRSH* is used by U26 and U8 to generate the memory refresh pulse. WR* is buffered into the memory array and to U36 for the I/O port write pulse. IOCYC* is also used by U41 for the same purpose. RESET* is used to clear port FF.

The memory array consists of eight chips. The chips are 16K by 1 bit MOS dynamic memory circuits. All the power supply voltages are bypassed on every chip to provide good noise immunity. The RAM chips are U45 through U52. C25 provides a bulk capacitance of 12 volts.

The address multiplexers U34 and U35 take the buffered address and drive the memory array through damping resistors R19 (DIP resistor array). The MUX signal, provided by the timing section, switches between the row address and the column address. The damping resistors minimize the undershoot on the signal lines which further enhances error-free operation.

The timing section consists of circuits U33, U26 (precharge extender), U13 (delay line), U20 (delay line buffer), U27 (CAS and MUX buffers), and U1 (CAS and write drivers). When MEMCYC*

is active, indicating that the CPU is going to do a read or a write, RAS is generated by the precharge circuitry and is gated with REFRSH* at U26 (i.e.; no RAS pulse is passed to the delay line during Refresh). The resulting pulse propagates down the delay line generating first MUX, which switches the address multiplexers from Row address to Column address, and second, CAS which through drivers provides the signal of the same name to the memory array.

RAS is also buffered by U8 to provide RAS to the memory array. If WR* is present on the bus, then RAS is appropriately buffered into the memory array and signals a write cycle. If WR* is not present on the bus, the data from the memory array is available for a read cycle. Note also that all RAS, CAS, and WR signals are damped into the memory array just as the address lines are and for the same reason. The damping resistors are R1, R2, and R15.

The memory select logic consists of packages U1, U7, U29, U32, and U8. The buffered address lines A14 and A15 and bits 1 to 3 of port FF are combined to produce select signals for pages 1 to 15. The memory select signal is then ORed with Refresh and the resulting signal gates RAS into the memory array through NAND gate U8.

I/O port FF controls U25 which is an 8-bit resistor and is selected by the strobe IOFFWR* which is generated by U36. U36 decodes the lower eight address lines, IOCYC, and the WR line to generate the Select. The RESET line clears port FF upon power-up or manual reset. Bits 1, 2, and 3 are used to decode the Bank Select. Bank Select is normally decoded as the lower four bits (D0 - D3). Due to the lack of bit D0, the Bank Select work in pairs. That is, if you select Bank F (D0 - D3 all ones), it will also be present on Bank E (D0 is zero, D1 - D3 are ones). Bank F is usually selected.

If you compare this to the Model II RAM board you will notice that it is very similiar. The video enable bit (D7) is not needed here. The video overlay is from F800H to FFFF. Since this board only has 16K of RAM and it is mapped from 8000 - BFFF, it would not conflict with the video.

10/ Supplement

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