APPENDIX

CONTENTS

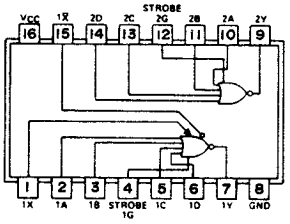
1. Table of Main ICs

Name	Part Code	Type	Location of Use	
			Q10SYM	Q10GMS
μPD416	X400104162	16K bit dynamic RAM		1B ~ 8B 2A ~ 9A
μPD449	X400004491	16K bit Static CMOS RAM	16M	
μPD765A	X400007650	Programmable Floppy Disk Controller	14H	
μPD780C-1	X400007801	8-bit Microprocessor	17J	
μPD4164	X400141640	64K bit dynamic RAM	6E ~ 9E 6F ~ 9F	1B ~ 8B 2A ~ 9A
μPD7220D	X400072200	Graphic Display Controller		10A
μPD2716	Y130801001	16K bit E-PROM	14M	
μPD2732A	*	32K bit E-PROM		2E (*)
μPD7201	X400072010	Multi-protocol Serial Controller		16B
μPD8237	X400082371	Programmable DMA Controller	19J, 21J	
μPD8253	X400082530	Programmable Interval Timer	14E, 16E	
μPD8255	X400082550	Programmable Peripheral Interface		18B
μPD8259	X400082591	Programmable Interrupt Controller	10E, 12E	
75188	X440751880	Line Driver (RS-232C level)	11B	
75189	X440751890	Line receiver (RS-232C level)	8B, 8C	
HD46818P	X400014680	Real-time Clock Plus RAM	21B	

* Y130800701 P ROM QGA-1 (U.S.A)
  Y130800501 P ROM QGE-1(Europe)

2. ICs

74LS23



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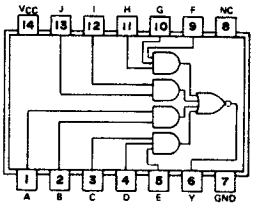

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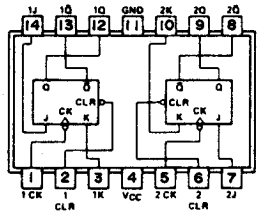
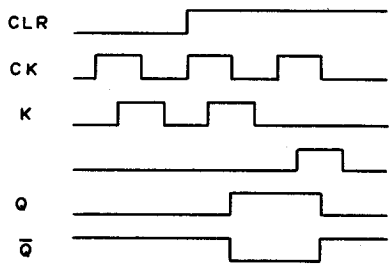
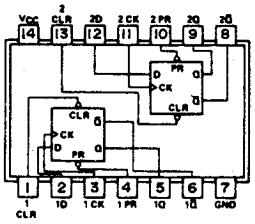
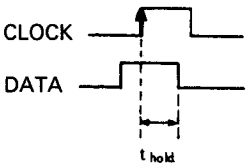




CLK	CK	K	J	Q	$\overline{Q}$
L	–	–	–	L	H
H	H/L	–	–	L/H	H/L
H	–Å	H	L	L → H H → L	H–L L–H
H	↓	L	H	L → H H → L	H → L L → H

74LS74

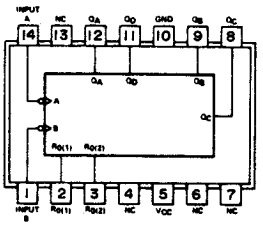


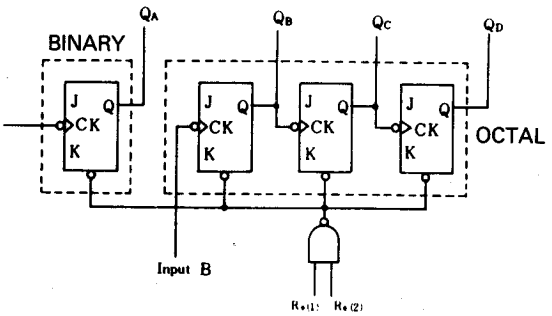


LOGIC

PR	CLR	CK	J	K	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↓	L	L	No change	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Reverse	

74LS93



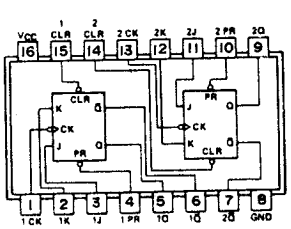


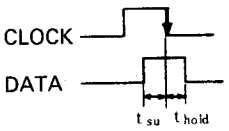
Function table

INPUT				OUTPUT		OPERATION
R_0	CK			Q_A	$Q_BQ_CQ_D$	
	A	B	PULSE			
L	CK to Q_A	CK to Q_B ~ Q_D	0	L	L L L	COUNT
			1	H	H L L	
			2	L	L H L	
			3		H H L	
			4		L L H	
			5		H L H	
			6		L H H	
			7		H H H	
			8		L L L	
⊓	×	×	—	L	L L L	CLEAR

$R_0 = R_{0(1)} \cdot R_{0(2)}$

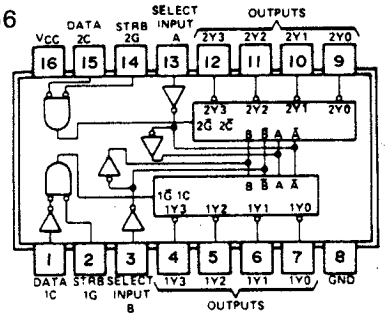
74LS112

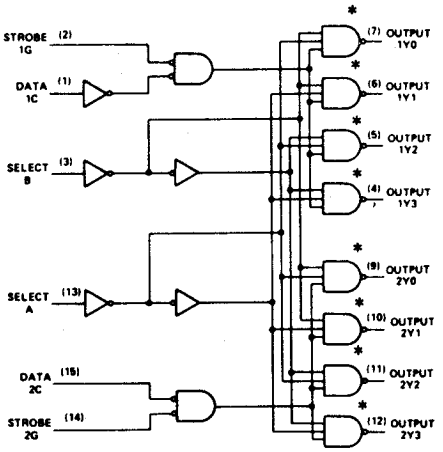




PR	CLR	CK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	No Change	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Reverse	

74LS156





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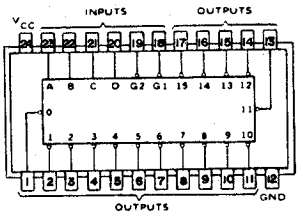
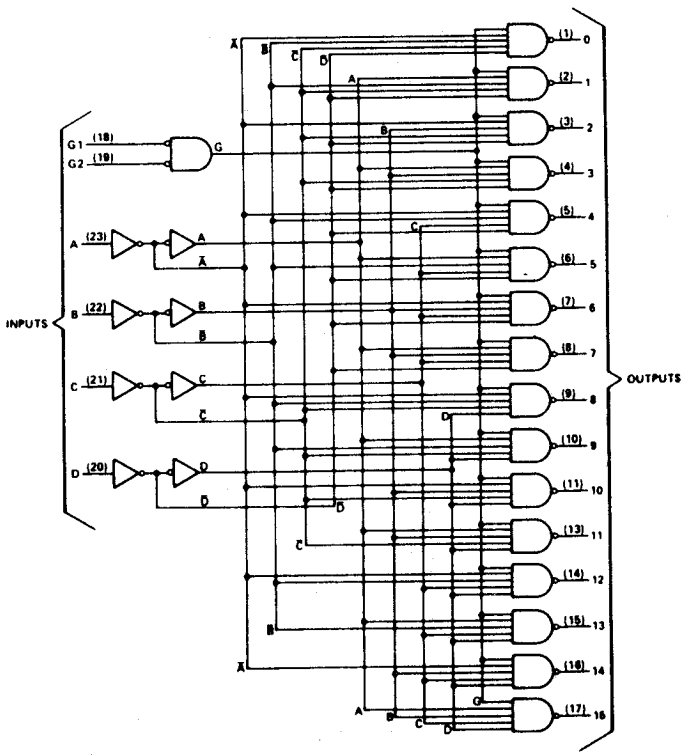


2-LINE-TO-4-LINE DECODER OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

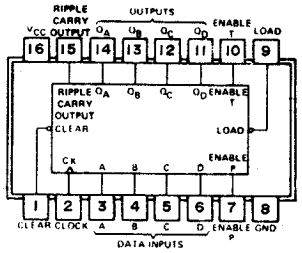
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H



3-LINE-TO-8-LINE DECODER OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

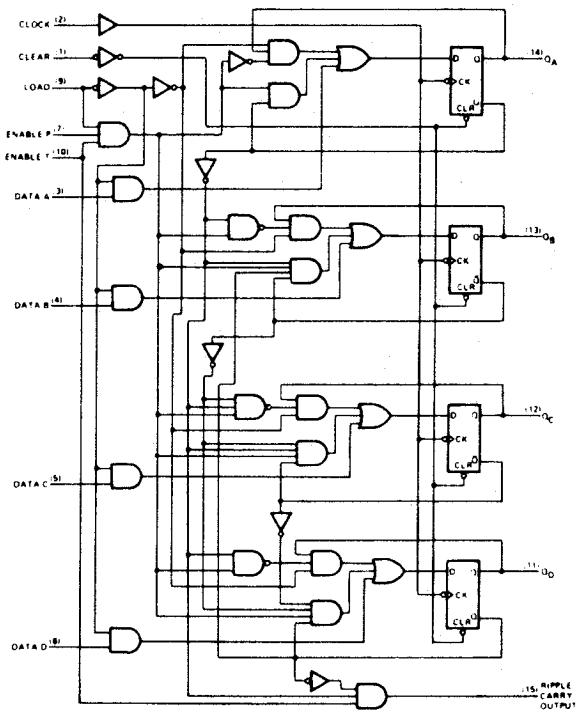
74LS161



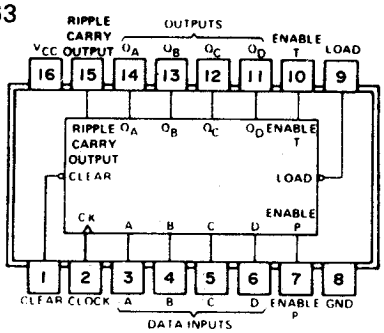
FUNCTION TABLE

INPUT					OUTPUT		OPERAITON
Clear	Load	CK	Enable P	Enable T	$Q_A Q_B Q_C Q_D$	Ripple Carry	
H	H	⌐‾	H	H		—	COUNT
H	L	⌐‾	X	X	$D_A D_B D_C D_D$	—	DATA SET
‾L	X	X	X	X	L L L L		CLEAR
H	X	X	X	H	H H H H (H L L H)	⌐‾H	—

( ) is at the time of 160



74LS163

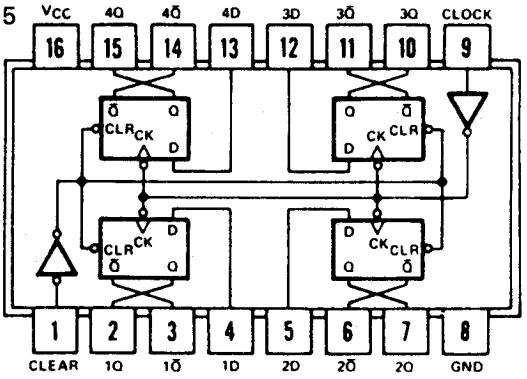


FUNCTION TABLE

INPUT					OUTPUT		OPERATION
Clear	Load	CK	Enable P	Enable T	$Q_A Q_B Q_C Q_D$	Ripple Carry	
H	H	⌐‾	H	H	——	–	COUNT
H	L	⌐‾	X	X	$D_A D_B D_C D_D$	–	DATA SET
L	X	⌐‾	X	X	L L L L	–	CLEAR
X	X	X	X	H	H H H H (H L L H)	⌐‾H	——

( ) is at the time of 162

74LS175



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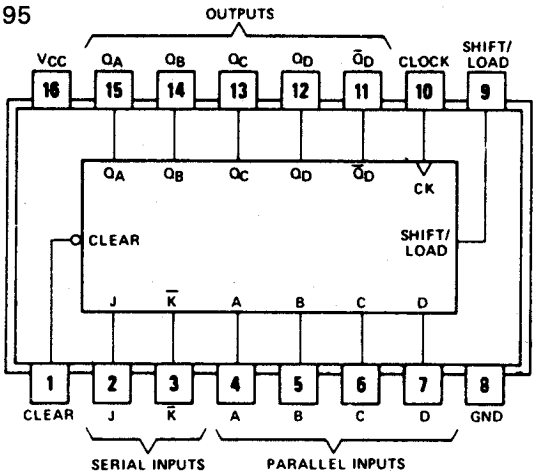
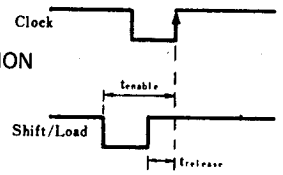
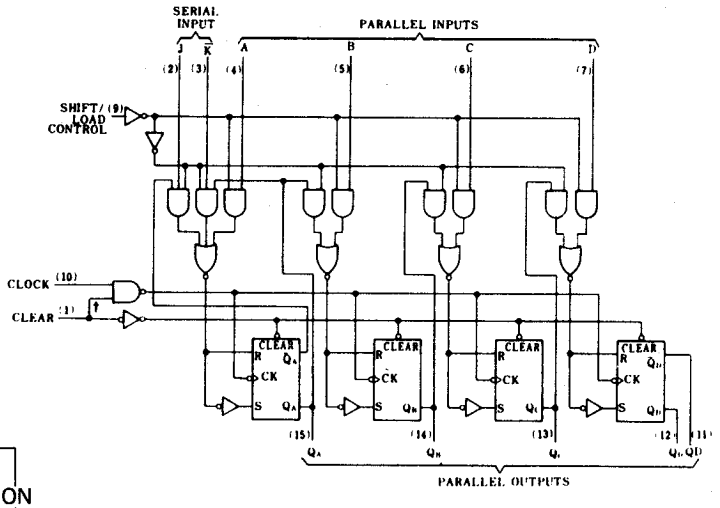


INPUT			OPERATION
Clear	Shift/Load	CK	
H	H	⌐‾	SHIFT/R
H	L	⌐‾	LOAD
‾L	X	X	CLEAR





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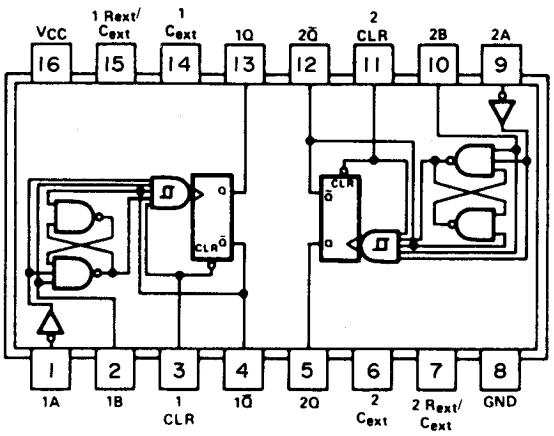

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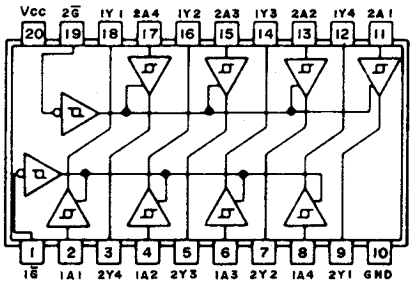

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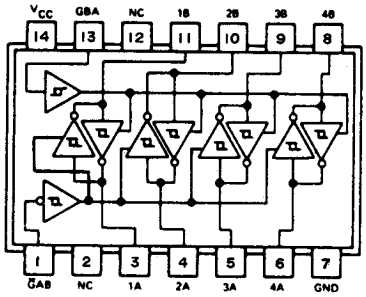
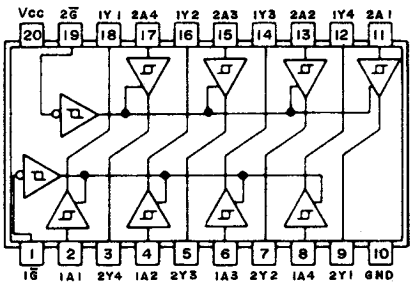


GAB	GBA	OPEATION
H	H	A ← B
L	H	Not allowed
H	L	A OFF B
L	L	B ← A

74LS244



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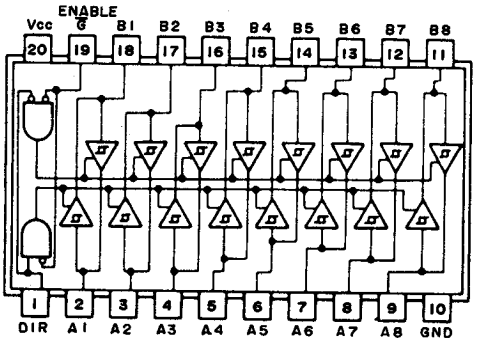

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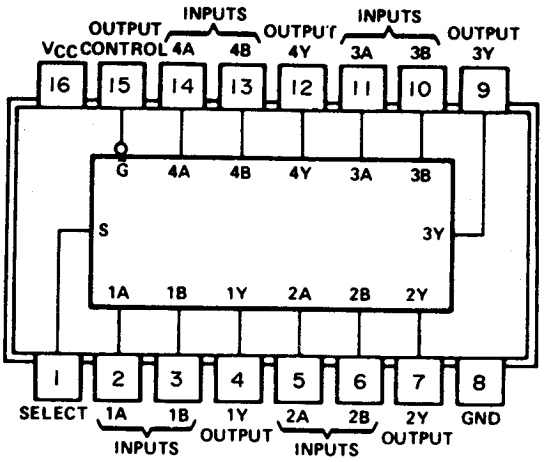
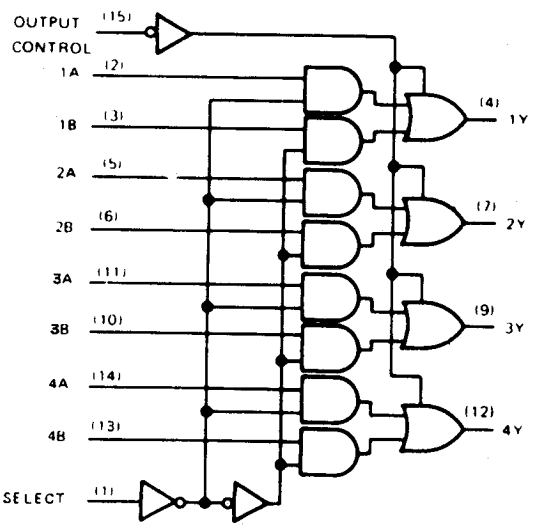


FUNCTION TABLE

INPUT		OUTPUT
Select	Output Control	Y
X	H	Z
L	L	A
H	L	B



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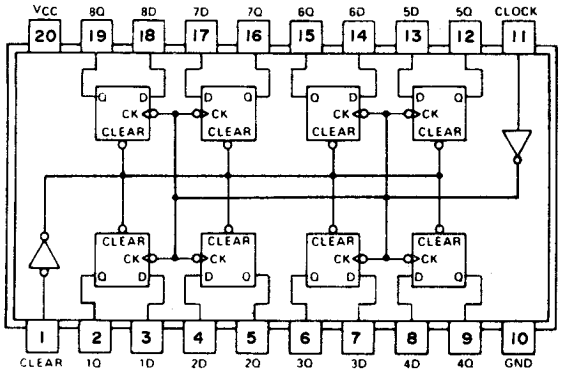

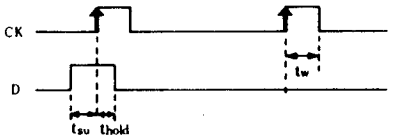

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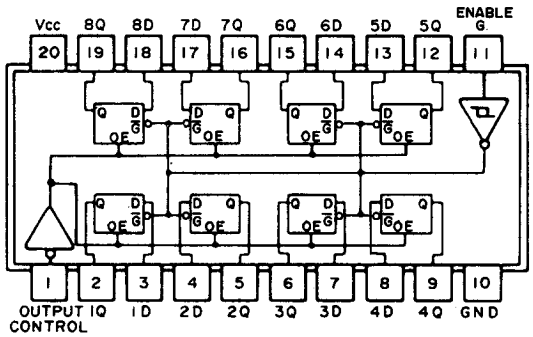

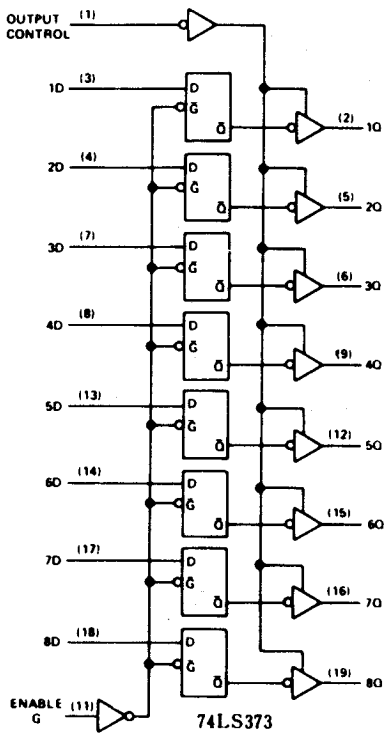

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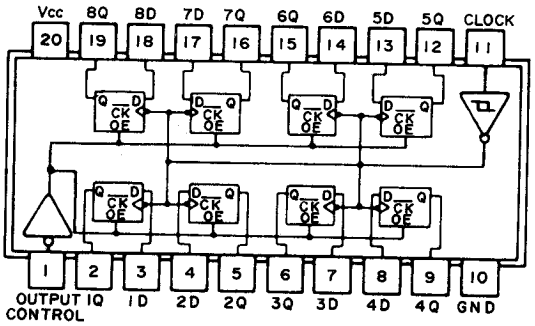

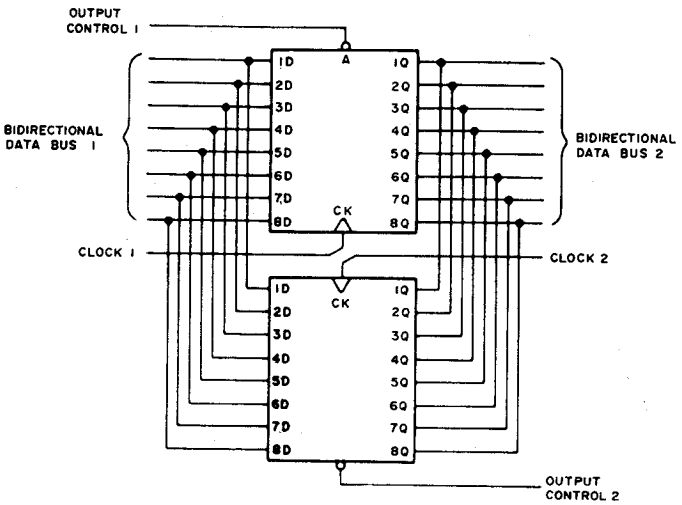

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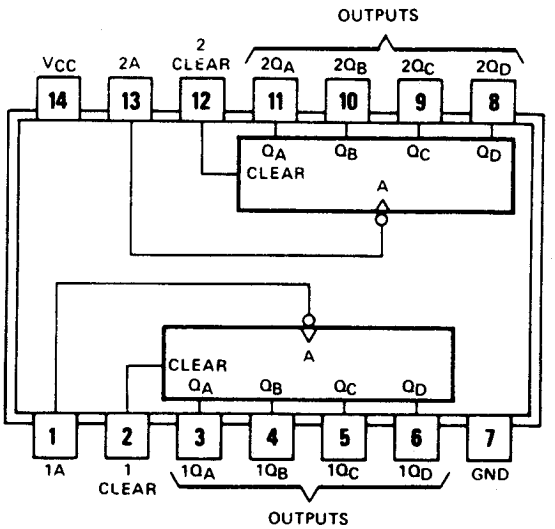
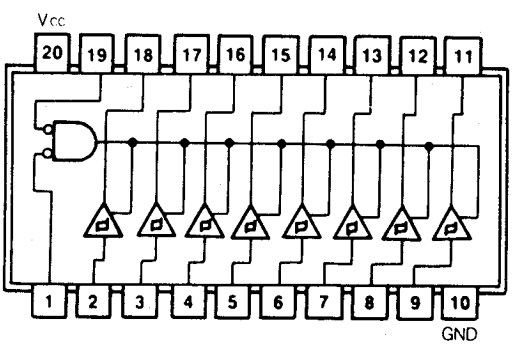
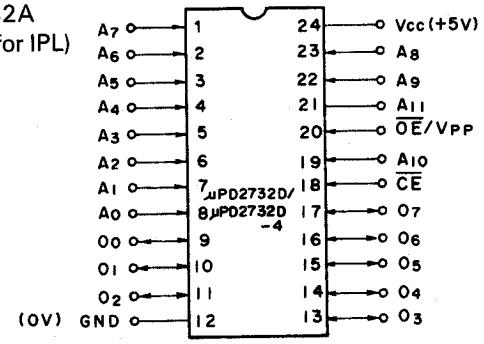


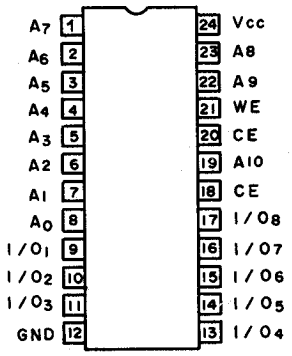
74LS541



μPD2732A
(PROM for IPL)



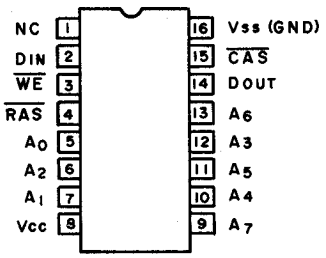
μPD449
(C MOS RAM)



FUNCTION TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	CHIP	OUTPUT MODE	POWER CURRENT
×	H	×	Nonselected	High Impedance	I_{CCS}
H	L	×			
L	L	H	READ	D_{OUT}	I_{CCA}
L	L	L	WRITE	D_{IN}	

μPD4164
(Dynamic RAM)



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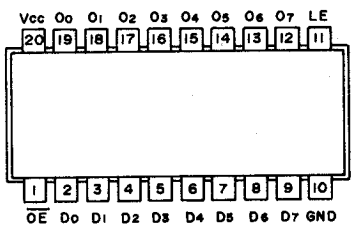
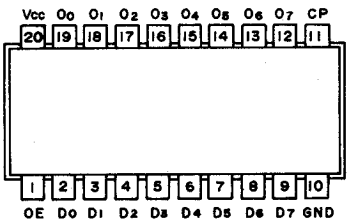


74LS574



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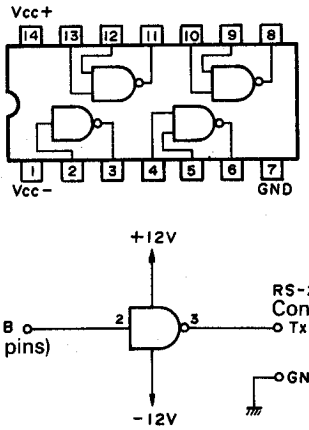
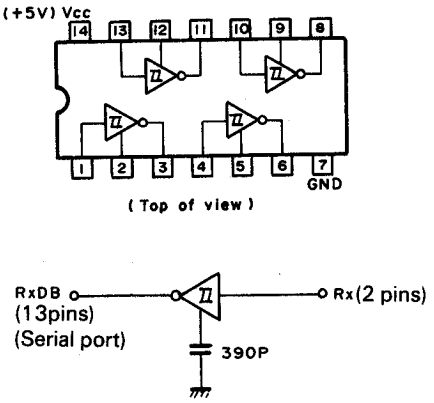
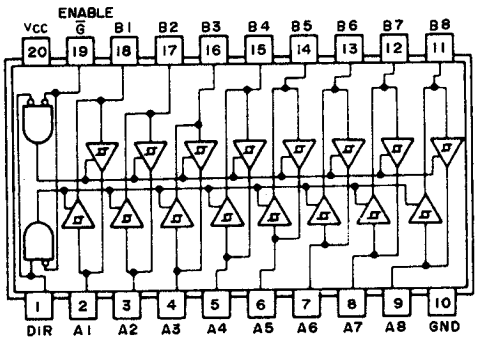


75189 (RS-232C for Interface)



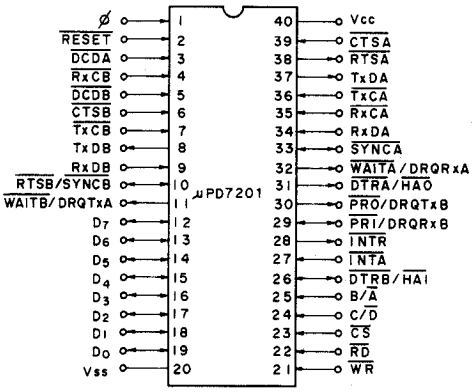
TYPES SN74LS245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



Function table

ENABLE G	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level,
L = low level,
X = irrelevant

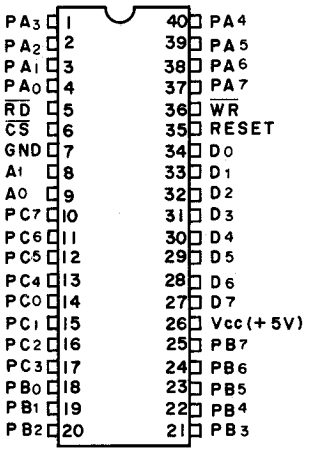


Pin (signal) name	I/O	Function
φ	I	3.9936 Hz clock (same as with the main CPU) is supplied.
C/D	I	H: command/status L: transmitted/received data
B/A	I	H: channel B L: channel A

B/A	C/D	WR	RD	CS	Function
0	0	0	1	0	Writes transmitted data
1					
0	0	1	0	0	Reads received data
1					
0	1	0	1	0	Writes in command/parameter register (WR 0 – 7)
1					
0	1	1	0	0	Reads from status/vector register (RR 0 – 2)
1					

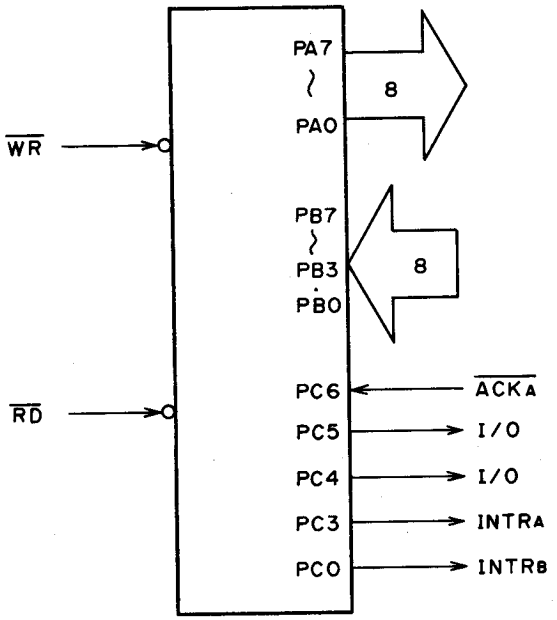
INTR	O	Interrupt request signal
PRI (priority output)	I	Kept at GND level in the QX-10 to indicate that no other devices of higher priority have service to interrupt offered.
DTR (data terminal ready)	I/O	Indicates to the communicating party that communication channel is ready.
CTS (clear to send)	I	Allows transmitter to send data (controls data transmission).
DCD (data carrier detect)	I	Allows receiver to receive data (control data reception).
RTS (request to send)	O	Indicates transmitter is requesting to transmit data.
RXD	I	Received data
TXD	O	Transmitted data
RXC (receive clock)	I	Received data are sampled at the rise of this signal.
TXC (transmit clock)	I	Transmitted data are output at the decay of this signal.
INTA	I	Acknowledge interrupt request.

Programmable peripheral interface



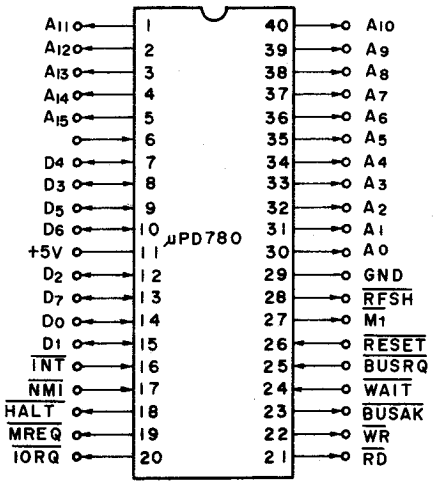
The μPD8255A (18B) is used in Mode 1 for the printer interface.

«Mode 1»



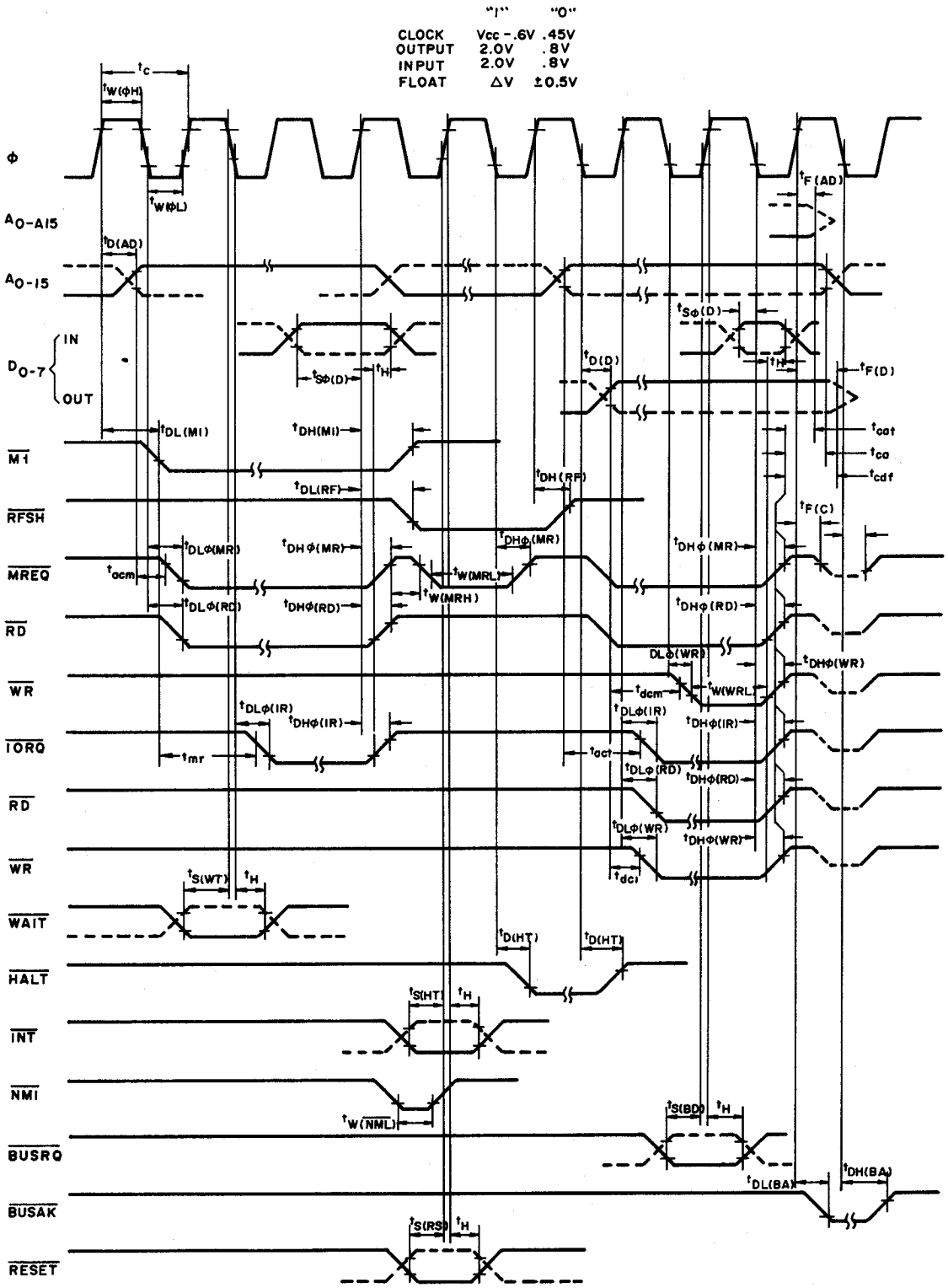
- $\overline{ACKA}$ (Acknowledge Input):
  Acknowledge signal to the reception of data from the CPU through port A
- INTR (Interrupt Request):
  Interrupt request signal (high) to the CPU

μPD780C/D-1 8-Bit microprocessor



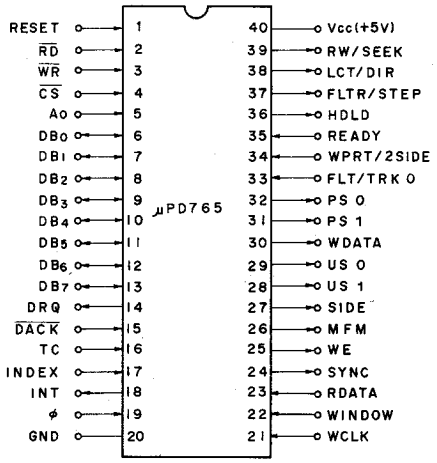
Pin (signal) name	I/O	Function
A0 – A15	O	Address bus
D0 – D7	I/O	Data bus
$\overline{M1}$	O	Indicates that the CPU is currently in operation code fetch cycle. with 2-byte instructions, $\overline{M1}$ is generated at the fetch time of each byte. In acknowledge-to-interrupt request cycle, $\overline{M1}$ is output along with $\overline{IORQ}$.
$\overline{MREQ}$	O	Indicates that address is entered on the address bus during memory read or write. During memory refresh time, this is also output for synchronization.
$\overline{IORQ}$	O	Indicates that a right I/O address is output to the address bus. If output together with $\overline{M1}$, this indicates acknowledge-to-interrupt request cycle.
$\overline{RD}$	O	Indicates the input status of the data bus.
$\overline{WR}$	O	Indicates the output status of the data bus.
$\overline{RFSH}$	O	Indicates that a refresh address is placed in the address bus lines of the least significant seven bits, so that dynamic RAM is refreshed, triggered by $\overline{MREQ}$ generated during this time.
$\overline{HALT}$	O	Indicates halt state.
$\overline{WAIT}$	I	The CPU remains in the wait state when $\overline{WAIT}$ is active, so that a low-speed memory or I/O device may be directly connected to the CPU.
$\overline{INT}$	I	Interrupt request
$\overline{NMI}$	I	Non-maskable interrupt request which is stable-high in the QX-10
$\overline{RESET}$	I	Initializes the CPU when: (1) Power on, Power off (2) Depression of reset switch (3) Resetting by an external I/O device
$\overline{BUSRQ}$	I	Puts the data bus, address bus, and 3-state output control line to high-impedance state, so that another device may use the buses. After receiving $\overline{BUSRQ}$, the CPU puts the buses to high impedance as soon as execution of the current machine cycle is completed.
$\overline{BUSAK}$	O	Indicates that the CPU has met the demand by $\overline{BUSRQ}$ and the buses are available to other devices.
ϕ	I	Single-phase clock. 3.9936 MHz is supplied in the QX-10.

▶ μPD780 Timing diagram



AC Characteristics (Ta = 0 ~ +70°C, Vcc = +5V ±5%)

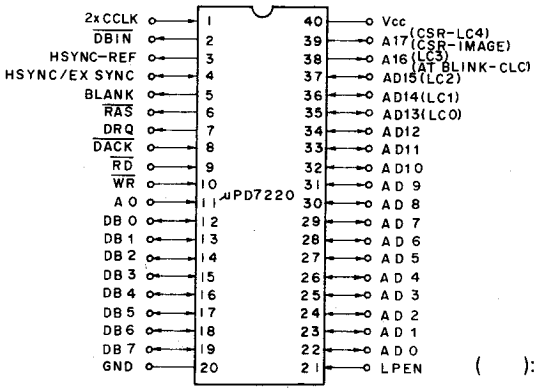
			Z80A CPU			
Signal	**Symbol**	**Parameter**	**Min**	**Max**	**Unit**	**Test Condition**
ϕ	t_c	Clock Period	25		μsec	
	$t_{w(\phi H)}$	Clock Pulse Width, Clock High	110		nsec	
	$t_{w(\phi L)}$	Clock Pulse Width, Clock Low	110	2,000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		110	nsec	C_L = 50 pF
	$t_{F(AD)}$	Delay to Float		90	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)			nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)			nsec	
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$			nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float			nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		150	nsec	C_L = 50 pF
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	35		nsec	
	$t_{S\bar{\phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	50		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)			nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)			nsec	
	t_{cdf}	Data Stable From $\overline{WR}$				
	t_H	Any Hold Time for Setup Time		0	nsec	
$\overline{MREQ}$	$t_{DL\bar{\phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		85	nsec	C_L = 50 pF
	$t_{DH\phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{DH\bar{\phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low			nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High			nsec	
$\overline{IORQ}$	$t_{DL\phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		75	nsec	C_L = 50 pF
	$t_{DL\bar{\phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		85	nsec	
	$t_{DH\phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		85	nsec	
	$t_{DH\bar{\phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		85	nsec	
$\overline{RD}$	$t_{DL\phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		85	nsec	C_L = 50 pF
	$t_{DL\bar{\phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		95	nsec	
	$t_{DH\phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		85	nsec	
	$t_{DH\bar{\phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		85	nsec	
$\overline{WR}$	$t_{DL\phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		65	nsec	C_L = 50 pF
	$t_{DL\bar{\phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		80	nsec	
	$t_{DH\phi(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock $\overline{WR}$ High		80	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low				
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		100	nsec	C_L = 50 pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		100	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		130	nsec	C_L = 50 pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		120	nsec	
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ SetupTime to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of clock		300	nsec	C_L = 50 pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NM1}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ SetupTime to Rising Edge of Clock	50		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock $\overline{BUSAK}$ Low		100	nsec	C_L = 50 pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock $\overline{BUSAK}$ High		100	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time To Rising Edge of Clock	60		nsec	
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80	nsec	
	t_{mr}	M1 Stable Prior to IORQ (Interrupt Ack.)			nsec	



Pin (signal) name	I/O	Function
ϕ	I	Single-phase clock. 4 MHz is supplied.
RESET	I	Makes FDC idle, drive interface outputs except PS0, PS1 and WDATA (planned), L level; outputs INT and DRQ L level; and DB to input state.
INT	O	Indicates that FDC is requesting service. This is output for every byte during non-DMA mode and, during DMA mode, on completion of command execution.
A0	I	0: Status register selected 1: Data register selected
DRQ	O	Data transfer request signal between FDC and memory by DMA
$\overline{\text{DACK}}$	I	Indicates that DMA cycle may be entered.
SYNC	O	Designates operating mode of VFO. "1" enables read and "0" inhibits it.
RW/SEEK	O	Distinguishes between read/write (RW) and seek (SEEK) drive interface signals. "0" designates RW and "1" SEEK.
HDLD	O	Loads the drive's read/write head.
SIDE	O	Selects head 0 or 1 of a double-sided disk drive. "0" selects head 0 and "1" head 1.
LCT/DIR	O	When RW/SEEK designates RW, this works as LCT to indicate that the drive's read/write head selects a cylinder beyond # 43. When RW/SEEK designates SEEK, this works as DIR to indicate seek direction (0: outward, 1: inward).
FLTR/STEP	O	When RW/SEEK designates RW, this works as FLTR to reset the fault state of the drive. When RW/SEEK designates SEEK, this works as STEP which is the seek step signal.
READY	I	Indicates drive is ready.
WPRT/2 SIDE	I	When RW/SEEK designates RW, this works as WPRT to indicate that the drive or disk is write-protected. When RW/SEEK designates SEEK, this works as 2 SIDE which indicates that a doublesided disk is mounted.
INDEX	I	Indicates the physical start of tracks on the disk.
FLT/TRK0	I	When RW/SEEK designates RW, this works as FLT to indicate that the drive is in fault state. When RW/SEEK designates SEEK, this works as TRK0 to indicate that the read/write head is positioned at cylinder 0.
TC	I	Indicates the end of read or write from the main system.
WDATA	O	Data to be written through the drive. This consists of clock and data bits.
WE	O	Enables the drive to write data.
WCLK	I	Write clock supplied to the drive. 500 kHz is used in FM mode and 1 MHz in MFM mode.
PS0 – PS1	O	Indicates to advance or delay the timing of writing WDATA In MFM mode as given below to provide read-time margin.
RDATA	I	Data read through the drive. This consists of clock and data bits.
WINDOW	I	Generated in VFO and used to sample RDATA. FDC synchronizes the data bits of RDATA with WINDOW in phase.

PS0	PS1	FM	MFM
0	0	Unchanged	Unchanged
0	1	–	LATE 225 ~ 250 ms
1	0	–	EARLY 225 ~ 250 ms
1	1	–	–

Graphic display Controller

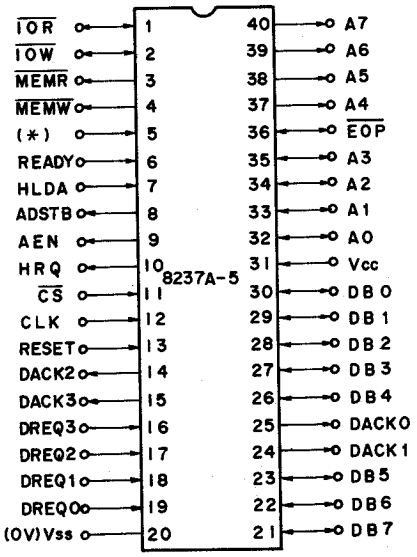


( ): Character display mode

Pin (signal) name	I/O	Function
AD0 – AD12	I/O	Bidirectional address bus lines
AD13 (LC0) AD14 (LC1) AD15 (LC2)	I/O	During graphic and character-graphic mixed mode: address bus lines During character mode: line count
DB0 – DB7	I/O	Bidirectional data bus
$\overline{RAS}$	O	Memory control signal output from GDC to VRAM. $\overline{CAS}$ is generated from this. Also used as the timing signal to latch address.
$\overline{AT\ BLINK}$-$\overline{CLC}$	O	During blanking time (BLANK signal output): Clears the line counter. During tracing time (video signal ouput): Outputs attribute-blinking-timing signals
CSR-IMAGE	O	During blanking time (BLANK signal output): Outputs cursor mark During tracing time (video signal output): Outputs character/graphic area switching timing signal
A0	I	Connected to an address line of the CPU and used to designate data type
$\overline{DACK}$	I	Supplied from the DMA controller to enable the GDC to distinguish between read and write performed by DMA.
LPEN	I	Light pen strobe signal. H level signal enters when the light pen has detected light input.
DRQ	O	DMA request
$\overline{DBIN}$	O	Memory control signal output from the GDC to VRAM (timing signal used to put VRAM output to the data bus).
V.SYNC	O	Vertical sync signal
H. SYNC	O	Horizontal sync signal
BLANK	O	Blanking signal output during: (1) Horizontal retrace time (2) Vertical retrace time (3) Time between execution of SYNC and START commands (4) Draw execution time
2XCCLK	I	Supplied from an external dot clock generator. The clock frequency is determined by the relationship between the horizontal resolution in dots and the horizontal scanning time (4.1665 MHz in the QX-10).

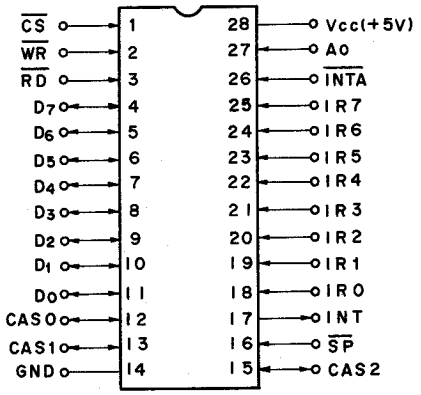
A0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	READ STATUS FLAG
1	0	1	READ DATA
0	1	0	WRITE PARAMETER
1	1	0	WRITE COMMAND

Programmable DMA Controller



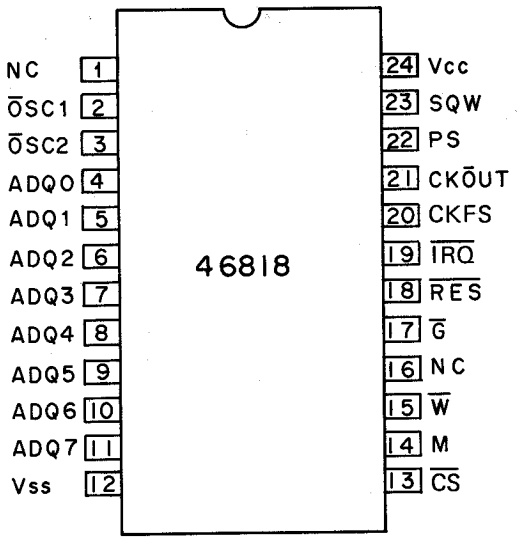
*: NC (unuse)

Pin (signal) name	I/O	Function
READY (ready)	I	Used to expand memory read/writer pulse output from 8237 to adapt to a low-speed memory or I/O device.
HLA (hold acknowledge)	I	Active-high signal indicating the CPU has left control of the system bus.
DREQ0 – DREQ3 (DMA request)	I	DMA request signals which peripheral devices use independently to receive DMA service through asynchronous channels. In a fixed-priority system, DREQ0 has the highest priority and DREQ3 the lowest. DREQ must be maintained until DMA becomes active.
DACK0 – DACK3 (DMA acknowledge)	O	Acknowledge signals to DMA request which inform specific peripheral devices of acceptance of DMA request.
ADEN (address enable)	O	Enables the latch, holding the most significant eight bits of address, to output them to the address bus.
ADSTB (address strobe)	O	Strobes an external latch for the most significant byte of address.
HRQ (hold request)	O	Hold request signal to the CPU. This requests control of the system bus.
$\overline{EOP}$ (end of process)	I/O	Information on completion of DMA service is available at this terminal. Signal $\overline{EOP}$ is generated internally or externally. This terminal must be connected to H level through a pull-up resistor to prevent entry of wrong signals.
DB0 – DB7	I/O	During DMA cycle, the most significant eight bits of address are output to the data bus and placed in an external latch, strobed by ADSTB.
A0 – A3 (address)	I/O	During idle cycle: Entered to address the control register loaded or read. During active cycle: Provides the least significant four bits of output address.
A4 – 7	O	Provides the most significant four bits of address, permitted only during DMA service.

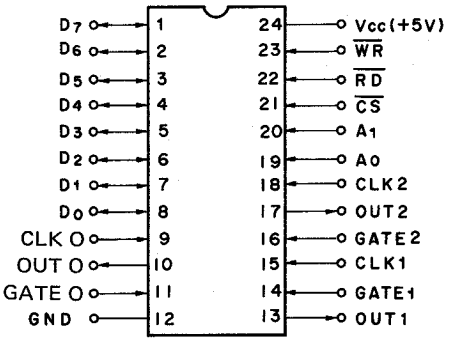


Pin (signal) name	I/O	Function
$\overline{CS}$	I	Signals $\overline{RD}$ and $\overline{WR}$ become valid when this is L level. Note that $\overline{INTA}$ is not affected by this signal.
D0 – D7	I/O	Through these terminals, 8-bit data of a status register or interrupt vector is output in read mode and, in write mode, a command is written in.
$\overline{SP}$	I	Determines whether the 8259 is to operate as a master ($\overline{SP}$ = 1) or a slave controller ($\overline{SP}$ = 0).
A0	I	Along with signals $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$, this is used to write commands or read contents of a register.
CAS0 – CAS2	I/O	Output terminals when the 8259 is used as a master ($\overline{SP}$ = 1) and input terminals when it is used as a slave ($\overline{SP}$ = 0). To control a system of more than one 8259, the CAS lines form the bus of the 8259's.
INT	O	When the 8259 requests interrupt, INT rises to H level and delivers an interrupt request to the CPU or master 8259.
$\overline{INTA}$	I	Permits output of interrupt vector data of the 8259. This operation is performed in the sequence of $\overline{INTA}$ generated by the CPU.
IR0 – IR7	I	IR0 has the highest interrupt priority assigned. These terminals are of asynchronous input.

HD146818P Real-time clock plus RAM RTC



Pin (signal) name	I/O	Function
Vcc	–	Supply power
Vss	–	GND
OSC1	I	External clock signal (32.768 kHz)
OSC2	–	External clock signal (32.768 kHz). Open during input.
AD0 – AD7	I/O	Bidirectional bus lines through which the CPU transfers address to access the RTC then data. Address is transferred during the first half of the cycle and data transferred during the second half. The address signal level must be fixed at the decay of signal M. The data bus driver, 3-state output buffer, is at high impedance except when the RTC outputs data.
M	I	Strobe signal used to read address from the address bus. Address is read into the RTC at the decay of this signal.
$\overline{G}$	I	System clock input terminal. The CPU reads data from the RTC while $\overline{G}$ is H level or writes data at the decay of $\overline{G}$.
$\overline{W}$	I	Input terminal of signal R/W coming from the CPU. The CPU sets $\overline{W}$ at H level to read from the RTC and at L level to write data into the RTC.
$\overline{CS}$	I	Chip select
$\overline{IRQ}$	O	Active-low signal requesting interrupt to the CPU.
$\overline{RES}$	I	RTC reset signal. Operation proceeds to subsequent steps when $\overline{RES}$ turns to L level. $\overline{RES}$ does not affect clock, calendar, or RAM.
PS	I	The valid RAM and Times (VRT) bit is cleared to "0" when PS turns to L level. Then the CPU should initialize the RTC, then set the VTR bit to "1" to prepare for power failure.



Pin (signal) name	I/O	Function
D7 – D0	I/O	Connected to the QX-10's system data bus. Through these terminals, data are input or output according to a CPU instruction IN or OUT. The μPD8253-5 deals with three types of data "control word" and "count" input according to signal $\overline{WR}$, and "count data" output according to $\overline{RD}$.
$\overline{WR}$	I	Signal $\overline{IOWR}$ enters from the CPU and it is used to write in "control word" and "count". The control word and count are read from the data bus and written into the count register at the rise of $\overline{WR}$.
$\overline{RD}$	I	Signal $\overline{IORD}$ enters from the CPU and is used to read the contents of a counter of the μPD8253-5. When the CPU sets $\overline{RD}$ to "0", the count data which is being counted or latched in the storage register is output to the data bus.
$\overline{CS}$	I	The data bus (D7 – D0) is active when $\overline{CS}$ = 0 and at high impedance when $\overline{CS}$ = 1. $\overline{CS}$ is put to 0 when control word and count are to be written in or count data are to be read out. In the QX-10, I/O addresses 00-04H are assigned to IC 14E and 05H – 07H to IC 16E.
A1, A0	I	When writing count in the count register or reading count data, # 0, # 1, or # 2 is selected with A1A0 put to 00, 01, or 10. A1A0 is set to "11" when writing in control word. A1 – 0 are connected to the system address bus.
CLK N (N: 0 – 2)	I	Clock signal determining count rate of counter # N. After "count " is designated, the counter increments at the decay of CLK.
OUT N (N: 0 – 2)	O	Output of counter # N. This may be rate output, square wave output, or one-shot output depending on selected mode. This may also be used as an interrupt request signal.
GATE N (N: 0 – 2)	I	GATE N gates, triggers, or resets counter # N depending on selected mode. Counter # N operates according to the gate inputs as shown in Table.

Operation is as follows depending on the combination of the control signals.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Loads to counter # 0
0	1	0	0	1	Loads to counter # 1
0	1	0	1	0	Loads to counter # 2
0	1	0	1	1	Control word
0	0	1	0	0	Reads from counter # 0
0	0	1	0	1	Reads from counter # 1
0	0	1	1	0	Reads from counter # 2
0	0	1	1	1	No operation (high impedance)
1	X	X	X	X	Disabled (high impedance)
0	1	1	X	X	No operation (high impedance)