CHAPTER 5
G10GMS BOARD

CONTENTS

5.1 General

The CRT controller mounted on the Q10 GMS board includes the graphic display controller (μPD7220) which converts data coming from the main control circuit into a video signal and supplies it, together with horizontal and vertical sync signals, to the CRT drive unit (CDU).

The graphic display controller (GDC) controls a raster scan-type CRT according to control commands and associated parameters which the CPU (μPD780) supplies, in character mode (80 characters by 25 lines) or in graphic mode (640 by 400 dots). It permits dynamical change over character display/draw mode and graphic display/draw mode.

One of the most distinct features of the QX-10 is that the CRT controller is assigned as an I/O device for the CPU. Ordinarily, the CRT controller is, for the CPU, just like the memory which the CPU can access directly by referring to an address and, in such a system, load instructions are used to move data into V-RAM to display images.

In our system, the CPU regards the GDC (μPD7220) as an I/O device and the bus lines which the GDC controls are separate from the system bus the CPU controls. This permits the GDC and CPU to operate in parallel and, naturally, the GDC's arithmetic capabilities are used to realize high-speed graphic functions.

5.2 Block Diagram

Fig. 5-1 is a block diagram of the CRT controller. The GDC is the interface between the main circuit and the CRT controller.

Receiving data from the main circuit, the GDC generates data, which are to be written into V-RAM, along with sync and control signals.

Each word of the data written in V-RAM consist of 16 bits. In graphic mode, all the 16 bits make up a graphic data. In character mode, the most significant eight bits make up an attribute data while the least significant eight bits make up a character code.

The data held in V-RAM are converted to serial data with a shift register and sent to the CRT as a video signal combined with sync signals.

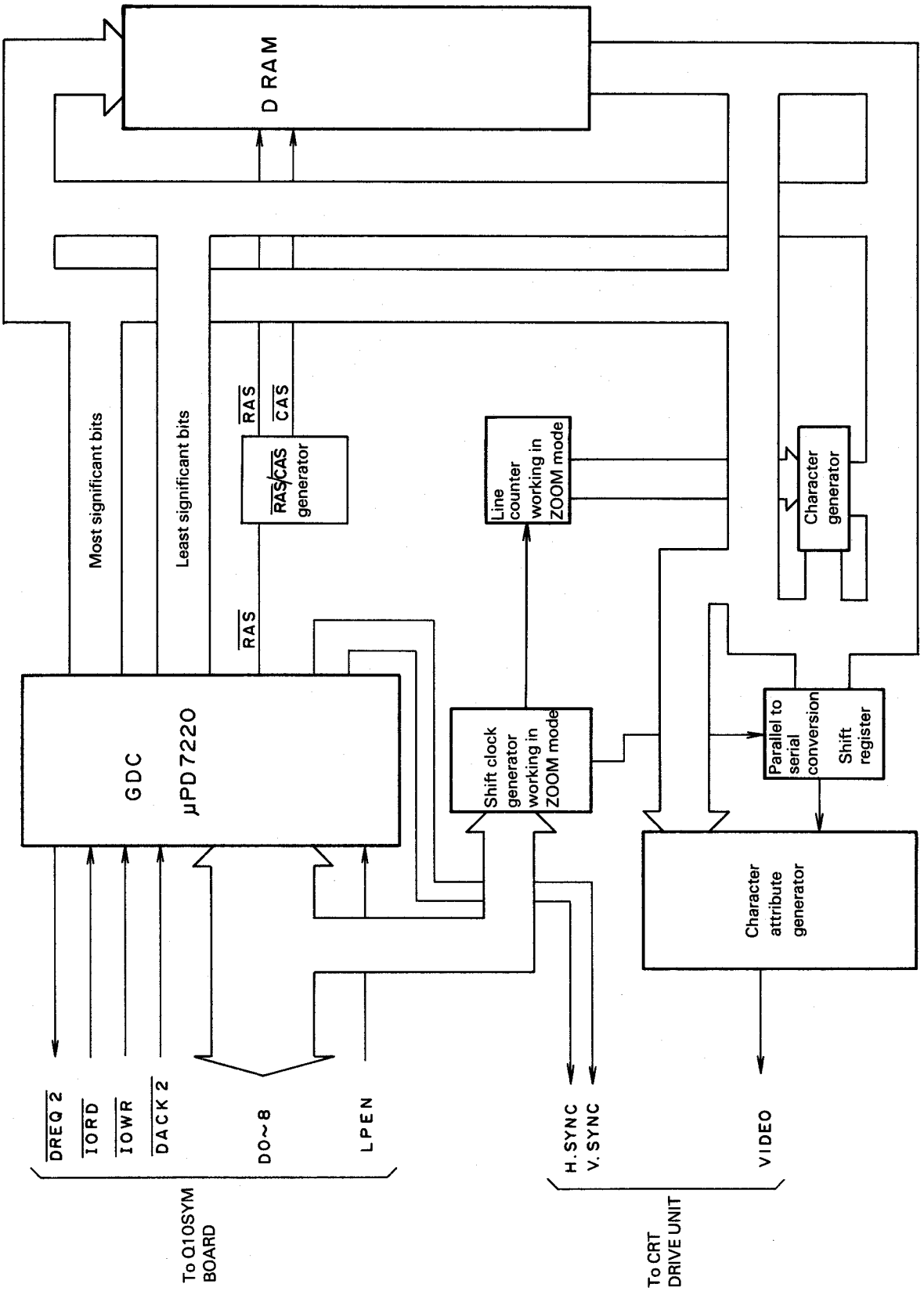


Fig. 5-1 Block Diagram of Q10 GMS Circuit

5.3 Graphic Display Controller (μPD7220)

5.3.1 General

The graphic display controller (μPD7220) is a peripheral device controller LSI which operates to display characters and graphic patterns on a raster scan-type CRT.

Its capabilities include not only generation of sync signals and control for displaying characters but also control of high-speed graphics and large-capacity video memory. So, its applications range from simple control of character displays to sophisticated graphics. Further, one of the applications which have nothing to do with display cotrol is control of large-capacity memory.

5.3.2 Features

(1) High-speed graphics capabilities

It permits drawing of line segments, quadrilaterals, arcs, circles, and other graphic figures at a speed of 960 nsec/word. During every word time of 960 nsec, it computes the address of the dot which is to be drawn next. That is, the dot time includes both the time needed to compute dot address and that to draw a dot. Figures, therefore, may be drawn continuously at high speed.

(2) Large-capacity V-RAM

V-RAM is the memory from which μPD7220 directly reads data from and into which writes data. Therefore, V-RAM may be provided separately from the main memory (RAM banks # 0 – # 3 on the Q10SYM board) which the CPU accesses directly. Actually our system incorporates a big-capacity V-RAM (ASCII type: 32 KB, HASCI type: 128 KB) by using sixteen 16-K bit or 64-K bit RAM chips.

(3) Scroll capabilities

The scroll commands of μPD7220 permit designation of SAD (display start address) and SL (number of lines of display area used) of V-RAM. This means the μPD7220's high speed scroll capabilities cover scrolling inside a page (INTRA PAGE) and over pages (INTER PAGE), paying, horizontal and vertical scrollings.

(4) Enlarging display/draw capabilities

The μPD7220 permits display of characters and drawing of graphic figures enlarged as many times as an integer multiple of 1 to 16.

5.3.3 Commands of the μPD7220

Twenty-one commands are prepared for the μPD7220 as listed below. (Table 5-1)

Operation Control

Command	Function	(MSB) Command code (LSB)
RESET	Initializes	0 0 0 0 0 0 0 0
SYNC	Defines operating mode and sync signal waveforms	0 0 0 0 1 1 1 DE
MASTER/SLAVE	Selects master or slave operation	0 1 1 0 1 1 1 M

Display Control

Command	Function	(MSB) Command code (LSB)
START	Starts displaying	0 1 1 0 1 0 1 1
		0 0 0 0 1 1 0 1
STOP	Stops displaying	0 0 0 0 1 1 0 0
ZOOM	Designates the times count of enlargement	0 1 0 0 0 1 1 0
SCROLL	Sets display start address and area	0 1 1 1 ——RA——
CSRFORM	Defines cursa of characters	0 1 0 0 1 0 1 1
PITCH	Defines horizontal length of V-RAM in words	0 1 0 0 0 1 1 1
LPEN	Reads light pen address	1 1 0 0 0 0 0 0

Graphics Control

Command	Function	(MSB) Command code (LSB)
VECTW	Sets parameters for drawing figures	0 1 0 0 0 1 1 0
VECTE	Designates line, quadrilateral, or circle to draw	0 1 1 0 1 1 0 0
TEXTW	Sets graphics text code	0 1 1 1 1 ——RA——
TEXTE	Designates graphic texts text to display	0 1 1 0 1 0 0 0
CSRW	Sets address to draw	0 1 0 0 1 0 0 1
CSRR	Reads address to draw	1 1 1 0 0 0 0 0
MASK	Sets mask register	0 1 0 0 1 0 1 0

V-RAM Control

Command	Function	(MSB) Command code (LSB)			
WRITE	Prepares to write parameters in V-RAM	0 0 1	WLH	0	MOD
READ	Reads data from V-RAM	1 0 1	WLH	0	MOD
DMAW	Starts DMA data transfer to V-RAM	0 0 1	WLH	1	MOD
DMAR	Starts DMA data transfer from V-RAM	1 0 1	WLH	1	MOD

Table 5.1

5.3.4 Timing diagrams

The GDC (μPD7220) operates through three cycles as follows.

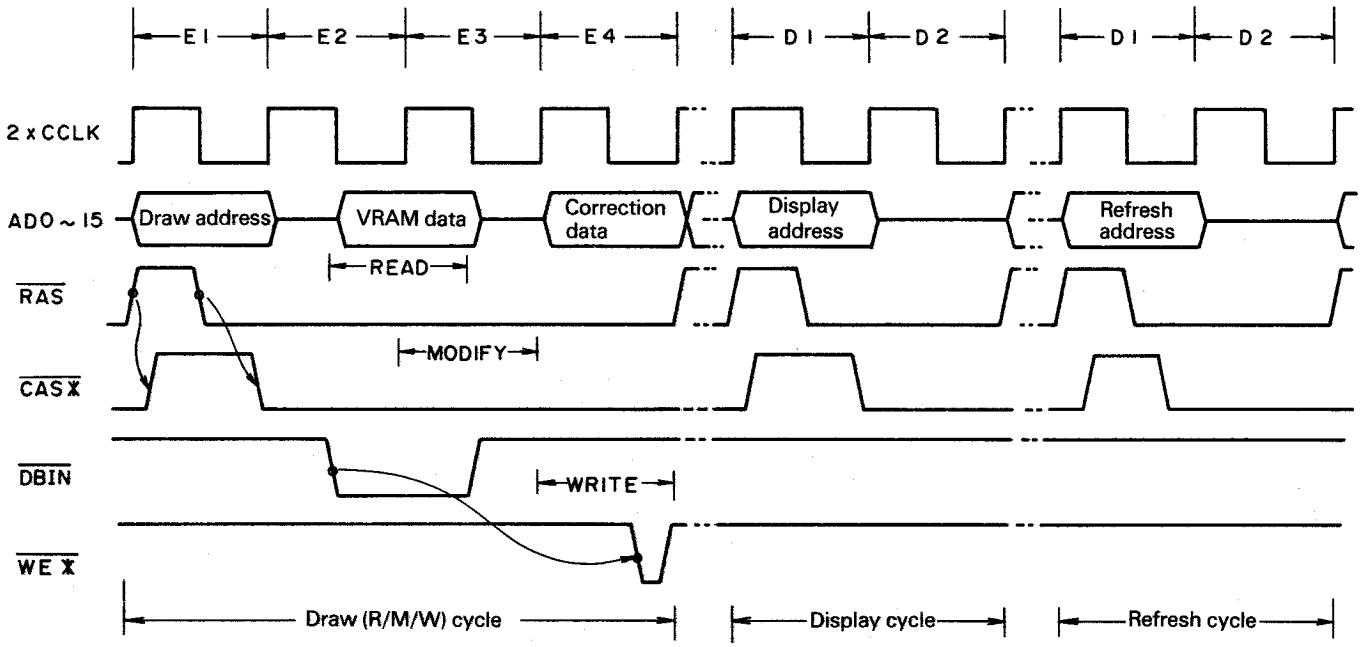
(1) Draw cycle

(2) Display cycle

(3) Refresh cycle

During the draw cycle (1), read/modify/write is executed. During the display cycle (2), data are read from V-RAM. During the refresh cycle (1) and when H. SYNC is "1", V-RAM is refreshed.

The timing diagrams of operations performed in these cycles are given below.



Note: * Indicates a signal generated by an external circuit.

Fig. 5-2 Timing diagrams

▶ Display memory RMW timing

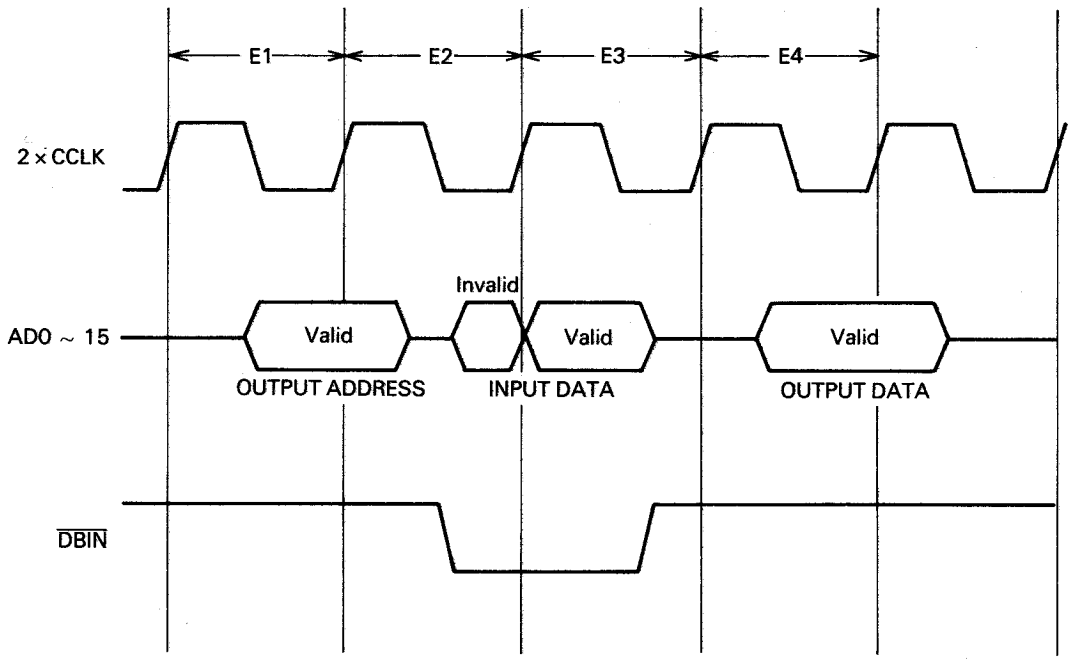


Fig. 5-3

► **Microprocessor interface write timing**

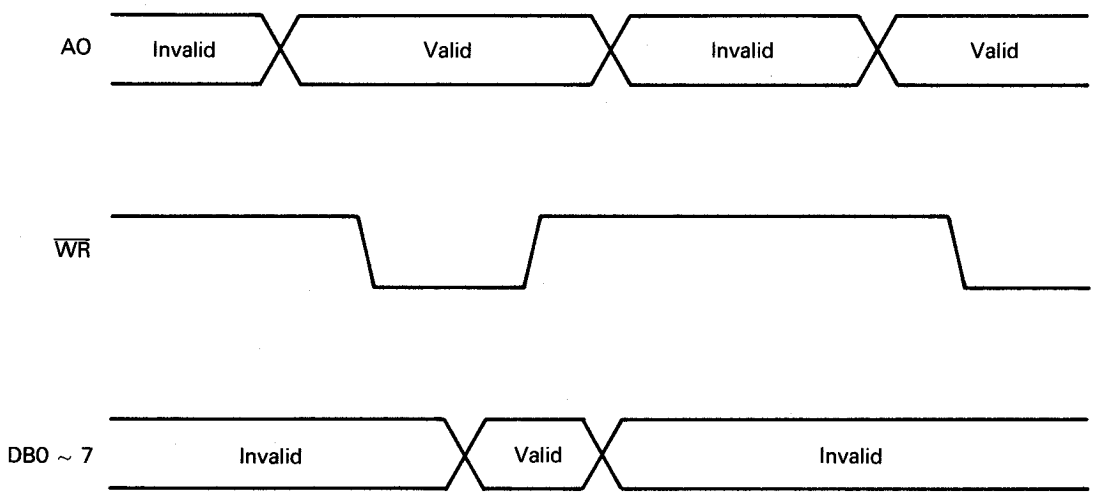


Fig. 5-4

► **Microprocessor interface read timing**

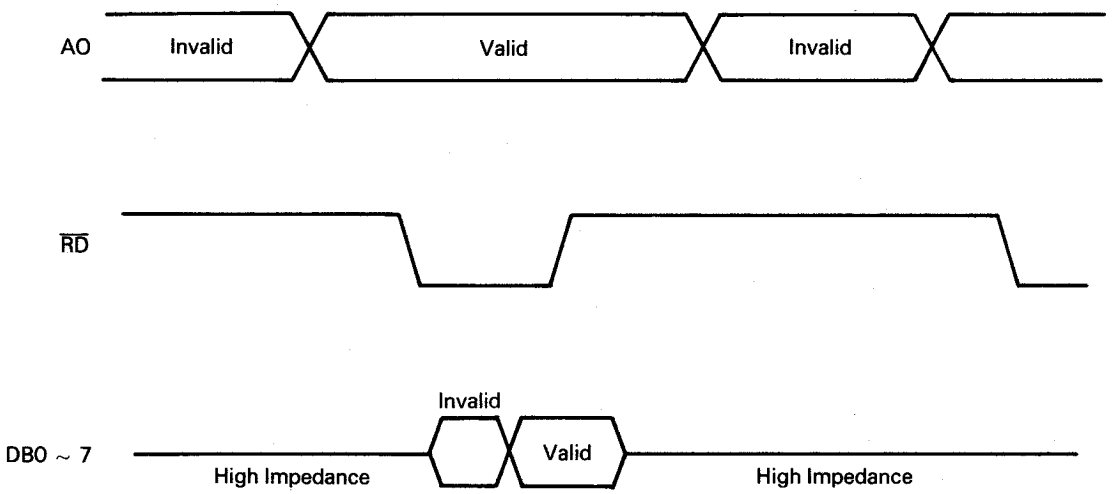


Fig. 5-5

► **Light pen input timing**

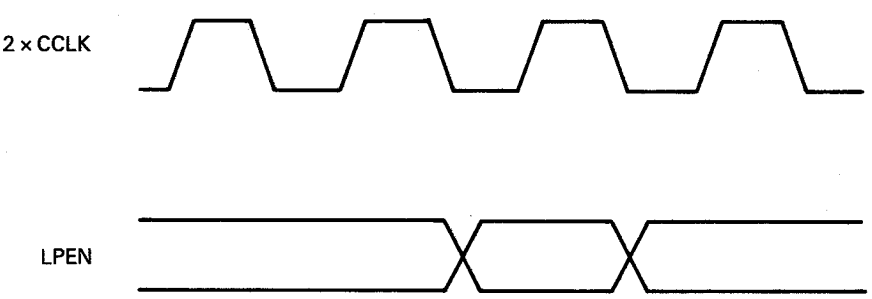


Fig. 5-6

► **Display memory Display cycle timing**

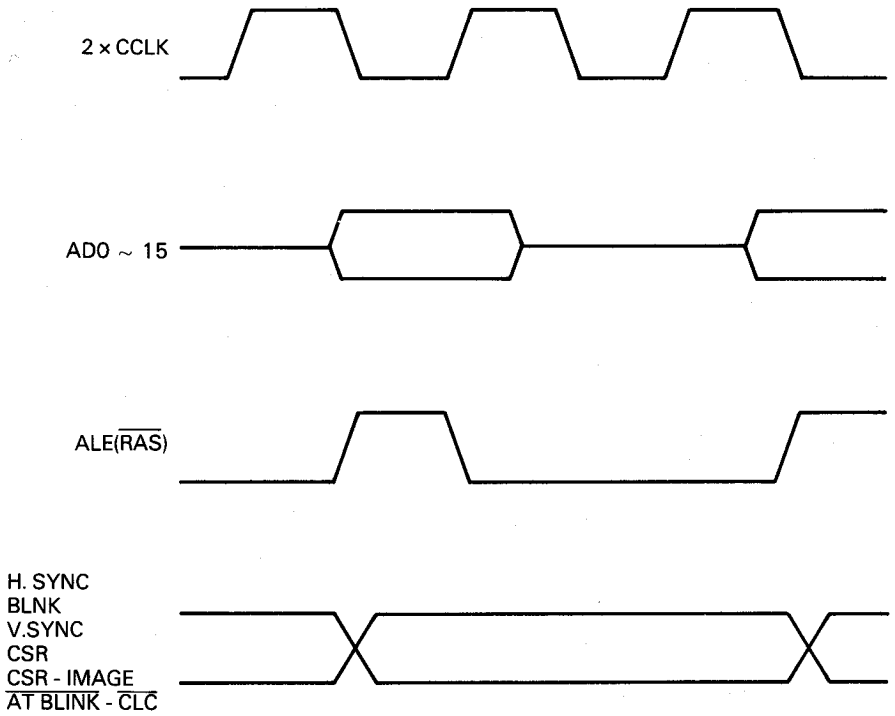


Fig. 5-7

► **Video sync signals timing**

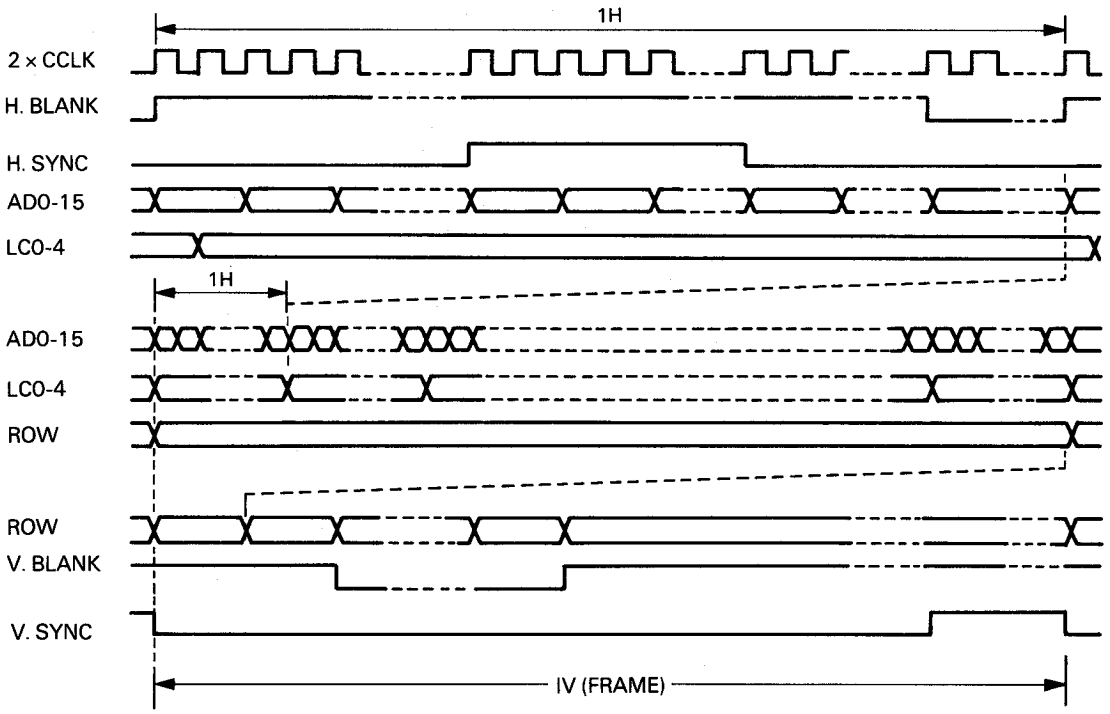


Fig. 5-8

▶ Display and RMW cycles (1 × ZOOM)

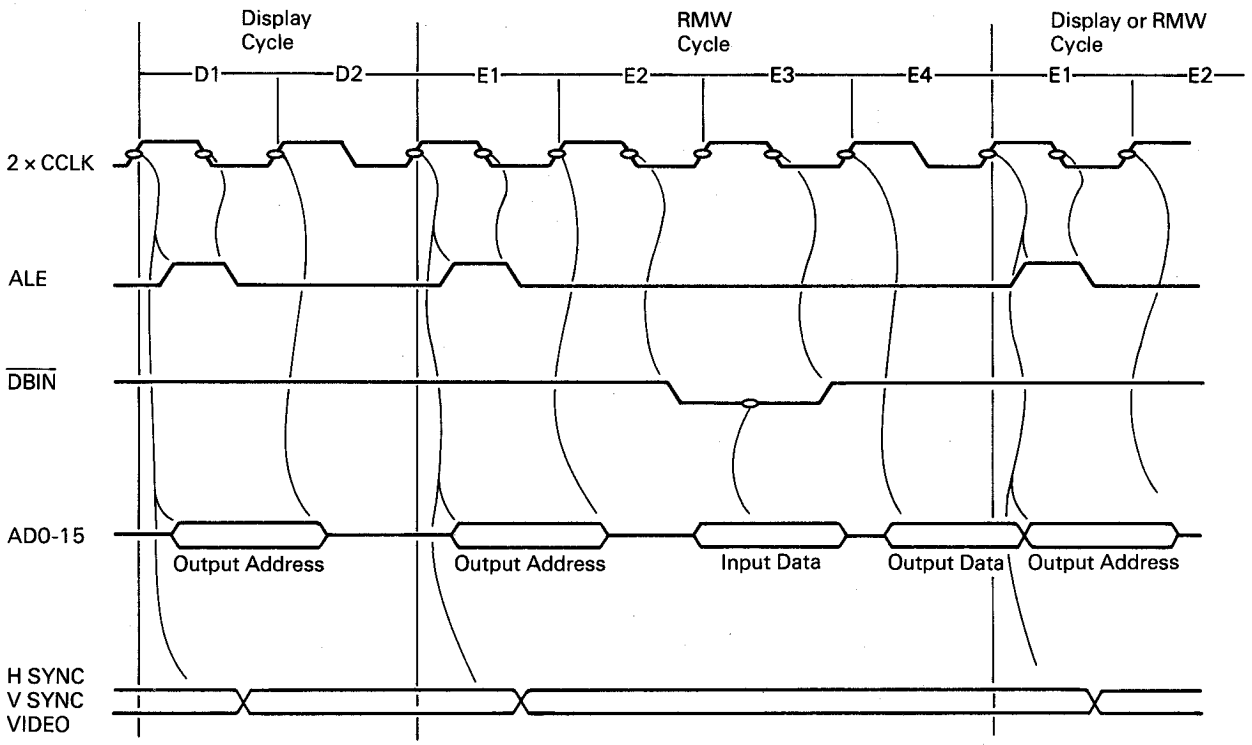


Fig. 5-9

▶ Display and RMW cycles (2 × ZOOM)

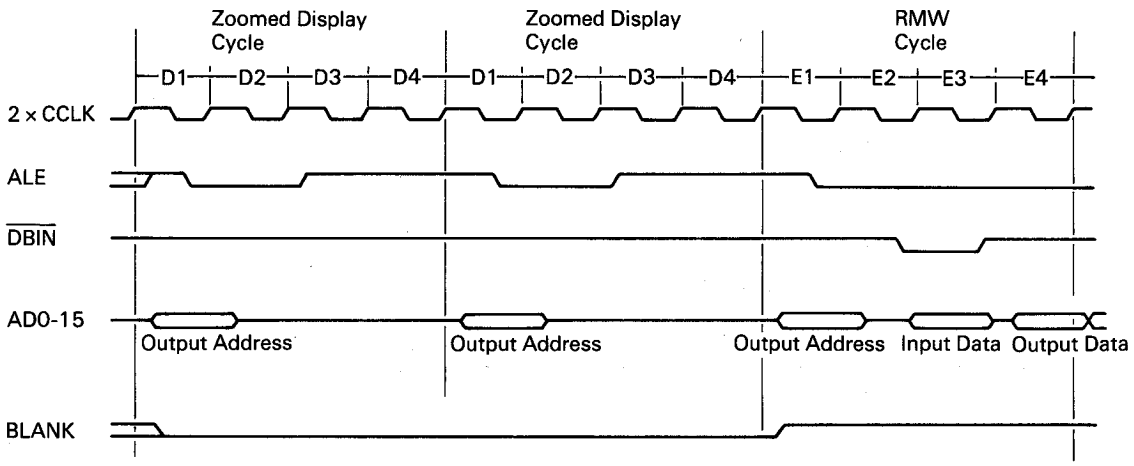


Fig. 5-10

▶ Display and RMW cycles (3 × ZOOM)

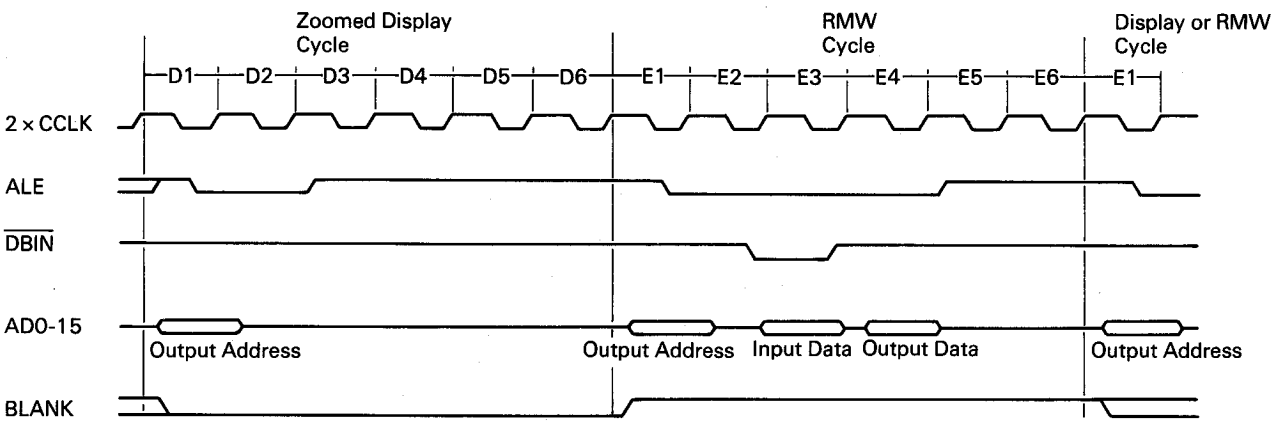


Fig. 5-11

5.4 Clock Generator

Fig. 5-12 shows the clock genrator provided for the GDC. This circuit divides the original frequency of 16.667 MHz by four into 4.16675 MHz which is delivered to terminal 2CCLK of the GDC.
The oscillator module is compensated for temperature changes so that pictures are not affected.

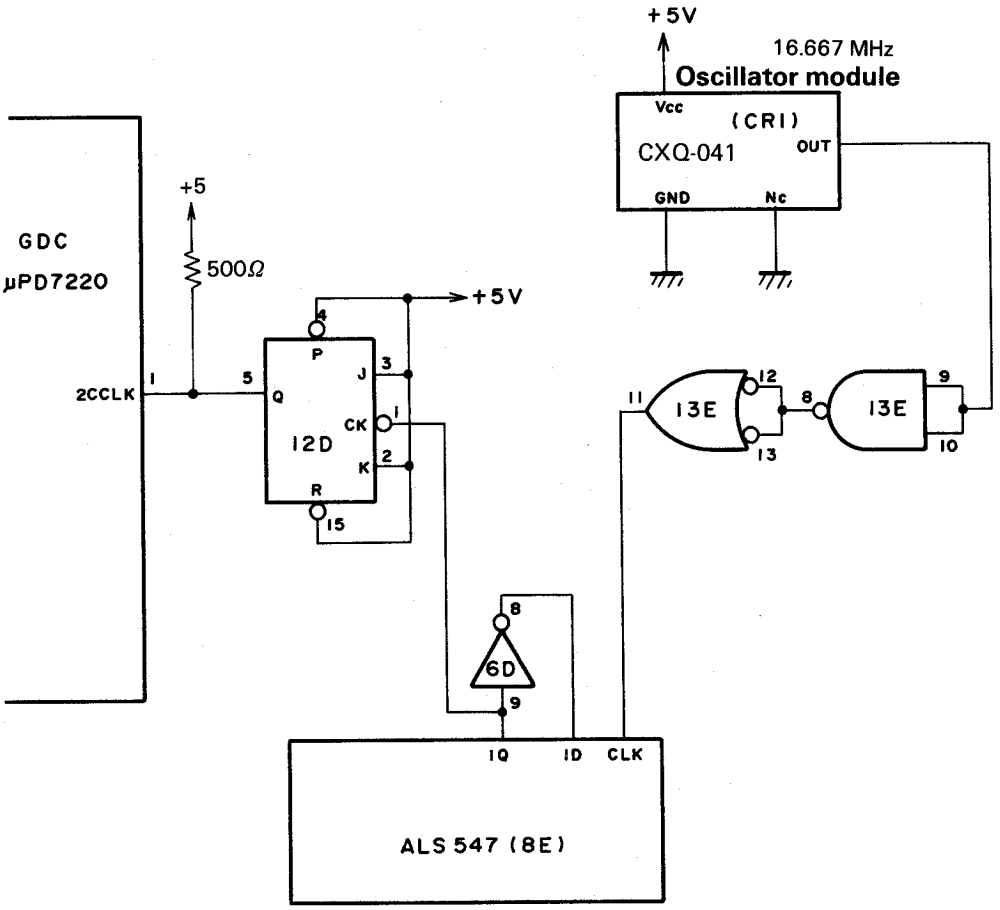


Fig. 5-12 Clock generator

5.5 Interface with the CPU

I/O addressess 38-3BH are assigned to the graphic display controller (μPD7220) and the CPU selects it with signals $\overline{\text{CSCRT}}$ and $\overline{\text{CSCCR}}$.
The μPD7220 is not provided with the input terminal of a chip select signal, and it is selected when signals $\overline{\text{RD}}$ and $\overline{\text{WR}}$, which are generated from signals $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ coming from the main circuit, are active.
The GDC exchanges information with the CPU via the data bus, in the mode determined by the combination of A0, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ as shown below. A0 is connected to the LSB line of the system address bus.

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	Mode
0	0	1	Reads status flag
1	0	1	Reads data (from GDC)
0	1	0	Writes parameter
1	1	0	Writes command

Table 5-2

The data bus is driven by a bidirectional bus driver LS245(12A) which not only switches the transfer direction of the bus lines according to the mode of data transfer but also drives the bus. Signal DIR used to switch the bus direction is signal $\overline{RD}$ of the μPD7220. If DIR is low level (that is, during read from the μPD7220), the data bus is directed from the μPD7220 to the CPU. If DIR is high level (during write to the μPD7220), the bus is directed from the CPU to the μPD7220.

DIR	Bus direction
Low	GDC → CPU
High	CPU → GDC

► **DMA controller**

DREQ, the DMA Request signal, enters the DREQ terminal of the DMA controller (μPD8237) mounted on the main board.

$\overline{DACK}$, the DMA Acknowledge signal which remains high during DMA transfer, comes from the $\overline{DACK}$ terminal of the DMA controller. This signal is used to count data bytes transferred and designate when to start transfer.

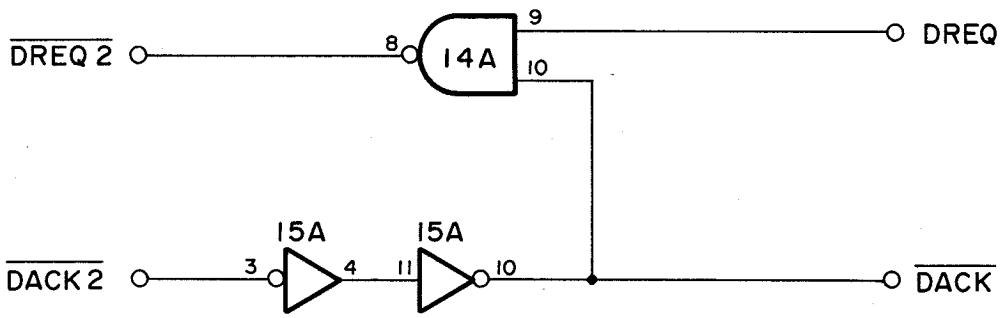


Fig. 5-13 DMA controller

The timing diagrams of $\overline{DREQ2}$ and $\overline{DACK2}$ are shown in Figs. 5-13 and 5-15.

► **Microprocessor interface DMA read timing**

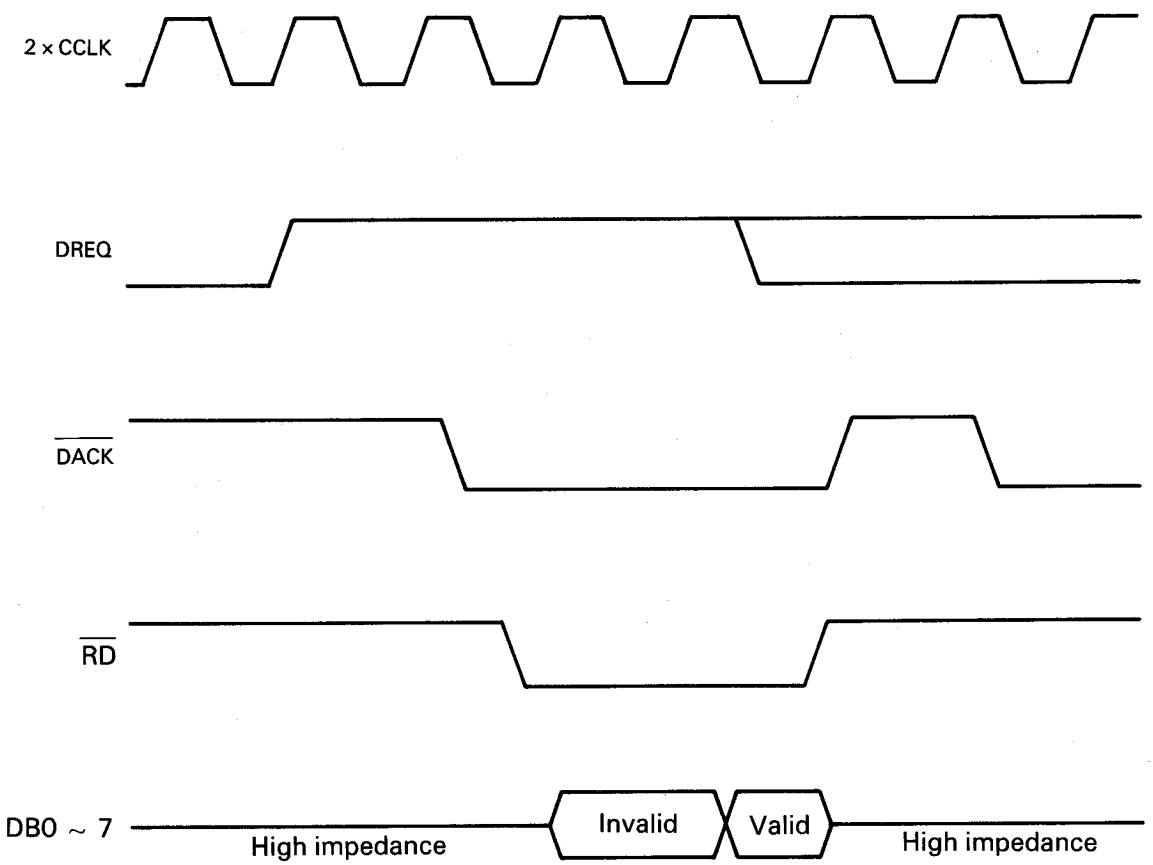


Fig. 5-14

► **Microprocessor interface DMA write timing**

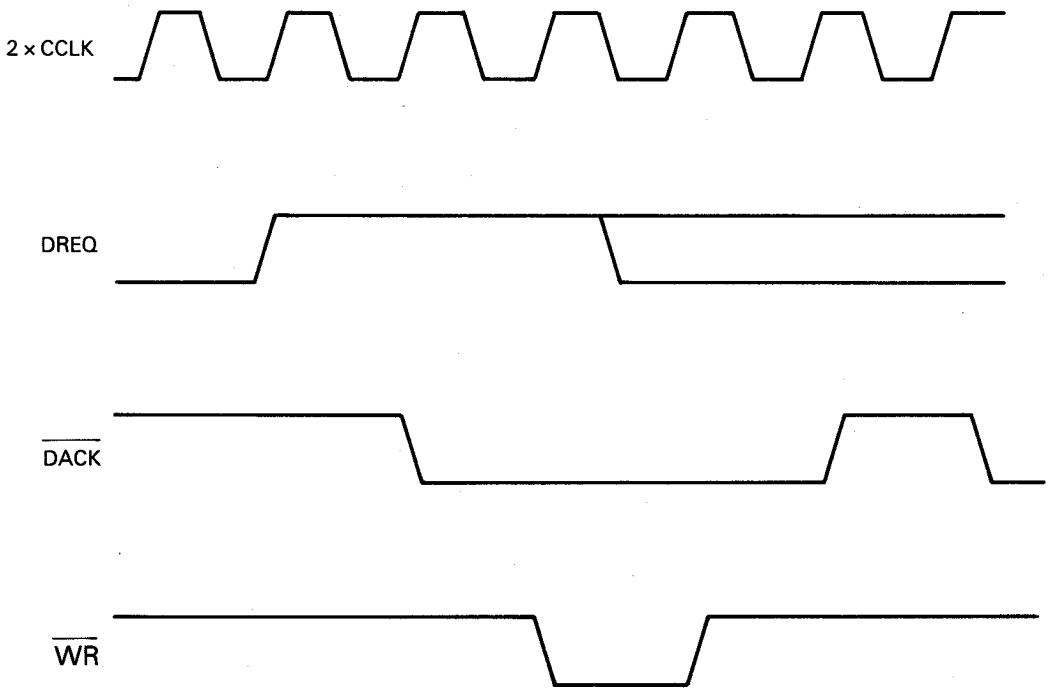


Fig. 5-15

5.6 Light Pen Interface

The μPD7220 is provided with input terminal LPEN (Light Pen) to which a signal, generated when the light pen connected detects light, maybe entered to find the location the light pen points to.

The light pen signal first enters the one-shot LS221 (1D) that converts the signal to a pulse of approximately 240 nsec wide, with the pulse width determined by the time constant of C and R externally connected. This pulse enters the GDC's LPEN terminal.

Receiving the signal, the GDC (μPD7220) computes the address of the location on the CRT and compares it with the contents of the light pen address register (LAD) of the GDC. If they are not equal, the address of the CRT location is moved to LAD. If they are equal, the light pen status flag (LPEN DETECT) is set to "1".

The CPU becomes ready to read data after it has detected that LPEN DETECT is "1".

In detection of a CRT location with the light pen, sensing is performed twice during two consecutive frame times, once per frame time. Then the coordinates detected are compared by hardware to prevent disturbance by any other light source e.g. room lighting.

Signal $\overline{\text{INTCR}}$ is the interrupt request signal which the light pen switch generates and sends to the CPU.

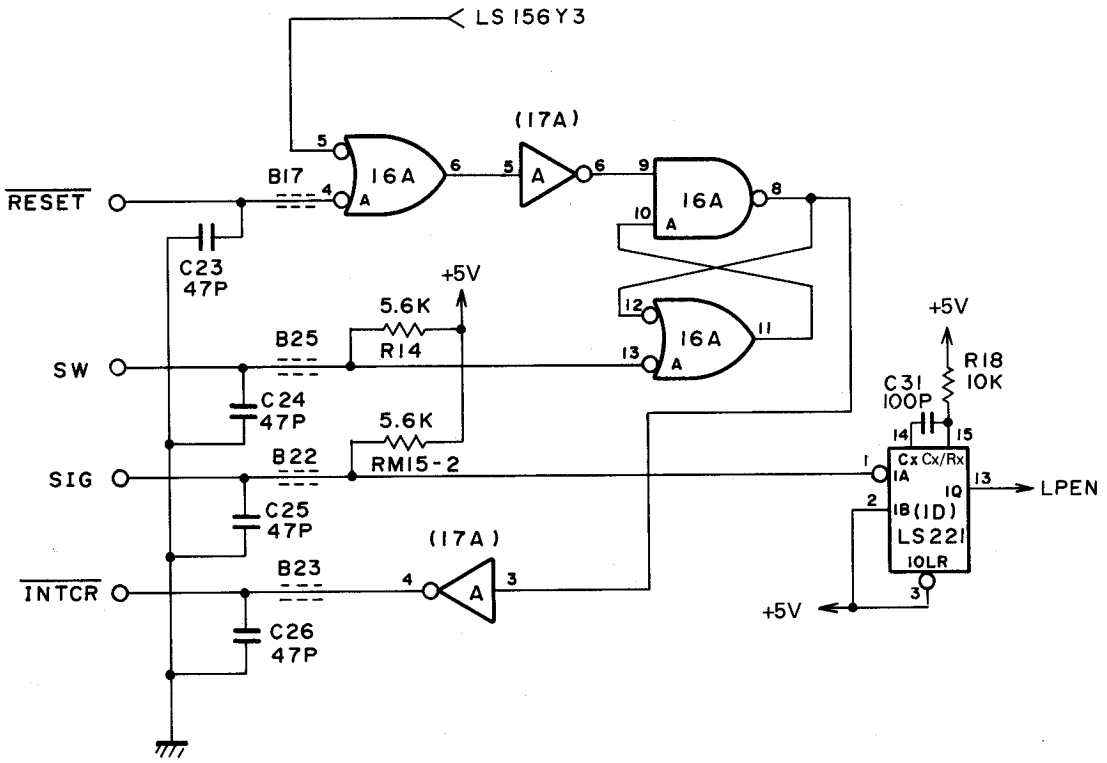


Fig. 5-16 Light pen signal input circuit

5.7 Memory Interface

5.7.1 Video RAM (V-RAM)

V-RAM consists of 16 D-RAM chips which are installed separately from the main card main memory and controlled directly by the GDC (μPD7220).

Eight address lines, A0 - A7, are connected to the D-RAM chips and addressing is performed in two cycles, with the most significant eight bits and the least significant eight bits separately. Signal $\overline{RAS}$ serves as the strobe signal for the least significant eight bits and signal $\overline{CAS}$ for the most significant eight bits.

The D-RAM capacity is 32 KB (with 16K x 1 bit Dynamic RAM used) for the ASCII type and 128 KB (with 64K x 16 bit Dynamic RAM used) for the HASCI type.

5.7.2 Basic cycles of the D-RAM

(1) Write cycle: At decay of $\overline{CAS}$ when $\overline{WE}$ is low level, the data which is currently supplied to the data input terminal DI is written into the D-RAM. The data output terminal DO remains floating at this time.

(2) Read cycle: At decay of $\overline{CAS}$ when only $\overline{WE}$ is high level, data is output to the data output terminal.

(3) Read/modify/write cycle: During this cycle, data is read out, modified, and written into the memory location where the data was stored originally. At this time, write operation is executed when $\overline{WE}$ turns to low level after data is developed at the data output terminal.

(4) Delayed write cycle: This is the same as the read/modify/write cycle but $\overline{WE}$ turns to low level earlier than in read/modify/write cycle and, therefore, write operation is executed before data develops at the data output terminal.

In this cycle, read/modify/write operation is not performed but ordinary write operation is executed. Data developing at the data output terminal is not used.

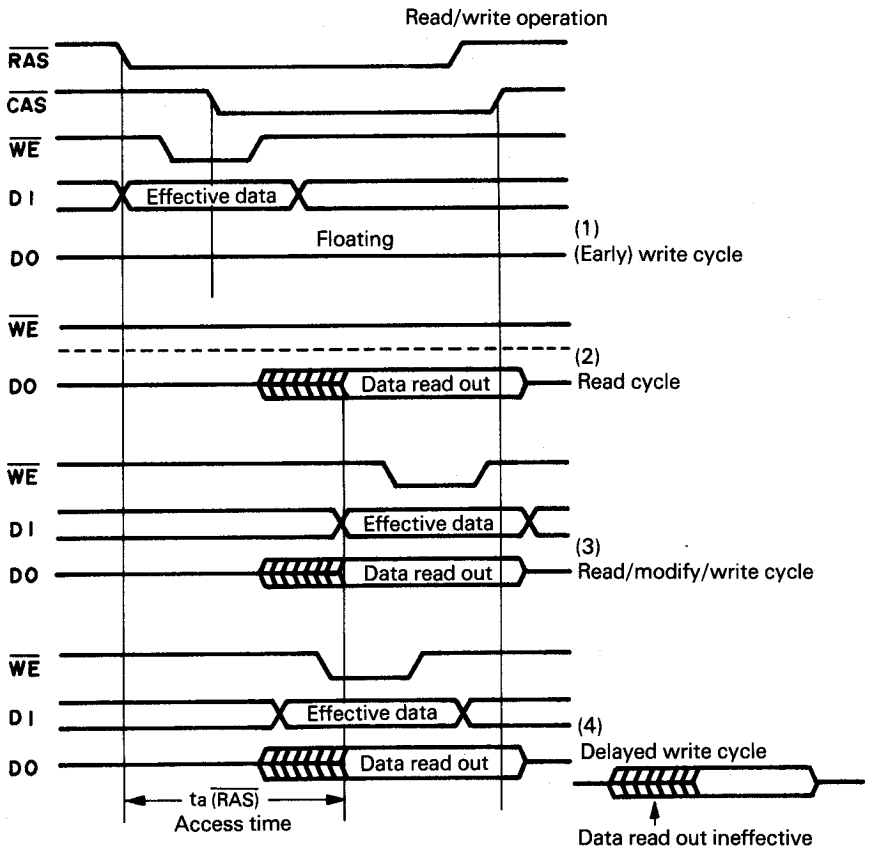


Fig. 5-17

5.7.3 Memory capacity and pages

(1) In graphic mode

In graphic mode, addresses are assigned to the locations on the CRT screen as shown in Fig. 5-18. The data associated with each location comprises 16 bits and the screen consists of 640 (vertical) by 400 (horizontal) locations called dots.

Data may be assigned to each dot in graphic mode. In full-graphic mode, 31.25 K bytes (640 × 400 dots) of data is required per a screen. Therefore the number of pages becomes one with 32 KB VRAM, four with 128 KB VRAM.

Further, one screen includes 16 K words (640 × 400 / 16) by counting 16 bits as 1 word. Memory Map becomes as shown in Fig. 5-18.

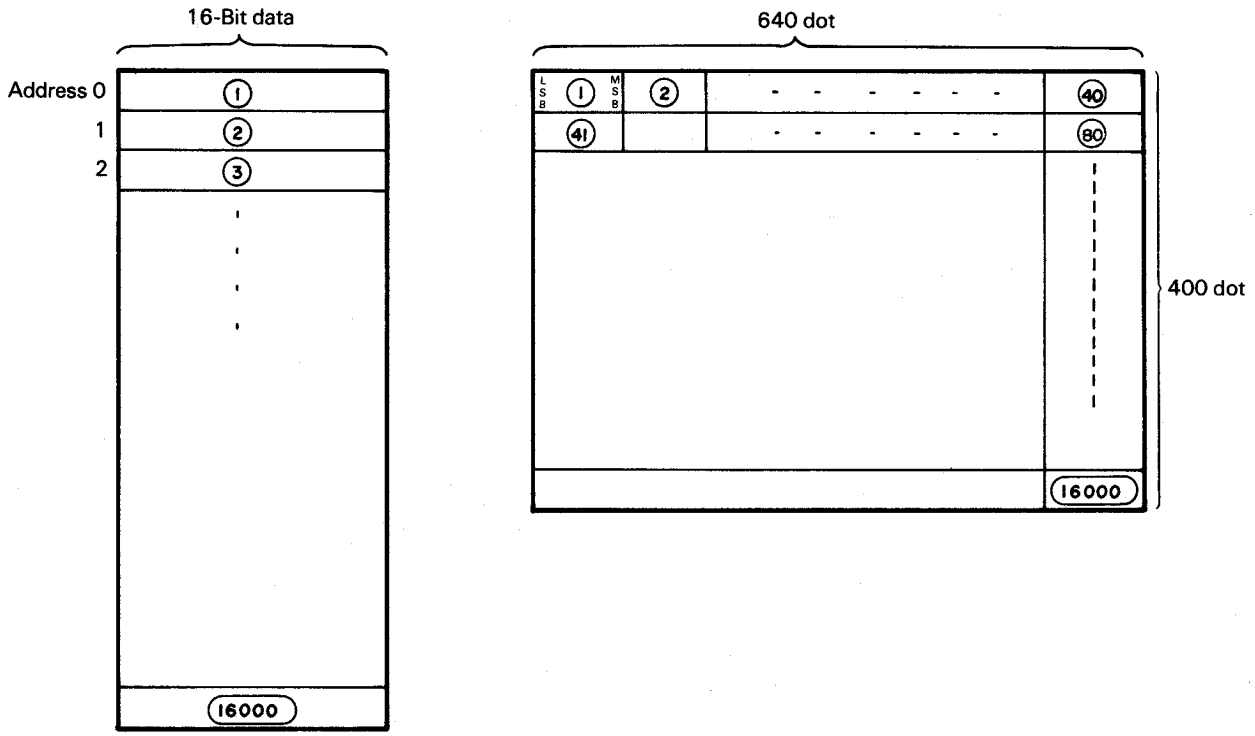


Fig. 5-18 Graphic data and memory map

(2) In character mode

In character mode, addresses are assigned to the locations on the CRT screen as shown in Fig. 5-19. Each character is composed of eight horizontal and 16 vertical dots and the whole screen may display 80 characters per line on 25 lines.

Compared with graphic mode, the number of independently addressable locations is twice as large horizontally and one-sixteenth as large vertically and, as a whole, one-eighth (2 × 1/16 = 1/8) as large. Therefore, the V-RAM capacity may be considered as 16 pages (1 page/32 KB × 64 KB × 8) if it is 64 KB.

Out of 16 bits of the data the GDC generates, the most significant eight bits serve as an attribute data whose function is summarized in Table 5-3.

The least significant eight bits designate an address in the character generator whose contents are to be displayed as a character.

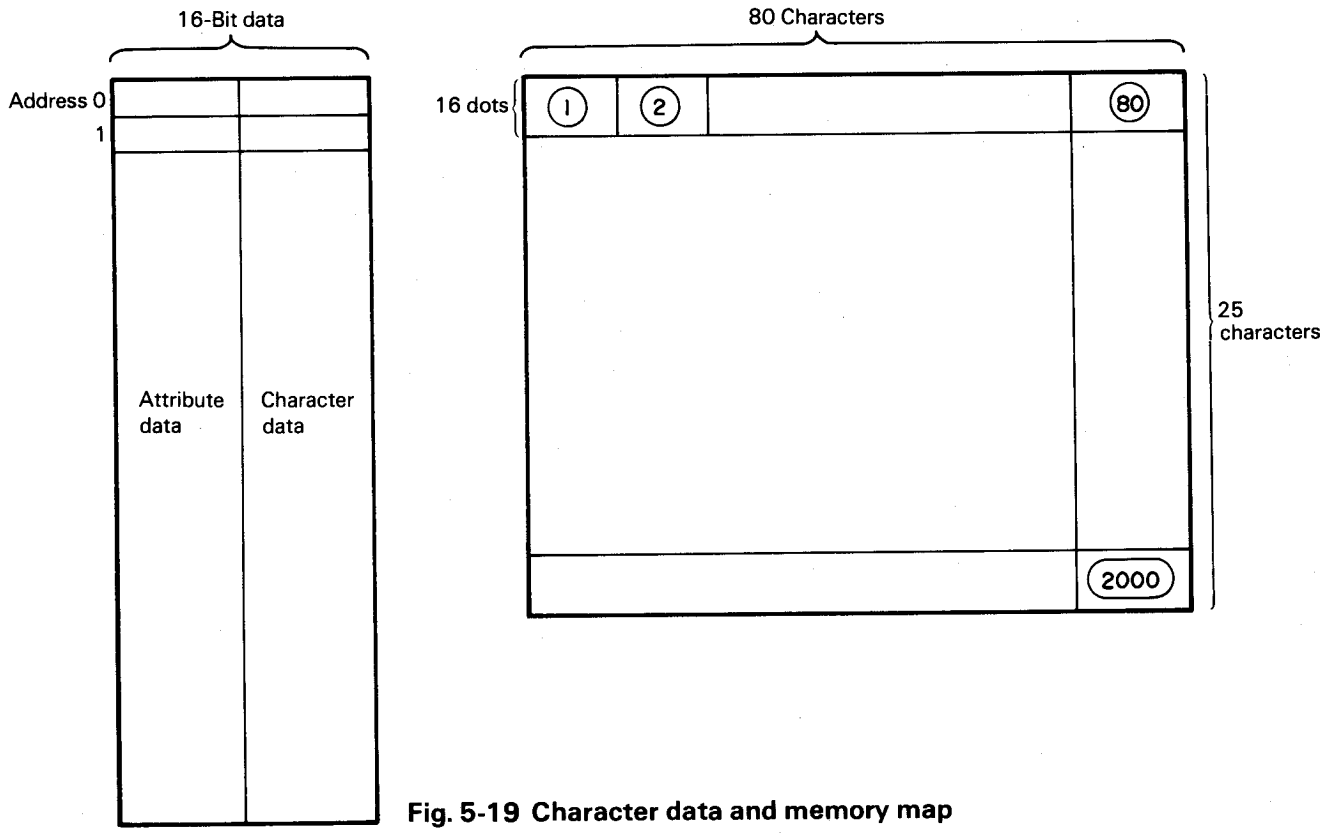


Fig. 5-19 Character data and memory map

Signal line	Signal name	Function
AD15	BLINK	BLINK
AD14	SECRET	INVISIBLE
AD11	RVS	REVERSE
AD10	HiLT	INTENSIFY

Table 5-3 Attributes

5.7.4 $\overline{RAS}$/$\overline{CAS}$ signal generator

Fig. 5-20 shows the circuit which supplies the D-RAM with signals $\overline{RAS}$ and $\overline{CAS}$. These signals are generated from the $\overline{RAS}$ (Row Address Strobe) signal of the GDC.

The J-K flip-flop ALS112 (12D) shifts $\overline{RAS}$ of the DGC to the trailing edge of 2CCLK to precharge RAS of the D-RAM.

$\overline{CAS}$ is generated by trailing $\overline{RAS}$ for 100 nsec and supplied to the D-RAM.

5.7.5 Address latch enabling/output control signal generating circuit

The $\overline{RAS}$ output by the GDC is used not only to supply the D-RAM with $\overline{RAS}$ and $\overline{CAS}$ but also to control the gates of address latches ALS573 (8C/9C).

The $\overline{RAS}$ output of the GDC is supplied directly to the ENABLE terminals of the address latches.

The input signals to the OUTPUT CONTROL terminals of ALS573 8C and 9C are basically the $\overline{RAS}$ signal supplied to the D-RAM but delayed for 40 nsec and inverted to opposite phases from each other.

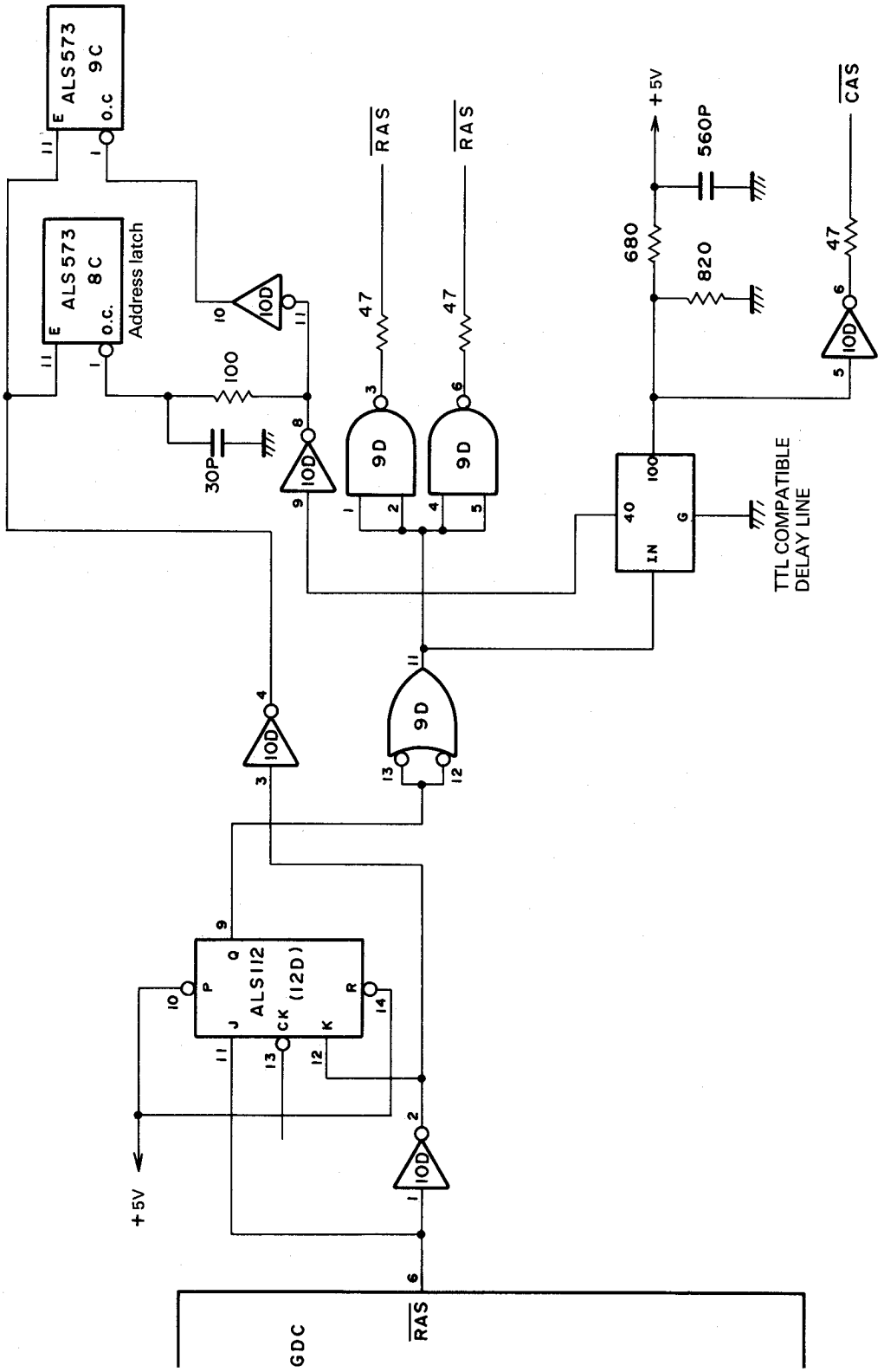


Fig. 5-20 $\overline{RAS}$/$\overline{CAS}$ signal generator and address latch enabling/output control signal genrating circuit

5.7.6 $\overline{\text{DBIN}}$ signal generator

Signal $\overline{\text{DBIN}}$ (Data Bus IN) is generated only during execution of read/modify/write (R/M/W) for V-RAM to put the V-RAM output onto its data bus.

$\overline{\text{DBIN}}$ of the GDC connects to terminals G1 and G2 of the 3-state buffers LS541 (1C and 7C).

That is the buffers output data when $\overline{\text{DBIN}}$ is active (input terminals G1 and G2 are at low level) so that the GDC can read the output data of the D-RAM.

5.7.7 $\overline{\text{WE}}$ signal generator

This circuit generates the $\overline{\text{WE}}$ (Write Enable) signal which is a trigger signal to write data in the D-RAM during draw (R/M/W) cycle.

$\overline{\text{WE}}$ is generated by the delay circuit (see Fig. 5-21) which delays $\overline{\text{DBIN}}$ coming from the GDC. $\overline{\text{DBIN}}$ is output when data are read out of V-RAM of the GDC. Two D flip-flops, LS374 (12C), timed by clock 2CCLK and LS574(7E), timed by DOT CLK, shift signal $\overline{\text{DBIN}}$ during E4 cycle when correction data are generated, generating $\overline{\text{WE}}$ which is delivered to the $\overline{\text{WE}}$ input terminals of the D-RAM.

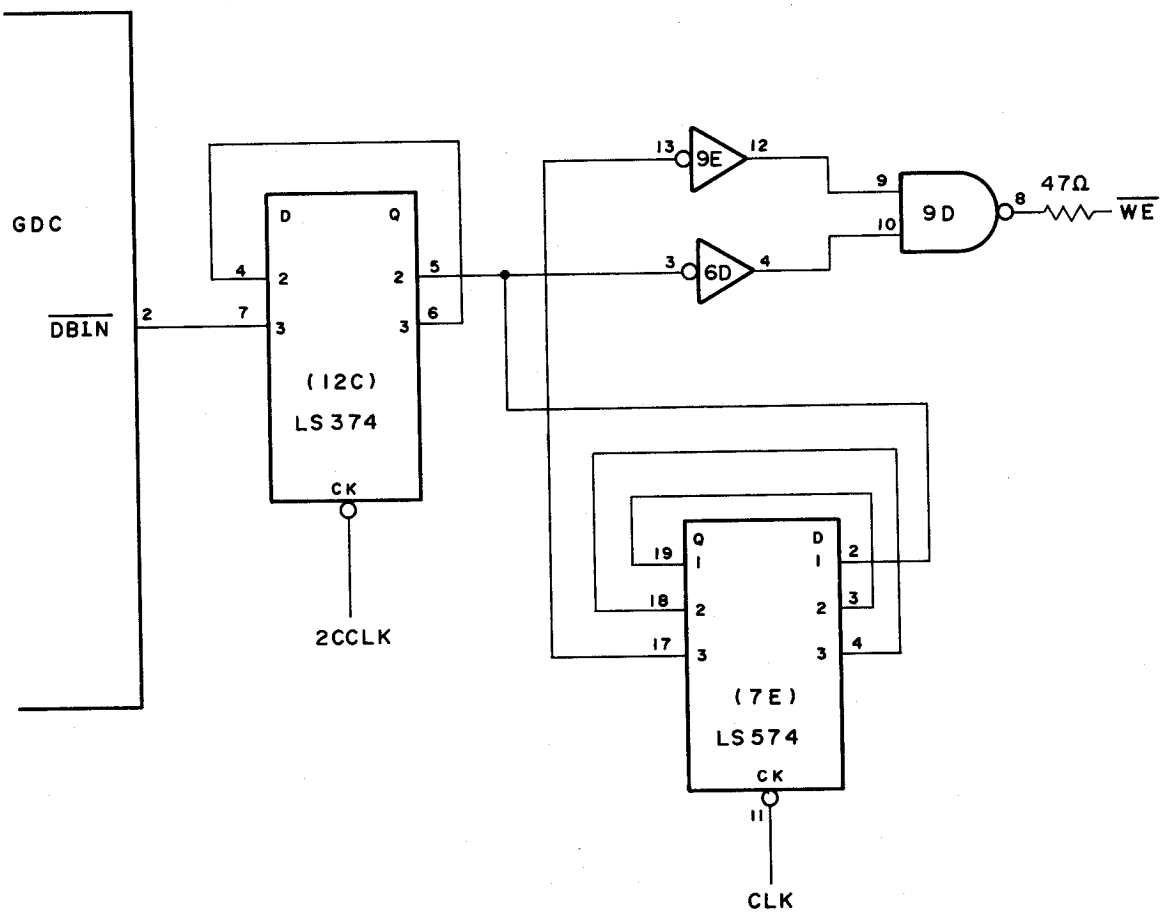


Fig. 5-21 $\overline{\text{WE}}$ signal generator

5.8 Video Signal Output Circuit

5.8.1 General

Picture data written in V-RAM are read out during the display cycle and supplied via the video signal output circuit to the CRT drive unit (CDU) as video signals.

The video signal output circuit operates as described below in a specific mode.

(1) In graphic mode

Sixteen-bit data output from V-RAM is first held in latches (D flip-flops) LS374 (2C and 6C), then enters D flip-flops LS374 (3C and 5C). Output pins 8 and 6 of NAND gate 13D are connected respectively to the OUTPUT CONTROL terminals of these flip-flops.

One input to each of the two NAND gates is the CSR-IMAGE signal which is high level during graphic mode. The other input to pin 4 is the Q output of D flip-flop LS74(14D) and that to pin 9 is the $\overline{Q}$ output.

LS74(17D) is timed by the clock signal which is the inversion of $\overline{RAS}$ supplied to V-RAM so that the data output from V-RAM are output, with its most significant eight bits and least significant eight bits separated, from latches LS374 (3C and 5C), and synchronized with addressing according to signal $\overline{RAS}$.

(2) In character mode

Signal CSR-IMAGE coming from the GDC is low level during character mode and, as a result, output of pins 6 and 8 of NAND gate 13D is high level, putting the OUTPUT CONTROL terminals of data latches LS374 (3C and 5C) to high level and inhibiting them from outputting data.

On the other hand, the OUTPUT ENABLE terminal of the character generator becomes active when CSR-IMAGE is low level. Now the data output from V-RAM enters data latches LS374 (2C and 6C) from where the least significant eight bits enter the character generator (2E). Its output, in turn, enters a shift register for parallel-to-serial conversion.

The most significant eight bits of the V-RAM output data (which include a 4-bit attribute data) enters D flip-flop ALS574(6E) and then goes to an attribute logic.

(3) In graphic-character mixed mode

The μPD7220 permits mixture of graphic and character modes on the same screen. In this case, the screen is divided into upper and lower sections, and graphic and character modes work in either of the two sections. (Fig. 5-22)

In graphic-character mixed mode, graphic and character data are output as described above. That is data latches LS374 (3C and 5C) work for graphic data and the character generator (2E) and attribute generator work for character data.

It might happen that, when the upper section of the screen is in graphic mode, characters in the lower character mode section do not appear wholly but only partly, as shown in Fig. 5-23.

However, this does not actually happen because the Q10 GMS resets the line counter with a reset signal which the one-shot LS221(1D) generates from the NAND output of the inversion of the GDC's output $\overline{AT. BLINK}$ - $\overline{CLC}$ with H. SYNC. Thus the line counter is reset at the end of the graphic mode section and it restarts counting line at the beginning of the character mode section.

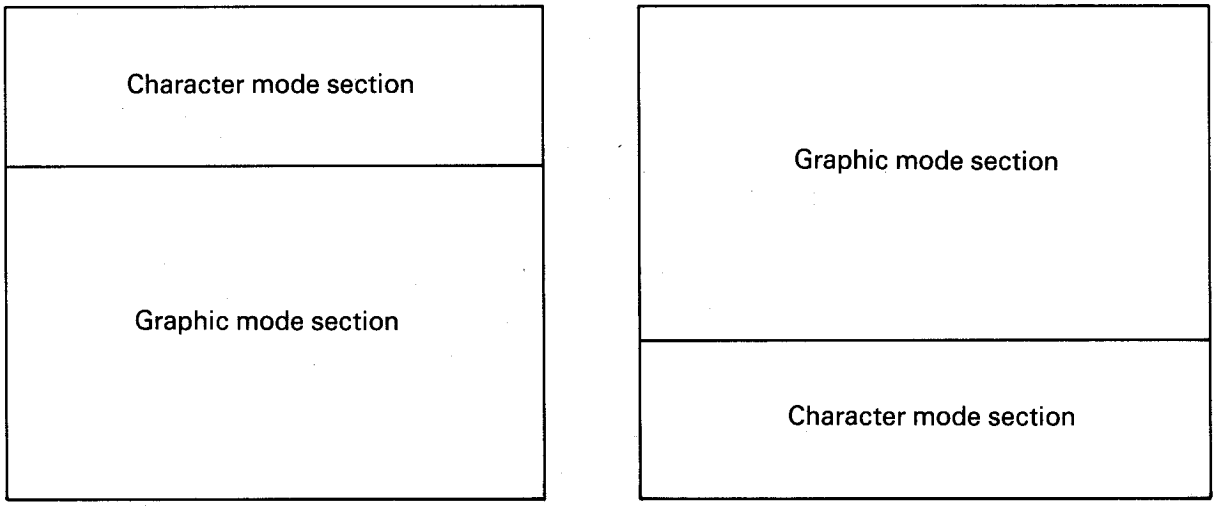
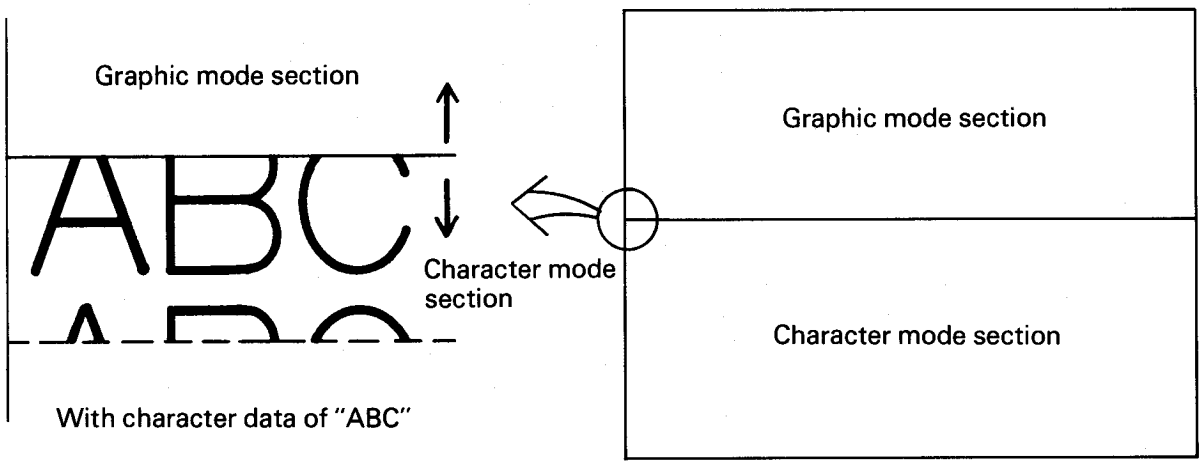


Fig. 5-22 Graphic-character mixed mode



If the first horizontal dot count where the character mode area starts is not an integer multiple of 16, characters might disintegrate unless the line counter is reset at the beginning of the character mode area.

As line counter reset is automatically done at any occation, user don't need to be bother with it.

Fig. 5-23

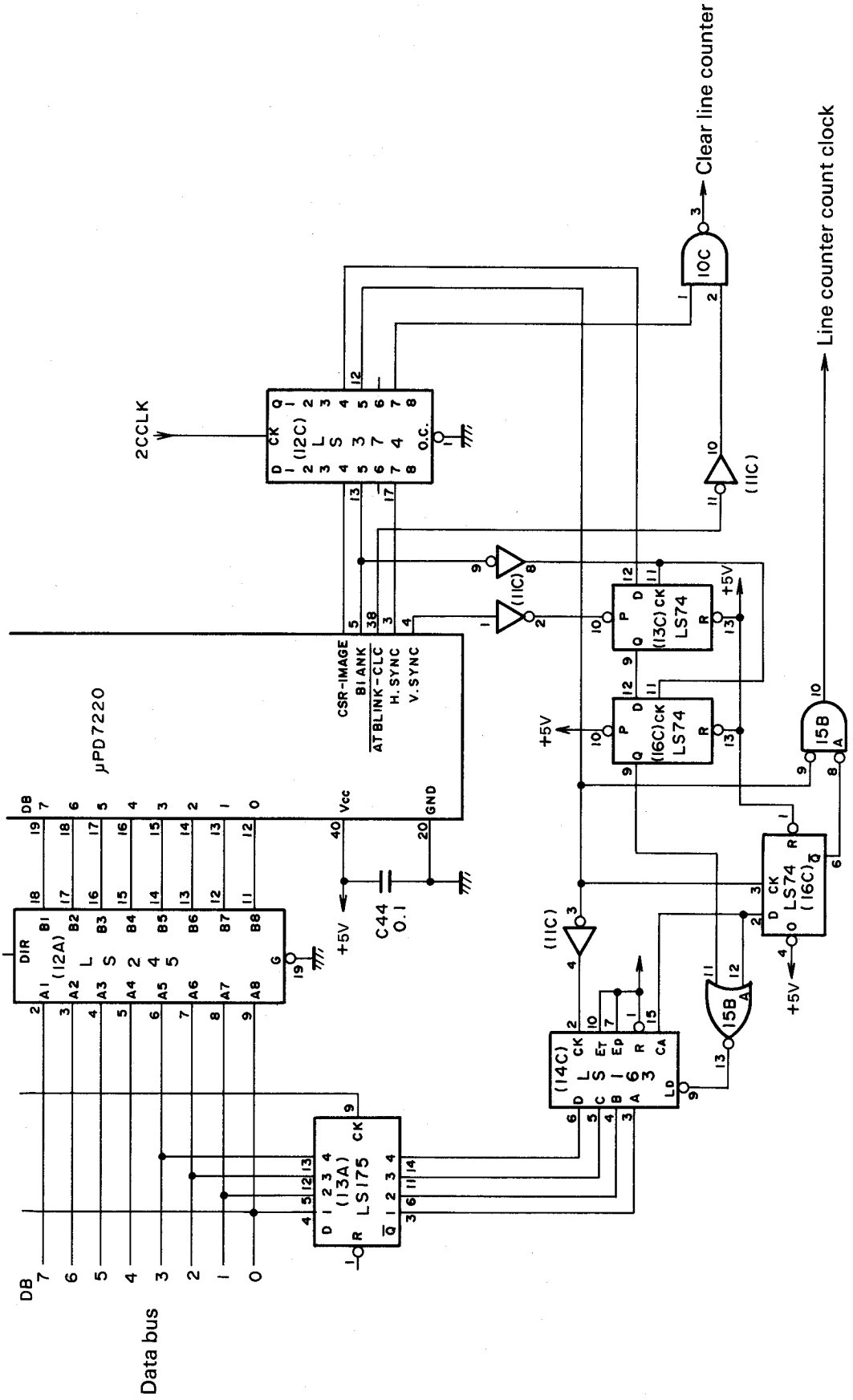


Fig. 5-24 Clock generator for the line counter operating in graphic-character mixed mode

5.8.2 Line counter

In character mode, the charachter data read out of V-RAM are actually addresses (A4 - A11) (A4 – A12, in use of 2764) of memory locations of the character generator (2E) which hold the dot pattern data of characters.

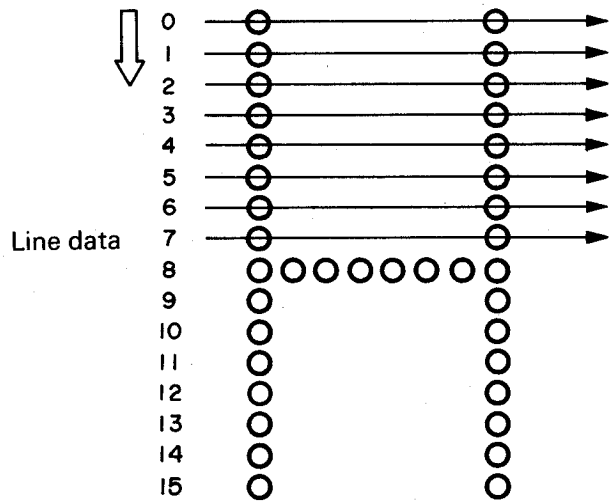
In the CRT, every horizontal scanning covers a vertical width as large as a dot and, therefore, it is necessary to count the line number of the character generator at every scanning.

The circuit shown in Fig. 5-25 performs this function. First, gate 10C NANDs H. SYNC with $\overline{\text{AT. BLINK}}$ $\overline{\text{-CLC}}$ and the output triggers the one-shot 2A to genrate a pulse, whose width is determined by external C40 and R19 at $\overline{2Q}$, so that the line counter LS161 (1E) gets reset. Next, character data are output from V-RAM.

The data giving line counter inputs are always high level because input A, B, C and D of LS161 (1E) is pulled-up to +5V.

, the line counter LS161 operates, controlled by a clock timed with the horizontal sync signal, to send line data to address A0 – A3 of the character generator from outputs QA - QD.

The character generator combines address data A0 – A3 with data of A4 – A11 and retrieves character data of line.



A 0 1 2 3	4 5 6 7 8 9 10 11
Line data	Character data
Repeats counting from 0H to FH. Dot data of characters of every line are obtained by varying this data on every scanning.	These are the codes of characters to be displayed.
Receiving address of A0 – A11, the character generator outputs the data held in the designated location.	

Fig. 5-24

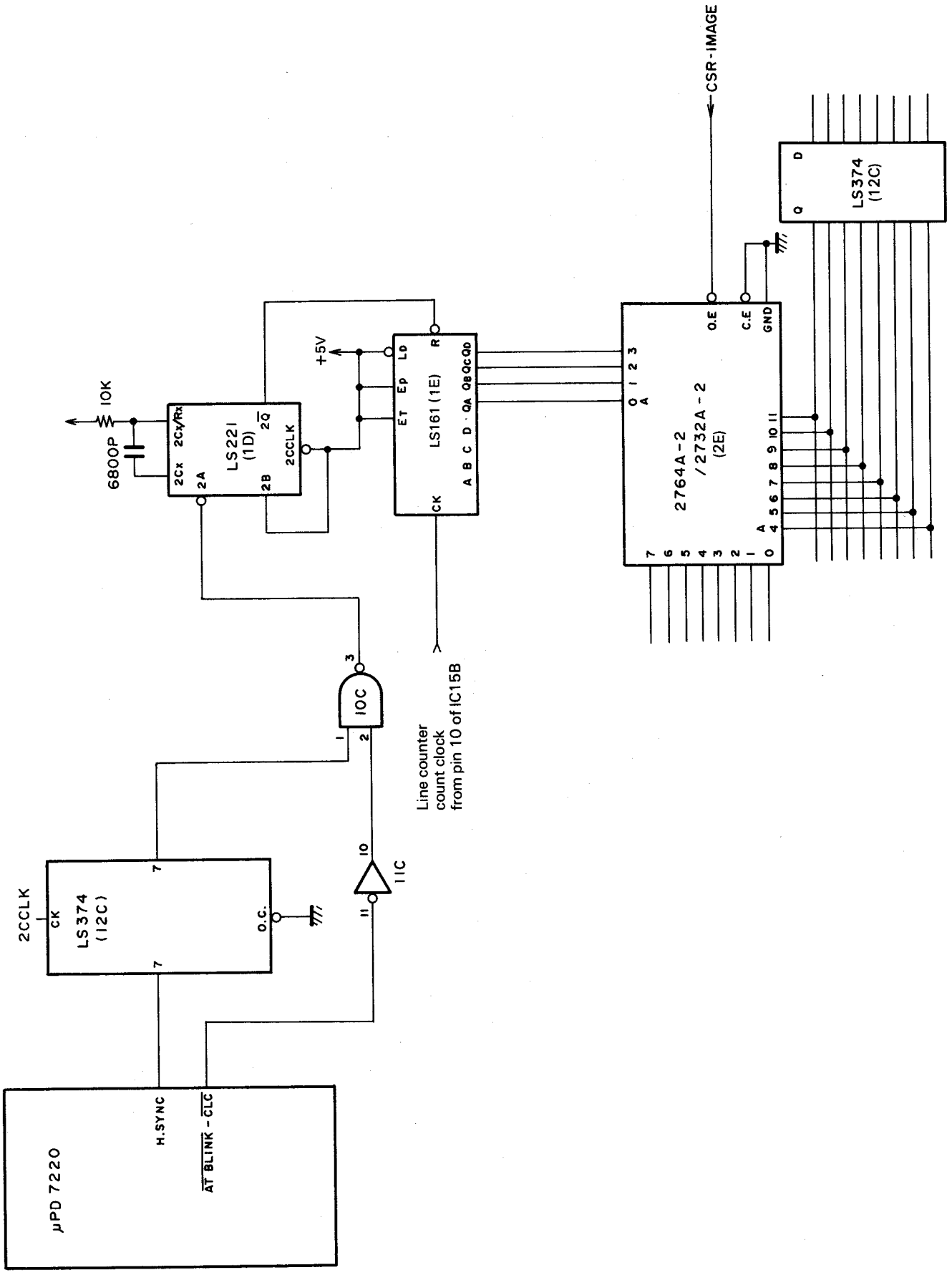


Fig. 5-25 Clear line counter generator

5.8.3 Blanking signal

The blanking signal is output from the BLANK signal terminal of the GDC to blank out retrace lines in any of the following conditions.

(1) During horizontal or vertical retrace time

(2) From execution of a display stop command such as RESET and STOP until execution of a START command

(3) During execution of R/M/W for V-RAM

Fig. 5-26 shows the circuits to which signal BLANK is supplied from the GDC. The BLANK signal is output from the BLANK signal terminal of the GDC and passes D flip-flop LS374(12C) over to terminal 2D of another D flip-flop LS175(15D). Output $2\overline{Q}$ of LS175(15D) is further delayed by two dot clocks by LS175(8D), and is output from 2Q of LS875(8D). This goes into ALS40(10E) of the last ladder of attribute logic. Also the video signal which has passed attribute logic is input to another input terminal of ALS40(10E). Thus, AND of these signals is ultimately made, and provided to the CDU. According to the situation of BLANK signal, the video signal will be output or stopped.

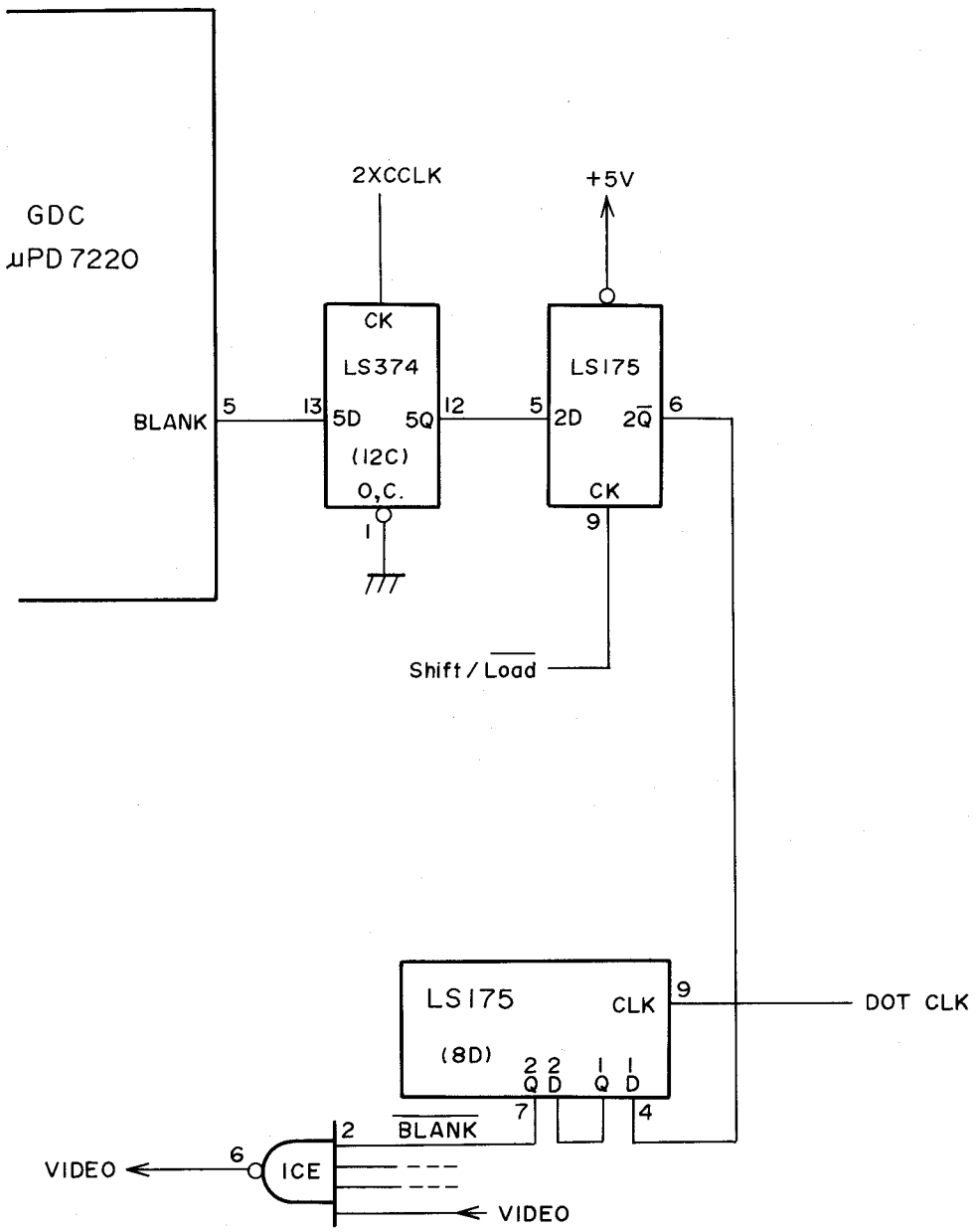


Fig. 5-26 Circuits of the BLANK signal

5.8.4 CSR-IMAGE signal

CSR means cursor and IMAGE graphic mode. These signals which are active at high level are output by time division.

The CSR signal remains output during the horizontal scanning time (one raster time). The IMAGE signal is output when the BLANK signal is output (during retrace blanking time).

If signal IMAGE is high level at the beginning of horizontal scanning when signal BLANK is output together, graphic mode is selected during the horizontal scanning time and the OE (Output Enable) terminal of the character generator does not become active.

At this time, the IMAGE signal turns the OUTPUT CONTROL signal of another D flip-flop LS374 (3C or 5C) to active, so that graphic mode is entered.

If the IMAGE signal is low level while the BLANK signal is output, character mode is selected during the horizontal scanning time and the signal turns terminal OE of the character generator 2732(2E) to active and, at the same time, the OUTPUT CONTROL terminals of D flip-flops LS374 (3C and 5C) to high level.

As a result, video data enters the shift register via the character generator.

5.9 Attribute Data Generator

The attribute data generator genrates VIDEO signal of the CRT by adding attribute data to VIDEO signal of character data.

First, the VIDEO signal enters pin 1 of NAND gate IC7D. The other input to the gate is the $\overline{\text{SECRET}}$ signal and, when it is low and active, the VIDEO signal is not output to the CRT. So, the character become invisible.

The $\overline{\text{SECRET}}$ signal is normally high level and, therefore, the output at pin 3 of IC7D is low level. This signal then enters pin 5 of OR gate IC7D. The other input to the gate is the CSR signal output through pin 11 of IC7D. This signal is low level when CSR appears and high level otherwise. The OR gate ORs the VIDEO and CSR signals to determine whether or not to display the cursor.

The output at pin 6 of IC7D is high level when there are display data and, therefore, the input to pin 13 of the subsequent EX-OR gate IC16B is also high level. The other input to this gate is the $\overline{\text{RVS}}$ signal, which is EX-ORed with the VIDEO signal to determine whether or not to reverse the image. The BLINK signal which designates image blinking is supplied from pin 8 of IC7D.

The $\overline{\text{BLINK}}$ signal coming to pin 9 of IC9E is an attribute data associated with a character data, but the $\overline{\text{AT-BLINK}}$ signal alternates between high and low levels for every screens to make the image appear as if it were blinking. The blinking signal is generated by NANDing these signals.

The BLANK signal further enters pin 2 of IC10E. This signal is low level and the screen becomes blank

The VIDEO signal passes through the gates as explained above and enters the CDU (CRT drive unit) as the VIDEO signal of the CRT.

The HILT (High Light) signal which intensified characters is generated by varying the voltage level which resistors R5 and R6 generate by dividing the level of the VIDEO signal obtained above.

The level of the VIDEO signal is 0 – 4V in normal mode and 0 – 5V in highlight mode.

All attribute data pass through a certain number of gates and synchronization is obtained at the time of output.

RVS	Reverse
CSR	Cusor
SECRET	Secret (Invisible)
BLINK	Blink
AT-BLINK	Attribute blink
BLANK	Blank
HILT	High light (Intensify)

Table 5-4 Attribute data

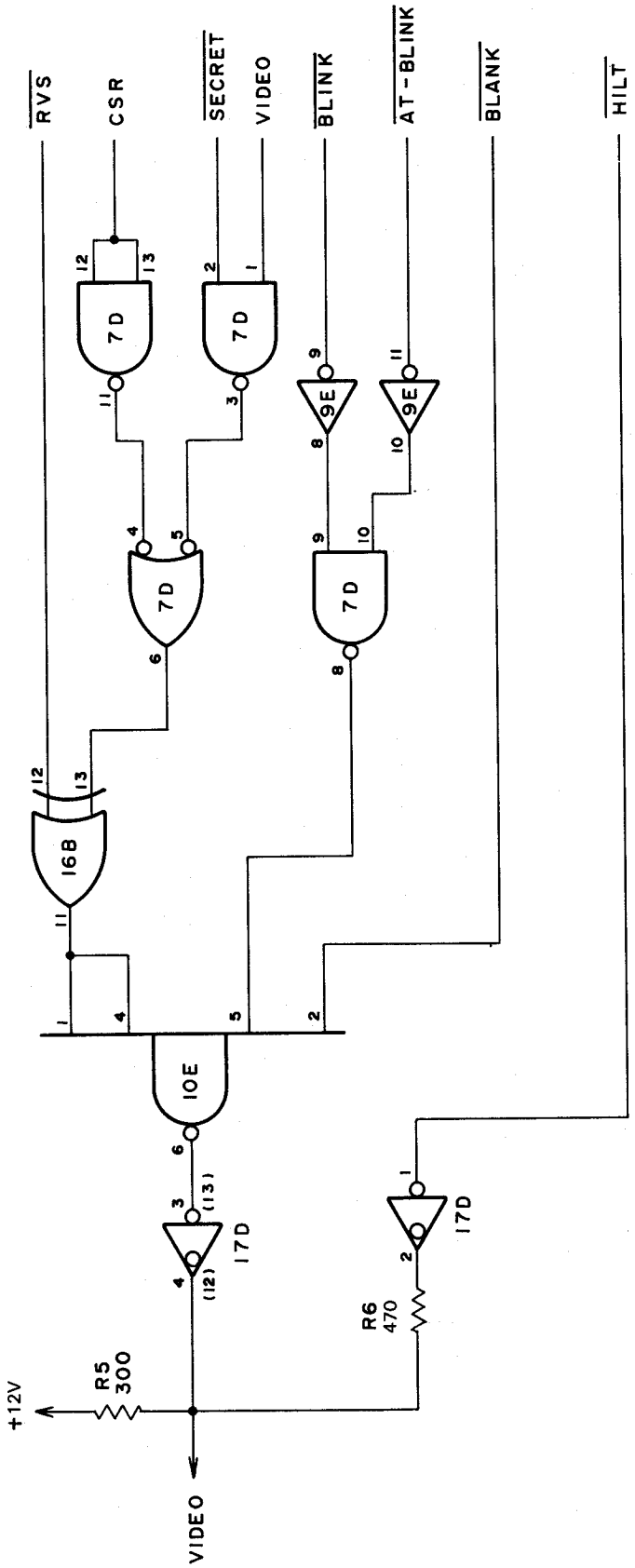


Fig. 5-27 ATTRIBUTE LOGIC CIRCUIT

5.10 Magnified Display (draw) Circuit

5.10.1 Timing diagram

It is possible to display characters and graphic figures which are magnified as many times as an integer multiple of 1 to 16. In this mode, display addresses are generated as shown in Fig. 5-5.

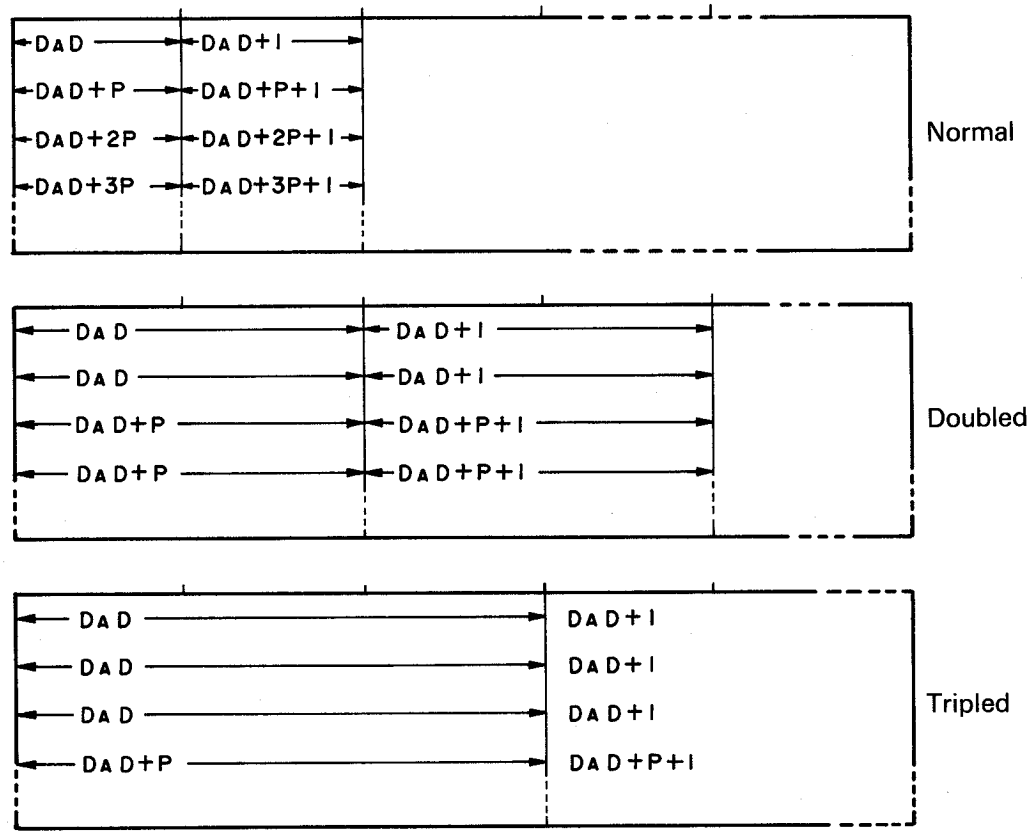


Table 5-5

Horizontal display address cycle is changed according to the magnification factor designated.
As shown in Fig. 5-28, the cycle of two clock signals (2CCLK) normally becomes four clock signals (2 × 2CCLK) during double-magnification time and six clock signals (3 × 2CCLK) during triple-magnification time.
At this time, output $\overline{RAS}$ rises to high level in magnified areas as shown in Fig. 5-28 to help the shift register, which generates serial video signals from V-RAM outputs, select timing of load clock generation.
In the vertical direction, line count is changed to display the same data.
Thus the GDC controls display address in units of word during magnified mode.
The circuit (see Fig. 5-29) working in magnified mode generates load and shift clocks and supplies the shift register with them.

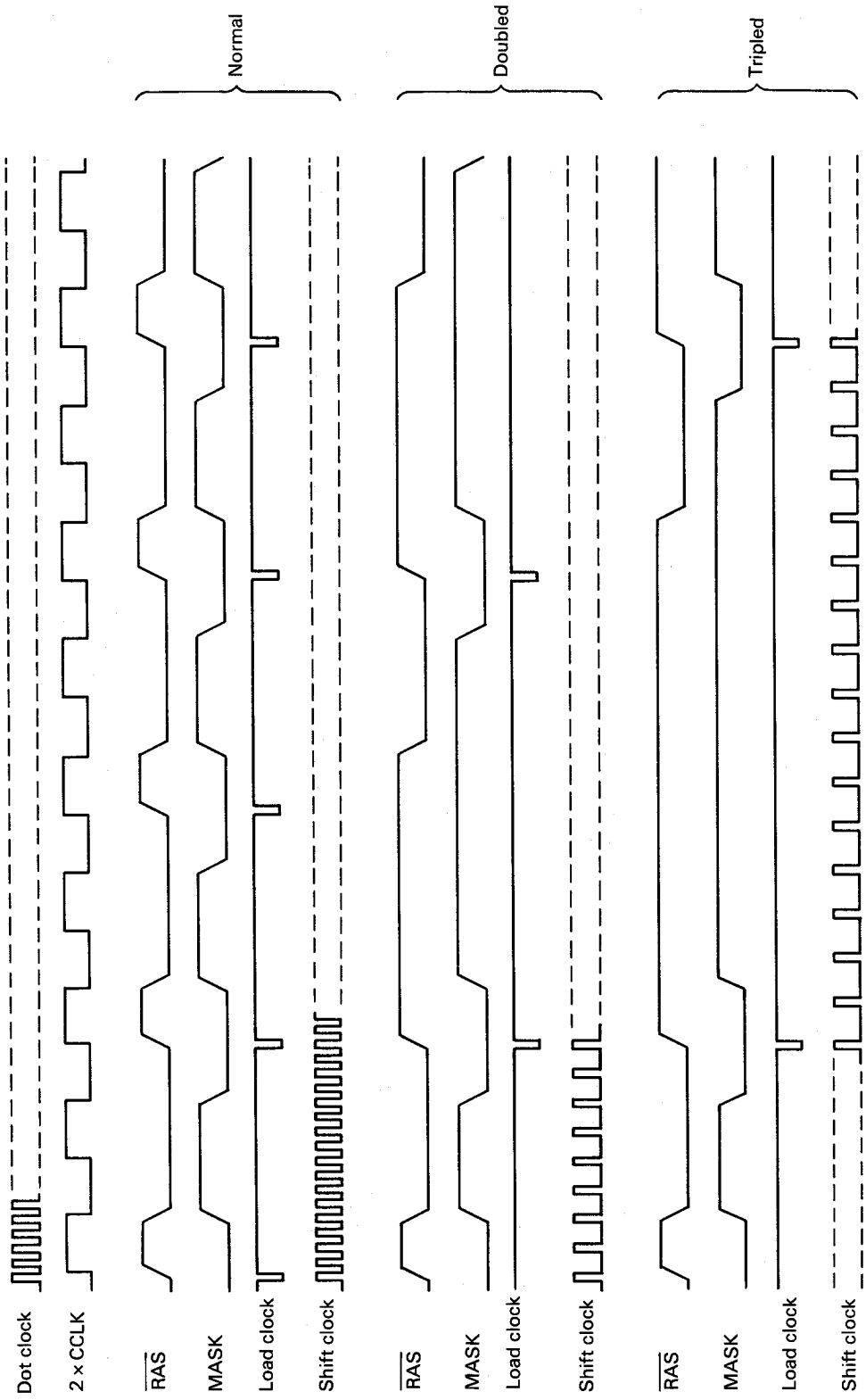


Fig. 5-28

5.10.2 Magnified Display Circuit

To display magnified data, it is necessary to vary the periods of the load and shift clock signals, which are supplied to the shift register, according to the magnification factor.

Display address is controlled by the GDC according to the magnification factor.

When a ZOOM command (46H) comes from the CPU, the GDC enters magnified display (draw) mode.

Then the magnification factor is set as a parameter in the least significant four bits of the data bus. (See Table 5-6)

Data	Magnification factor
0000	1
0001	2
0010	3
.	.
.	.
.	.
.	.
1101	14
1110	15
1111	16

Table 5-6 Magnification parameter

The data bus lines of the least significant four bits are connected to D flip-flop LS175(13A) and its $\overline{Q}$ outputs enter counter S161(13B) and LS163(14C).

When the magnification factor is two, for example, the parameter set in the data bus lines of the least significant four bits is "0001" and, therefore, the data entering the data input terminals of the counter S161(13B) and LS163(14C) is $Q_D\ Q_C\ Q_B\ Q_A = 1110$. S161(13B) operates, timed by dot clock of the GDC. Since the input data is now "1110", the subsequent clock signal triggers a pulse to develop at the RIPPLE-CARRY OUTPUT terminal and this pulse enters pin 3 of the subsequent NOR gate IC 15B.

The other input to the NOR gate (15B) is the inversion of the shift load signal of the shift register of the video signal. The ORed output of these signals returns to the LOAD terminal of S161(13B).

This signal is routed via inverter 14E to pin 1 of IC13E and, after NANDed with the dot clock supplied to pin 2, exits through pin 3 to shift register (5D and 5E) as shift clock.

Thus, when the magnification factor is two, the shift clock frequency is halved so that image size is doubled.

LS163(14C) generates clock signal for the line counter of the character generator during character ZOOM mode. Like S161(13B), it generates RIPPLE CARRY OUTPUT signal according to the magnification factor. To the LOAD input terminal of LS163(14C), the NANDed result of output C_A of LS163 and output Q of LS74(16C) generated according to CSR-IMAGE is supplied. This signal resets the LS163(14C) when its own C_A output is present or graphic mode is changed to character mode on the same screen, and counts up for every horizontal scanning. Signal C_A enters D flip-flop LS74(16C), whose output $\overline{Q}$ in turn enters pin 8 of IC15B. On the other hand, NANDed with BLANK signal, the output at pin 10 of IC15B becomes the clock signal of line counter LS161(1E). Thus, clock frequency controlled according to the magnification factor is supplied to LS161(1E) so that characters appear magnified in magnified display mode.

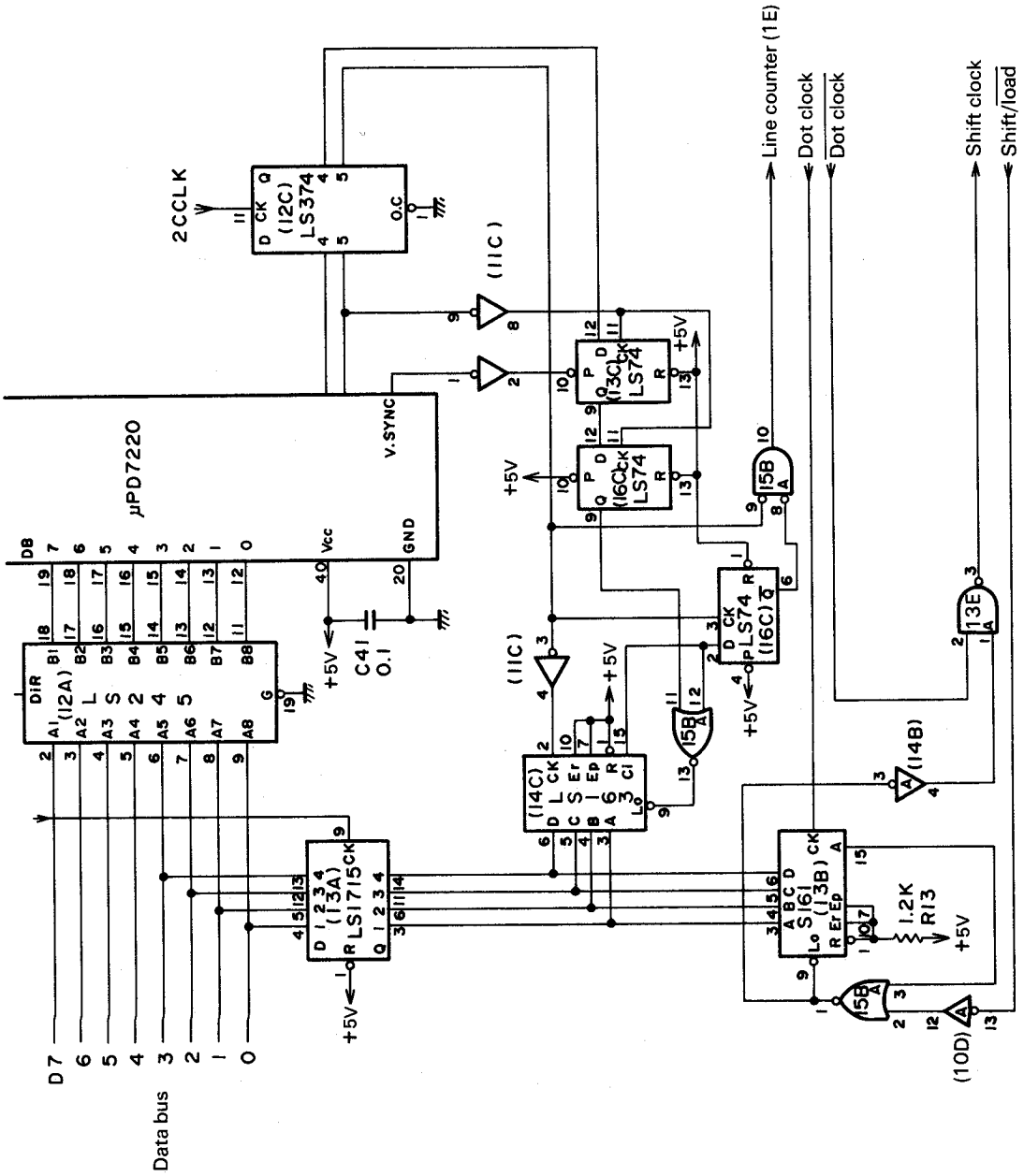


Fig. 5-29 Magnified display circuit

5.11 Sync Signal Generator

The μPD7220 generates the vertical and horizontal sync signals for the CRT.

Fig. 5-30 shows the circuit through which the sync signals are supplied to the CRT. These signals are output at the same timing as the address and cursor signals of V-RAM and routed through a latch circuit (D flip-flop) to normalize the jitter at the output to the CRT.

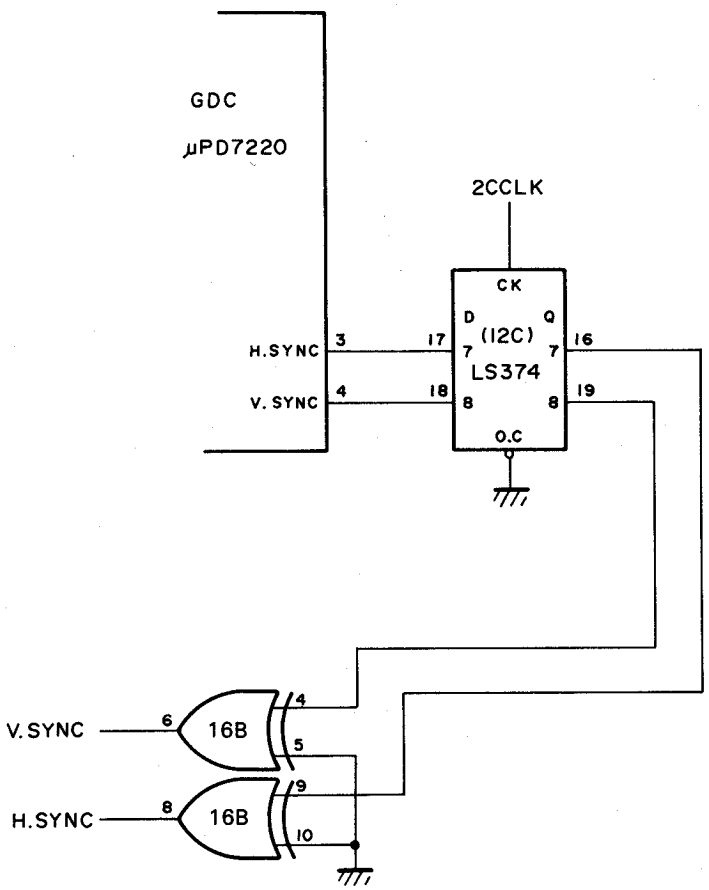
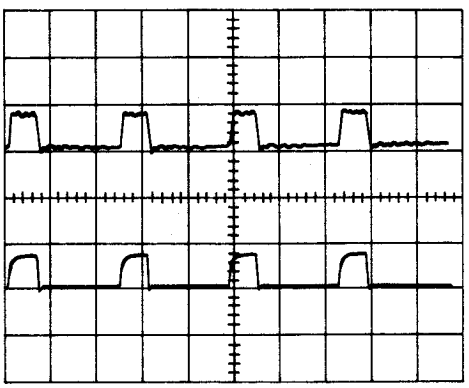
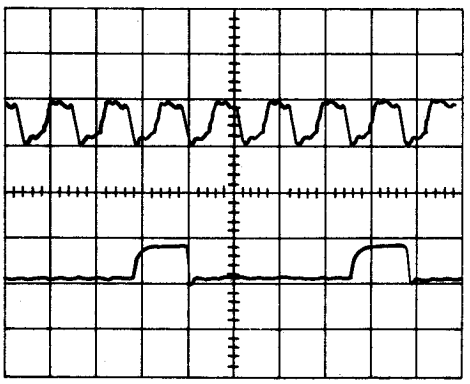


Fig.5-30 Circuit of sync signal



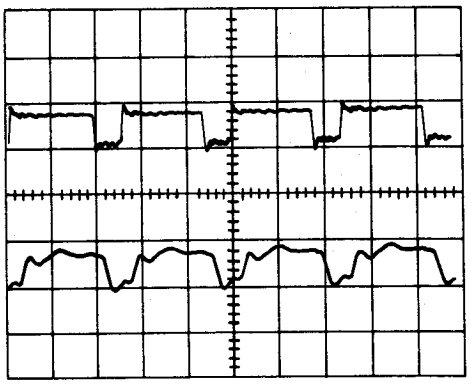
Upper: $\overline{RAS}$
Lower: IC12D (pin 9)
(Sweep 0.2 μsec 5V/div)

Fig. 5-31



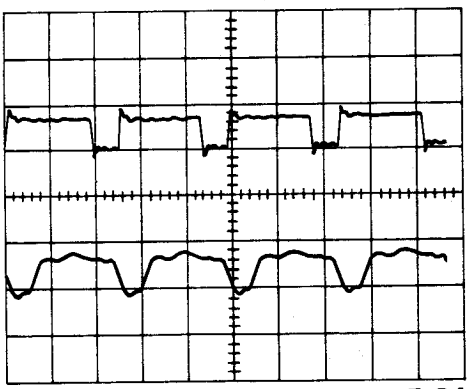
Upper: IC12D (pin 13)
Lower: IC12D (pin 9)
(Sweep 0.1 μsec 5V/div)

Fig. 5-32



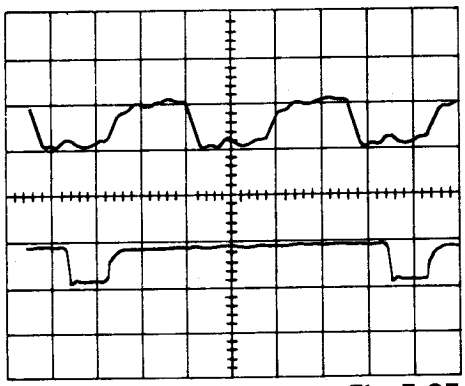
Upper: IC9D (pin 11)
Lower: IC10D (pin 9)
(Sweep 0.2 μsec 5V/div)

Fig. 5-33



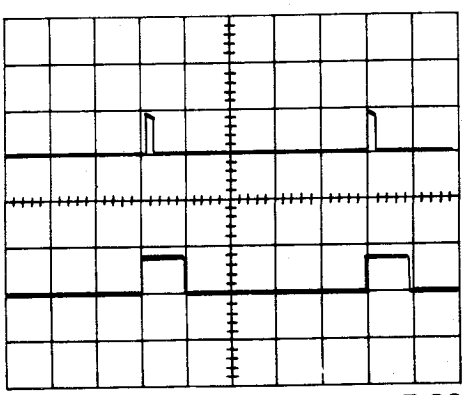
Upper: IC9D (pin 11)
Lower: IC10D (pin 5)
(Sweep 0.2 μsec 5V/div)

Fig. 5-34



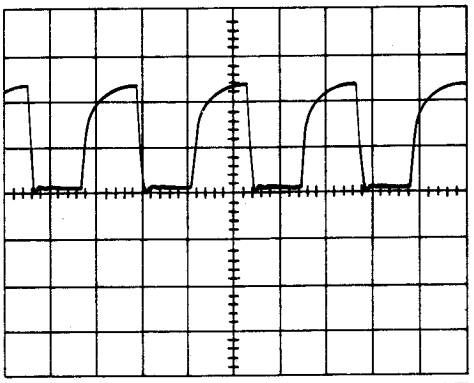
Normal
Upper: 2CCLK
Lower: S/L
Sweep 0.2 μsec 5V/div

Fig. 5-35



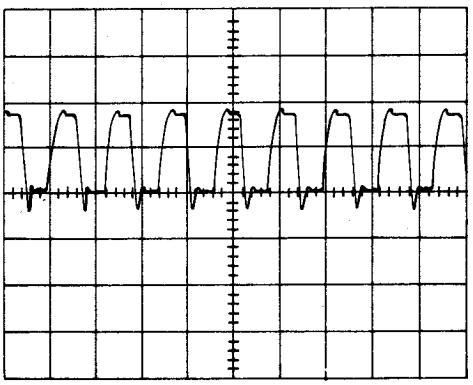
Upper: IC9D (pin 11)
Lower: IC10D (pin 9)
(Sweep 0.2 μsec 5V/div)

Fig. 5-36



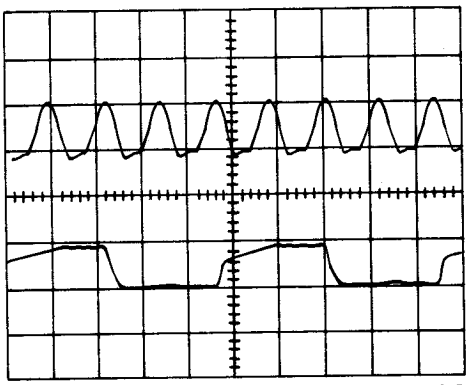
2CCLK
(Sweep 0.1 μsec 5V/div)

Fig. 5-37



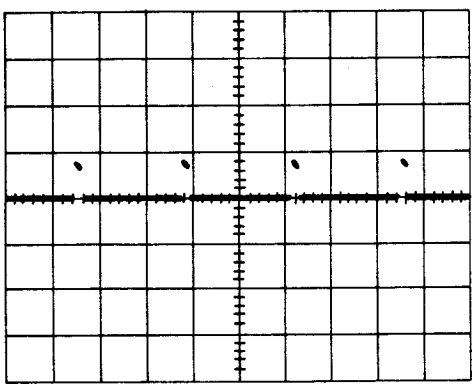
DOT CLK
(Sweep 50 nsec 2V/div)

Fig. 5-38



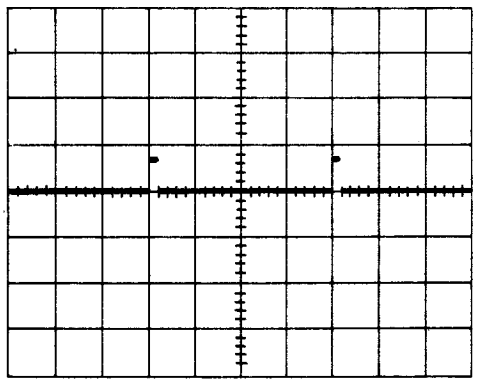
Upper: DOT CLK
Lower: 2CCLK
(Sweep 50 nsec 5V/div)

Fig. 5-39



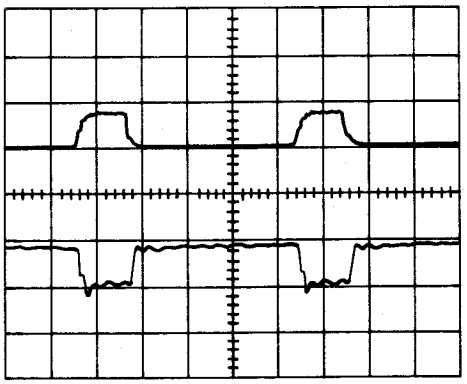
H. SYNC
(Sweep 20 μsec 5V/div)

Fig. 5-40



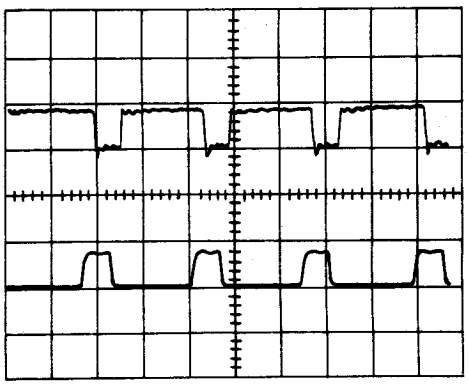
V. SYNC
(Sweep 2 nsec 5V/div)

Fig. 5-41



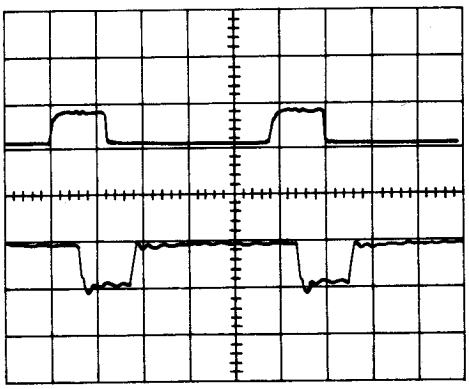
Upper: IC8C (pin 1)
Lower: IC9C (pin 1)
(Sweep 0.1 μsec 5V/div)

Fig. 5-42



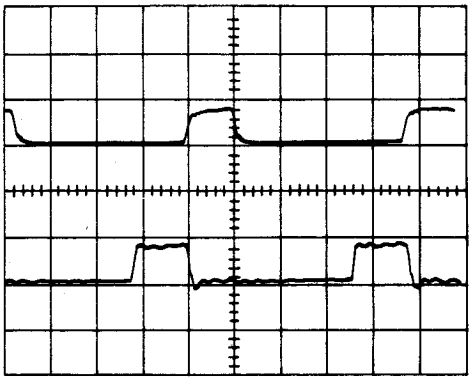
Upper: IC9C (pin 1) O.C
Lower : RAS
(Sweep 0.2 μsec 5V/div)

Fig. 5-43



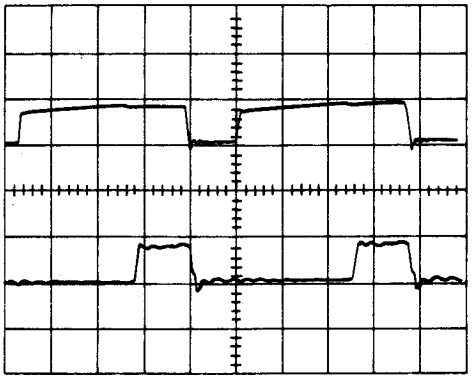
Upper: RAS
Lower: IC9C (pin 1) O.C
(Sweep 0.1 μsec 5V/div)

Fig. 5-44



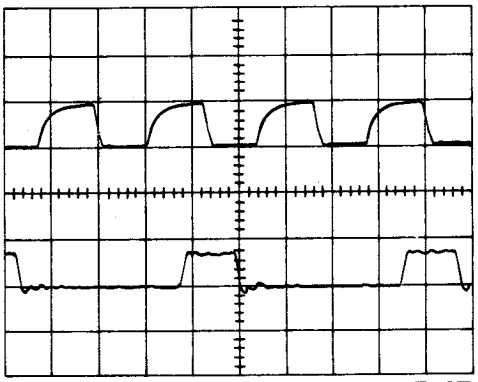
Upper: IC8C (pin 1) O.C
Lower: IC8C (pin 11) ENABLE
(Sweep 0.1 μsec 5V/div)

Fig. 5-45



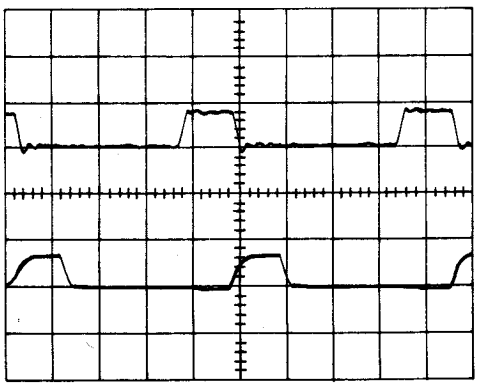
Upper: IC9C (pin 1) O.C
Lower: IC9C (pin 11) ENABLE
(Sweep 0.1 μsec 5V/div)

Fig. 5-46



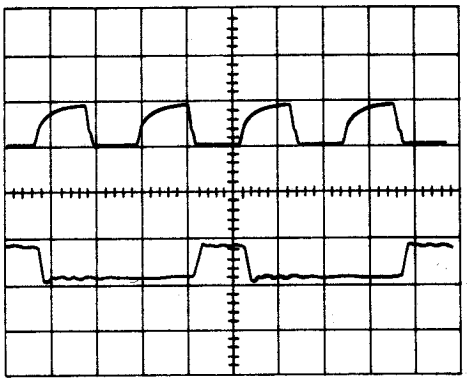
Upper: 2CCLK
Lower: RAS
(Sweep 0.1 nssec 5V/div)

Fig. 5-47



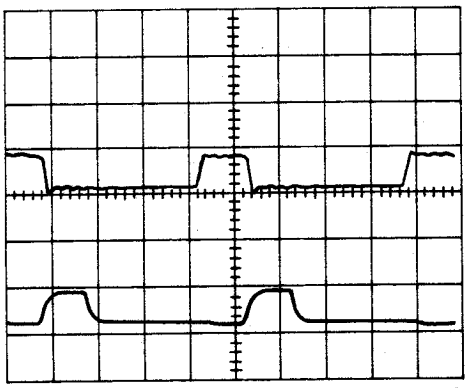
Upper: RAS
Lower: CAS
(Sweep 0.1 μsec 5V/div)

Fig. 5-48



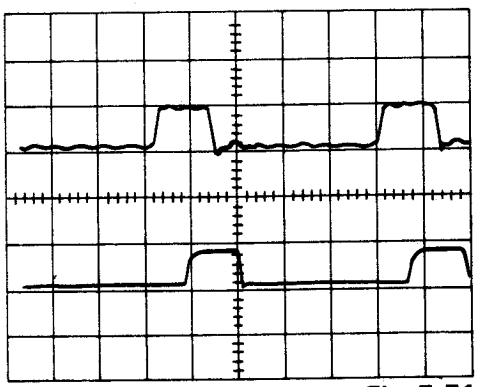
Upper: 2CCLK
Lower: RAS
(Sweep 0.1 μsec 5V/div)

Fig. 5-49



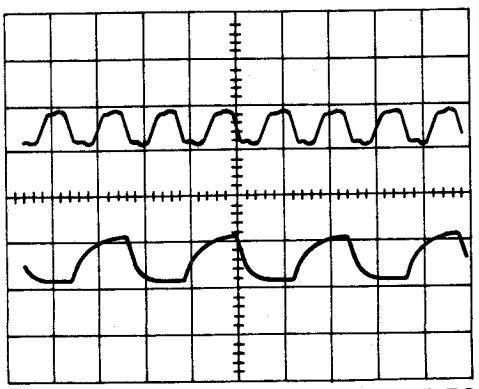
Upper: RAS
Lower: CAS
(Sweep 0.1 μsec 5V/div)

Fig. 5-50



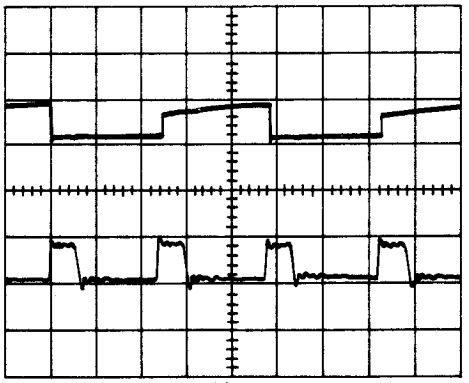
Upper: IC12D (pin 11) J
Lower: IC12D (pin 9) Q
(Sweep 0.1 μsec 5V/div)

Fig. 5-51



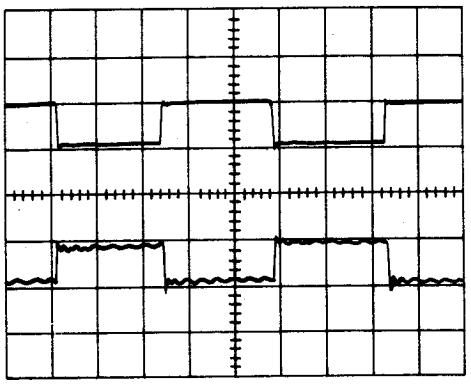
Upper: IC12D (pin 1) CK
Lower: IC12D (pin 5) 2CCLK
(Sweep 0.1 μsec 5V/div)

Fig. 5-52



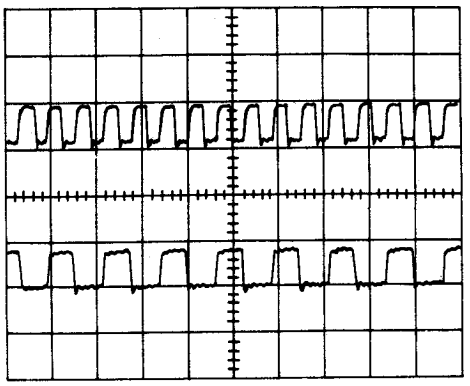
Lower: IC14D (pin 8) $\overline{Q}$
Lower: IC14D (pin 11) CK
(Sweep 0.2 μsec 5V/div)

Fig. 5-53



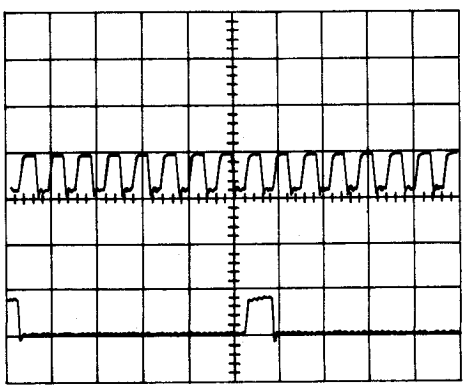
OUTPUT CONTROL
Upper: IC3C (pin 1)
Lower: IC5C (pin 1)
(Sweep 0.2 μsec 5V/div)

Fig. 5-54



ZOOM (× 2)
Upper: IC13E (pin 2)
Lower: IC13E (pin 1)
(Sweep 0.1 μsec 5V/div)

Fig. 5-55



ZOOM (×8)
Upper: IC13E (pin 2)
Lower: IC13E (pin 1)
(Sweep 0.1 μsec 5V/div)

Fig. 5-56