CHAPTER 4
Q10SYM BOARD

CONTENTS

4.1 Reset Circuit

A reset signal is supplied to the main CPU μPD780 and peripheral ICs in the following four cases.

(1) Power on reset.
(2) Reset by RESET switch (Manual reset).
(3) Reset from external option I/O.
(4) Power down reset.

Receiving the reset signal, the CPU sets the program counter (PC) to 0 and holds the address bus and data bus at high impedance during reception of the reset signal.

Reset signal supply circuits are described below.

(1) Power on reset circuit

When the power is turned on, +5V is supplied to the emitter of transistor Q3. At the same time, this voltage is lowered by resistor R78 giving the potential difference between the emitter and base of transistor Q3 to turn it on.

This voltage is applied to the positive side of capacitor C3 to charge it, and then set the input of pin 9 of IC23E to high level.

The reset time by power on depends on the time constants of capacitor C3 and resistor R122, and in this system is 0.3 ~ 0.5 seconds.

That is, since the input of pin 9 of IC23E is at low level after the power is turned on and at the beginning of capacitor charging, the gate input of IC21M is applied to pin 2 through the two-stage inverter IC23E.

Therefore, the output of pin 12 of IC21M or the reset signal to the CPU is set to low level, resetting the CPU and peripheral ICs.

(2) Reset by RESET switch (Manual reset)

When the RESET switch is turned on, the D-type FFs of IC24M are reset and the Q-output is set to Low level. By the next CK-input to IC24M, Q-output is set to high level. This signal is applied to the B-terminal of IC24K as its input. IC24K outputs a single shot signal according to the externally mounted CR. In this case, since the input to the A-terminal is GND, a signal of 5 ~ 10μsec at low level is generated as a Q-output, which is applied to pin 13 as a gate input of IC21M, providing a signal to reset the CPU. This circuit is needed to hold contents of D-RAM.

(3) Reset by external I/O

A reset signal from the extended external I/O is accepted. The reset signal is applied to pin 1 of IC21M, providing a reset signal to the CPU or peripheral ICs.

(4) Power down reset

By the power down signal and the output from pin 10 of IC23E, a low level signal is output with a delay of about 10msec after detection of the PWD signal.

Power down reset is made by this signal.

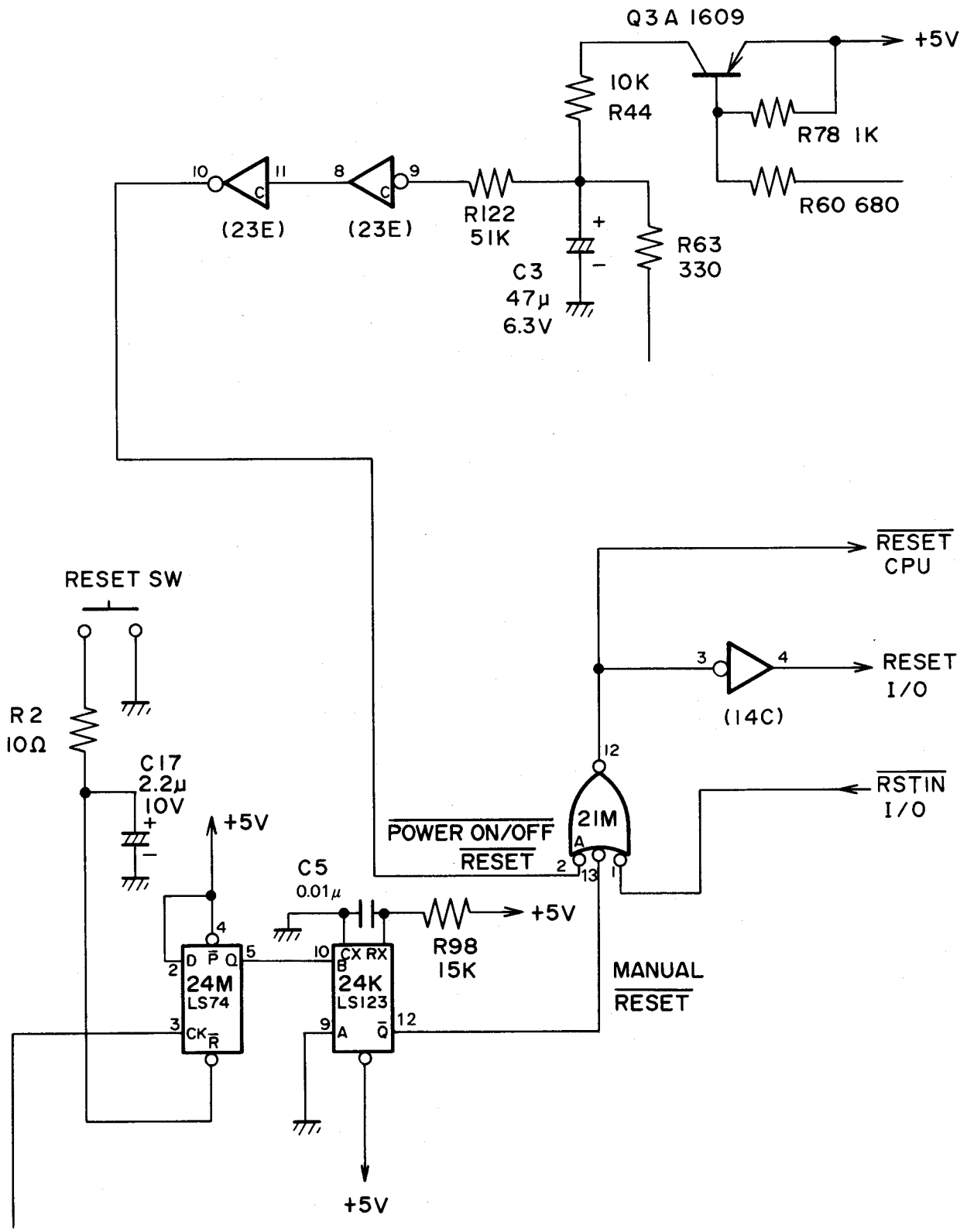


Fig. 4-1 Reset circuit

4.2 PWD Signal Supply Circuit

When the supply voltage drops to lower than about 80V AC in the 100V AC channel and 160V in the 200V channel, the PWD signal is detected by the signal of low to high level from the power supply circuit Q10PS board.

When the PWD signal is set to high level, the base voltage of the transistor Q3 rises to high level to cut it off. On the other hand, with the PWD signal, the inverter output at pin 6 of IC21C is set to low level, making an interrupt request to the interrupt input terminal IR0 of the interrupt controller μPD8259 (12E) through the inverter output at pin 10 of IC23C.

This interrupt made by power down is programmed in the interrupt controller as an interrupt with the highest priority, and supplies an interrupt signal for the CPU.

Receiving this interrupt signal, the CPU selects C-MOS RAM and activates the $\overline{CS1}$ terminal of C-MOS RAM μPD449.

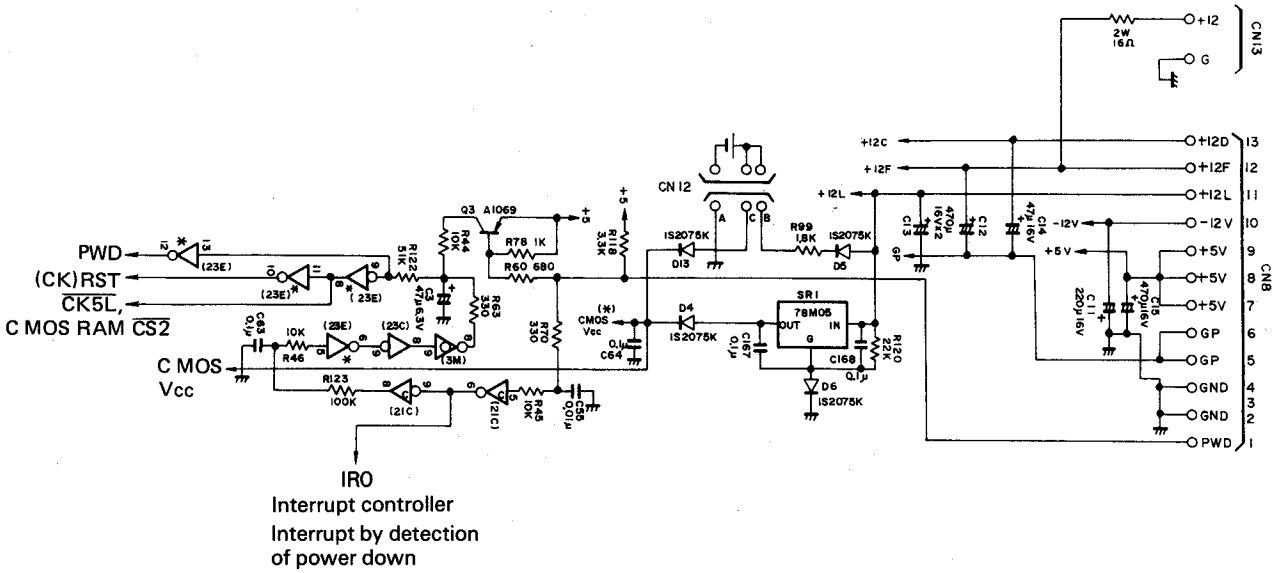


Fig. 4-2 PWD signal supply circuit

Further, the inverter output of IC21C supplies a low level signal to the output of pin 8 of IC3M after a delay of 10msec through the delay circuit comprising four inverters, R123 (100 kΩ) and C63 (0.1 μF).

This delay circuit prevents the CPU from being reset due to momentary power down.

Receiving this low level signal, the output of pin 8 of the inverter IC23E is set to high level.

This output is connected to the $\overline{CS2}$ terminal of C-MOS RAM μPD449, and before it is set to high level by detection of the PWD signal, the signal of the $\overline{CS1}$ is set to low level. Thus, the C-MOS RAM is activated and the data of each register or stack pointer is written.

Thereafter, by detection of the PWD signal, the signal of $\overline{CS2}$ is set to high level by the battery backup of IC23E, and the C-MOS RAM is separated from the system to preserve the data.

Further, the PWD detection signal supplies a PWD signal to an external device from the inverter output of pin 12 of IC23E, and a $\overline{RESET}$ signal for the CPU and peripheral I/Os from the output of pin 10 of IC23E.

These signals are shown in Fig. 4-3.

The $\overline{CS2}$ signal is re-set to low level when the power is turned on. Thus, the contents of C-MOS RAM are read by setting the $\overline{CS1}$ signal to low level by selecting the C-MOS by the I/O select signal from the CPU.

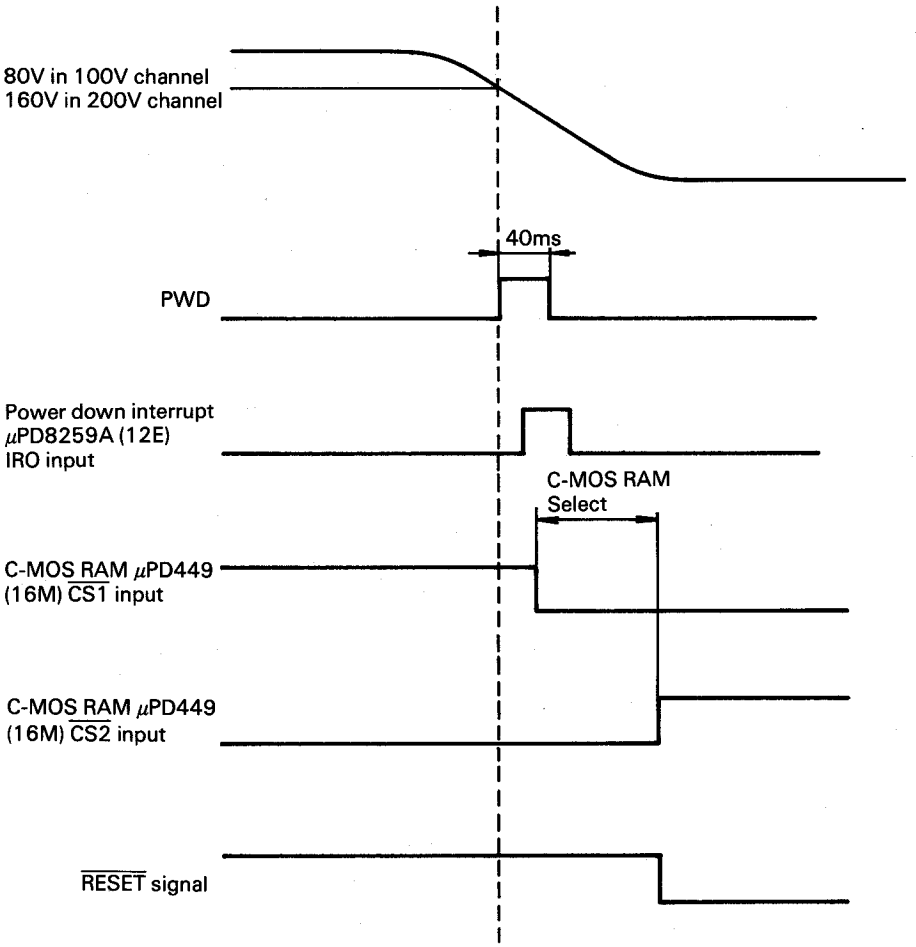


Fig. 4-3

4.3 C-MOS IC Power Supply Circuit

When the AC power is turned off, the C-MOS IC is backed up by the NiCd battery (3.6V, 90mAh). When the AC power is turned on, +5V is provided from the +12V supplied from the power supply Q10PS board through the series regulator 78M05 (SR1) and supplied to the C-MOS IC, because the C-MOS IC requires a very stable power supply.

At this time, the diode D4 functions to prevent reverse current from the NiCd battery at power down.

Diode D6 is inserted between the regulator GND terminal and GND line to raise the regulator potential by about 0.6V for ensuring +5V in the output in order to compensate the voltage drop by diode D4.

The NiCd battery is charged by the +12V line through diode D5 (1S2075K) and resistor R99 (1.8kΩ).

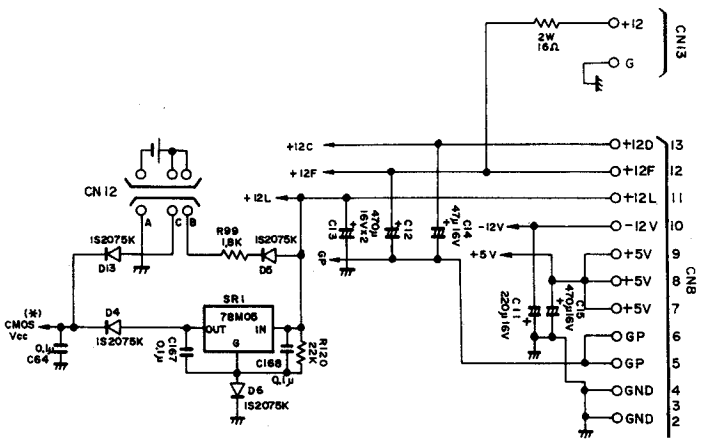


Fig. 4-4

4.4 System Clock Supply Circuit

The system clock supply circuit of Q10SYM board is shown in Fig. 4-5. The CPU μPD780 applies the original oscillation of 15.9744 MHz to the INPUT A terminal of the 4-bit binary counter LS93 and its output or Q_A output to the INPUT B terminal. Thereby it is operated by the 4-divided clock of 3.9936 MHz from the Q_B terminal.

This system clock is also supplied to the flip-flop which controls the pulse width and position.

The Q_C output which is 8-divided frequency of the original oscillation supplies a clock to the programmable interval timer 8253 (14E/16E).

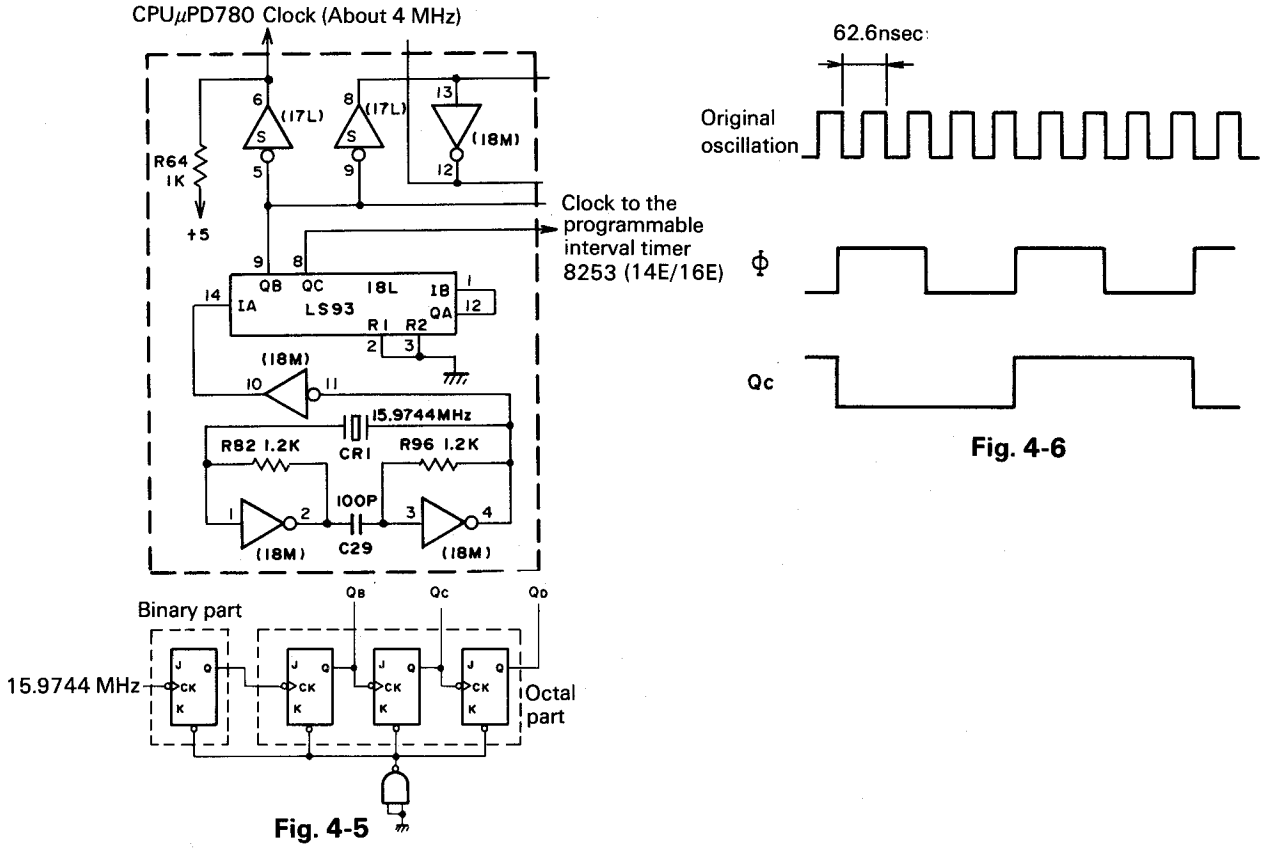


Fig. 4-6

Fig. 4-5

4.5 I/O and Memory Read/Write Signal Supply Circuit

The CPU μPD780 has 64K bytes, 0000H ~ FFFFH as a memory address and 1K port, 00 ~ FFH as an I/O address.

Access to each address and port is available with the following four methods.

(1) Reading from I/O
(2) Writing into I/O
(3) Reading from memory
(4) Writing into memory

In the μPD780, the following four signal lines are combined by the gate of the circuit shown in Fig. 4-7, thereby supplying the signals of (1) ~ (4) above.

(a) $\overline{IORQ}$: Specifies I/O.
(b) $\overline{MREQ}$: Specifies memory.
(c) $\overline{RD}$: Read timing.
(d) $\overline{WR}$: Write timing.

Therefore, the above signal lines become as follows.

(1) $\overline{IORQ} \cdot \overline{RD} \rightarrow \overline{IORD}$
(2) $\overline{IORQ} \cdot \overline{WR} \rightarrow \overline{IOWR}$
(3) $\overline{MREQ} \cdot \overline{RD} \rightarrow \overline{MERD}$
(4) $\overline{MERQ} \cdot \overline{WR} \rightarrow \overline{MEWR}$

These signals are output through the 3-state line buffer S241 (23J). The S241 (23J) has the G-signal input terminal to determine the state of the output signal of the Y-terminal: the input signal of S241 (23J) is output when the G-signal level is high, and the output of S241 (23J) is in the high impedance state when the G-signal level is low.

The G-signal is supplied by the gate made by IC21E shown in Fig. 4-7.

To pin 9 of IC21E, the $\overline{\text{BUSAK}}$ signal from the CPU is connected via the inverter (IC22H). When the $\overline{\text{BUSAK}}$ signal is at high level, that is, the system address and data bus can be used by the CPU only, S241 (23J) is permitted to output a signal.

In other words, when the $\overline{\text{BUSAK}}$ signal is active during DMA transmission, output of signals (1) ~ (4) from the CPU is inhibited.

To pin 8, which is another input of gate IC21E, an interrupt acknowledge signal at active $\overline{\text{IORQ}}$ signal output in the M1 cycle is connected.

When the interrupt acknowledge signal applied to pin 8 of IC21E is active and at high level, the G-terminal of S241 (23J) becomes low level. Thus, the output of S241 is set to high impedance, inhibiting the CPU from outputting signals (1) ~ (4) to an external device.

To release this interrupt processing, an $\overline{\text{WR}}$ signal is supplied from the CPU. When the $\overline{\text{WR}}$ signal is made active, the input to pin 8 of IC21E is set to low level and a high level signal is supplied to the 2G terminal of S241 (23J). The timing chart is shown in Fig. 4-8.

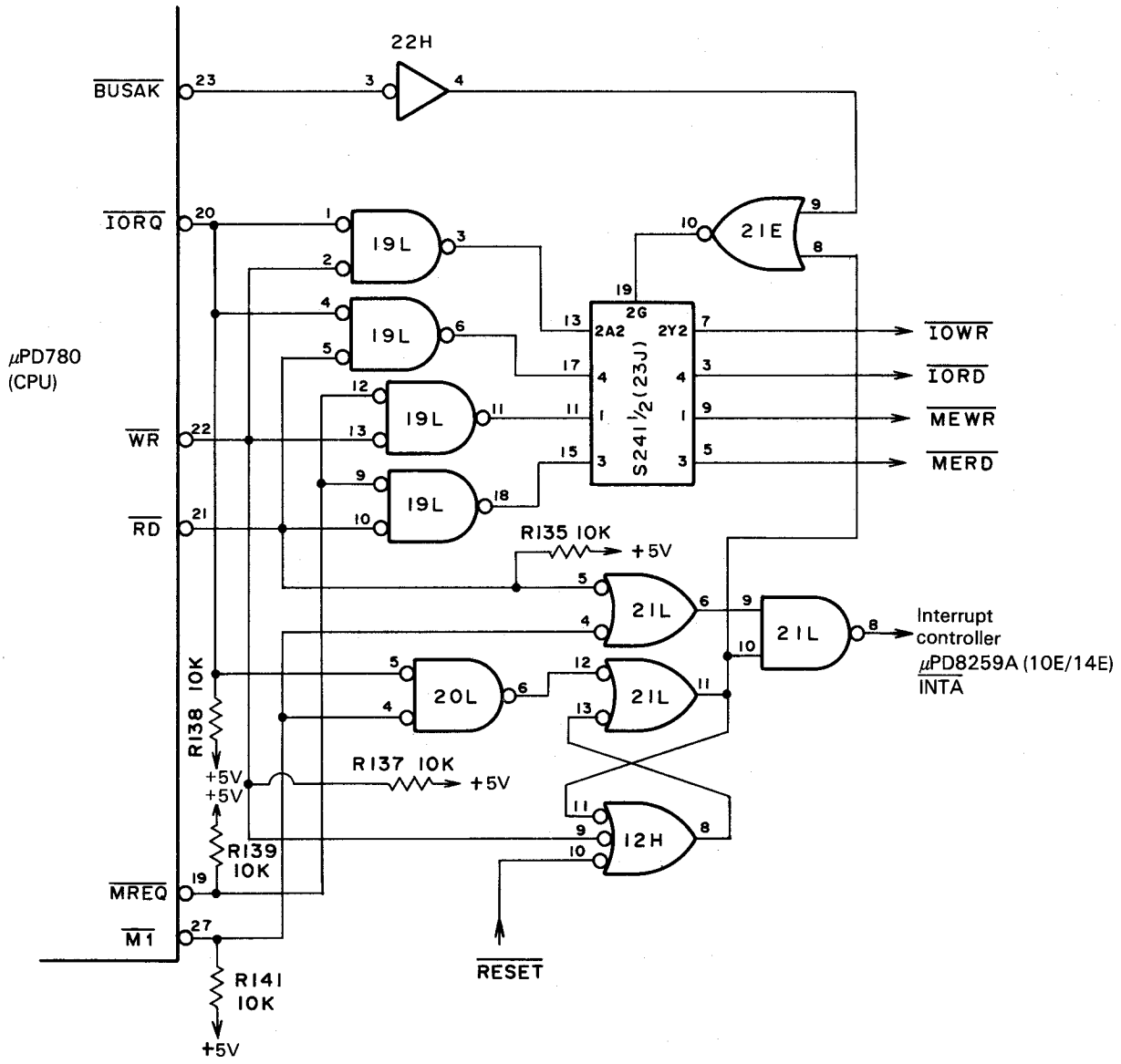


Fig. 4-7 Circuit to supply read/write signal to I/O and memory

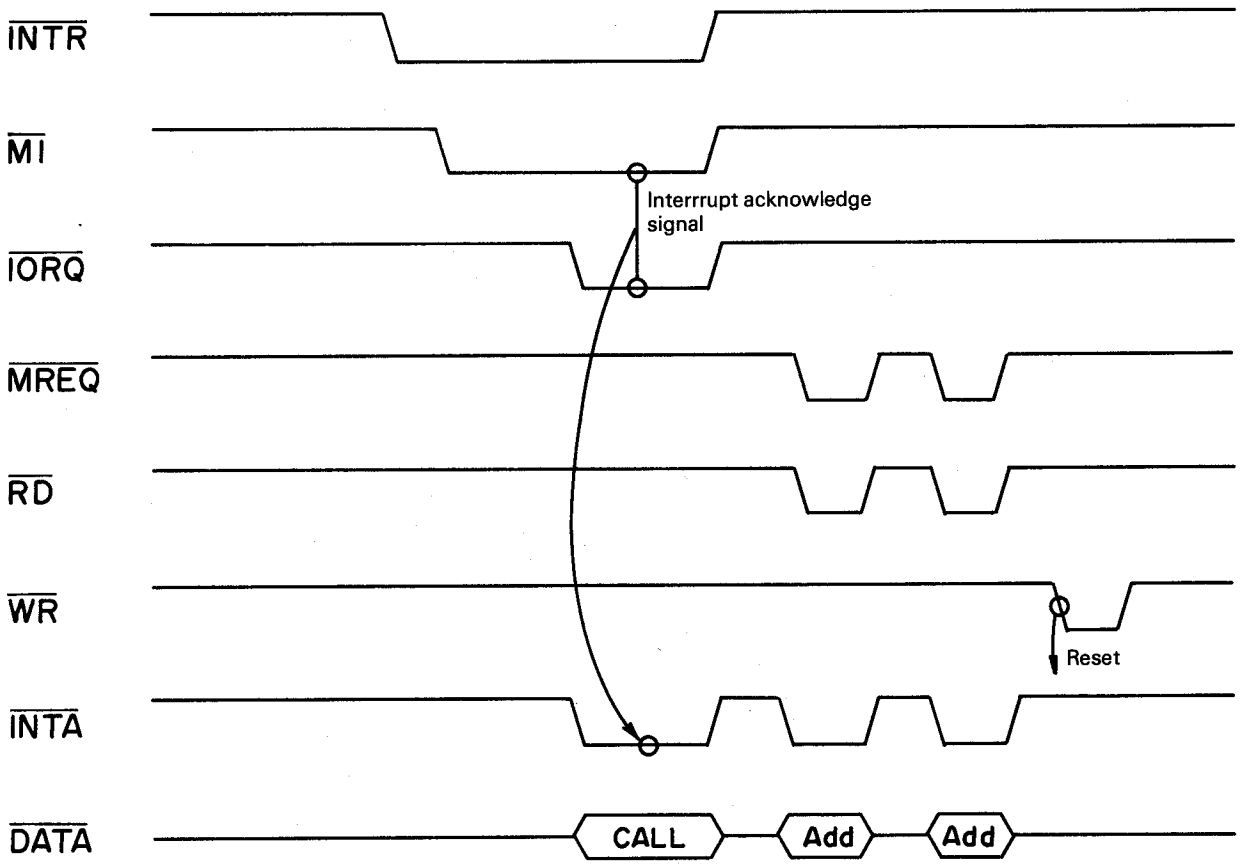


Fig. 4-8 Interrupt acknowledge signal timing

▶ $\overline{\text{IOWR}}$ Signal Supply Circuit

As described in the preceding paragraph, the write ($\overline{\text{WR}}$) signal to the I/O device can be supplied by taking AND of $\overline{\text{IORQ}}$ signal of the CPU and $\overline{\text{WR}}$ signal.

The timing of the output data D0 ~ 7 from CPU and $\overline{\text{IOWR}}$ signal is shown in Fig. 4-10.

The output data is sampled at the leading edge of the $\overline{\text{IOWR}}$ signal.

However, when an I/O device is provided by an external option, the sampling timing for data writing needs to be set to the ensured time of data output in order to guarantee the writing data.

The circuit shown in Fig. 4-9 is used for this purpose, which reduces the $\overline{\text{IOWR}}$ signal by one clocks and makes its leading edge earlier and performs data writing.

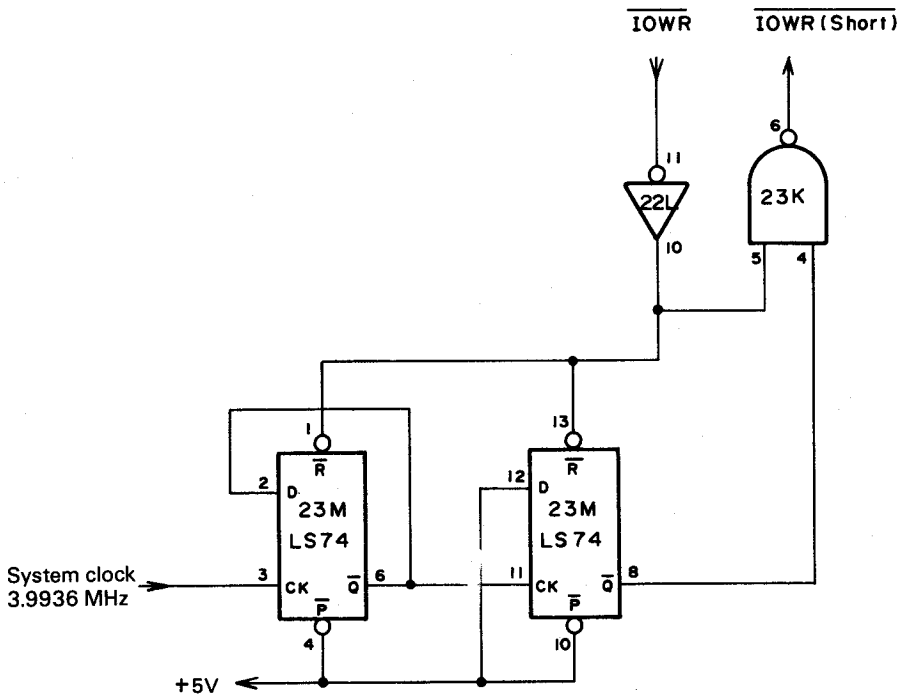


Fig. 4-9

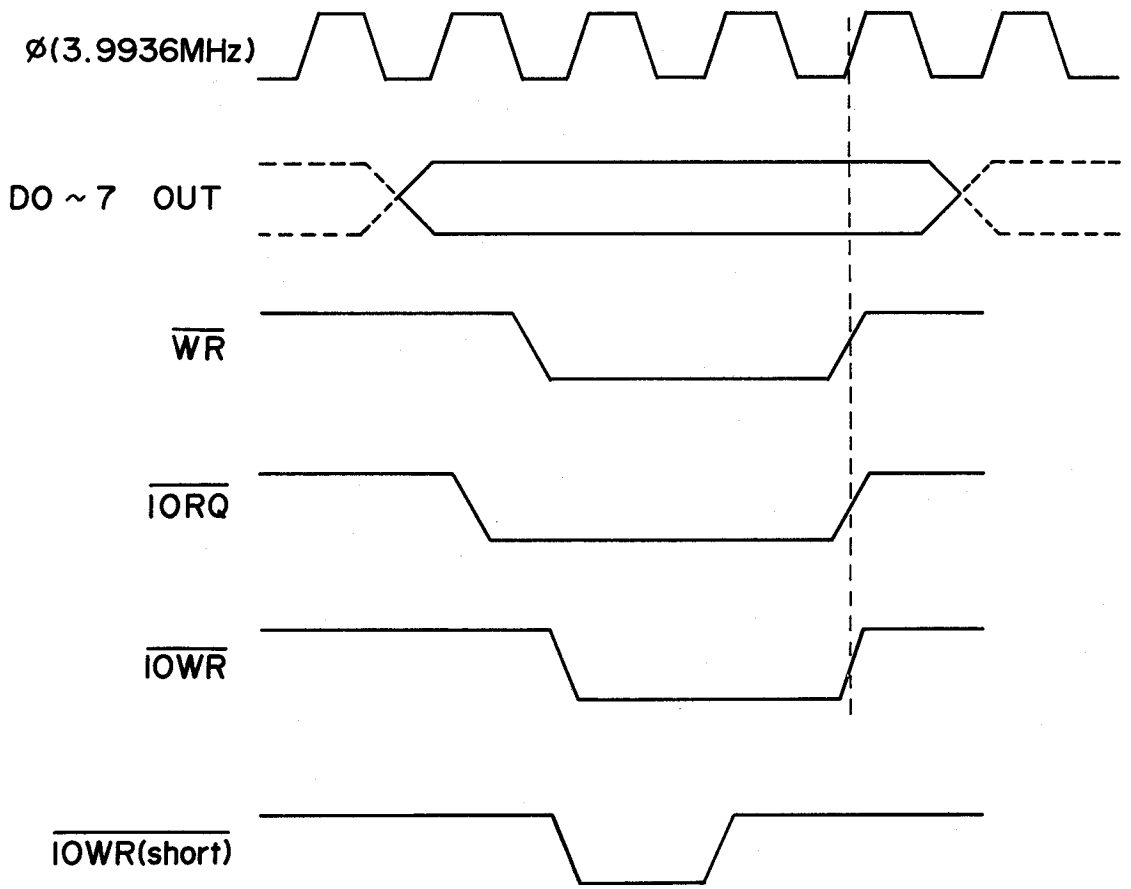


Fig. 4-10

4.6 Data Bus line Signal Direction Selector (LS245 (14K))

D-RAM, I/O device and external memory are connected through the data bus line for the CPU as shown in Fig. 4-11.

In normal operation, data is transferred from the CPU to the I/O device or external memory. However, in the DMA transfer mode, the data transfer direction needs to be changed to the CPU in the following cases (1) ~ (6).

(1) CPU ← I/O (Read)
(2) CPU ← External memory (Read)
(3) D-RAM ← I/O device (Read)
(4) I/O device (Write) ← External memory (Read) } DMA
(5) External memory ← I/O device (Read)
(6) CPU (Int) ← 8259 (Read)

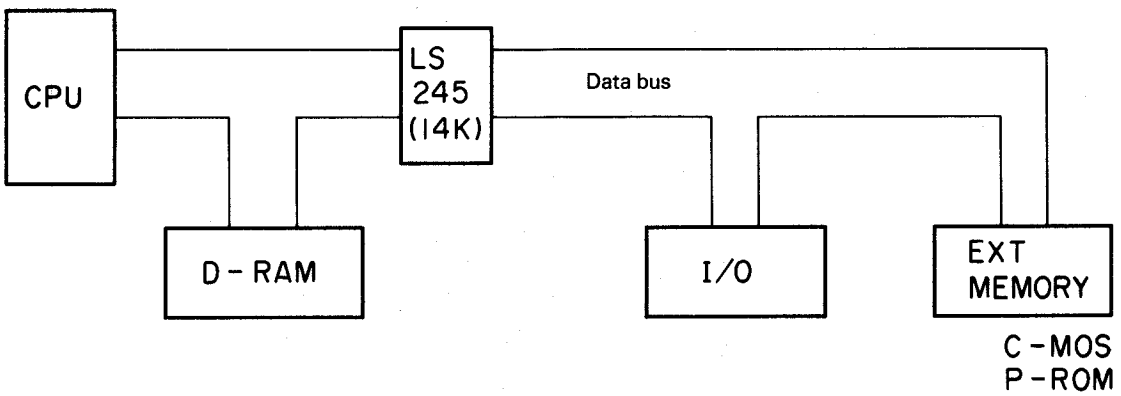


Fig. 4-11 Data bus line and peripheral devices

So, in this circuit, a 3-state bus transceiver (LS245) is inserted to change the data bus line signal direction according to the status of data transfer.
LS245 has DIR signal terminal to change the bus line direction. Data is transferred from the CPU to the I/O device or external memory when the DIR signal is low, and vice versa when the signal is high.
As shown in Fig. 4-12, in any one of the above states (1) to (6), AND is taken by IC20F in this circuit and a high level signal is sent to the DIR terminal of LS245.

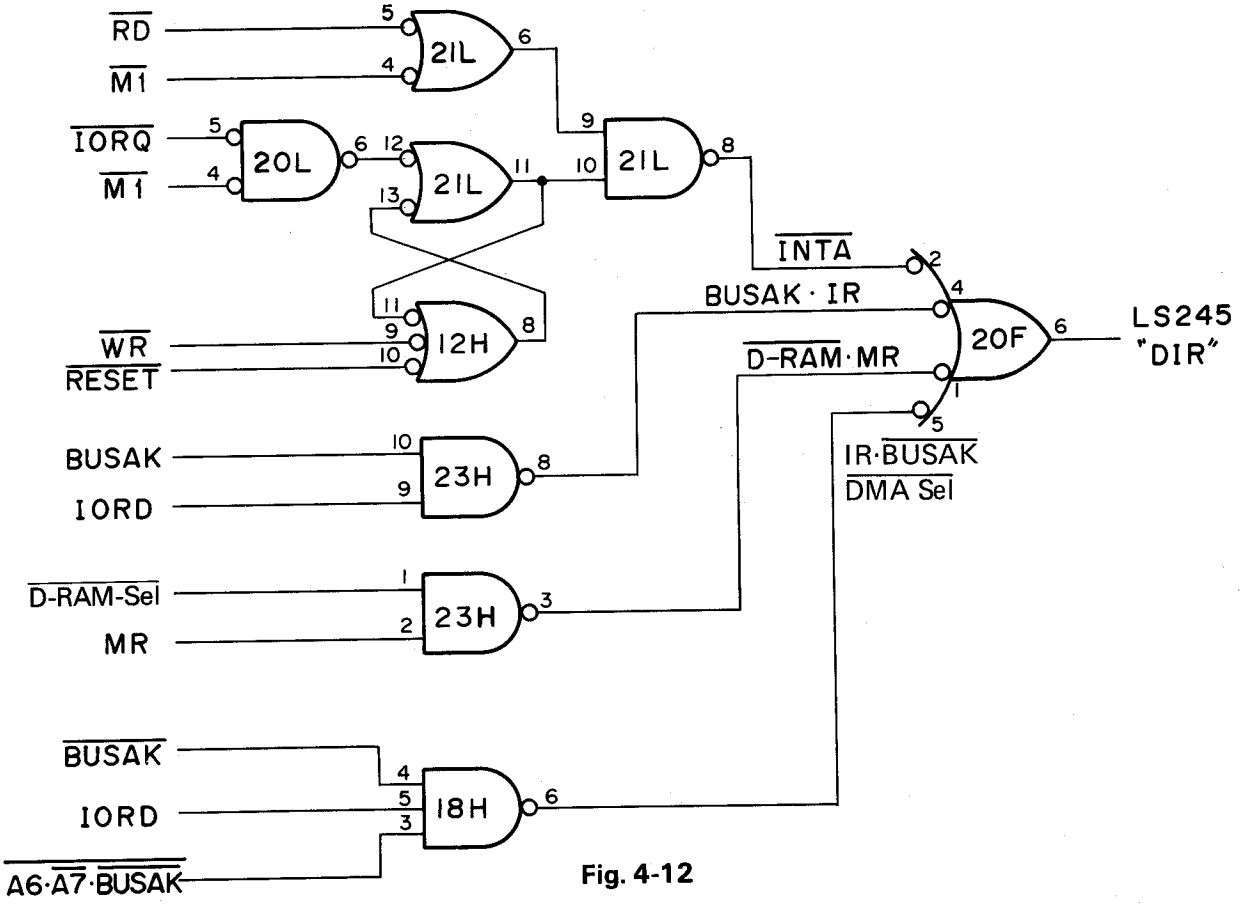


Fig. 4-12

(a) Input signal of pin 2 of IC20F
The same signal as the $\overline{\text{INTA}}$ signal of the interrupt controller 8259A is entered. This is an interrupt acknowledge signal of CPU against the interrupt request from the peripheral device, and made from the $\overline{\text{IORQ}}$ signal and $\overline{\text{RD}}$ signal output from the CPU accompanied by the M1 (machine cycle 1) signal. This signal is reset by the $\overline{\text{WR}}$ signal or $\overline{\text{RESET}}$ signal. Therefore, it gives a direction signal in case of (6).

(b) Input signal of pin 4 of IC20F
AND of $\overline{\text{BUSAK}}$ and $\overline{\text{IORD}}$ signals from the CPU is entered.
The $\overline{\text{BUSAK}}$ signal indicates that the CPU data bus, address bus and 3-state output control signal line are in the high impedance state and these buses can be used by the other device (I/O device).
The $\overline{\text{IORD}}$ signal indicates the read signal from the I/O device. Therefore, taking AND of these signals meets the data bus condition for D-RAM from the I/O device at DMA transfer or READ for an external memory.
Namely, this signal gives a direction signal in cases (3) and (5).

(c) Input signal of pin 1 of IC20F
This signal is composed of AND of the $\overline{\text{MR}}$ signal of the interrupt controller 8237 and the signal indicating selection of memory.
Therefore, pin 1 of IC20F is made active when the external memories including P-ROM and RAM of C-MOS are selected and the CPU and I/O devices read these memories.
This signal meets cases (2) and (4).

(d) Input signal of pin 5 of IC20F

$\overline{\text{IORD}}$, $\overline{\text{BUSAK}}$ and $\overline{\text{DMASel}}$ signals are applied to pin 5.

When the DMA is not selected and the CPU is read by the I/O device, this input signal is made active.

Therefore, this signal meets case (1).

4.7 External Option Bus Line Signal Direction Selector

The data bus direction in data transfer between the CPU or memory and external option is selected by the 3-state bus transceiver LS245 (8H). The DIR signal of LS245 (8H) releases the data bus from the external option toward CPU/memory when the signal level is high, and vice versa when it is low.

DIR signal	Data bus transfer direction
H	CPU/Memory → External option
L	External option → CPU/Memory

To meet these conditions, the DIR signal is supplied by the circuit shown in Fig. 4-13 at the hardware level.

Data transfer from the external option to CPU/memory is made in the following three cases.

(1) The memory is read by an external option memory.

(2) DMA transfer from an external option. (6 channels)

(3) Reading form external I/O.

The DIR signal provides the signal to meet these conditions through the gate composed of IC7K and IC9K.

Therefore, it is an output signal except when data is entered from an option card.

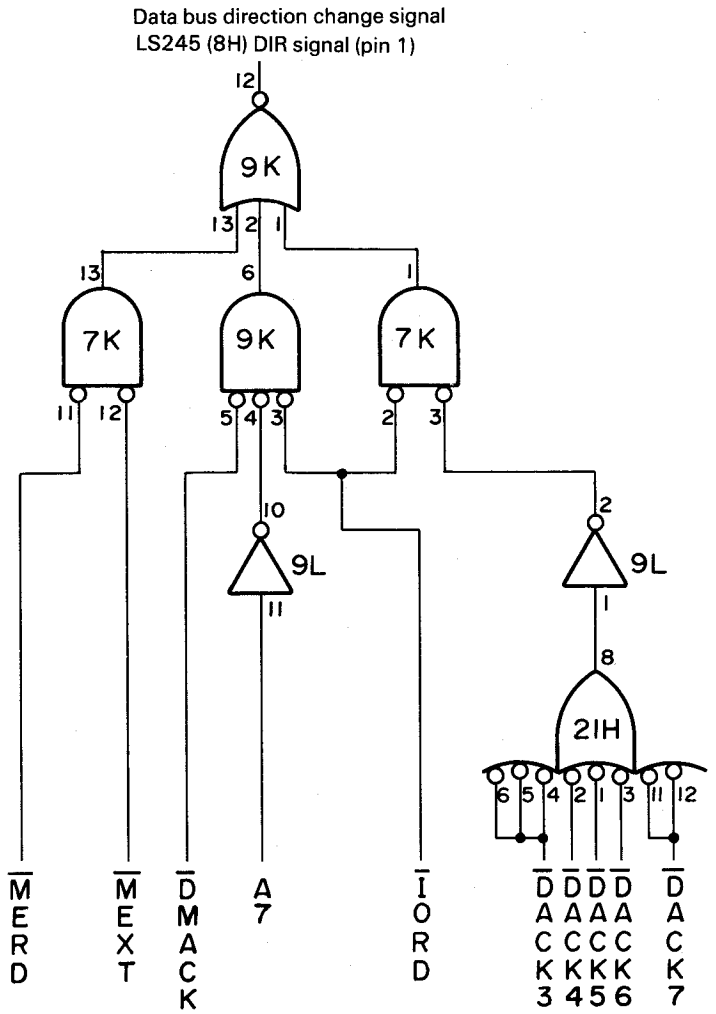


Fig. 4-13 Option card – data bus direction change signal supply circuit

4.8 $\overline{\text{WAIT}}$ Signal Supply Circuit

CPU μPD780 fetches the OP code when the $\overline{\text{M1}}$ signal is active. Usually, the machine cycle $\overline{\text{M1}}$ comprises 3 or 4 cycles T1 to T3 or T1 to T4 as shown in the timing chart (Fig. 4-14). During this cycle, an instruction is read and executed.

The CPU outputs the address value (program counter data) containing the instruction to be next executed in the T1 cycle to the address bus and reads the instruction from the data bus (D0 ~ D7) at the end of T2 cycle.

Namely, an external program memory must read the data within this time difference and give it to the CPU.

In this system, to ensure time for reading the data from D-RAM (access time 150ns) and C-MOS RAM (access time 450ns), the circuit shown in Fig. 4-16 is provided to generate the $\overline{\text{WAIT}}$ signal which is active low in the T2 cycle when the $\overline{\text{M1}}$ signal is active.

Thus, as shown in the timing chart (Fig. 4-15), the CPU takes in the $\overline{\text{WAIT}}$ signal in the leading signal in the T2 cycle, provides one extra T2 cycle in the next cycle and prolongs the time to ensure reading the data from the memory. This cycle is called a TW cycle. The $\overline{\text{WAIT}}$ signal is supplied through jumper J6, and J6 is usually set in the jumper state.

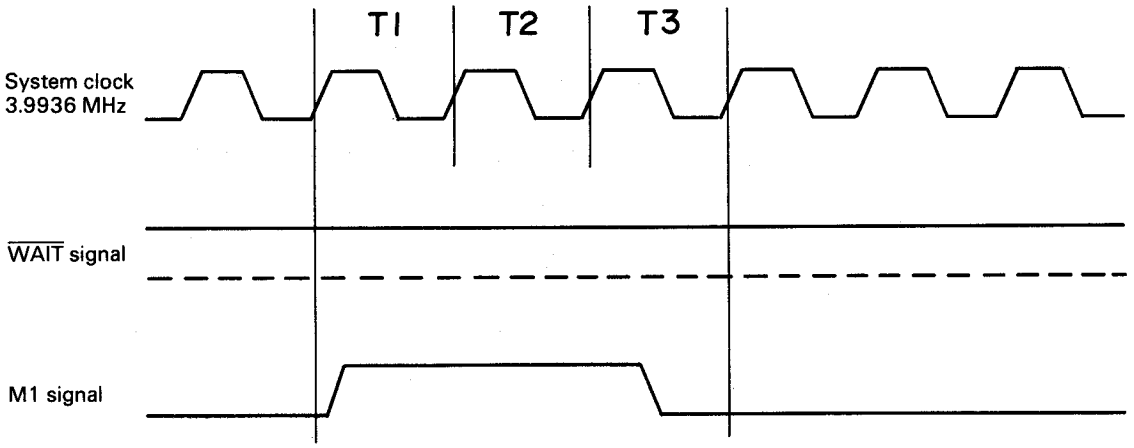


Fig. 4-14 M1 timing without Tw cycle (At 3 cycles)

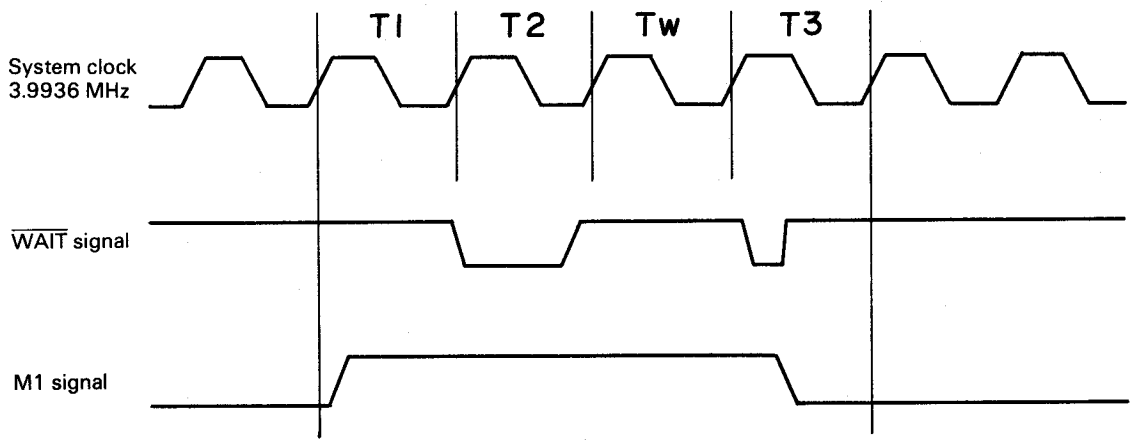


Fig. 4-15 M1 cycle with Tw cycle (At 4 cycles)

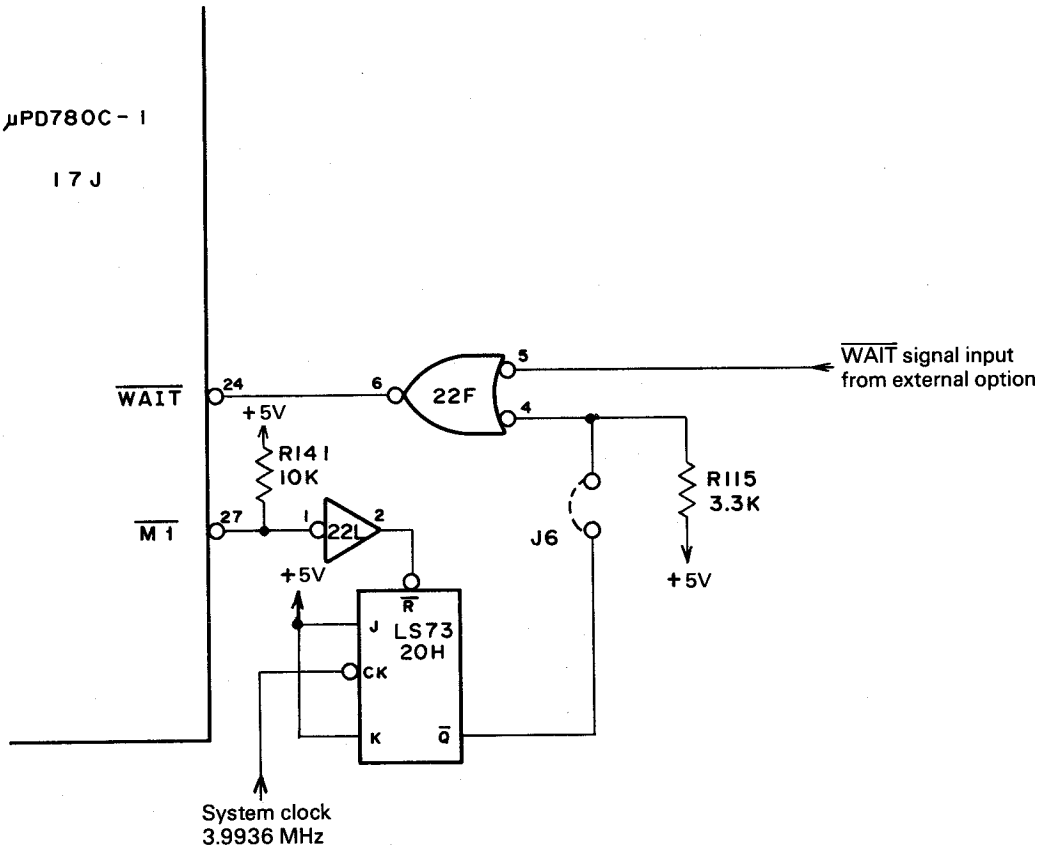
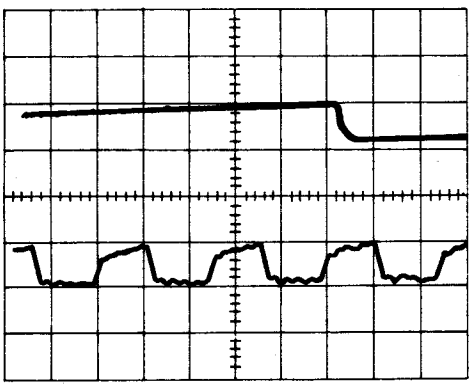
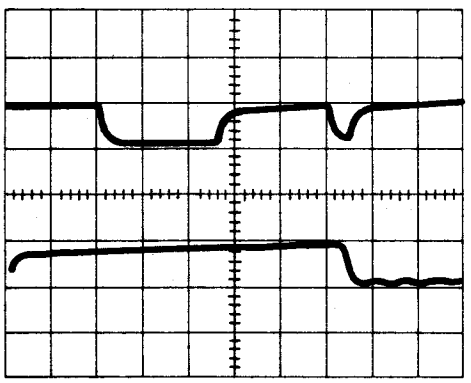


Fig. 4-16 WAIT signal supply circuit



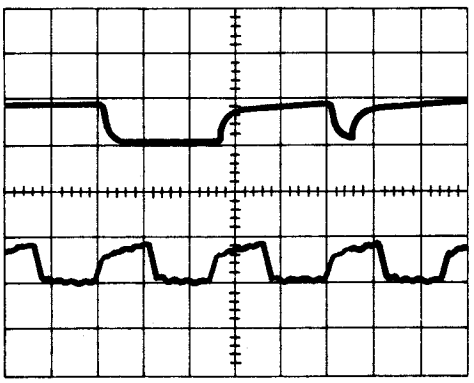
Upper: M1 signal
Lower: CLK
(Sweep 0.1 μsec. 5 volts/div.)

Fig. 4-17



Upper: WAIT signal (with J6)
Lower: M1 signal
(Sweep 0.1 μsec. 5 volts/div.)

Fig. 4-19



Upper: WAIT signal
Lower: CLK
(Sweep 0.1 μsec. 5 volts/div.)

Fig. 4-18

4.9 I/O Selector

Each I/O port is accessed by decoding the low-order 4 bit addresses (A2 ~ A5) of the CPU by the I/O selector LS154 (16H).

The functions of this I/O selector are shown in Table 4-1. One output terminal must be set to low level for the inputs at terminals A ~ D. The output signal provides the $\overline{CS}$ signal for each I/O device or CLK signal, and thereby a desired I/O device is selected.

In this case, to the terminals $\overline{1G}$ and $\overline{2G}$ which control the gate of LS154 (16H), the signal of the address line A6 is applied to the $\overline{1G}$ terminal, and the AND of the signal of the address line A7 and the $\overline{BUSAK}$ signal from CPU is applied to the $\overline{2G}$ terminal. The $\overline{BUSAK}$ signal indicates that the bus line can be used by the other devices when the signal level is low. The $\overline{2G}$ terminal is made active when the $\overline{BUSAK}$ signal and the address line A8 are at high level.

Therefore, selection of I/O device is made when the $\overline{BUSAK}$ signal is at high level and the address line and bus line are inhibited from being used by the other devices except for the CPU.

The I/O port address map is shown in Table 4-2.

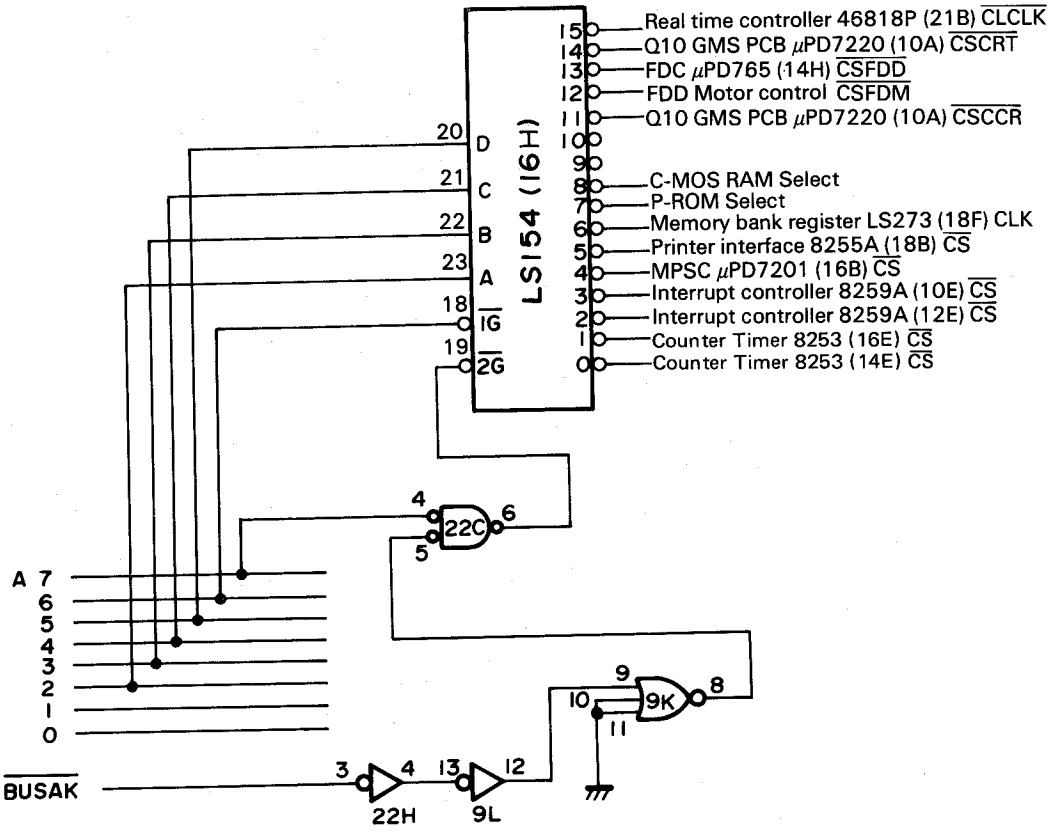


Fig. 4-20 I/O selector

FUNCTION TABLE

INPUTS						OUTPUTS														
$\overline{1G}$	$\overline{2G}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

Table 4-1

I/O PORT ADDRESS MAP (Table 4.2)

	0	1	2	3
0 0	Speaker timer	SOFT timer No.2	SOFT timer No.1	8253 No. 1 command
0 4	Speaker Freq.	Keyboard clock	RS232C clock	8253 No. 2 command
0 8	8259 (Master)			
0 C	8259 (Slave)			
1 0	Keyboard data	RS232C data	Keyboard command	RS232C command
1 4	Printer data	Printer status	Printer control	8255 command
1 8	DIP./SW./Mem. bank reg.			
1 C	P·ROM select			
2 0	C·MOS select			
2 4				
2 8				
2 C	CRT, PCB TYPE			
3 0	FDD motor control			
3 4	FDC status	FDC data		
3 8	GDC 7220	GDC	Zoom	Light pen
3 C	Clock data	Clock adress		

	0	1	2	3
4 0	8237 DMA controller # 1			
4 4				
4 8				
4 C				
5 0	8237 DMA controller # 2			
5 4				
5 8				
5 C				
6 0				
6 4				
6 8				
6 C				
7 0				
7 4				
7 8				
7 C				

	0	1	2	3
8 0				
8 4				
8 8	GPIB Interface Q10IE			
8 C				
9 0				
9 4	Memory Box (Optical Fiber) Interface Q10OF			
9 8				
9 C	Pulse Transformer Interface Q10PT			
A 0	AD/DA Interface Q10AD			
A 4	RS-232C Interface Q10RS			
A 8				
A C				
B 0	Direct Modem Interface Q10DM			
B 4				
B 8				
B C				

	0	1	2	3
C 0	Bar-code Reader Interface			
C 4				
C 8				
C C				
D 0				
D 4				
D 8				
D C				
E 0				
E 4				
E 8				
E C				
F 0				
F 4				
F 8				
F C				

Table 4.2

4.10 I/O Commands

The commands and status of each I/O device are described below. An important I/O device is initialized within IPL, and need not be re-set. The appropriate command is marked by "Set in IPL".

LSI 8253 **Function: Timer counter** #1, #2

I/O address 00H ~ 03H #1
04H ~ 07H #2

	7	6	5	4	3	2	1	0
03H (07) W	00: Counter 0 01: Counter 1 10: Counter 2		00: Counter latch 01: LSB Read/write 10: MSB Read/write 11: 2 byte Read/write		000: Terminal count 001: One shot 010: Repeated waveform	011: Squre wave output 100: Software trigger 101: Hardware trigger		0: Binary 1: BCD

Command register

00H ~ 02H (04 ~ 06) R/W	Counter value (Low-order and high-order digits are continuously read and written in this order.)

Timer counterof each channel

03H W	0	0 Counter 0	1	1 2-byte mode	0	0	1 One shot mode	0 Binary
00H W	0	1	1	1	0	0	0	0
00H W	0	0	0	0	0	0	0	0

Initial setting related to speaker timer (Set in IPL)
Set to about 100 ms (1200 Hz ÷ 112)

07H W	0	0 Counter 0	1	1 2-byte mode	0	1	1 Square wave output	0 Binary
04H W	0	0	0	0	0	0	0	0
04H W	0	0	0	0	1	0	0	0

Initial setting of speaker frequency (Set in IPL)
Set to about 1kHz (2 MHz ÷ 2048)

	7	6	5	4	3	2	1	0
07H W	0	1	1	1	0	1	1	0
	Counter 1		2-byte mode		Square wave output			Binary
05H W	1	0	0	0	0	0	0	0
05H R/W	0	0	0	0	0	1	1	0

Initial setting related to keyboard clock (Set in IPL)

Set 1200 BPS. (1.9968 MHz ÷ 1664)

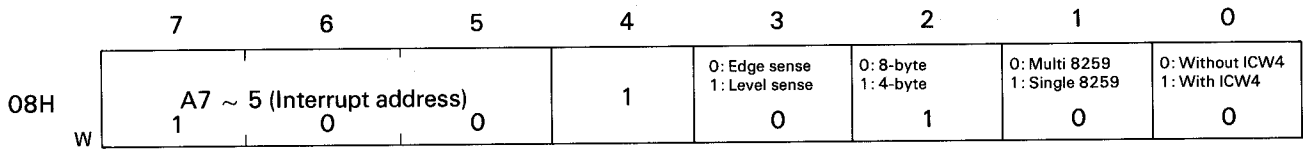
	7	6	5	4	3	2	1	0
07H W	1	0	1	1	0	1	1	0
	Counter 2		2-byte mode		Square wave output			Binary
06H W	1	1	0	1	0	0	0	0
06H W	0	0	0	0	0	0	0	0

Initial setting RS-232C clock (Set in IPL)

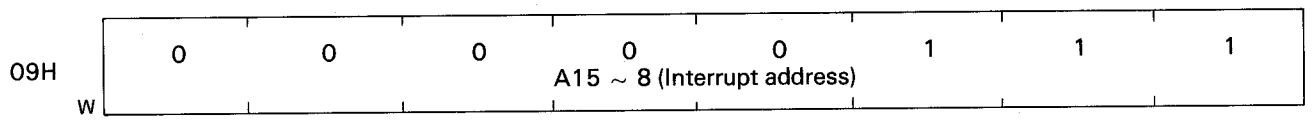
Set 9600 BPS. (1.9968 MHz ÷ 208)

LSI 8259A **Function: Interrupt controller (master)**

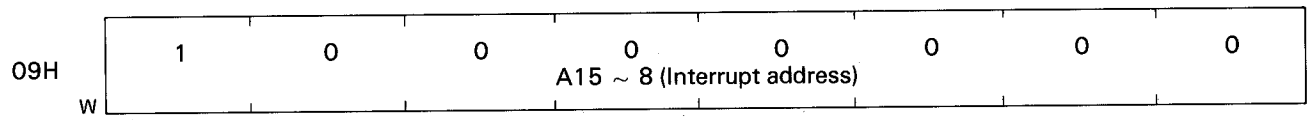
I/O address 08H ~ 09H



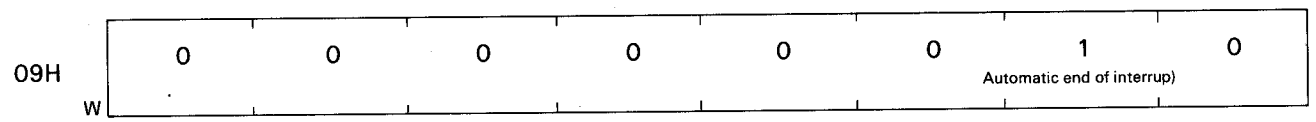
Setting of ICW1 (Set in IPL)



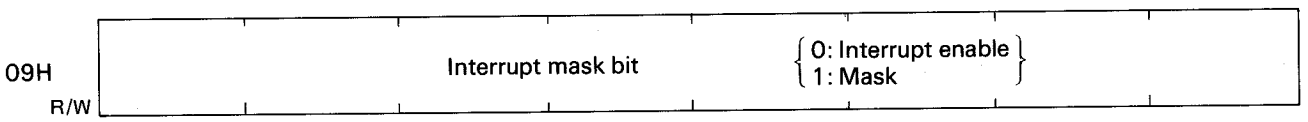
Setting of ICW2. Start interrupt address is 780H in IPL. (Set in IPL)



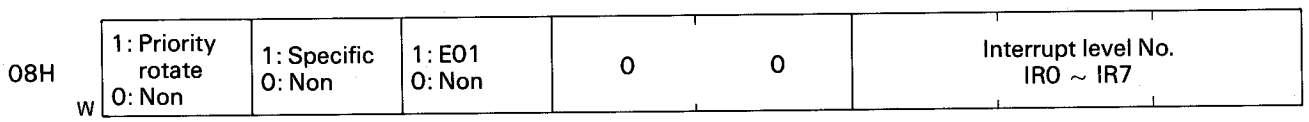
Setting of ICW3. Indicates slave 8259 is connected to the master IR7. (Set in IPL)



Setting of ICW4. (Set in IPL)



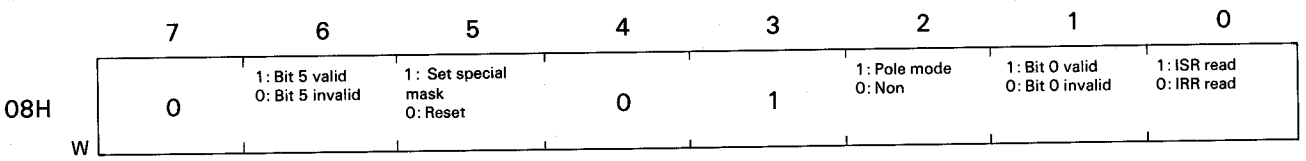
OCW1



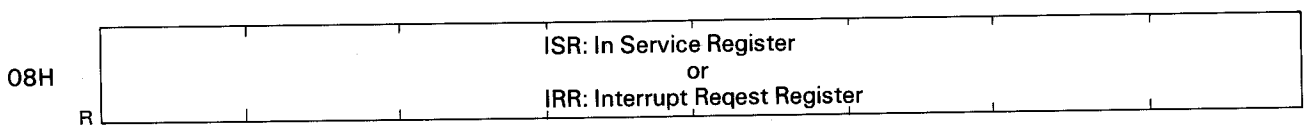
OCW2 End. of intr. command and priority rotate command

(Attention)

- ICW1 ~ 4 must be set continuously.
- Even when the interrupt address is changed, ICW1 ~ 4 must be set in sequence.
- OCW1 is usually readable and writable.

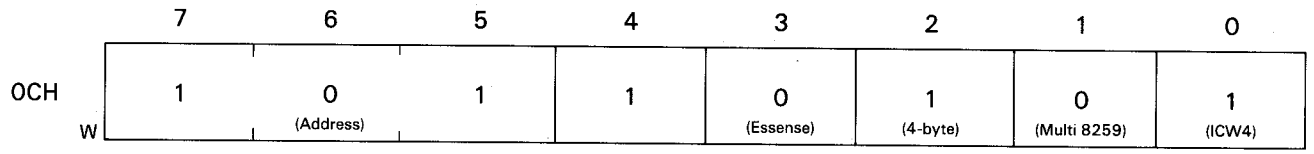


OCW3 When bit 1 = 1, 08H must be read next.

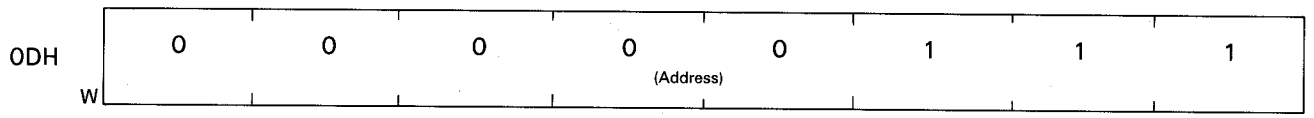


LSI 8259A **Function: Interrupt controller (master)**

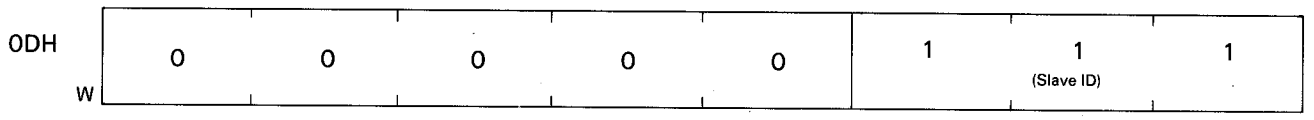
I/O adress 0CH ~ 0DH



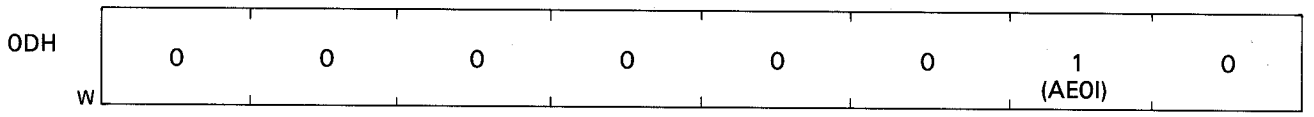
ICW1 (See 8259 master) (Set in IPL)



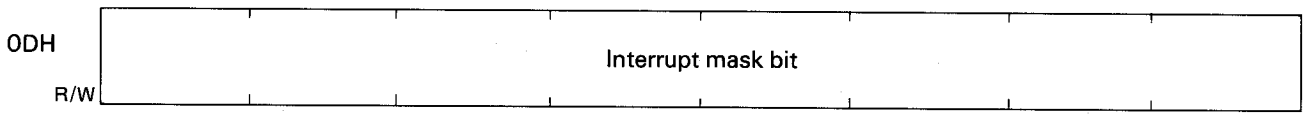
Setting of ICW2. Start interrupt address is 780H in IPL. (Set in IPL)



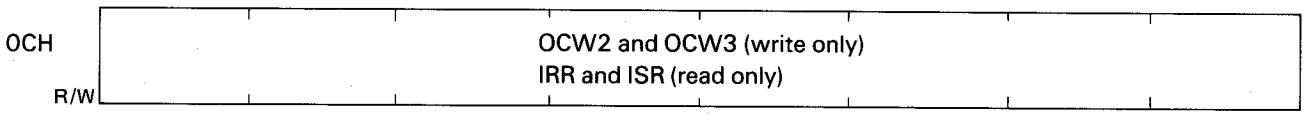
Setting of ICW3. Interrupt level of slave in master (Set in IPL)



ICW4 (See 8259 master) (Set in IPL)



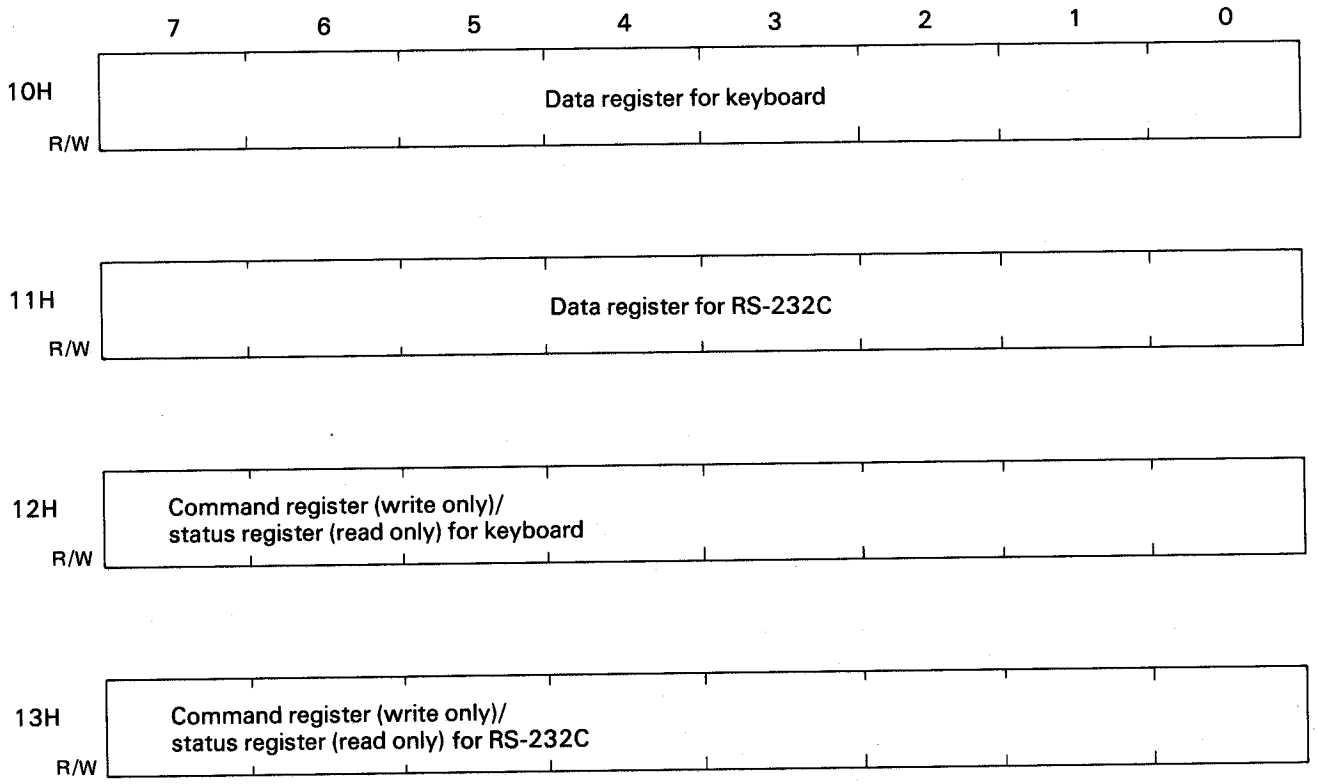
OCW1



(See 8259 master)

LSI 7201 **Function: Serial interface**

I/O address 10H ~ 13H



I/O adress H ~ H **Continued**

		7	6	5	4	3	2	1	0
WR0 12H (13)	W	00: NO-op 01: Reset Rx CRC 10: Reset Tx CRC 11:Reset Tx underline		000: No-op 001: Send abort 010: Reset EX/INT 011: Channel reset	100: Next Rx. interrupt enable 101: TxINT hold reset 110: Error reset 111: Return from INT		Resister pointer 0 ~ 7		
WR1 12H (13)	W	Wait enable	0	Wait on Rx/Tx	00: Rx INT/DMA disable 01: First chr. Int enable 10: All chr. Int enable 11: All chr. Int enable		Status affect Vector	Tx INT/DMA enable	Ex/ST INT enable
WR2 12H	W	1: $\overline{\text{SYNCB}}$ 1: $\overline{\text{RTSB}}$	0	Vector mode	0: 85 mode 1: 86 mode Intr.	0: 85 IM1 1: 85IM2 Intr.	Priority Select	Intr./DMA mode	
WR3 12H (13)	W	Rx bits/chr. 00: 5 bit/chr. 01: 6 bit/chr. 10: 7 bit/chr. 11: 8 bit/chr.			Enter Hunt Mode	Rx CRC Enable	Address Search Mode	Sync chr. latch Inhibit	Rx enable
WR4 12H (13)	W	Clock Rate 00: X1 01: X16 10: X32 11: X64		Sync Mode 00: 8 bit 01: 16 bit 10: SDLC 11: External		00: Sync 01: 1 bit STOP bit 10: 1-1/2 bit STOP bit 11: 2 bit STOP bit		Parity 0: ODD 1: EVEN	Parity 0: Disable 1: Enable
WR5 12H (13)	W	0: $\overline{\text{DTR}}$ = 1 1: $\overline{\text{DTR}}$ = 0	Tx Bits/chr. 00: 5 bit/chr. 01: 6 bit/chr. 10: 7 bit/chr. 11: 8 bit/chr.		Send Break	Tx enable	CRC-16/ CCITT	0: $\overline{\text{RTS}}$ = 1 1: $\overline{\text{RTS}}$ = 0	Tx CRC enable
WR6 12H (13)	W	SYNC chr. Bit 7 ~ 0							
WR7 12H (13)	W	SYNC chr. Bit 15 ~ 8							
RR0 12H (13)	R	Break/Abort	Tx underrun/EOM	CTS	$\overline{\text{SYNC}}$/Hunt	DCD	Tx Buff Empty	Int. Pending (ch. A only)	Rx chr. Available
RR1 12H (13)	R	End of Frame (SDLC)	CRC/Framing Error	Rx Overrun Error	Parity Error	Result Code			All Send
RR2 13H	R	Interrupt vector							
WR2 13H	W	Interrupt vector							

(Attention)

Though WR0 and RR0 are able to be read or written at any time, when the other resistors (WR1 ~ 7, RR1 ~ 2) are to be read or written, the resistor-pointer should be set to WR0 right before being read or being written.

LSI 8255 **Function: Printer interface**

I/O address 14H ~ 17H

17H W

7	6	5	4	3	2	1	0
1 Mode select	Port A Mode Select 00: Mode ϕ (bit) ★01: Mode 1 (byte) 10: Mode 2 (two-way)		Port A 1: Input ★0: Output	Port C High-order 1: Input ★0: Output	Port B Mode 1: Mode 1 (byte) ★0: Mode ϕ (bit)	Port B ★1: Input 0: Output	Port C Low-order 1: Input ★0: Output

Mode set command (Set ★mark in IPL)

17H W

7	6	5	4	3 ~ 1	0
0 Bit control	0	0	0	Bit No. (Port C) 0 ~ 7	1: Set 0: Reset

Bit control

14H W

Printer Output Data

Output data

15H R

7	6	5	4	3	2 ~ 1	0
Select out	Power off detect	Ready	No paper detect	Error	0	RS-232C DSR signal

Status input

16H R

7	6	5	4	3	2 ~ 1	0
OBF	Interrupt enable	Reset	No paper detect	Interrupt flag	0	Strobe signal

Control Use the above bit controls to set/reset each bit of this register.

MSI74LS273 **Function: Memory bank switch and DIP switch**

I/O address 18H

	7	6	5	4	3	2	1	0
18H W	#3	#2	#1	#0	External memory select	Speaker continuous ON	Software timer trigger	Speaker timer trigger
	Memory bank register							

18H R	DIP switch data input

LSI **Function: FDD motor control/memory bank status**

I/O address 30H

	7	6	5	4	3	2	1	0
30H W	FDD motor start pulse							

FDD motor is started by accessing this port. See the calendar clock of 46818 about the motor on time.

	7	6	5	4	3	2	1	0
30H R	#3	#2	#1	#0	FDD ready signal	Interrupt flag from the clock LSI	$\overline{\text{FDD motor ON}}$	Interrup flag from FDC
	Memory bank register							

The above status information can be obtained by reading this port.

LSI 765AC **Function: FDD Controller**

I/O address 34H ~ 35H

	7	6	5	4	3	2	1	0
34H R	RQM request	Data In/Out Read/Write	Non DMA	DDC Busy	#3	#2	#1	#0
					Device Busy			

Status register

35H R/W	Data register

Data and command register

For control of this port, see the μPD765AC user's manual.

LSI 7220 **Function: Graphic Display Controller**

I/O address 38H ~ 3BH

38H R

7	6	5	4	3	2	1	0
Light Pen Detect	Horizontal Blank	Vertical Sync.	DMA Excute	Drawing	FIFO EMPTY	FIFO FULL	DATA READY

39H W

GDC command

For details, see the 7220 manual.

38H W

GDC parameter

39H R

GDC data

3AH W

Zoom control (Zoom magnification: x 1)

A command to set the zoom magnification at the hardware level, since the functions of 7220 are insufficient at the zoom read command.

3BH W

Light pen service request F/F clear (DATA / Don't care)

Next light pen interrupt is not effected unless the port is accessed each time the light pen interrupt is accepted.

2CH

This port informs whether the video board which is provided on QX-10 is for the color monitor or for the mono chrome monitor.

When this port is read, following signals will be provided.

In case of being provided the mono chrome board: bit 0 = 0, bit 1 ~ 7 = 1

In case of being provided the color monitor: bit 1 = 1, bit 0 = 0, bit 2 ~ 7 = 0

LSI 46818 **Function: Clock with calender**

I/O address 3CH ~ 3DH

	7	6	5	4	3	2	1	0
3DH W	RAM address in clock							

When the RAM in the clock IC is accessed, first the RAM address must be written into this port and then the RAM data must be read/writen.

3CH R/W	RAM data

Address and data come as follows.

3DH port		3CH port
00H R/W	Second data	00 ~ 59 (BCD mode) 00 ~ 3B (Binary mode)
01H R/W	Alarm second data	00 ~ 59 (BCD mode) 00 ~ 3B (Binary mode)
02H R/W	Minute data	00 ~ 59 (BCD mode) 00 ~ 3B (Binary mode)
03H R/W	Alarm minute data	00 ~ 59 (BCD mode) 00 ~ 3B (Binary mode)
04H R/W	Hour data	01 ~ 0C/81 ~ 8C (Binary 12-hour mode) 01 ~ 12/81 ~ 92 (BCD 12-hour mode) 00 ~ 17 (Binary 24-hour mode) 00 ~ 23 (BCD 24-hour mode)
05H R/W	Alarm hour data	01 ~ 0C/81 ~ 8C (Binary 12-hour mode) 01 ~ 12/81 ~ 92 (BCD 12-hour mode) 00 ~ 17 (Binary 24-hour mode) 00 ~ 23 (BCD 24-hour mode)
06H R/W	Day-of-week data	(01 ~ 07)
07H R/W	Day data	01 ~ 31 (BCD mode) 01 ~ 1F (Binary mode)

LSI 46818 **Function: Clock with calender**

Continued

I/O address 3CH ~ 3DH

3DH port 3CH port

	7	6	5	4	3	2	1	0
08H R/W	Month data { 01 ~ 12 (BCD mode) / 01 ~ 0C (Binary mode) }							
09H R/W	Year data { 00 ~ 99 (BCD mode) / 00 ~ 63 (Binary mode) }							
0AH R/W	Update in-process (Ready only)	0	1	0	Setting of FDD motor timer length 01: 1/8 sec. ~ 0F: 1024 sec. (1/16 × 2^n sec.)			
		Setting of reference clock (32.768 kHz)						
0BH R	0: Update start 1: Update stop	Periodic interrupt enable	Alarm interrupt enable	Update end interrupt enable	Square wave output enable (FDD timer)	0: BCD mode 1: Binary mode	0: 12-hour 1: 24-hour	Special update enable
0CH R	Interrupt flag	Periodic interrupt flag	Alarm interrupt flag	Update end interrupt flag	0	0	0	0
0DH R/W	RAM valid	0	0	0	0	0	0	0
0EH ~ 3FH R/W	User RAM area							

PWD (When the battery power drops to zero). Indicates that the power supply is dropping.

LSI **Function: PROM, CMOS RAM select**

I/O address 1CH, 20H

	7	6	5	4	3	2	1	0
1CH W								1: disable 0: enable

P-ROM Select

	7	6	5	4	3	2	1	0
20H W								1: enable 0: disable

C-MOS RAM select

LSI 8237-5 **Function: DMA controller #1, #2**

I/O address 40H ~ 4FH (#1)
50H ~ 5FH (#2)

	7	6	5	4	3	2	1	0
40H (50) R/W	Ch.0 Base address				40H: For FDD 50H: Option 1 for DMA slow			
41H (51) R/W	Ch.0 Word address							
42H (52) R/W	Ch.1 Base address				42H: For CRT 52H: Option 2 for DMA slow			
43H (53) R/W	Ch.1 Word address							
44H (54) R/W	Ch.2 Base address				44H: Option 1 ~ 5 for DMA Fast 54H: Option 3 for DMA Slow			
45H (55) R/W	Ch.2 Word address							
56H R/W	Ch.3 Base address				56H: Option 4 for DMA Slow			
57H R/W	Ch.3 Word address							
48H (58) W	PACK 0: Low act 1: High	DREQ 0: High 1: Low	Write Select 0: Late Wr. 1: Extend.	Priority 0: Fix 1: Rotate Command register	Timing 0: Normal 1: Compres.	Controller 0: enable 1: disable	Address Holt Ch. 0 0: disable 1: enable	Mem to Mem. 0: disable 1: enable
48H (58) R	#0	#1	#2	#3	#0	#1	#2	#3
	Existence of DREQ signal				Existence of terminal count			
	Status register							
49H (59) W	0	0	0	0	0	DREQ 0: Reset 1: Set	DMA channel #0 ~ #3	
	Request status							
4AH (5A) W	0	0	0	0	0	DMA mask 0: No mask 1: Mask	DMA channel #0 ~ #3	
	Single mask register							
4BH (5B) W	00: Demand mode 01: Single mode 10: Block transfer mode 11: Cascade mode		Address 0: increment 1: decrement	Auto Init. 0: disable 1: enable	Transfer mode 00: Verify 10: Read 01: Write		DMA channel 0 ~ 3	
				Mode register to/from Mem.				
4CH (5C) W	Clear byte pointer F/F Clears the F/F to determine high or low order when the address work count is read/written.							
4DH (5D) R	Temporary register Latest data transferred with memory							
4DH (5D) W	Master clear Same as the hardware reset							
4FH (5F) W	0	0	0	0	#3	#2	#1	#0
	All mask register					o: Clear mask bit 1: Set mask bit		