CHAPTER 6
CRT DRIVE UNIT

CONTENTS

6.1 General

The 12-inch CRT Drive Unit (hereinafter called CDU) comprises a Cathode-Ray Tube (CRT) deflecting circuit and a video circuit. It receives video and synchronizing signals from the controller (Q10GMS board) and displays 640 x 400 pixcells on the CRT screen.

6.2 General Specifications

6.2.1 Deflecting frequency:

Horizontal : 19.3 kHz
Vertical : 45.8 Hz

6.2.2 Power conditions:

At the CDU input terminal
DC input voltage: 12V ±5%
Power consumption:
1.5A or less (mean value)
2.2A or less (peak value)

6.2.3 Environmental conditions:

(1) Temperature and humidity

	Storage	Operation
Temperature:	−20 – +65°C	0 – 55°C
Humidity:	5 – 90%	5 – 90%
	(with no dew)	(with no dew)

(Wet bulb temperature: 27°C max.)

(2) Insulation resistance (between GF and GL):
10 MΩ (500 Vdc)
(with GF and GL separated)

6.3 Interface Specifications

6.3.1 Pin Definition

Pin No.	Function
1	Video signal
2	Vertical synchronizing signal
3	Horizontal synchronizing signal
4	Power supply +12V DC
5	Grounding (power supply horizontal)
6	Grounding (video vertical)
7	Grounding (power supply horizontal)
8	Frame grounding

Table 6-1

6.3.2 Input Conditions

Video signal:

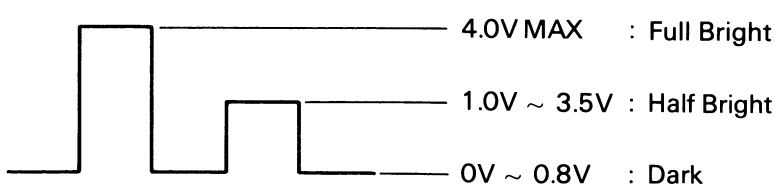


Fig. 6-1

Video input impedance	:	300 Ω min. 100 pF max.
Horizontal driving signal	:	TTL (positive) L: 0 – 0.8V H: 2.4 – 5.5V
Horizontal input impedance	:	500Ω min.
Vertical driving signal	:	TTL (positive) L: 0 – 0.3V H: 2.4 – 5.5V
Vertical input impedance	:	3.0 kΩ min.

6.3.3 Input signal timing

(a) Horizontal driving signal
19.3 kHz

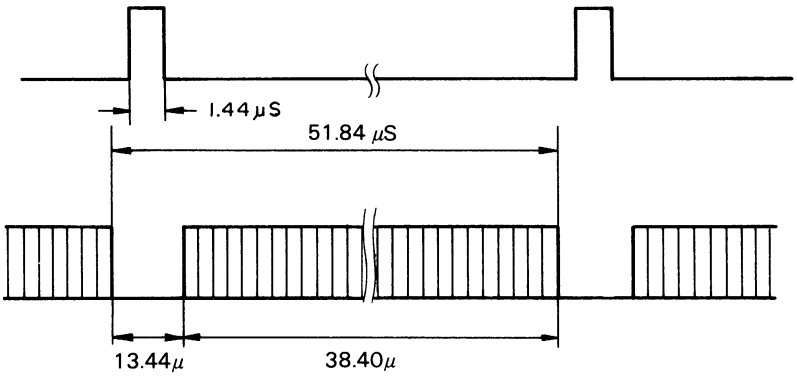
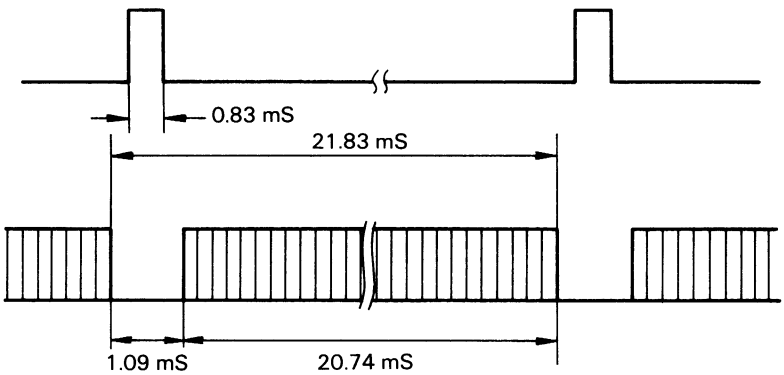


Fig. 6-2

(b) Vertical driving signal
45.8 Hz



(c) Video signal

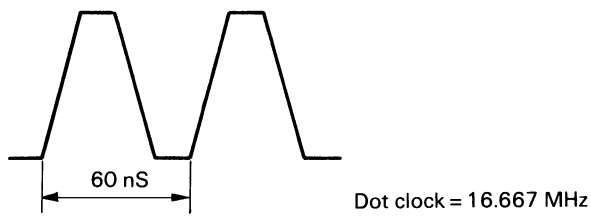


Fig. 6-3

6.4 Block Diagram

The CDU takes a video signal and horizontal/vertical synchronizing signals as input signals. The primary components are signal drive circuits to drive these signals, and a CRT deflecting circuit as shown in the block diagram (Fig. 6-4).

The video signal is applied to the CRT's cathode through the drive circuit. Horizontal and vertical synchronizing signals go through the respective drive circuits and are applied to the fly-back transformer (FBT) and the deflecting yoke (DY) to supply deflecting current to the CRT deflecting magnet field. The CDU is provided with a high voltage limiter which detects abnormally high voltage applied to the CRT and stops the horizontal drive circuit and reduces the high voltage to zero.

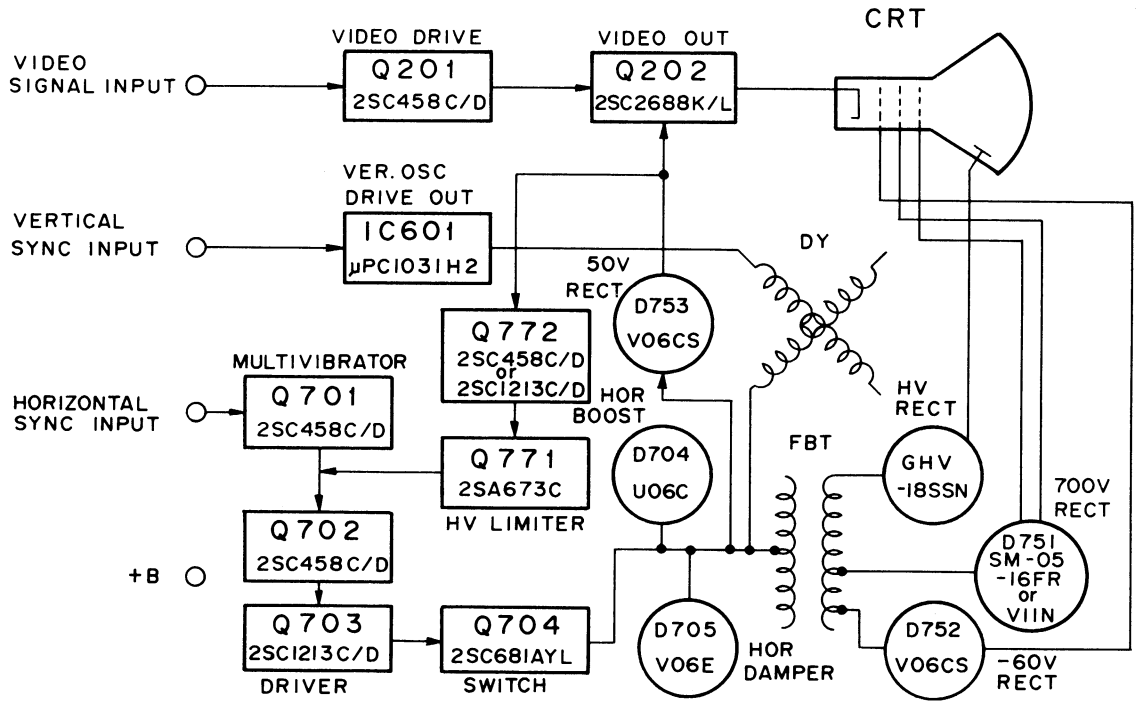


Fig. 6-4 CDU Block Diagram

6.5 Vertical Deflection Circuit

The vertical deflection circuit comprises a synchronous circuit, an oscillator, a saw tooth waveform generator, a linearity correction circuit, and an output circuit. It supplies the deflecting yoke with the saw tooth wave current.

In the CDU, the above operations are made by IC601 (μPC1031H2). A basic block diagram of this IC is shown in Fig. 6-8. The basic operation is as follows:

Self-oscillation is effected by the CR time constant of terminals 5 and 6, and synchronization is effected at terminal 5. The oscillator drives the saw tooth wave generator, and generates a saw tooth wave through the discharge slope of the CR circuit connected to the terminal 4. The saw tooth wave is applied to terminal 7, and amplified by the output amplifier to allow the saw tooth wave deflecting current flow in the deflecting yoke connected to the terminal 1.

The output amplifier comprises a current feedback amplifier circuit which feeds the voltage proportional to the saw tooth wave back to terminal 9.

The basic circuit is shown in Fig. 6-9.

The oscillator comprises a CR time constant Schmitt trigger circuit. The time constant or oscillation frequency is determined by R611, R613 and C612. Synchronization is effected at terminal 5 by capacitor coupling.

C611 is a coupling capacitor. R601 adjusts the size of the synchronizing signal.
The oscillation frequency can be varied by varying the value of R611. The circuit equivalent to the saw tooth wave generator is shown in Fig. 6-5. SW is formed within IC. By varying the value of R622, the saw tooth voltage can be varied to permit height adjustment.

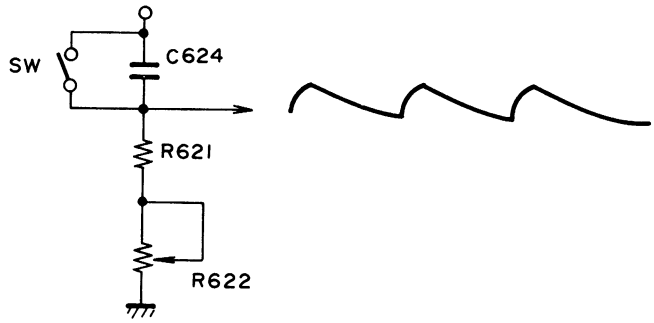


Fig. 6-5 Saw Tooth Wave Generator (Equivalent Circuit)

The linearity correction circuit is of the CR time constant type comprising R623, R624 and C621. The operating principle is shown in Fig. 6-6.
The saw tooth wave form can be changed by changing the value of R624. When the saw tooth wave form is changed, the saw tooth voltage is also changed and the screen size is changed. Thus, the picture size needs to be adjusted by R622 after adjustment of the linearity.

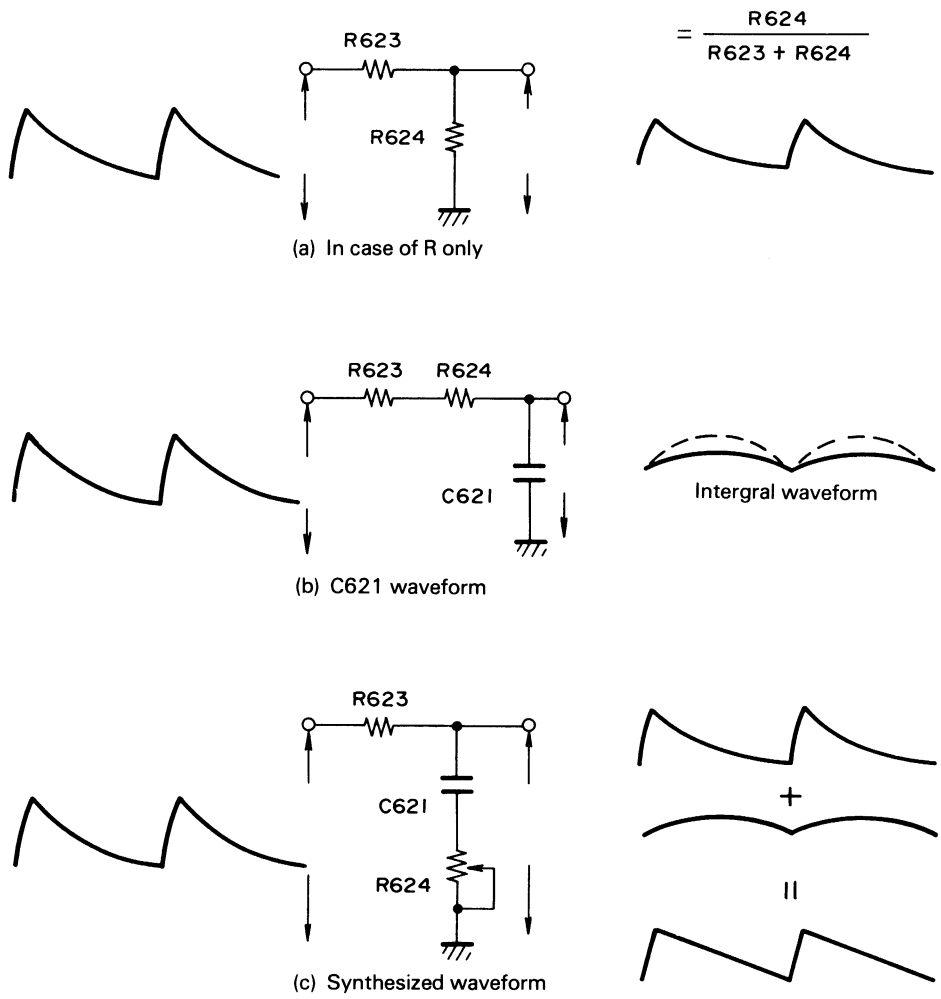


Fig. 6-6 Principle of Linearity Correction circuit

The output amplifier comprises a differential amplifier as shown in Fig. 6-7.

The saw tooth voltage is applied to the positive input terminal 7 of the differential amplifier through the coupling capacitor C622.

The deflecting yoke L601 and current feedback resistors R651 and R652 are connected in series to the output terminal 1 through capacitor C651.

The voltage with the same wave form as that of the deflecting yoke current is fed back to the negative input terminal 9 of the differential amplifier through the coupling capacitor C653. C652 is a bootstrap capacitor of the differential amplifier circuit. C654 is a capacitor to prevent oscillation of the output amplifier.

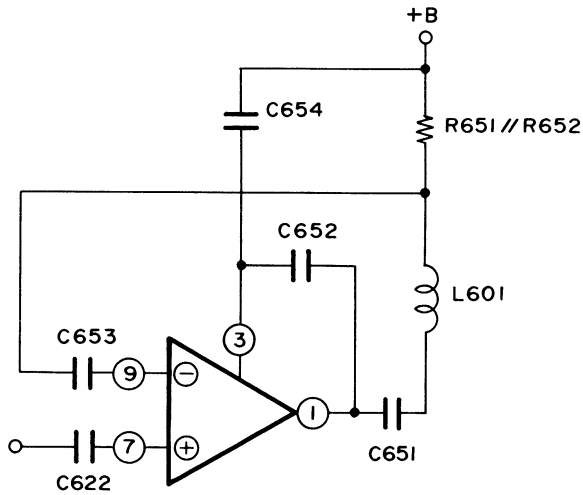


Fig. 6-7 Output Amplifier Basic Circuit

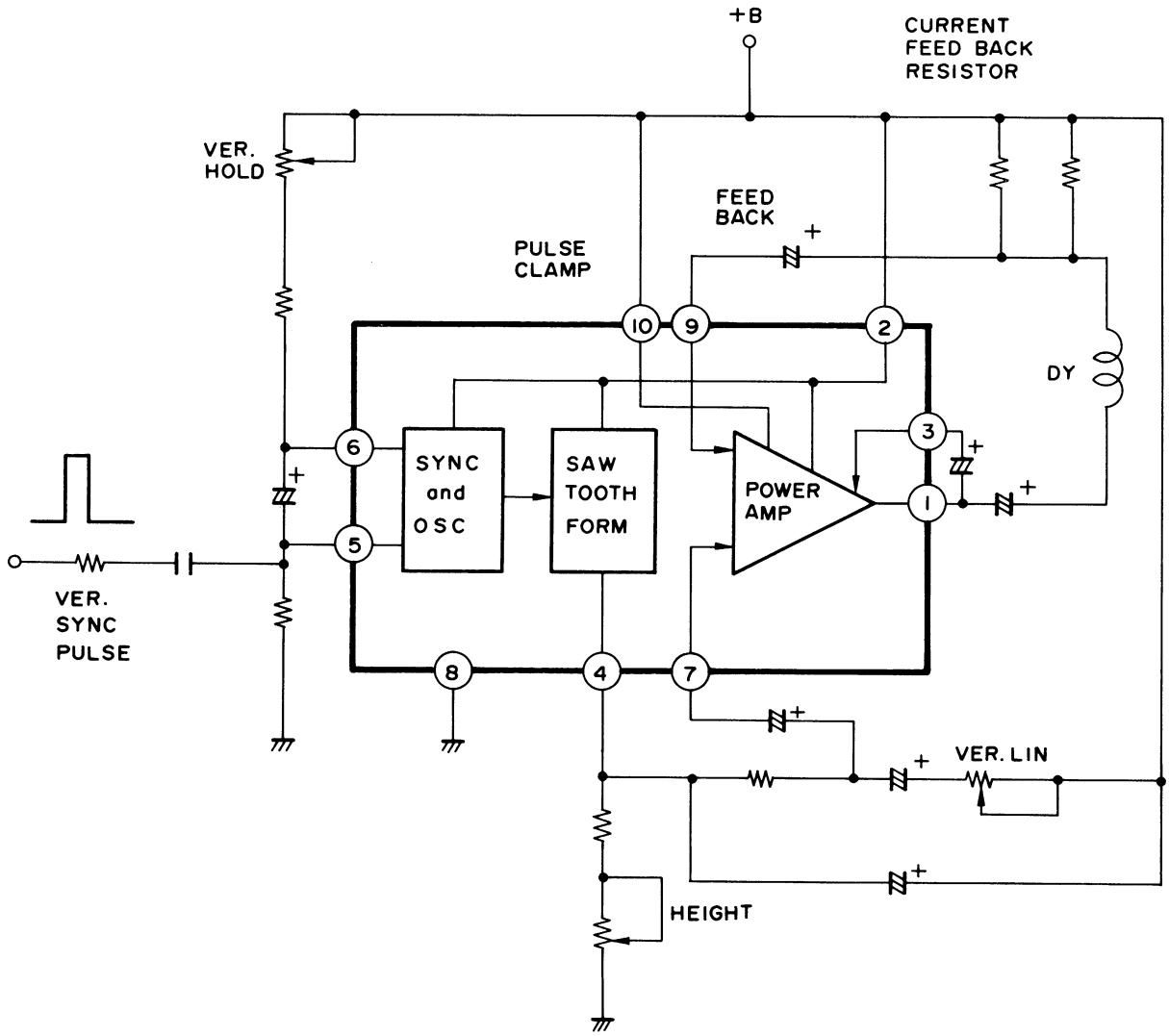


Fig. 6-8 Basic Block Diagram

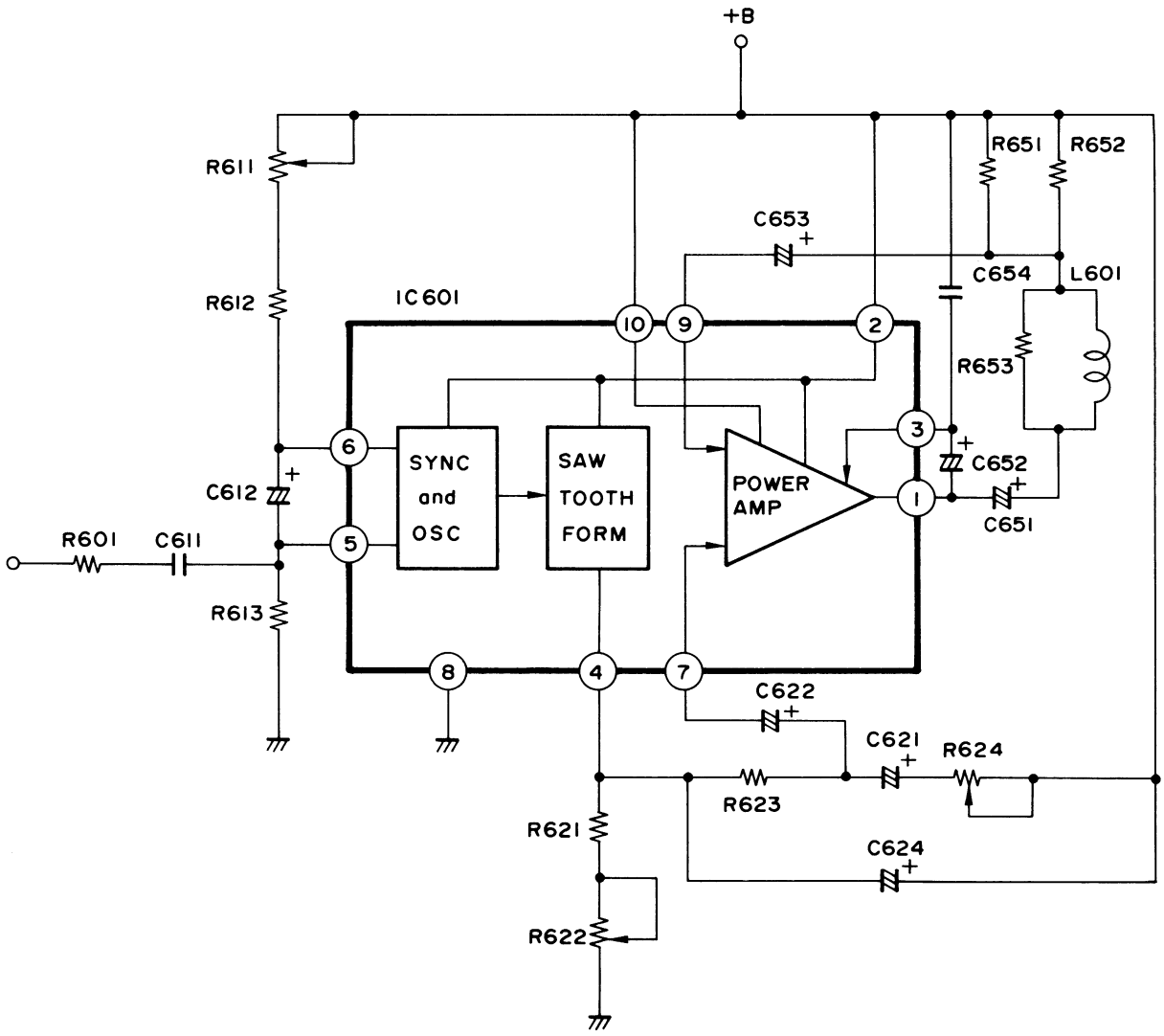


Fig. 6-9 Basic Circuit Diagram

6.6 Horizontal Deflection Circuit

The horizontal deflection circuit comprises a multivibrator, a drive transistor, an output transistor and a fly-back transformer. The basic block diagram is shown in Fig. 6-10. The multivibrator is triggered by an input synchronizing signal, and supplies a pulse of certain length to the drive transistor. This turns the output transistor on and off, thereby supplying a saw tooth current to the horizontal yoke winding and a voltage pulse to the fly-back transformer. The voltage pulse is boosted or reduced to CRT anode voltage or serveral bias voltages.

The positive edge of the input signal goes through D702 (the negative edge goes through D701) and triggers the monostable multivibrator. Then, Q702 turns on, and it turns off after the period determined by the time constants of R704, R705 and C702, thereby supplying a pulse of appropriate width to Q703.

The collector voltage of the drive transistor Q703 works as an inverse base current to the output transistor and turns it off.

When Q704 or D705 is ON, the yoke current flows like a saw tooth wave. When it is OFF, a fly-back pulse of about 200V is induced at the collector of Q704 by the resonance with the inductance composed mainly of the inductance L703 of C731 and yoke.

The peak-to-peak value of the yoke current, i.e. the picture width, can be adjusted by size inductor L704 provided on the board.

The asymmetrical form of the yoke current is modified by linearity inductor L705.

The fly-back pulse applied to the primary winding of flyback transformer T702 is divided and rectified into a high voltage of the CRT anode, 700V to G2, –60V to G1 and 50V to the video amplifier.

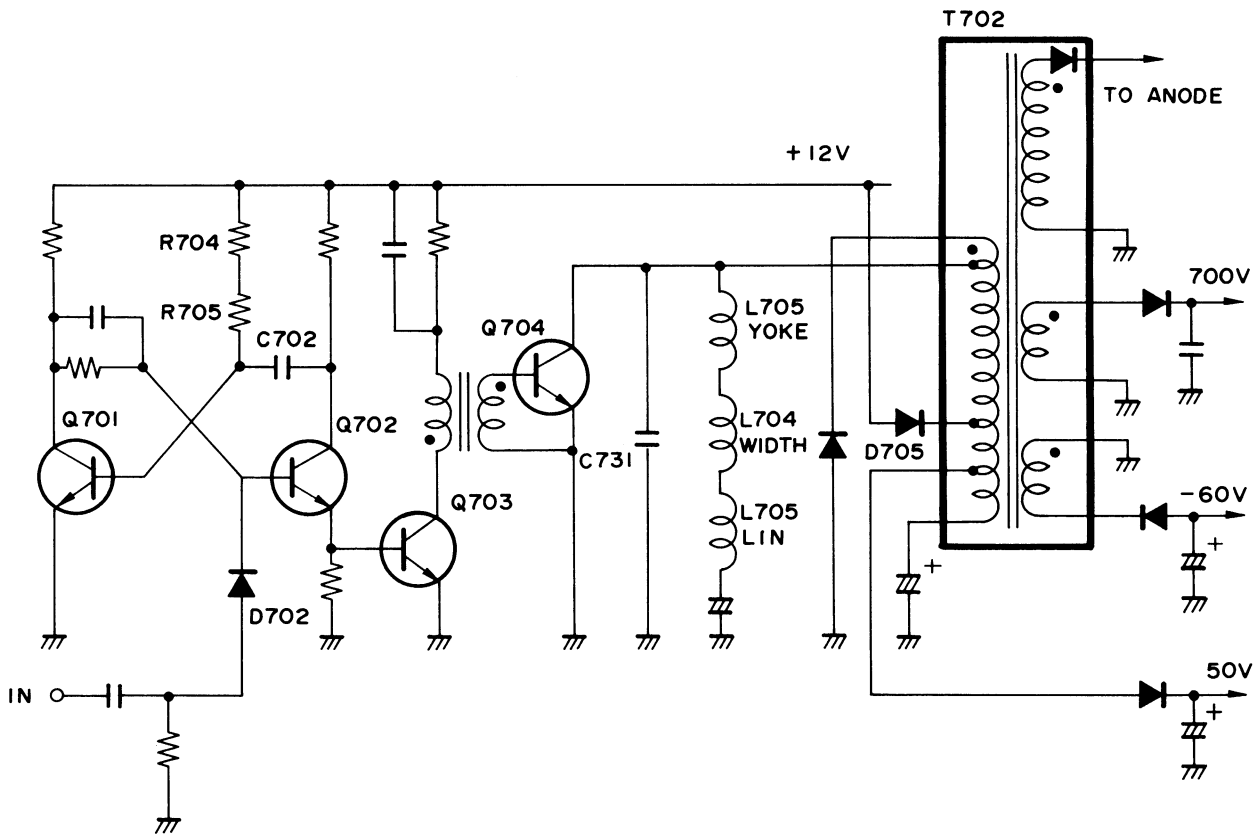


Fig. 6-10 Basic Horizontal Circuit

6.7 HV Limiter Circuit

If high voltage applied to the cathode-ray tube under abnormal operating conditions rises excessively, the cathode-ray tube may generate X-rays. To prevent this, the CDU employs a high voltage limiter which detects abnormally high voltage applied to the cathode-ray tube and stops operation of the horizontal drive circuit and reduces the high voltage to zero. Fig. 6-11 shows the high voltage limiter.

If an abnormally high voltage is generated, the pulse voltage at terminal 5 of the primary winding of fly-back transformer T702 is increased, and the medium voltage E50 obtained by rectifying the pulse voltage by D753 is also increased.

The base voltage of Q772 obtained by dividing medium voltage rises to a level where Q772 becomes conductive, and Q772 conducts. As a result, Q771 connected to Q772 via a thyristor conducts, too.

On the other hand, the collector of Q772 is connected to the base of Q702, the trigger input of the multivibrator comprising Q701 and Q702, through D771. If the potential at this base is grounded, the multivibrator stops operation. Therefore, when Q771 and Q772 conduct, the horizontal oscillation stops and the high voltage drops to zero. Once Q771 and Q772 conduct, they are held in the conduction state by the thyristor characteristic unless the power switch is turned off, and the high voltage is held at zero.

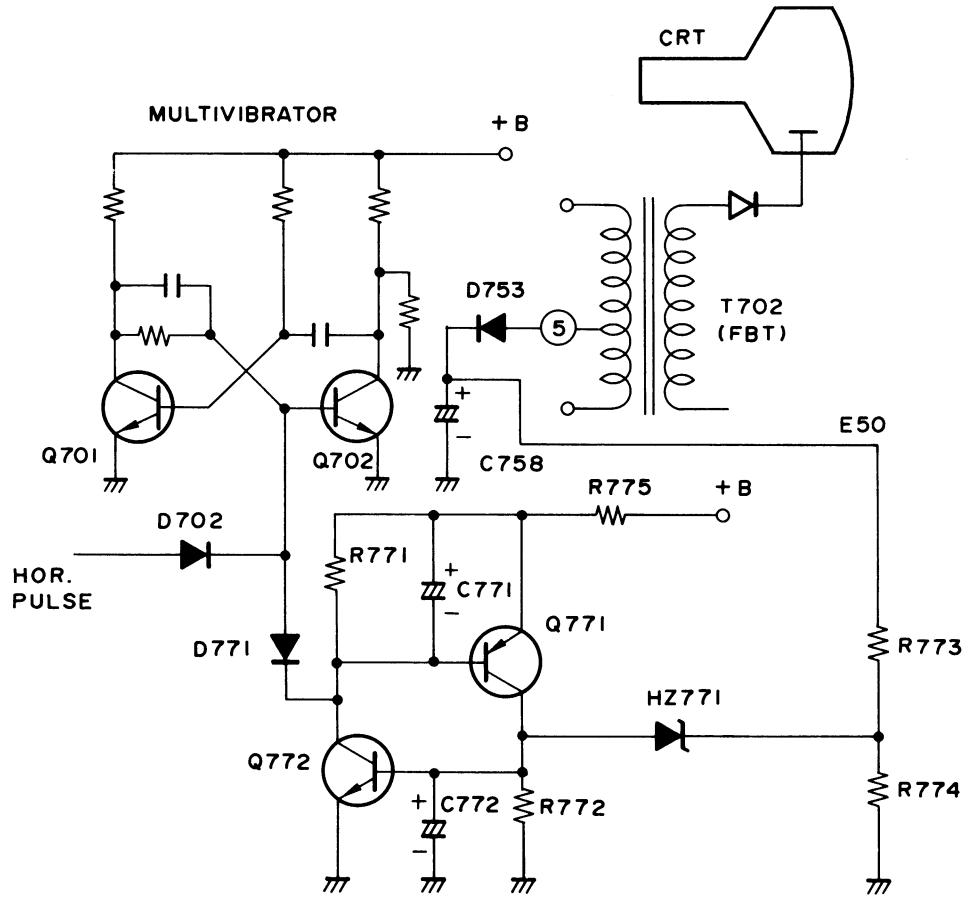
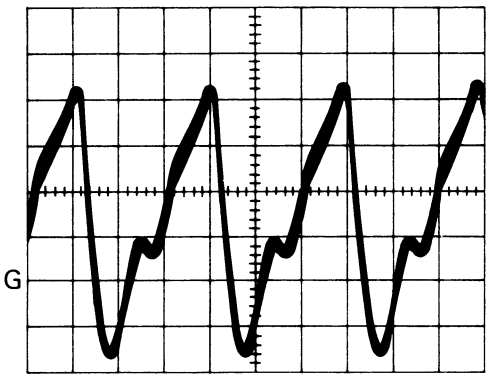


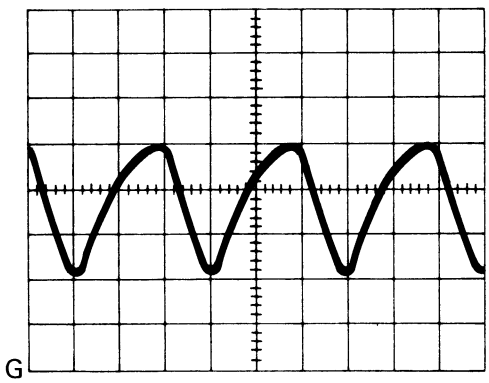
Fig. 6-11 High Voltage Limiter

CDU-12A01K CIRCUIT OPERATION WAVEFORM



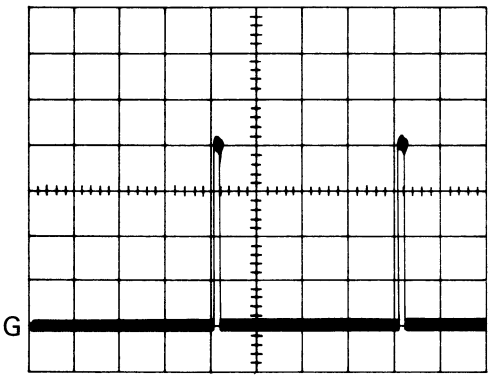
① 1V/DIV 20 nS/DIV

Fig. 6-12



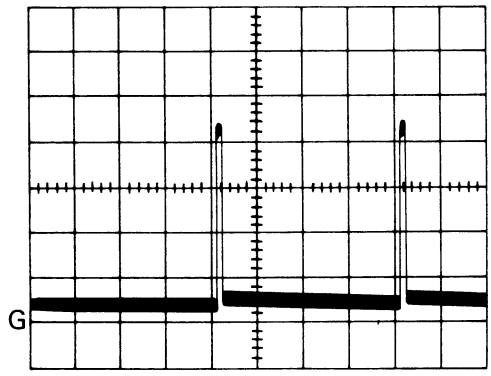
② 10V/DIV 20 nS/DIV

Fig. 6-13



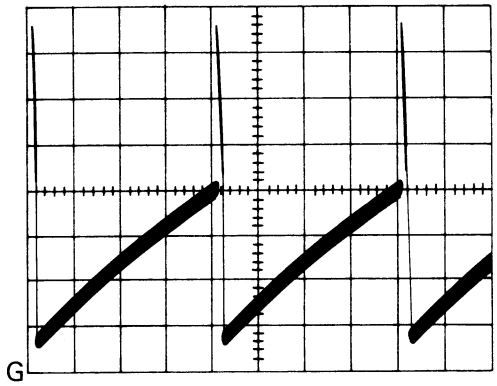
③ 1V/DIV 5 mS/DIV

Fig. 6-14



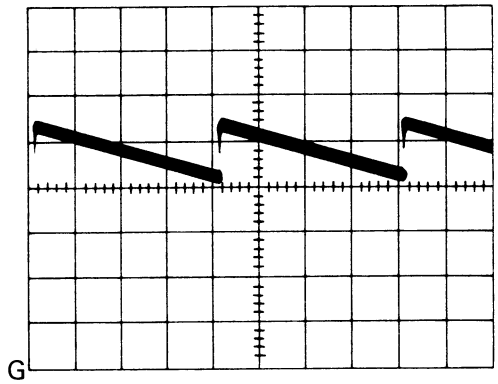
④ 1V/DIV 5 mS/DIV

Fig. 6-15



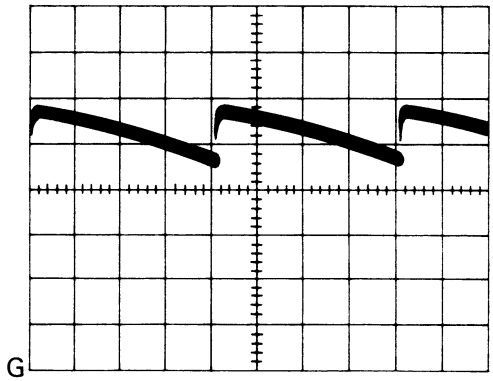
⑤ 1V/DIV 5 mS/DIV

Fig. 6-16



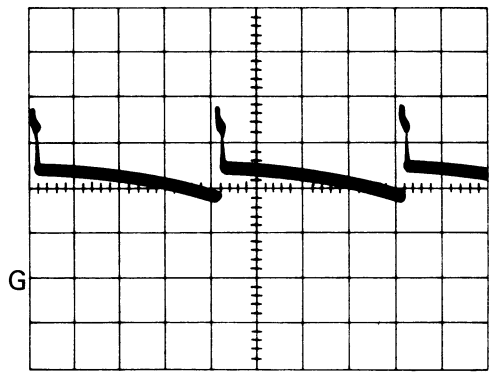
⑥ 2V/DIV 5 mS/DIV

Fig. 6-17



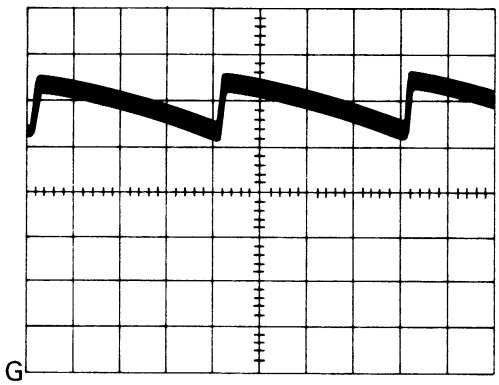
⑦ 1V/DIV 5 mS/DIV

Fig. 6-18



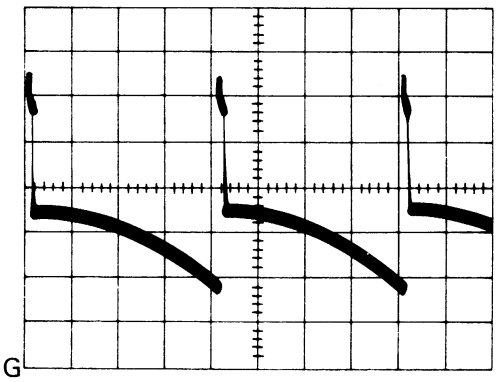
⑧ 5V/DIV 5 mS/DIV

Fig. 6-19



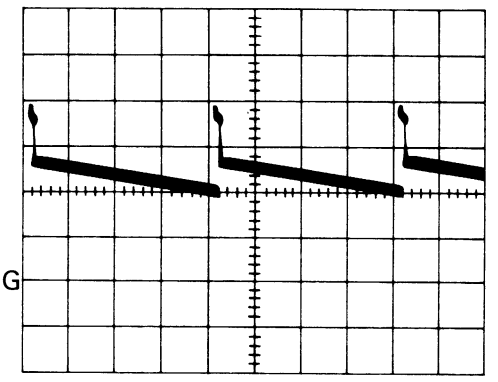
⑨
1V/DIV
5 mS/DIV

Fig. 6-20



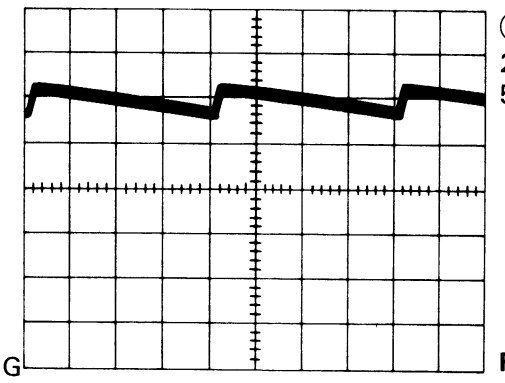
⑩
2V/DIV
5 mS/DIV

Fig. 6-21



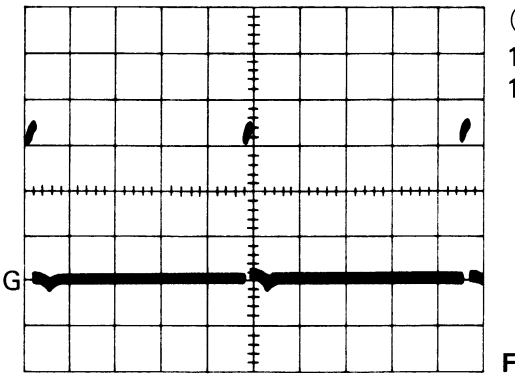
⑪
5V/DIV
5 mS/DIV

Fig. 6-22



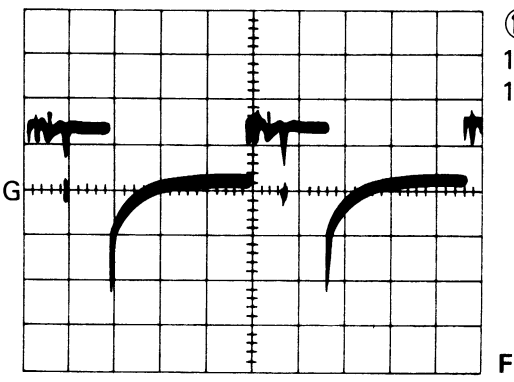
⑫
2V/DIV
5 mS/DIV

Fig. 6-23



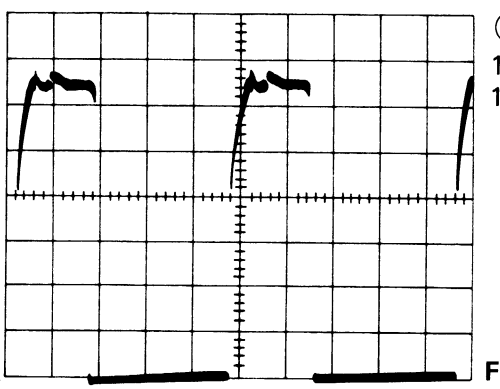
⑬
1V/DIV
10 μS/DIV

Fig. 6-24



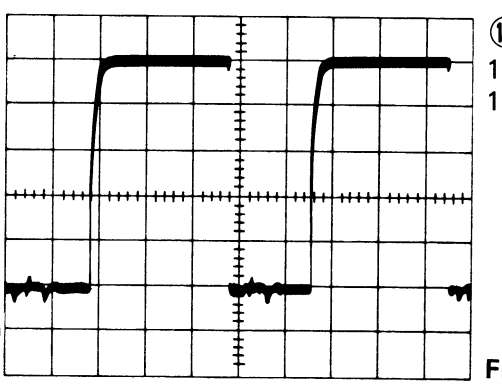
⑭
1V/DIV
10 μS/DIV

Fig. 6-25



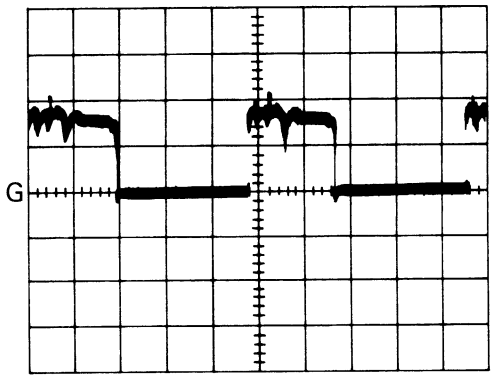
⑮
1V/DIV
10 μS/DIV

Fig. 6-26



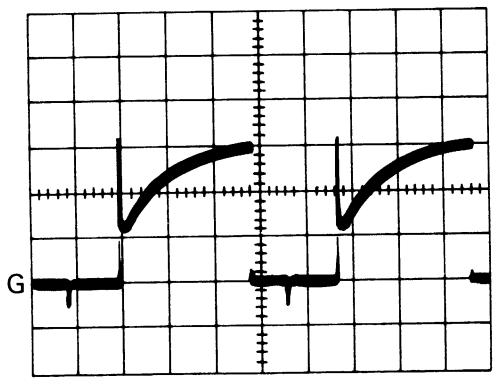
⑯
1V/DIV
10 μS/DIV

Fig. 6-27



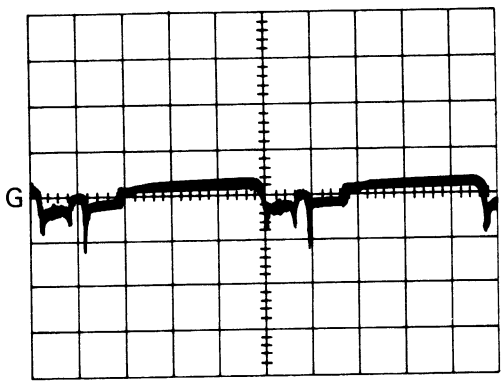
⑰
500 mV/DIV
10 μS/DIV

Fig. 6-28



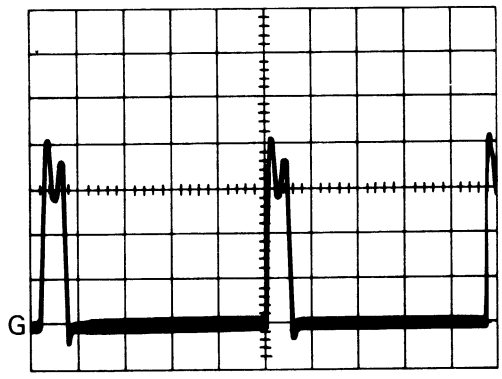
⑱
5V/DIV
10 μS/DIV

Fig. 6-29



⑲
5V/DIV
10 μS/DIV

Fig. 6-30



⑳
50V/DIV
10 μS/DIV

Fig. 6-31

CHAPTER 7
KEYBOARD UNIT

CONTENTS

7.1 General

The QX-10's keyboard is available in two types:

(a) ASCII type

(b) HASCI type

TYPE OF KEYBOARD ITEMS	ASCII TYPE	HASCI TYPE
Keyboard Diagram	See figure (Appendix)	See figure (Appendix)
Keyboard Scan code	See Table 7-5	See Table 7-4
Number of keys Typewriter keys Number keys Cursor keys Function keys	103 58 19 8 18	104 61 18 8 17
Remarks Keys with LED	CAPS LOCK INS SF1 SF2 SF3 SF4	SHIFT LOCK INSERT CALC DRAW SCHED
Temporarily shift keys	GRPH SHIFT (L) SHIFT (R) CTRL	GRPH SHIFT (L) SHIFT (R) CTRL (L) CTRL (R)

Table 7-1

In addition, the QX-10's ASCII type keyboard is available in eight language fonts as listed below.

1 : US ASCII 2 : ENGLISH

3 : GERMAN 4 : FRENCH

5 : ITALIAN 6 : SPANISH

7 : DANISH 8 : SWEDISH

Actually, the only differences of these keyboards are in the key-top labels. They are all the same in physical design.

7.2 Key-switches

The key-switch is composed of the parts shown in Fig. 7-1. When the key top is depressed, metal reed Ⓐ descends to establish continuity with Ⓑ. The stroke of the contact is shown in Fig. 7-2.

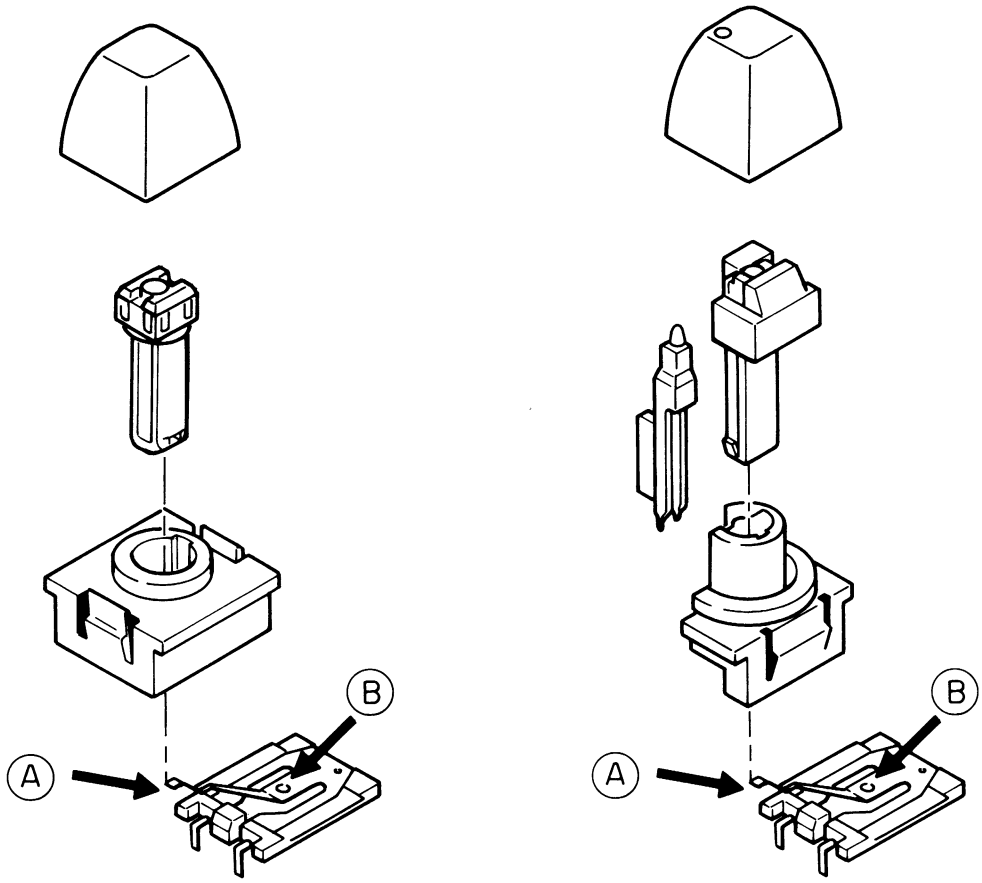


Fig. 7-1 Key-switch constructions

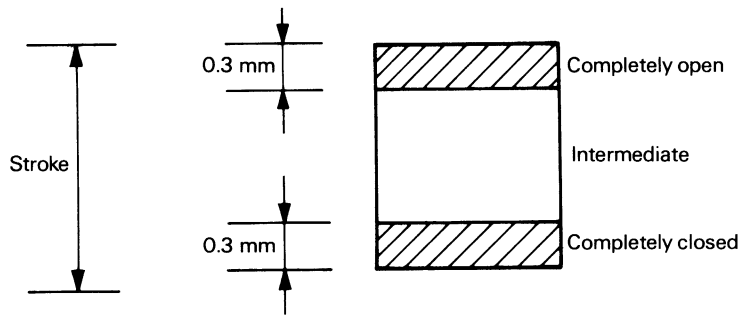


Fig. 7-2 Stroke of the key-switch contact

7.3 Key-switch Signals

(1) Fig. 7-1 shows the connections of the key-switches.

The key-switches are connected to some of the intersections of the row lines of the keyboard scan signals (KSC) generated by decoders LS145 (1A and 2A) and the column lines of the keyboard return signals (KRTN) which are the data bus lines of 8049 (5A). Thus, this arrangement of the key-switches looks like a 16 by 8 matrix in mathematical terminology.

The KSC lines and KRTN lines are pulled up by +5V. A pair of KSC and KRTN lines become continuous when a key-switch is depressed, otherwise they are open.

Suppose that a certain KSC line is low level. If a switch has been depressed, the KRTN line that becomes continuous with the KSC line also becomes low level and, since an inverter inverts it, high level develops at the associated data bus line of 8749 (5A).

This is the principle of detecting the depression of a key. Actually, an active-low signal scans over the KSC lines and, timed with it, levels of the data bus lines of the 8049 (5A) a lines of the 8049(5A) are checked so that the entire keyboard is equally sensed.

(2) The KSC signals are generated by two binary-to-decimal decoders LS145 from the output signals developing at P10 - P13 of the 8049 (5A).

The input signals to the two decoders (1A and 2A) are distinguishable because an inverter is connected to the D input terminal of decoder (1A). That is, the output of the decoder is of eight bits and, if input D is high level, the decoder is not selected and consequently it does not output any scanning signal.

Thus, keyboard scanning proceeds with only one KSC line put to low level at a time. The scanning signal is normally 830 μsec.

Table 7-2 below summarizes the relationships of the inputs and outputs of decoder LS145.

NO.	INPUT				OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L									
1	L	L	L	H		L								
2	L	L	H	L			L						Unused	
3	L	L	H	H				L						
4	L	H	L	L					L					
5	L	H	L	H						L				
6	L	H	H	L							L			
7	L	H	H	H								L		

H: High level
L: Low level

Table 7-2

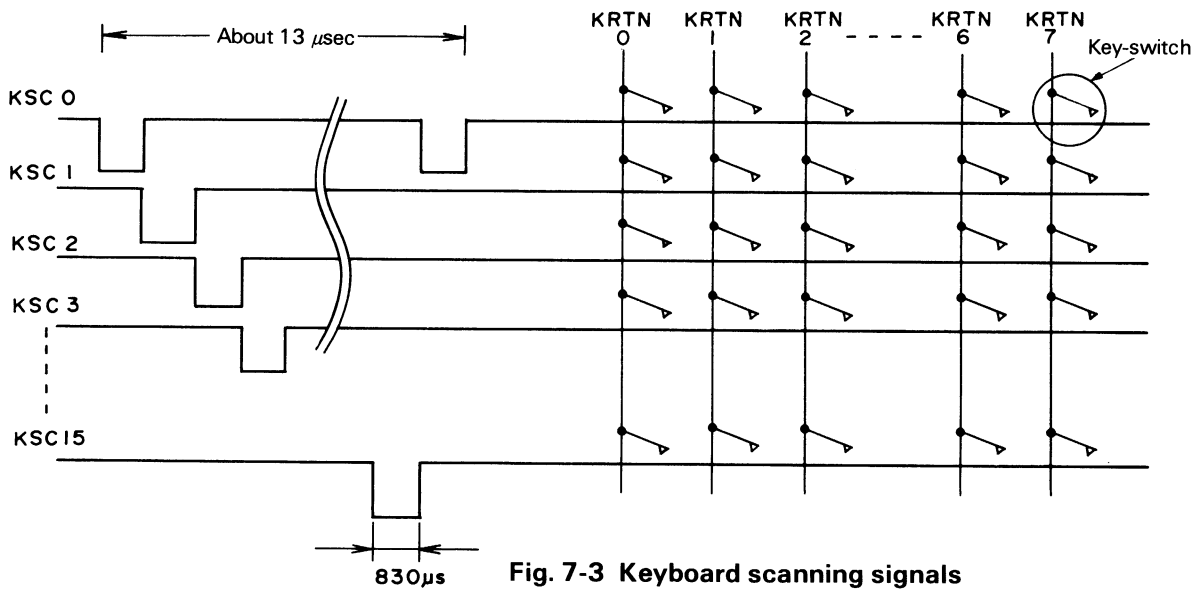


Fig. 7-3 Keyboard scanning signals

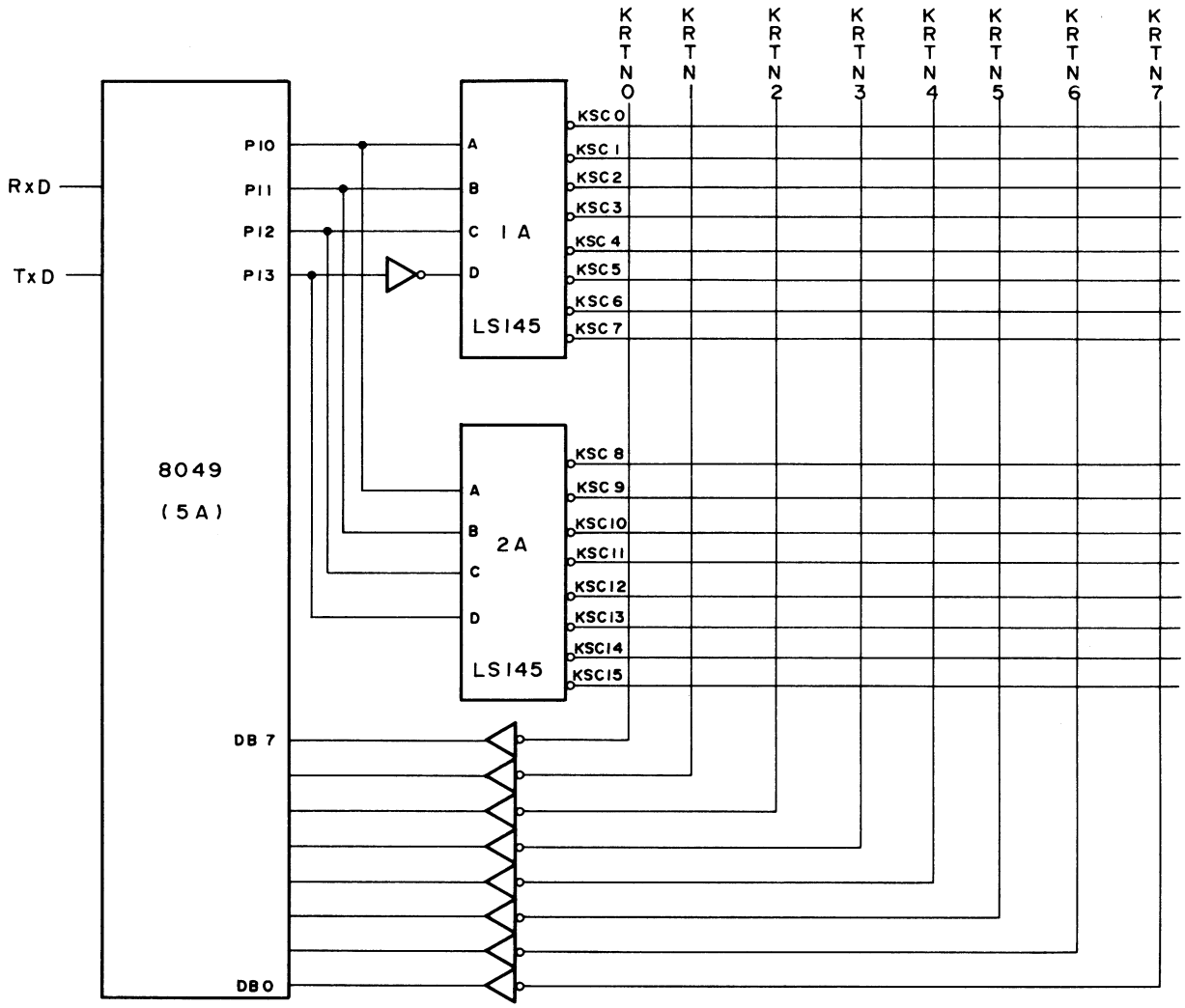


Fig. 7-4

(3) P20 – P27 of the 8749 (5A) are connected to the LEDs built in some key-switches. When a key-switch with key-top LED is depressed, the associated line out of P20 – P27 turns to low level to light the LED. A program held in the ROM (2 KB) of the 8749 (5A) is executed to find a depressed key and light its built-in LED.

7.4 Data Transfer to and from the Keyboard

Data are synchronously transferred between the keyboard and the QX-10 at the rate of 1,200 baud. The clock signal used at this time is supplied from terminal OUT 1 of the programmable interval timer 8253 (16E) mounted on the main board (Q10SYM board).
Commands given to the keyboard enter terminal T1 (pin 39) of the 8749 (5A) from external RXD.
Output data exit from TXD through P17 of the 8749 (5A).
The input commands and output data are explained below.

(1) Input commands (data coming from RXD)

1) Reset

1	1	1	X	X	X	X	$\overline{\text{Diagnostic program}}$

Functions: Initializes the keyboad controller.
Clears the key code buffer (of 32 characters' capacity).
Validates repeat function.
Designates repeat start time (500 msec).
Designates repeat interval (50 msec).
Extinguishes all LEDs.

Diagnostic program bit:
0: Causes one LED to another to blink; lights, then extinguishes all LEDs; scans key matrix; and sends out 00H if no key is depressed and FFH if one or more keys are depressed.
1: Does not execute the diagnostic program.

2) Set repeat start time

0	0	0	300 ms + N × 25 ms

Function: Sets the time interval after which repeat is to start when a key is kept depressed. This parameter may be varied from 300 msec to 1,075 msec in intervals of 25 msec. The least significant five bits of the command represent the interval in such a manner that 00H corresponds to 300 msec, 01H to 325 msec, ..., and 1FH to 1,075 msec.

3) Read SW status

1	0	0	X	X	X	X	X

Function: Sends back the current on/off statuses of all SWs. The 8-byte output data is sent out in preference to other key codes.

4) Control repeat

1	0	1	X	X	X	X	ON/OFF

Function: Enables or inhibits repeat according to the content of bit 0 of this command.
Bit 0 = 0 ..... Inhibits repeat function and, if repeat function is operating, stops it.
Bit 0 = 1 ..... Enables repeat.

5) Enable keyboard to send

1	1	0	X	X	X	X	ON/$\overline{\text{OFF}}$

Function: Enables or inhibits the keyboard sending data.
Bit 0 = 0 ..... Inhibits the keyboard sending data. Transmission of data which is in progress will be completed.
Bit 0 = 1 ..... Enables the keyboard to send data.

6) Set Repeat Interval

0	0	1	30 ms + N × 5 ms

Function: Sets the interval at which repeat function is to work after it has begun. The least significant five bits of the command represent the interval in such a manner that 00H corresponds to 30 msec and the interval becomes longer by 5 msec up to 185 msec as the parameter increases by one.

7) Turn On/Off LED

0	1	0	X	LED No.	ON/$\overline{\text{OFF}}$

Function: Turns on (ON/$\overline{\text{OFF}}$ = 1) or off (ON/$\overline{\text{OFF}}$ = 0) the LED designated with parameter LED No.

8) Read LED status

0	1	1	X	X	X	X	X

Function: Sends back the current on/off statuses of all LEDs. The output data is of eight bytes in total, with one byte assigned to each LED. The data is output with the highest priority and placed at the top of the key code buffer. If overflow takes place in the key code buffer, some of the latest input data (but not of LED statuses) will be discarded.

(2) Output Data (data going out from TXD)

1) Key code

0	DB 0 ~ 7	P13 P12 P11 P10

Operation: A key code is generated by combining KSC signal (P13, P12, P11, and P10) with KRTN signal (DB0 – 7).

2) SW data

1 0 0 0	DB 0 ~ 7	ON/OFF

Operation: The statuses of the SHIFT, CTRL, and GRPH SHIFT keys are read as SW data. DB0 – 7 are associated with the keys as assigned in the key code tables. The least significant bit becomes "1" if the key is on and "0" if it is off.

3) LED status

1 1 0 0	LED No.	ON/OFF

Operation: The status of a key-top LED is sent out. LED No. is supplied from the contents of the least significant byte of the code given from the key code tables. The least significant bit is "1" if the LED is on and "0" if it is off.

▶ Timing Diagram

Fig. 7-5 is the timing diagram of the transmitted and received data (RXD and TXD) of the key-board.

The clock signal is supplied from teh counter timer μPD8259 mounted on the Q10SYM board for transmission at 1,200 baud.

The interface between the keyboard and CPU is channel A of the serial controller μPD7201 mounted on the Q10SYM board.

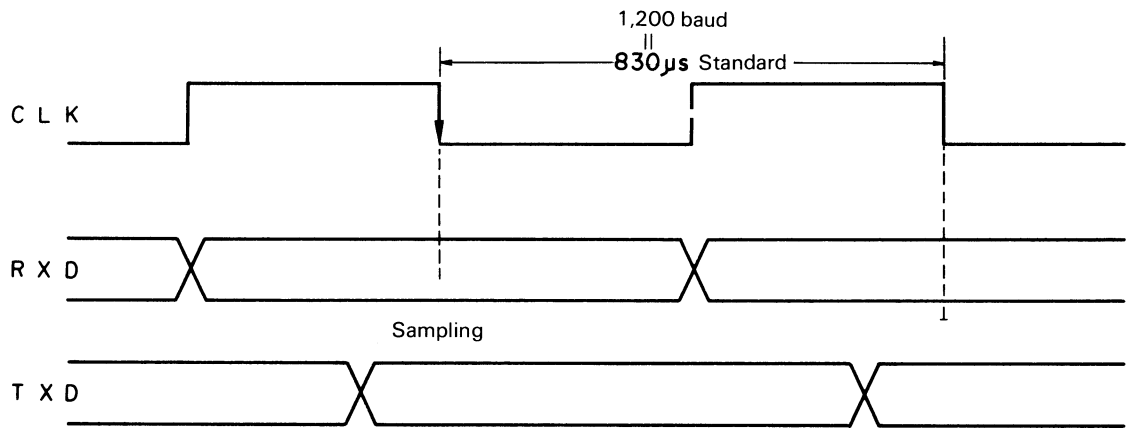


Fig. 7-5 Timing diagram

7.5 Key Code Tables

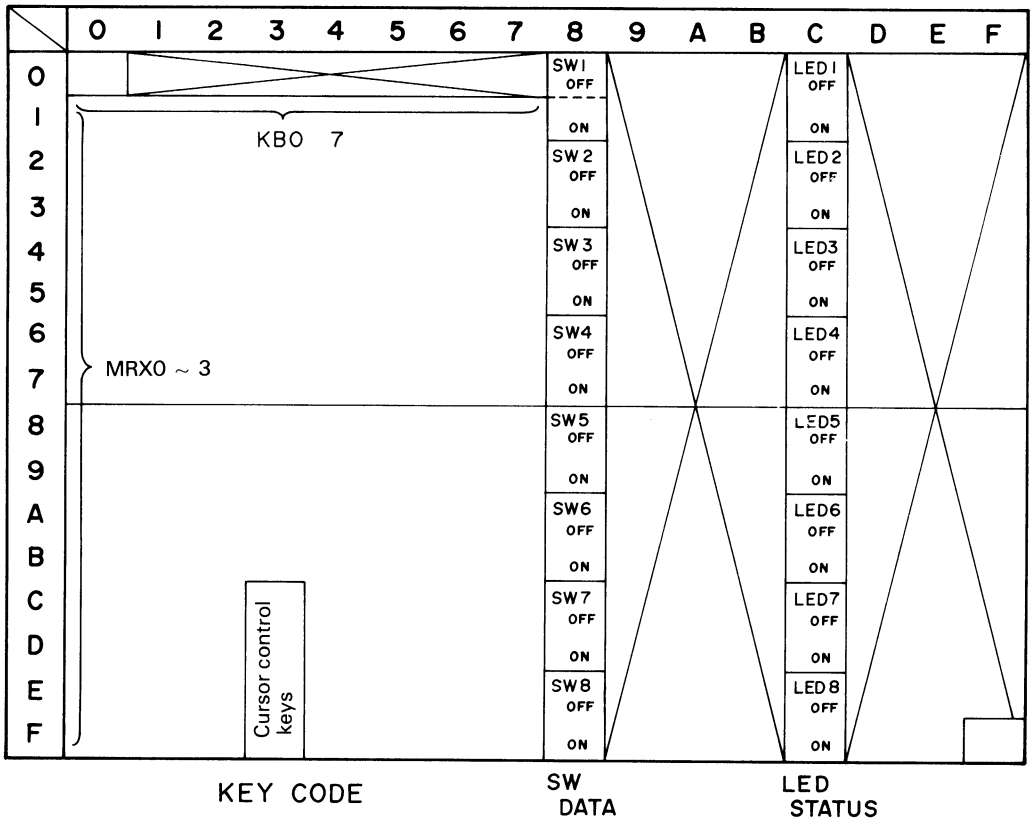


Table 7-3

KEYBOARD SCAN CODES (HASCI)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0			SHIFT (R)	SHIFT (L)		CTRL (R)	GRPH SHIFT	CTRL (L)					(H6) OFF			
1	UNDO			(H6)	TAB REL	Q	@ 2	COPY DISK					(H6) ON			
2	(H1)			SPACE	SHIFT LOCK	W	# 3	HELP								
3	STORE			Z	A	E	$ 4	STOP								
4	RE-TRIEVE			X	S	R	% 5	MAR SEL	SHIFT (R) BRK				INS OFF			
5	PRINT	ENTER	3	C	D	T	¢ 6	^ ±	SHIFT (R) MAKE				INS ON			
6	INDEX	·	2	V	F	Y	& 7	! 1	SHIFT (L) BRK				SHIFT LOCK OFF			
7	MAIL	0	1	B	G	U	* 8	TAB	SHIFT (L) MAKE				SHIFT LOCK ON			
8	(H2)	=	+	N	H	I	(9	TAB SET					(H4) OFF			
9	MENU	6	9	M	J	O	) 0						(H4) ON			
A	CALC	5	8	' ,	K	P	— -		CTRL (R) BRK				DRAW OFF			
B	SCHED	4	7	: .	L	1/4 1/2	+ =		CTRL (R) MAKE				DRAW ON			
C	DRAW	(H5)	—	↑	; :	[<	° \		GRPH BRK				SCHED OFF			
D	(H3)	(H4)	X	←	▼▼ ▼	] >	⌫		GRPH MAKE				SCHED ON			
E	BOLD	STYLE	÷	→	RETURN	INSERT	⌦		CTRL (L) BRK				CALC OFF			
F	ITALIC	SIZE	DEC TAB	↓	? /	WORD	LINE		CTRL (L) MAKE				CALC ON			

Shift key

LED

When a key is pressed, the keyboard generated above matrix code only.

Table 7-4

KEYBOARD SCAN CODES (ASCII)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0													CAPS LOCKS OFF			
1	F4	LF		CAPS LOCK		Q	▼▼ 2	F3					CAPS LOCK ON			
2	F5	(A5)	(A4)	(SPACE)		W	# 3	F2								
3	F6			Z	A	E	$ 4	F1								
4	F7	000		X	S	R	% 5		SHIFT (R) BRK				INS OFF			
5	F8	↵	3	C	D	T	& 6	ESC	SHIFT (R) MAKE				INS ON			
6	F9	·	2	V	F	Y	▼ 7	! 1	SHIFT (L) BRK							
7	F10	0	1	B	G	U	(8	TAB	SHIFT (L) MAKE							
8	(A1)	+	−	N	H	I	) 9						MF4 OFF			
9	BREAK	6	9	M	J	O	Ō						MF4 ON			
A	PAUSE	5	8	< ,	K	P	= -		CTRL BRK				MF3 OFF			
B	SCRN DUMP	4	7	> .	L	' @	~ △		CTRL MAKE				MF3 ON			
C	HELP		=	↑	+ ;	{ [	¦ ¦ /		GRPH BRK				MF2 OFF			
D	(A2)	MF4	*	←	* :	}]	BS		GRPH MAKE				MF2 ON			
E	(A3)	MF3	/	→	↵	INS	HOME						MF1 OFF			
F	MF1	MF2	'	↓	? /	DEL	CLS						MF1 ON			
									⇑ Shift key				⇑ LED			

When a key is pressed, the keyboard generated above matrix code only.

Table 7-5

7.6 N-Key Rollover Function

Suppose that two keys, G and F, are depressed as shown in Fig. 7-6. The depression is detected and the keys are identified as the key matrix is scanned.

If the V key is also depressed, current would flow via the path shown in Fig. 7-6 (b) and it could not be distinguished from the depression of key B.

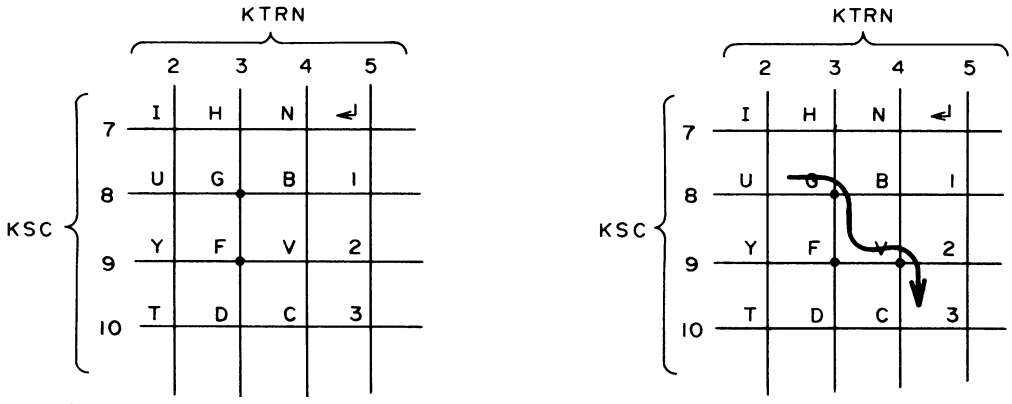
In the QX-10, if more than one key is depressed at a time (during a cycle of scanning), the keyboard encoder program does not work until only one key is depressed.

Note that two-key rollover is employed for the SHIFT, CTRL, and GRPH SHIFT keys, which are normally used along with other keys, by installing blocking diodes.

The keyboard is provided with a 32-byte buffer for transmitted data. When more than one key is depressed one after the another, key codes will be sent out serially.

Transmitted data are transfered to the TXD buffer from the 32-byte buffer on the FIFO baiss and further to the main unit as serial data whose format is shown in Fig. 7-5.

As to SW data, all data will be transmitted every time a status changes, regardless of the depression of other keys.



(a) G and F are identifiable individually.

(b) Current would flow as shown with the directed line and key B would be recognized as depressed.

Fig. 7-6

7.7 Repeat Function

The keyboard is provided with a repeat function so that, when a key is kept depressed, generation of its code repeats in predetermined intervals. Not only the repetition intervals but also the time when repetition is to start after the first-time generation of the code are predetermined for the system.

The repeat function works as follows.

(1) With cursor control keys, if more than one key at a time is kept depressed, the codes of the keys are generated cyclically.

(2) If more than one non-cursor control key is kept depressed, the code of the key depressed later than the others is generated repeatedly unless error results.

(3) If more than one key, including cursor control key and non-cursor control keys, is kept depressed, the code of the non-cursor control key depressed later than the other non-cursor control keys is generated alternately with the code of the cursor control key unless error results.

(4) If a key has been released in the middle of repeated generation of its code, the repeat function stops even when another key is kept depressed.

CHAPTER 8
FLOPPY DISK DRIVE SD-321

CONTENTS

8.1 General

Double sided, double density type of 5-1/4" floppy disk drive SD-321 has the features as described below:

1) SD-321 produces an ultra thin structure of 1/2 – 1/3 the convertional models.
2) The VCM (Voice coil motor) type linear actuater which is developed originally is adopted to the head drive mechanism, so it is of high reliability.
3) In order to miniaturize the circuit board and get high reliability, most of the control circuit is integrated to two LSIs.

8.2 General Specifications

8.2.1 Memory capacity		
(1) Unformatted	:	250k byte (Single density recording) 500k byte (Double density recording)
(2) Formatted (16 sectors/track)	:	164k byte (Single density recording) 328k byte (Double density recording)
8.2.2 Recording density (side 1, trk 39):		2938 BPI (Single density recording) 5876 BPI (Double density recording)
8.2.3 Transmission speed		125k bit/sec (Single density recording) 250k bit/sec (Double density recording)
8.2.4 Track mean speed waiting time		100 msec
8.2.5 Access time		
(1) Between tracks	:	15 msec
(2) Between tracks moving average	:	220 msec
(3) Settling time	:	15 msec
8.2.6 Motor starting time		0.5 sec
8.2.7 Motor speed		300 rpm
8.2.8 Track density		48 TPI
8.2.9 Total number of tracks		80
8.2.10 Inner circumference track radius		36.52 mm (trk 39, side 0) 34.40 mm (trk 39, side 1)
8.2.11 Outer circumference track radius		57.15 mm (trk 00, side 0) 55.03 mm (trk 00, side 1)
8.2.12 Recording system		MFM
8.2.13 R/W head positioning		Voice coil motor
8.2.14 Main axis motor		Outer rotor-type brushless transistor motor
8.2.15 Power supply		
(1) +12V (± 5%):		0.7A (typ) (at reading/writing) 1.9A (max) (at motor starting)
(2) +5V (± 5%):		0.25A (typ) 0.4A (max)
8.2.16 Power consumption:		9.7W (typ)

8.3 Outline of Mechanisms

The SD-321 is an ultra thin 5.25-inch floppy disk device and comprises the following nine elements:

1) Read/write head
2) Head access mechanism
3) Head loading mechanism
4) Disk drive mechanism
5) Disk protection mechanism
6) Disk eject mechanism
7) Index detector
8) Write protection detector
9) Control circuit

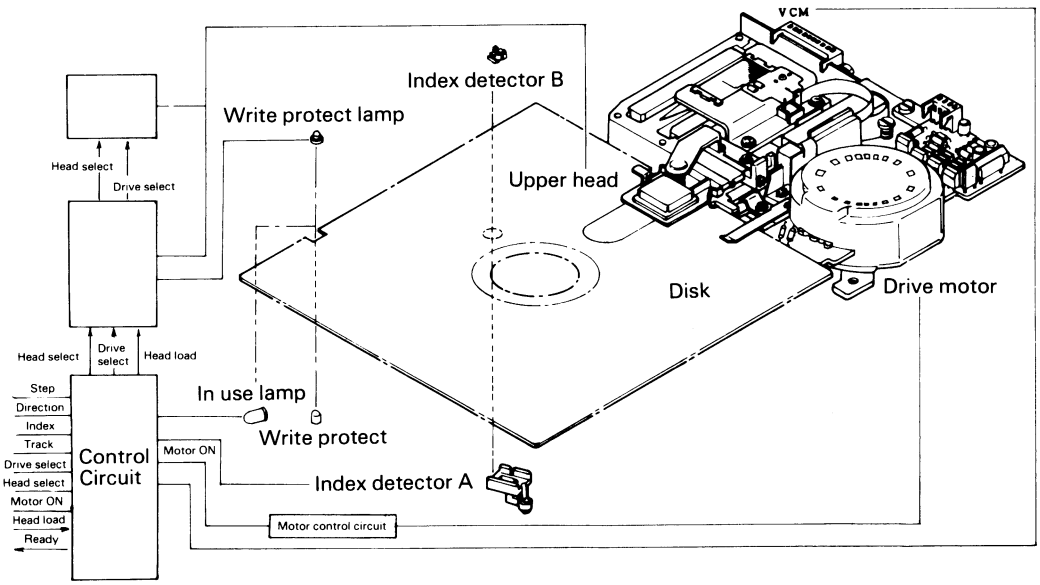


Fig. 8-1 General Block Diagram

8.3.1 Read/Write head

The read/write head uses a reliable tunnel-erase type ferrite ceramic head with erase gaps on both sides of the read/write gap. Upper and lower read/write heads are supported by upper and lower head holders by thimbles. This makes head touch to media good and minimizes the influence on the media at loading and unloading.

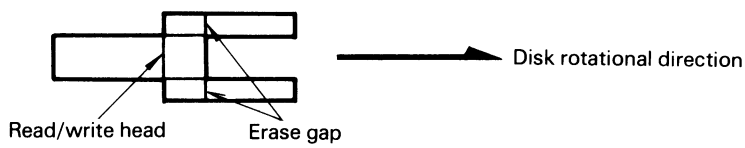


Fig. 8-2 Read/Write Head

8.3.2 Head access mechanism

The read/write head track is positioned highly accurately and delicately by the voice coil motor by directly moving it. The moving direction is selected by the host system. The voice coil motor can be moved by the distance equivalent to the specified number of tracks if one pulse is entered for one track.

8.3.3 Head loading mechanism

When the disk is inserted and the pushbutton is pressed, the collet lever gets down. At the same instant, the read/write head makes contact with trhe disk and the pad holds the disk. Data transmission is made in this state.

8.3.4 Disk drive mechanism

The disk drive pulley is connected to the disk drive motor via a belt and rotates at a speed of 300 rpm. When the disk is inserted and the pushbutton switch is pressed, the disk drive pull rotation is transmitted to the disk. The disk drive motor is a brushless DC motor, and has an FG coil inside so that it is controlled to rotate at a constant speed by the speed detection signal of the FG coil.

8.3.5 Disk protection mechanism

To protect the disk center hole, the pushbutton can not be pressed unless the disk is inserted in the correct position.

8.3.6 Disk eject mechanism

When the pushbutton switch is pressed to remove the disk, the disk is automatically ejected and pops out from the front panel.

8.3.7 Index detector

This detects the index hole on the disk to determine the data start point in the track, and comprises a pair of light emitting diodes and a phototransistor.

8.3.8 Write protection detector

This detects the disk's write protection notch, and comprises a pair of light emitting diodes and a phototransistor.

When the disk with the write protection label pasted is inserted, the control circuit inhibits writing onto the disk.

8.3.9 Control circuit

The circuit which electrically controls each mechanism's operation is divided into a main PCB, a drive motor PCB and a voice coil motor PCB. The control circuit is largely divided into the following sections. Most of these sections are constructed in the custom LSI as shown below.

1) Read/write logic and amplifier
2) Voice coil motor control circuit
3) Track 00 dectector
4) Index detector
5) Side selector
6) Write protection detector
7) Drive selector
8) Drive motor control circuit

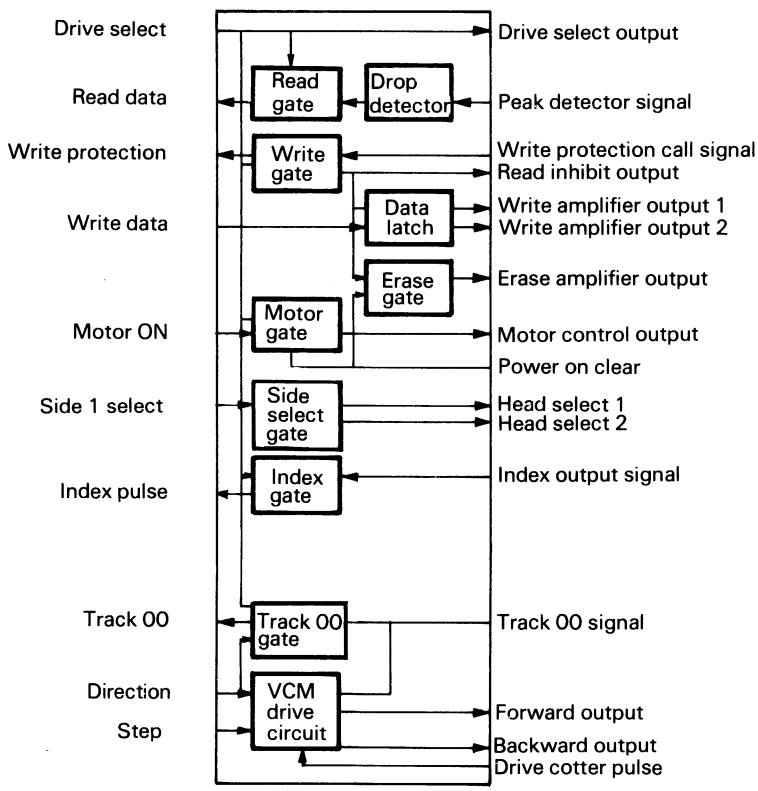


Fig. 8-3 LSI Block Diagram

8.4 Operating Principles

8.4.1 Disk drive motor

The SD-321 uses a long-life outer rotor type DC motor for disk driving. As shown in Fig. 8-4., the motor mechanism comprises a motor unit containing the frequency generator (FG) which can take out the frequency proportional to the rotor rotation, and a circuit section.

The circuit section comprises the following circuits:

Motor speed control circuit
Start/stop control circuit
Motor drive circuit

When a low-level motor drive signal is entered into the start/stop control circuit, the motor drive circuit drive transistor turns on and the disk drive motor starts operation. By applying the output of the built-in FG to the motor speed control circuit, the motor drive circuit drive transistor is controlled to keep the disk drive motor speed constant. When a high-level motor drive signal is entered into the start/stop control circuit, the motor drive circuit drive transistor turns off and the disk drive motor stops.

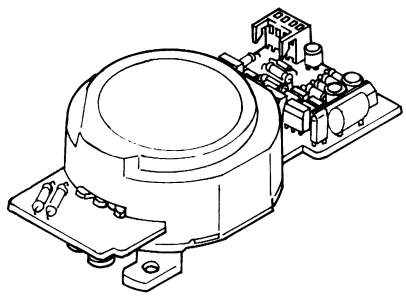


Fig. 8-4 Disk Drive Motor

8.4.2 Head access mechanism

Use of a voice coil motor in the head access mechanism improves positioning accuracy and delicacy and produces an ultra thin structure of 1/3 the conventional models. The voice coil motor (VCM) construction is shown in Fig. 8-5. The drive circuit generates a drive signal of aimed direction from a step signal and a direction signal, and moves the voice coil motor through the adder and power amplifier.

In this step, the intermediate position between the tracks adjacent to the position detector connected to the voice coil motor is detected, and the drive signal is reset. Since the position detector continously generates a control signal except for each track position, the voice coil motor is moved to the adjacent track and stopped there. The voice coil motor speed is maximum at the intermediate position, and needs to be rapidly reduced after passing the intermediate position. The voice coil motor is thus braked using the speed detector.

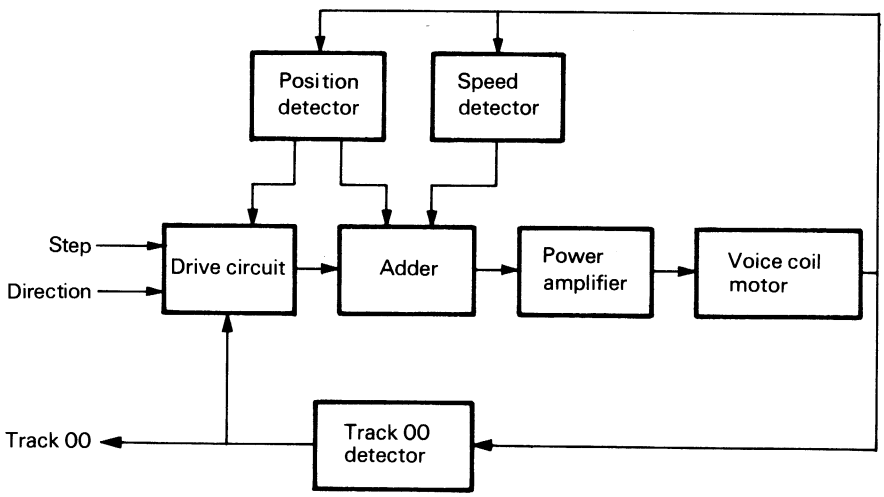


Fig. 8-5 VCM Block Diagram

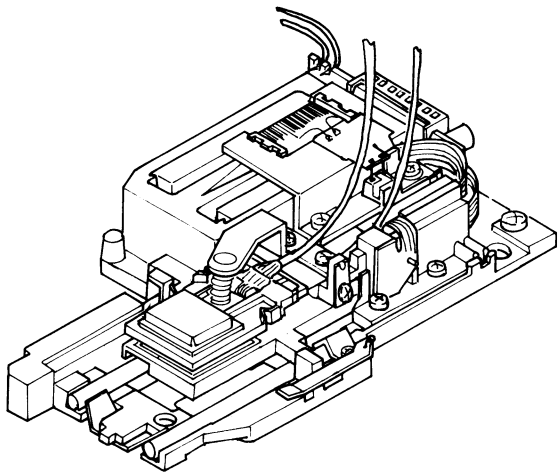


Fig. 8-6 VCM External View

8.4.3 Head loading mechanism

When the disk is inserted and the pushbutton is pressed, the collet lever gets down by being transmitted mechanically. Then, the upper head holder is released and presses the upper head to the lower head through the disk with a constant pressure, by using the upper head spring.

At the same time, the pad attached to the pad lever holds the disk between the pad and the pad receive the disk is rotated smoothly and the dust on the disk surface is eliminated by the liner provided inside the envelope.

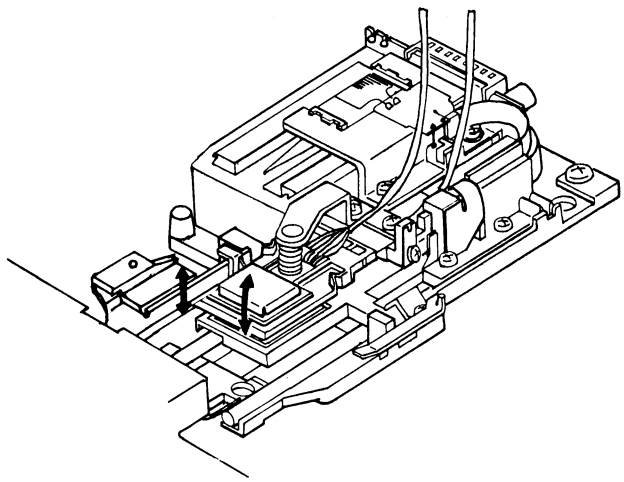


Fig. 8-7 Head Loading Mechanism

8.4.4 Operation channel

A) At disk insertion

When the disk is inserted through the front panel, the disk pushes the ejector and when the disk reaches the specified position, the eject lock pin attached to the eject lock lever falls into the groove of the ejector. At this time the eject lock lever locks the front panel cover, determining the position of the inserted disk and preventing insertion of the next disk.

Further, the eject lock lever rotates the safety lever to release the slide lever to allow it to be freely pushed. When the pushbutton switch is pressed, the collet is pushed down to clamp the disk between it and the disk drive pulley, bringing it to the position where the disk drive motor rotation can be transmitted to the disk.

As soon as the collet is pushed down, the upper head lowers to a position about 0.7 mm above the lower head, and the slide lever engages with the latch in this position and holds it.

B) At disk ejection

When the pushbutton switch is pressed, the slide lever is disengaged from the latch, the eject operation lever rotates the eject transmission lever, and the eject transmission lever disengages the eject lock pin from the ejector groove. At the same time the front panel entrance held by the eject lock lever is released, and the ejector is set free in the entrance direction.

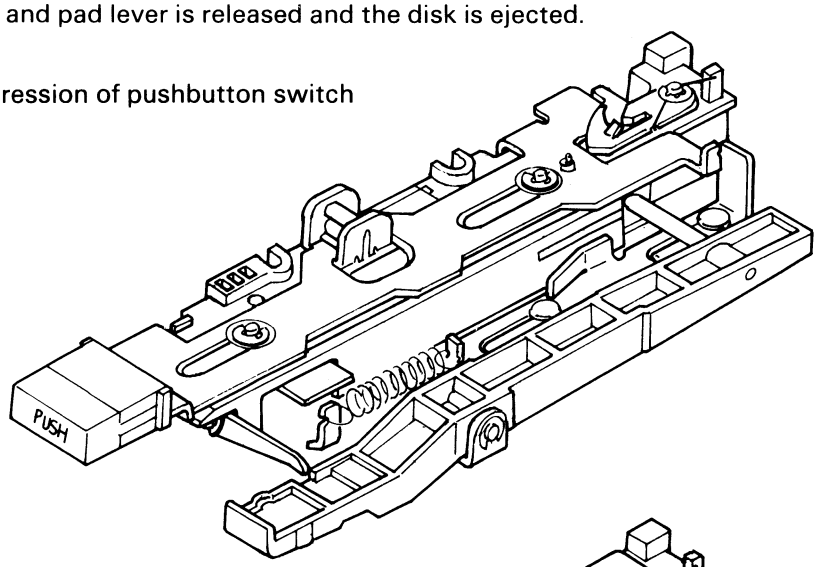
After disengaging from the eject lock pin, the ejector attempts to push out the disk, but fails as its motion is restricted by the pad lever.

As the slide lever disengaged from the latch approaches the disk setting position, the pad lever and the head rise together.

At the same time the collet also rises to set the disk free.

When the pad lever and the upper head rise to the specified position, the engagement between the ejector and pad lever is released and the disk is ejected.

Before depression of pushbutton switch



After depression of pushbutton switch

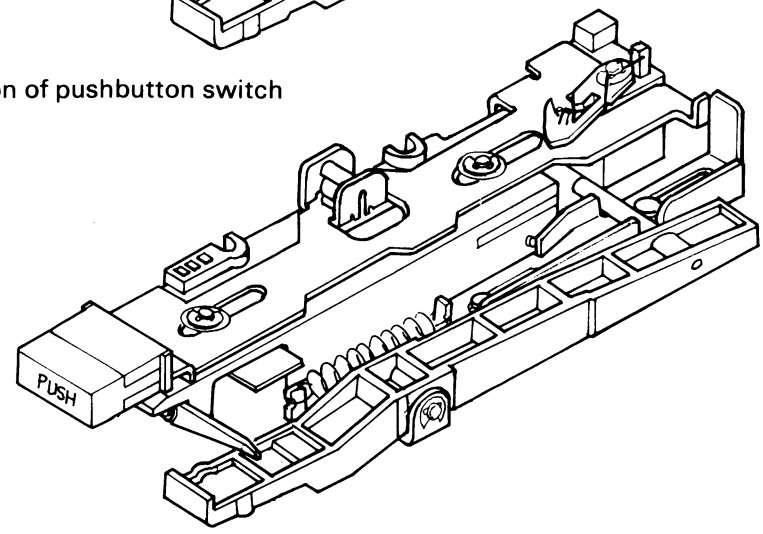


Fig. 8-8 Operation Channel Mechanism

8.4.5 Disk protection mechanism

To protect the disk, one end of the safety lever is usually engaged with the eject lock lever. When the disk is not in the correct position, the safety lever tip projects into the path of the slide lever to restrict the slide lever motion, so that the collet does not fall.

The eject lock lever also lifts the disk from the lower head surface to protect the head either at insertion or ejection of the disk.

8.5 Interface

Up to four SD-321s can be connected in a daisy chain. Input/output of all signals is compatible with TTL level. +12V and +5V are required as a power supply interface.

8.5.1 Signal Interface (Main PCB J2)

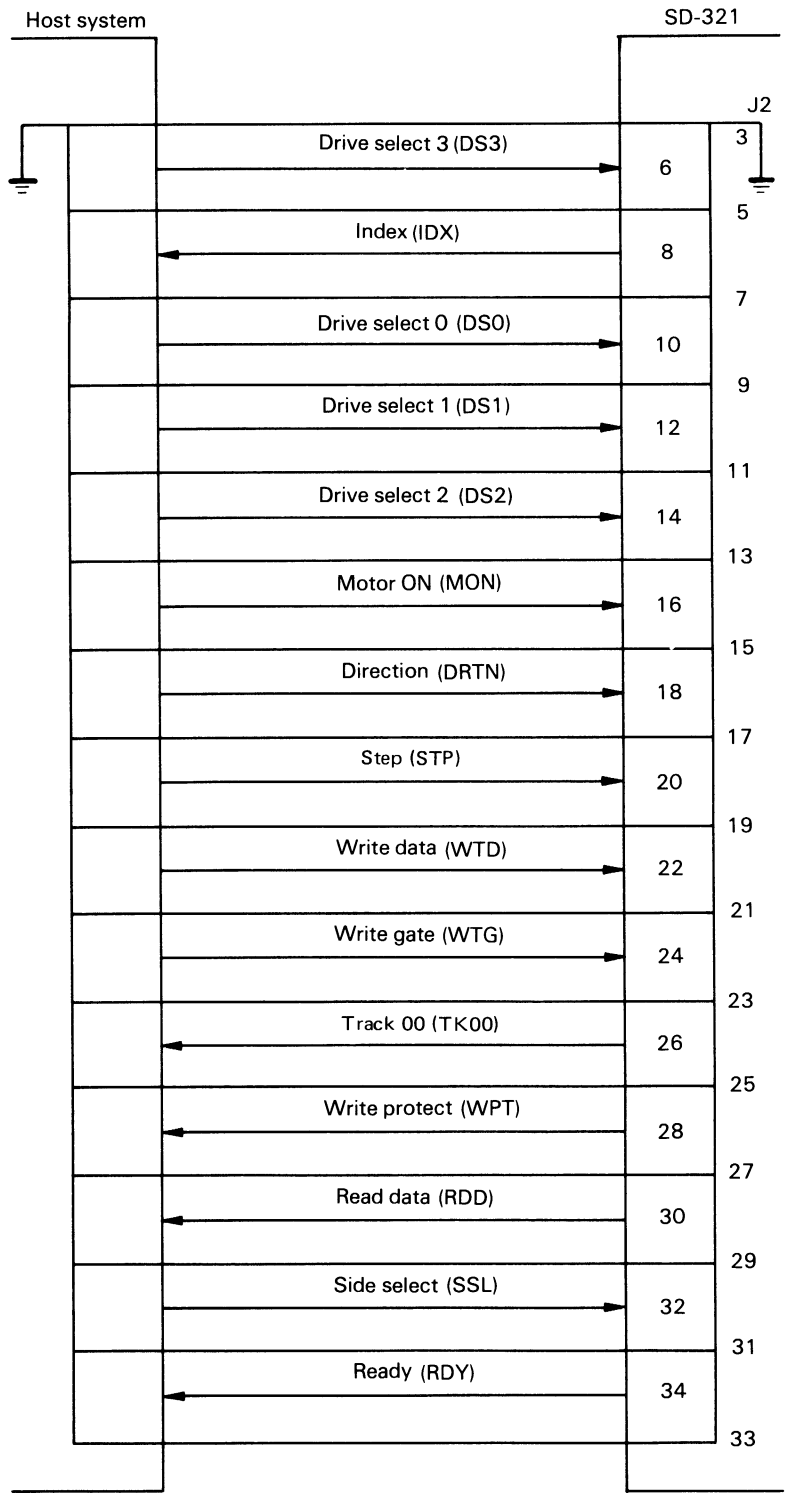


Fig. 8-9 Signal Interface

8.5.2 Electrical specifications of input and output signals

LOW = TRUE	(V_{IN}: 0V – +0.4V)
	(I_{IN} : 40 mA max.)
HIGH = FALSE	(V_{IN}: 2.5 – 5.25V)
	(I_{IN}: 0 mA Open)

The SD-321 uses SN7406 (or equivalent) as an output driver. Each input terminal is pulled up at 5V with 150Ω, and connected to LSI through a resistor of 10 kΩ.

8.5.3 Functions of input signals

1) Drive select 0 – 3 (DS0 – DS3)

The SD-321 can be connected to up to four sets in a daisy chain. Connected sets are selected by the dip switch located on the main PCB. (The SD-321 has been set to operate at drive select 0 before shipment.) Transmission/reception of input and output signals is permitted only for the drive selected by this switch.

2) Motor ON (MON)

When the motor ON signal is set to logic 0, the disk drive motor starts operation. However, seek, write and read operations should be performed after the ready signal is set to logic 0. The ready signal is set to logic 0 within one second after the motor ON signal is entered.

3) Direction (DRTN)

The direction signal determines the voice coil motor moving direction. The voice coil motor moves from track 00 to 39 when this signal is set to logic 0, and vice versa when the signal is set to logic 1.

4) Step (STP)

By entering a pulse into the step signal, the voice coil motor for positioning the read/write head can be moved in the direction specified by the DRTN signal.

The maximum response step cycle is 15 mS/track.

Step is inhibited when the write gate signal is at logic 0.

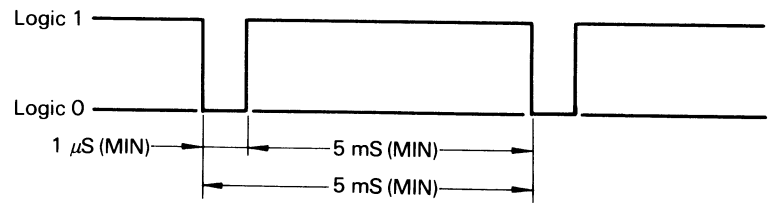


Fig. 8-10 Step Signal

5) Write gate (WTG)

The write gate signal controls write data and read data signals, makes the write data signal valid at logic 0 and the read data signal valid at logic 1. For a disk with the write protect label pasted on, the write operation is inhibited in LSI.

6) Write data (WTD)

The write data signal inverses the read/write head writing current and allows it to flow to generate a change in the magnetic flux when the input pulse changes from logic 1 to 0 in the signal line of the data to be written onto the disk. The write data signal is valid only when the write gate signal is at logic 0.

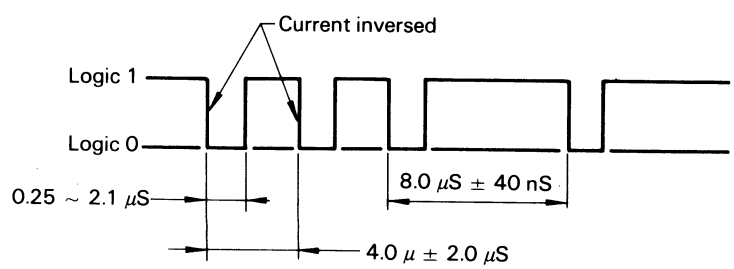


Fig. 8-11 Write Data Signal (In Case of FM Recording)

7) Side select (SSL)

The side select signal selects two upper and lower read/write heads to be used for operation.

Logic 0: SIDE 1 (Upper head)

Logic 1: SIDE 0 (Lower head)

When the head loading signal is at logic 0, the read/write head is loaded on the disk.

8.5.4 Functions of output signals

1) Ready (RDY)

The ready signal is set to logic 0 when the power is turned on, the disk is inserted or the disk rotates normally.

2) Track 00 (TK00)

The track 00 signal is set to logic 0 when the read/write head is in the position of track 00.

3) Index (IDX)

The index signal generates a pulse of logic 0 once per disk rotation.

The position where the index signal changes from logic 1 to 0 indicates the beginning of data on the track.

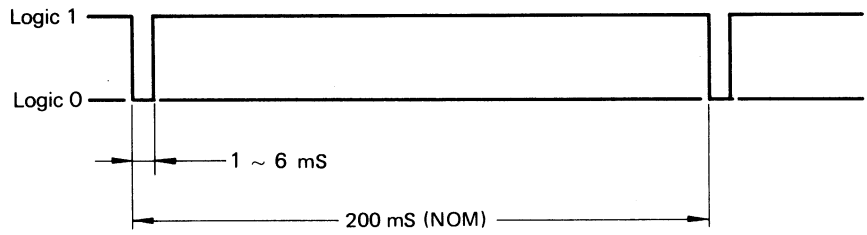


Fig. 8-12 Index Signal

4) Read data (RDD)

The read data signal outputs the raw data pulse train read by the read circuit. It is usually at logic 1 and turns to 0 when magnetization is inversed on media.

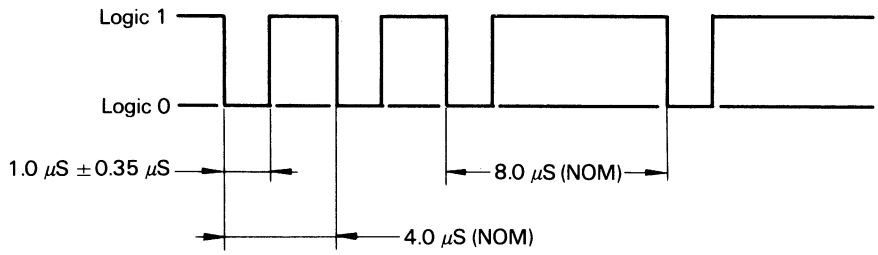


Fig. 8-13 Read Data Signal

5) Write protect

The write protect signal is set to logic 0 for a disk with the write protect label pasted on.

8.5.5 Timing

The track initial position is 00 .

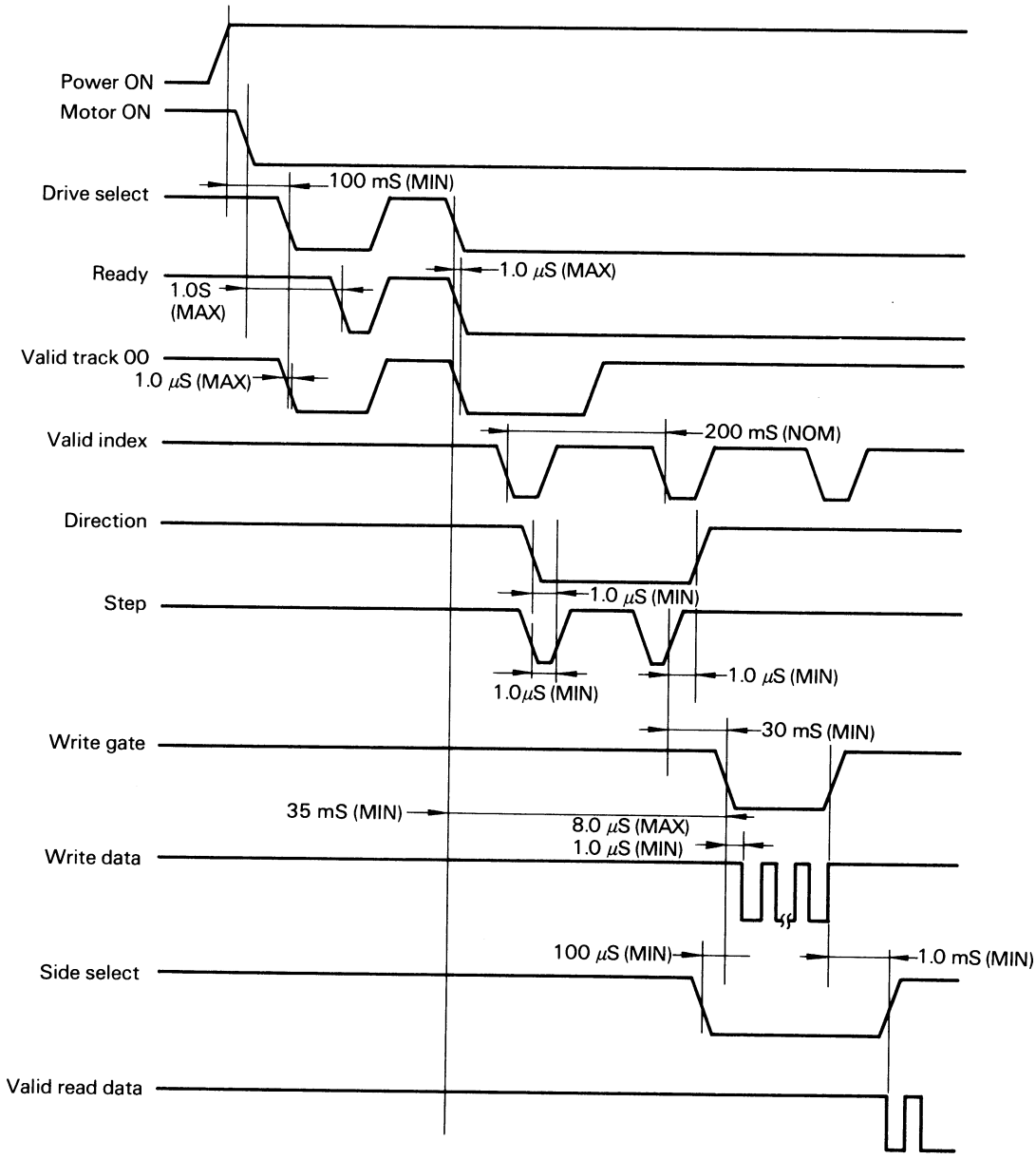


Fig. 8-14 Timing

8.5.6 Connectors

1) Power connector (J1/P1)

The DC power supply connector is located on the main PCB and uses a 4-pin AMPP/ N1-450426-0.

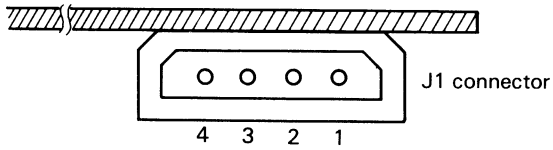
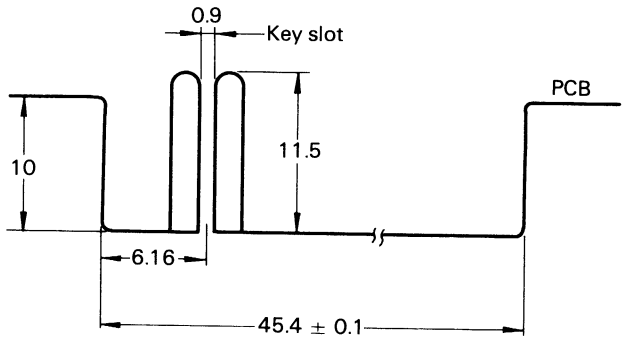


Fig. 8-15 Connector

2) Signal connector (J2/P2)

The connection of the J2 connector is a 34-pin card edge connector, and patterns 1 and 2 are omitted. The parts mounting surface is an odd number, and the soldering surface is an even number. There is a key slot between 4 and 6. The connector dimensions are given below. The following connector is recommended for the user.

Connector : 3M P/N 3463-0001
Polarity key : 3M P/N 3479-0000
Flat cable : 3M P/N 3365134



Unit: mm
Connector contact width: 1.27
Connector pitch : 2.54

Fig. 8-16 Signal Connector

CHAPTER 9
GENERAL SPECIFICATIONS FOR QX-10 OPTION CARD VERS. A

CONTENTS

9.1 Option Connector Signal Assignment Diagram

The following signals are assigned to the option slots:

Signal	Pin No.	Pin No.	Signal
GND	1	2	GND
DTB 0	3	4	DTB 1
2	5	6	3
4	7	8	5
6	9	10	7
−12V	11	12	−12V
ADR 0	13	14	ADR 1
2	15	16	3
4	17	18	5
6	19	20	7
8	21	22	9
10	23	24	11
12	25	26	13
14	27	28	15
GND	29	30	GND
CLK	31	32	GND
$\overline{\text{BSAK}}$	33	34	$\overline{\text{MEMX}}$
$\overline{\text{IRD}}$	35	36	$\overline{\text{IWR}}$
$\overline{\text{MRD}}$	37	38	$\overline{\text{MWR}}$
$\overline{\text{RSIN}}$	39	40	INT (H) 1
INT (H) 2	41	42	INT (L)
+5V	43	44	$\overline{\text{RSET}}$
+5V	45	46	+5V
$\overline{\text{DRQ (F)}}$	47	48	$\overline{\text{DRQ (S)}}$
$\overline{\text{RDY (F)}}$	49	50	$\overline{\text{RDY (S)}}$
$\overline{\text{WAIT}}$	51	52	$\overline{\text{IWS}}$
$\overline{\text{DAK (F)}}$	53	54	$\overline{\text{DAK (S)}}$
$\overline{\text{EOP (F)}}$	55	56	$\overline{\text{EOP (S)}}$
+12V	57	58	+12V
GND	59	60	GND

9.2 Description of Signals

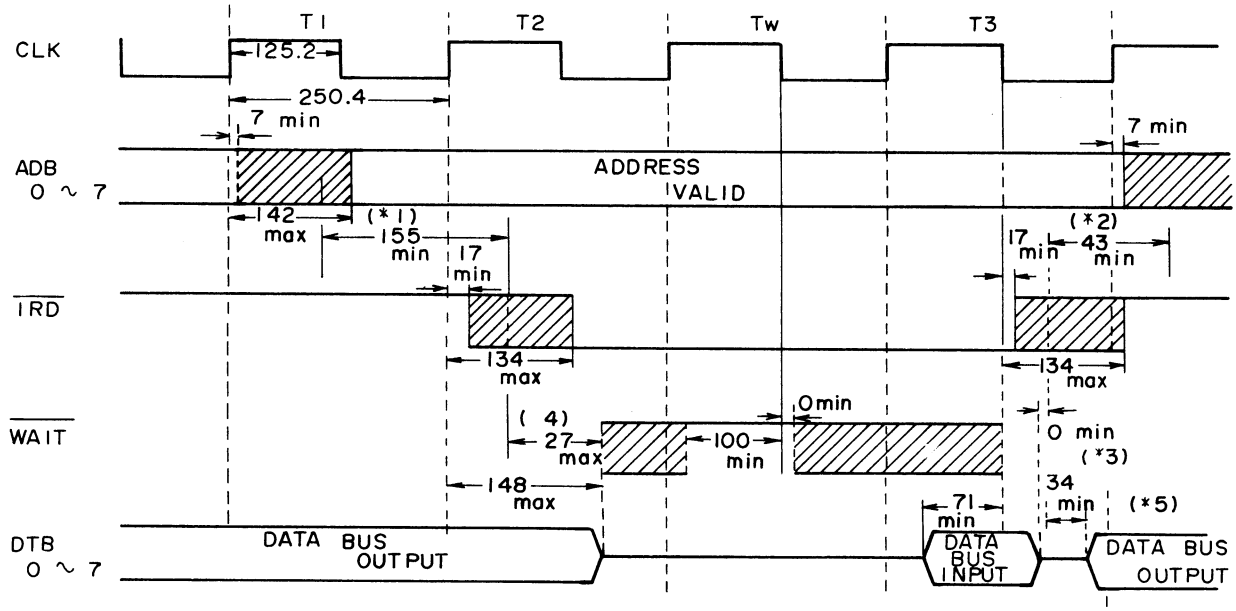
Signal	Pin No.	Description
GND	1, 2, 29, 30, 32, 59, 60	Potential OV. Return lines of respective power supplies (+ 5, + 12, – 12). All pins are connected to the signal ground on the main board.
DTB 0 — DTB 7	3 ~ 10	DATA BUS. Input/Output signals. These are buffered by the bidirectional buffer on the main board. All of these are output signals except for data input from the option slot.
ADR 0 — ADR 15	13 ~ 28	ADDRESS BUS. Output signals. These signals designate memory addresses and an input/output device.
CLK	31	SYSTEM CLOCK. Output signal. It is the main system clock (3.9936 MHz). The phase is the same as that supplied to the CPU.
$\overline{\text{BSAK}}$	33	BUS ACKNOWLEDGE. Output signal. This is a bus acknowledgement signal for CPU. When LOW, this signal indicates that the DMA is operating.
$\overline{\text{MEMX}}$	34	EXTERNAL MEMORY SELECT. Output signal. When Low, this signal indicates that memory at the option slot has been selected.
$\overline{\text{IRD}}$	35	I/O READ. Output signal. Set to LOW for data input from an I/O device; the CPU receives data at the rising edge of the signal.
$\overline{\text{IWR}}$	36	I/O WRITE. Output signal. Set to LOW for data output to an I/O device.
$\overline{\text{MRD}}$	37	MEMORY READ. Ouput signal. Set to LOW for data input from memory; the CPU receives data at rising edge of the signal.
$\overline{\text{MWR}}$	38	MEMORY WRITE. Output signal. Set to LOW level for data output to memory.
$\overline{\text{RSIN}}$	39	RESET IN. Input signal. Input of this signal form the option side resets the CPU when the signal goes LOW, while the reset operation ends when the signal is set to HIGH.
INT (H) 1	40	HIGH PRIORITY EXTERNAL INTERRUPT. Input signals. High priority interrupts applied when signals are set to HIGH.
INT (H) 2	41	These signals are connected to the 8259 on the main board.
INT (L)	42	LOW PRIORITY EXTERNAL INTERRUPT. Input signal. This signal is used in the same manner as INT (H), but the priority of the interrupt is low.

Signal	Pin No.	Description
$\overline{\text{RSET}}$	44	RESET. Output signal. This signal initializes the device at the option slot. When the system is in the reset condition, this signal is set to LOW.
$\overline{\text{DRQ (F)}}$	47	DMA REQUEST. Input signals. These signals are set to LOW to request DMA transfer from a device at the option slot. DRQ (F) has a higher DMA request level than DRQ (S).
$\overline{\text{DRQ (S)}}$	48	
$\overline{\text{RDY (F)}}$	49	DMA READY. Input signals. WAIT can be applied to the DMA controller by setting these signals to LOW. RDY (F) and RDY (S) correspond to DRQ (F) and DRQ (S), respectively.
$\overline{\text{RDY (S)}}$	50	
$\overline{\text{WAIT}}$	51	WAIT. Input signal. CPU operation can be interrupted by setting this signal to LOW.
$\overline{\text{IWS}}$	52	I/O WRITE SHORT. output signal. Used when the IWR signal does not provide sufficient time to write data from an external memory to an I/O device during a DMA transfer.
$\overline{\text{DAK (F)}}$	53	DMA ACKNOWLEDGE. Output signals. When the DMA controller receives DRQ, these signals are set to LOW when the DMA is started. DAK (F) and DAK (S) correspond to DRQ (F) and DRQ (S), respectively.
$\overline{\text{DAK (S)}}$	54	
$\overline{\text{EOP (F)}}$	55	END OF PROCESS. Output signals. These signals indicate the end of 1 block during a DMA transfer. They are set to LOW together with DAK when the last byte is sent. EOP (F) and EOP (S) correspond to DRQ (F) and DRQ (S), respectively.
$\overline{\text{EOP (S)}}$	56	
+ 5V	43, 45, 46	+ 5V power supply lines. (Up to 2.5A.)
+ 12V	57, 58	+ 12V power supply lines. (Up to 0.5A.)
− 12V	11, 12	− 12V power supply lines. (Up to 0.5A.)

9.3 I/O Port Access Timing

① I/O Read Timing

[Unit: nsec]



(*1) Address stabilization prior to $\overline{IRD}$.

(*2) Address holding time after $\overline{IRD}$.

(*3) Data holding time after $\overline{IRD}$.

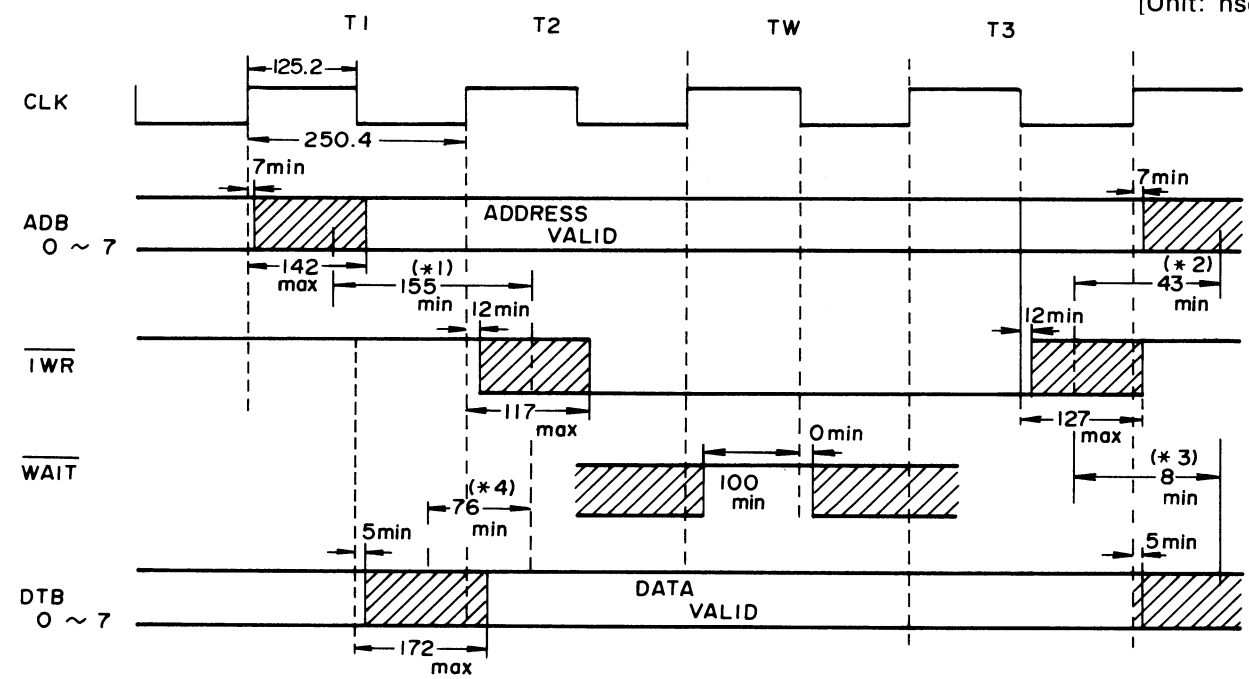
(*4) Delay before float after $\overline{IRD}$.

(*5) Floating hold time after $\overline{IRD}$.

Note: The data bus is normally in the output state, and serves as an input terminal only when data is output from the option side.

② I/O Write Timing

[Unit: nsec]



(*1) Address stabilization prior to $\overline{IWR}$.

(*2) Address holding time after $\overline{IWR}$.

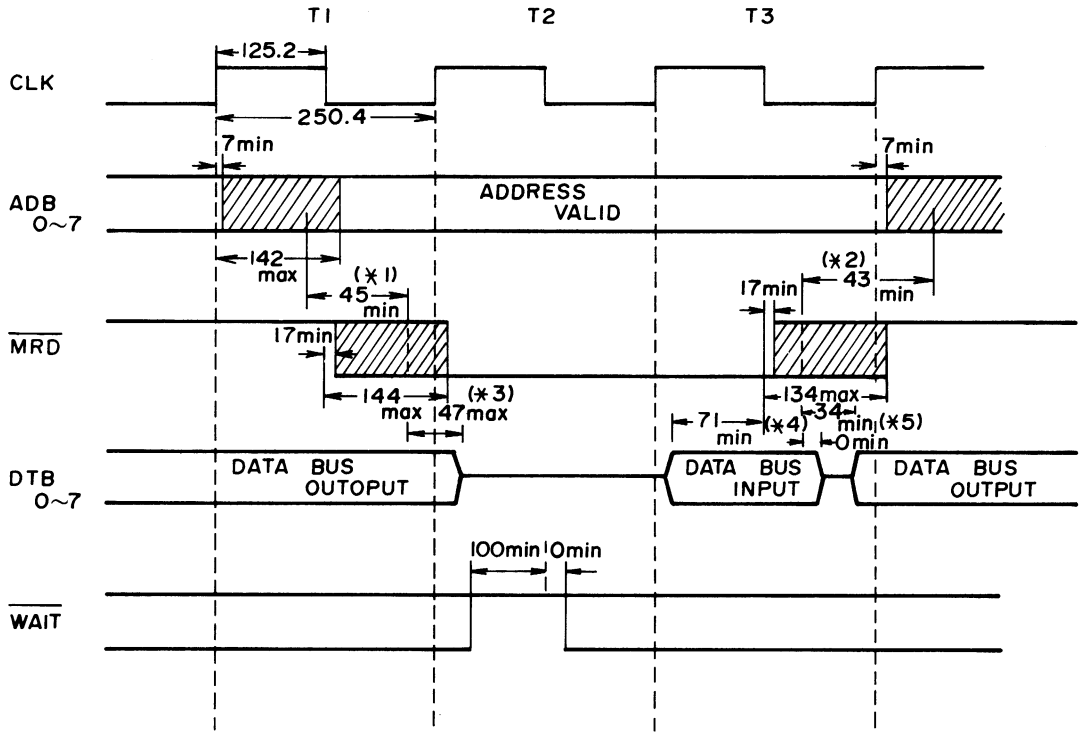
(*3) Data stabilization after $\overline{IWR}$.

(*4) Data stabilization prior to $\overline{IWR}$.

9.4 Memory Access Timing

① Memory read timing

[Unit: nsec]



(*1) Address bus stabilization time preceding the falling edge of $\overline{MRD}$.

(*2) Address bus holding time following the rising edge of $\overline{MRD}$.

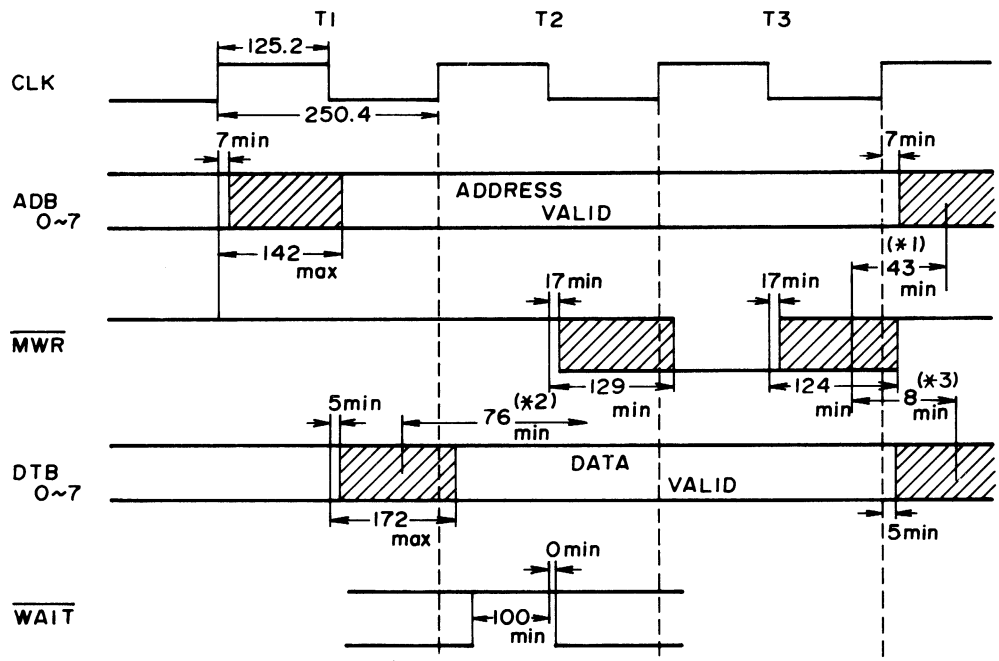
(*3) Time following the falling edge of $\overline{MRD}$ before the data bus starts floating.

(*4) Data bus holding time following the rising edge of $\overline{MRD}$.

(*5) Data bus floating time following the rising edge of $\overline{MRD}$.

② Memory write timing

[Unit: nsec]



(*1) Address bus holding time following the rising edge of $\overline{MWR}$.

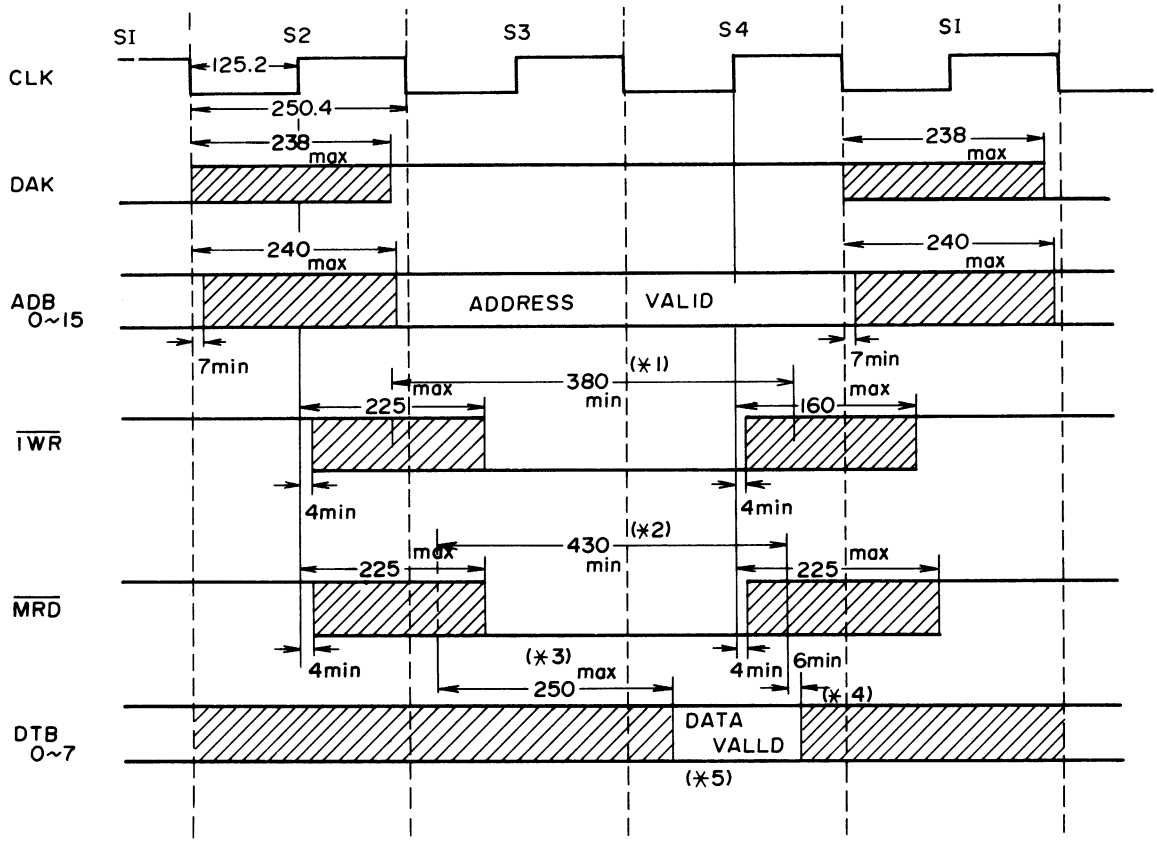
(*2) Data bus stabilization time preceding the falling edge of $\overline{MWR}$.

(*3) Data bus holding time following the rising edge of $\overline{MWR}$.

9.5 DMA Access Timing

① Memory read, I/O write timing

[Unit: nsec]



(*1) Low level pulse width of IWR

(*2) Low level pulse width of MWR

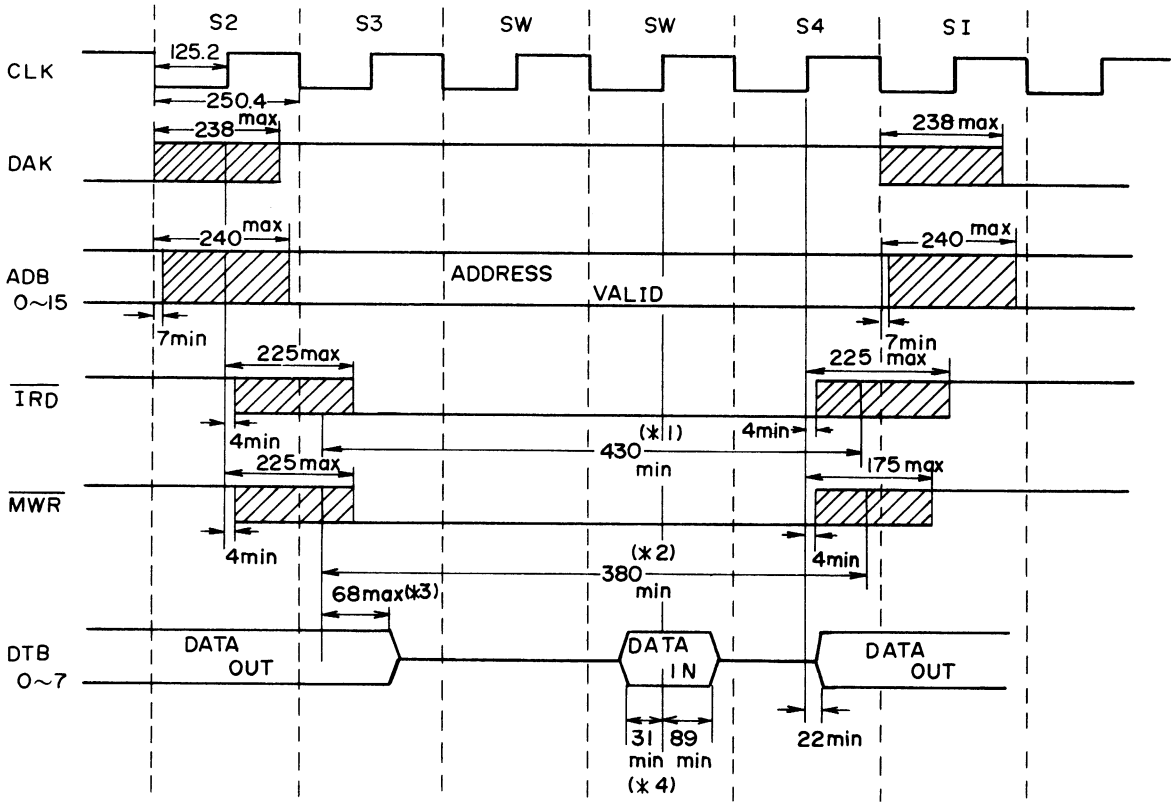
(*3) Data bus stabilization time following the falling edge of MRD

(*4) Data bus holding time following the rising edge of MRD

(*5) Data from internal memory to I/O in DMA

② I/O read, memory write timing

[Unit: nsec]



(*1) Low level pulse width of IRD

(*2) Low level pulse width of MWR

(*3) Time following the falling edge of MWR before the data bus starts floating

(*4) Limitation of input data from I/O to internal memory

9.6 I/O Port Address Map for Options

The addresses of I/O ports allocated for options are from 80H to FFH. Of these, some are already assigned to existing interface cards. Therefore, when other option cards are prepared, contact the Electronic Instruments Design Dept. of the EPSON Corporation for confirmation that the addresses are free. (This precaution must be observed to prevent the same port from being allocated to more than one option.)

Port address	0	1	2	3
80 84				
88 8C	GPIB interface			
90				Q10IE
94 98	Memory box (optical fiber) interface			
				Q100F
9C	Pulse transformer interface			Q10PT
A0	AD/DA interface			Q10AD
A4 A8 AC	RS 232C interface			Q10RS
B0 B4	Direct modem interface			Q10DM
B8 BC				
C0	Bar code, drawer interface			
C4 C8 CC				
D0 D4 D8 DC				
E0 E4 E8 EC				
F0 F4				
F8	1st level kanji Q10K1		2nd level kanji Q10K2	
FC	Multifont Q10 MF			

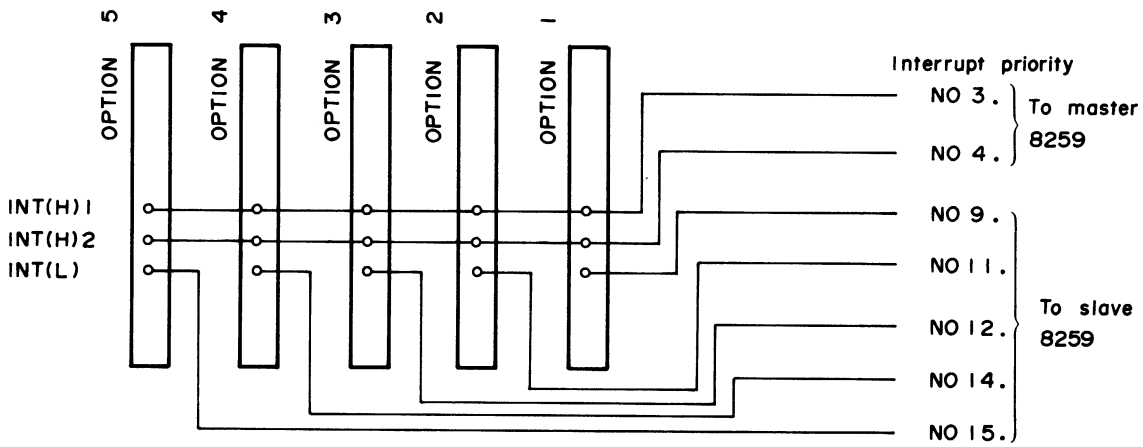
9.7 Cautions for Interface Preparation

Take note of the following when preparing option cards.

① $\overline{\text{RSIN}}$ is the input signal for system reset. Since this signal is directly input to the CPU reset terminals with no particular synchronization, it is recommended that it be synchronized with the rising edge of the read/write pulse and that the pulse width be held to less than 1 mS when D-RAM data is to be saved, however, note that the pulse width must be greater than three clocks.

② Difference between INT(H) and INT(L)

Although there are three types of interrupt request signals (INT(H)1, INT(H)2, and INT(L)) for each option connector, INT(H)1 and INT(H)2 are common to all of the connectors. Therefore, only one card which utilizes INT(H)1 or 2 can be used at any given time. However, since INT(L) is assigned to the various connectors individually, it can be used with several cards simultaneously. Connection of the INT(H) and INT(L) interrupts on the main board is shown below.



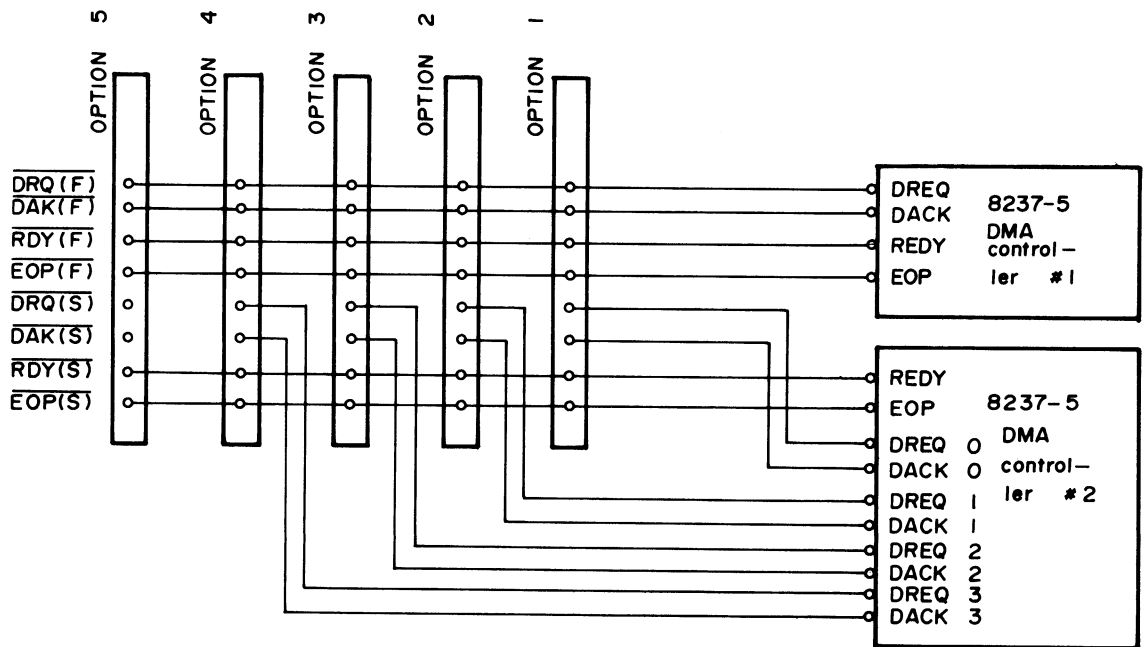
③ Difference between $\overline{\text{DRQ(F)}}$ and $\overline{\text{DRQ(S)}}$

There are also two types of DMA request signals for each option connector, $\overline{\text{DRQ(F)}}$ and $\overline{\text{DRQ(S)}}$. $\overline{\text{DRQ(F)}}$ is common to all of the connectors, while $\overline{\text{DRQ(S)}}$ is assigned individually. However, $\overline{\text{DRQ(S)}}$ and $\overline{\text{DAK(S)}}$ are not connected to option connector 5.

Also, $\overline{\text{RDY(F)}}$ and $\overline{\text{EOP(F)}}$ corresponding to $\overline{\text{DRQ(F)}}$ and $\overline{\text{DRQ(S)}}$ are common to all of the connectors, as are RDY(S) and EOP(S).

This is because all the $\overline{\text{DRQ(S)}}$ signals use the same DMA controller. Finally, $\overline{\text{DAK(S)}}$ is individually assigned to all of the connectors in the same manner as $\overline{\text{DRQ(S)}}$.

These relationships are shown in the figure below.



④ Difference between $\overline{BSAK}$ and $\overline{DAK}$

Both of these signals are active during DMA operation, but whereas $\overline{BSAK}$ is active during all DMA operations (i.e., the signal is output even when the CPU is stopped), $\overline{DAK}$ ($\overline{DAK(F)}$ or $\overline{DAK(S)}$) becomes active only when the corresponding $\overline{DRQ}$ is accepted and that DMA is operating. For this reason, it is recommended that these two signal types be used as follows.

a. $\overline{BSAK}$ should be ANDed upon I/O port address decoding and the I/O port non-selected when it is LOW. (This is because the address bus contains a memory address when $\overline{BSAK}$ is LOW.)

b. Use $\overline{DAK}$ for chip selection of the I/O port outputting the corresponding $\overline{DRQ}$.

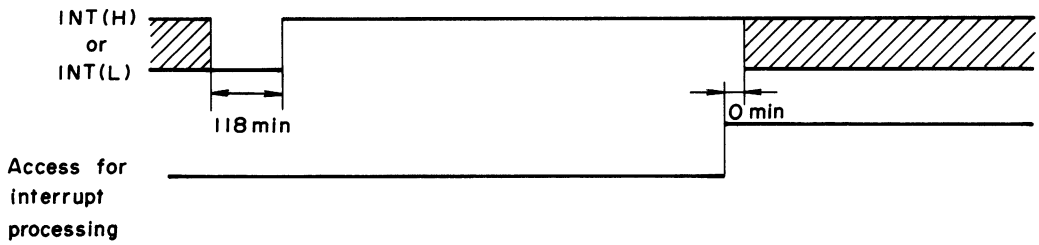
It is particularly important that $\overline{BSAK}$ is used as described, since incorrect operation will result (regardless of whether the DMA is used) if this processing is not performed.

⑤ $\overline{MEMX}$ is required when the option card includes memory. This signal becomes LOW when bit 3 in the memory bank register is 1 and neither P-ROM, C-MOS RAM, nor the common area are selected. Thus, programming considerations are necessary when external memory (on the option card) is to be used. In other words, when external memory is to be selected, bit 3 in the memory bank register must be set to 1 and bits 7-4 (the internal memory bank) must be set to 0 so that memory on the main board is not selected. Note must also be taken of the fact that the resident RAM area cannot be placed on external memory.

⑥ Interrupt processing

Interrupts from the option slots are controlled by the INT(H) or INT(L) signals. An 8259A is used as the interrupt controller in the main system, and the INT signals are connected directly to the IR terminal of this 8259A. When the INT signal goes from LOW to HIGH, it must be kept HIGH from its rising edge until the $\overline{INTA}$ from the CPU has been accepted by the 8259A; however, since the $\overline{INTA}$ signal is not output to the option connector, the INT signal must also be kept HIGH until interrupt processing is started for that device. Finally, since a rising edge is necessary, be sure to observe the rules concerning the duration of the LOW level for the INT signal. These considerations are outlined in the figure below

[Unit: nsec]



⑦ Notes concerning inclusion of options in the OS

When option cards are prepared, some additional circuits must be provided to make it possible for the OS to determine whether previously reserved options are present, and to allow it to automatically control interrupt tables and so forth. The OS must use the following sequence to determine whether the various options are connected to the option connectors.

First, data is output to the ports designated for each option (with a different port for each option); depending on the option, the content of the data may also be designated. If the applicable option is connected, an interrupt is generated, causing INT(H) or INT(L) to go HIGH. In the case of an INT(L) interrupt, the main system is able to determine the slot to which the card is connected from the interruption address, which differs according to slot number. If the option card is not connected, the OS recognizes the fact because no interrupt is generated.

Therefore, a circuit must be provided so that an intrrupt is applied when data is written into one of the port addresses assigned to options controlled by the OS, and to clear the interrupt when that same port is read out.

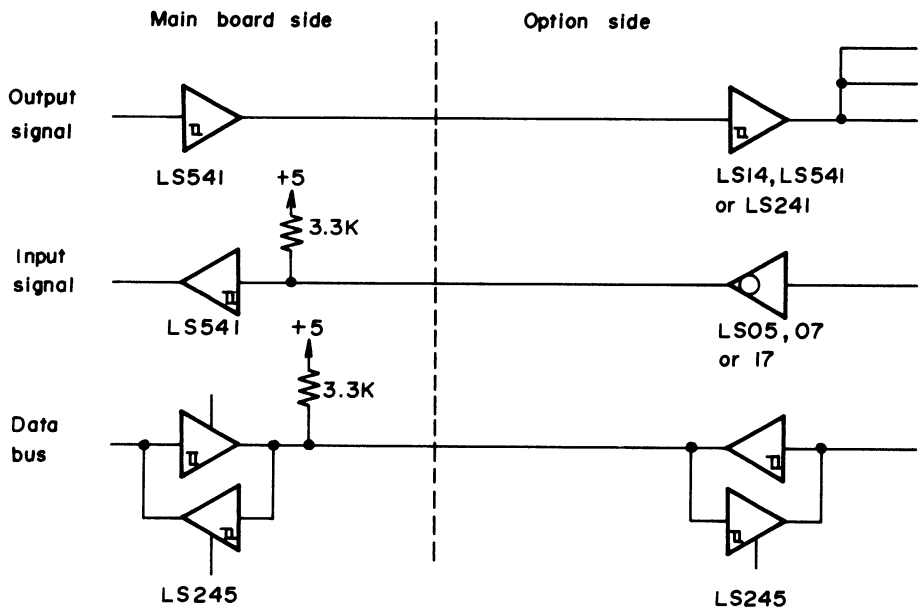
⑧ I/O signal interface

All input signals fed to the main board from the option side are pulled up by 3.3k ohm resistors. These signals (other than bidirectional data bus signals) are received by the 74LS541, and therefore should be controlled by an open collector circuit. The 74LS541 is also used for driving output signals (other than data bus signals) which are fed to the option side from the main board. The option side should be provided with a one-stage buffer for connection of multiple options.

I/O switching for the data bus must be controlled by the 74LS245 bidirectional bus buffer on the main board, as well as on the option side. This is to prevent data conflicts.

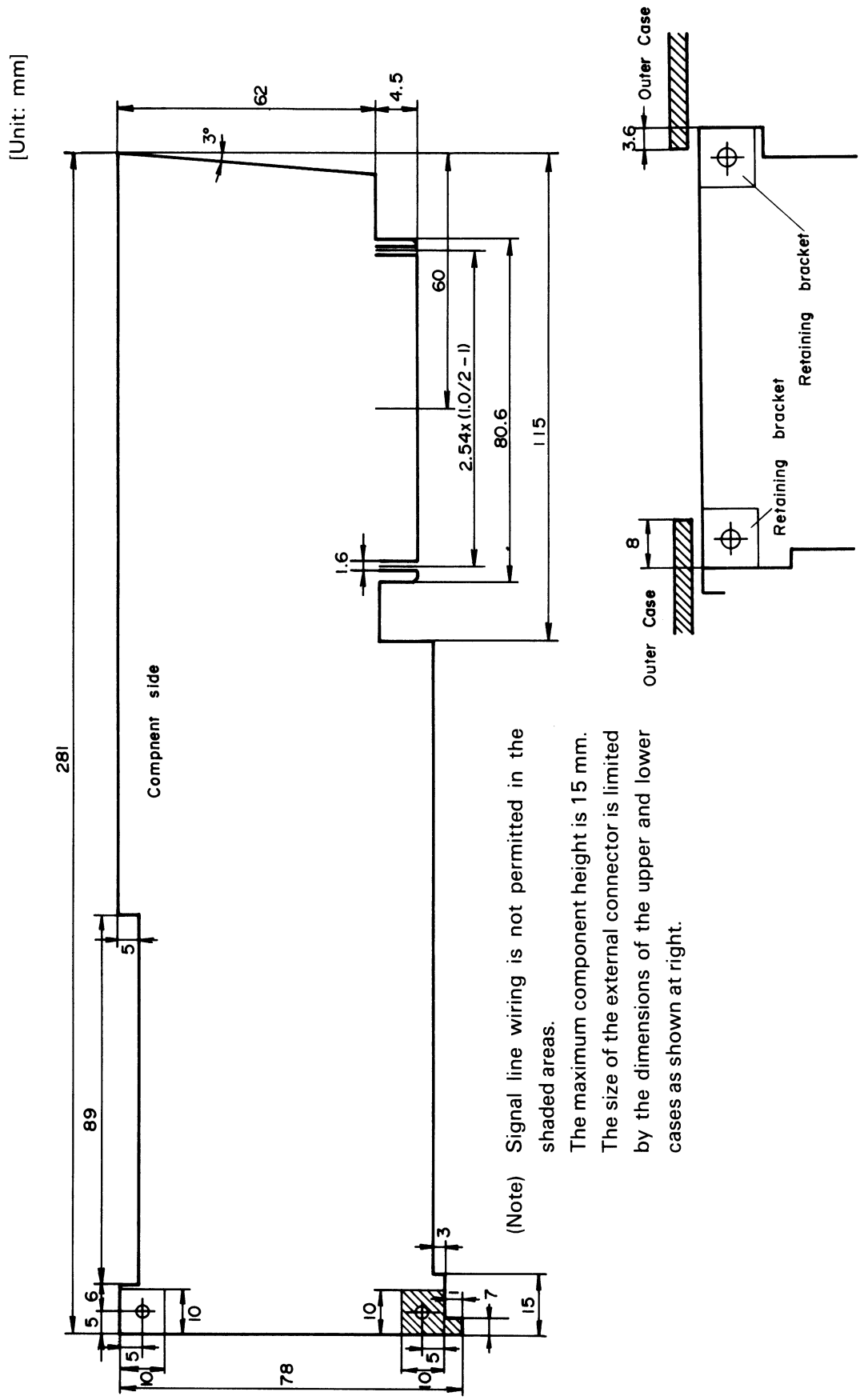
Signal lines which are not used must be left open.

The recommended I/O interface circuit is shown below:



9.8 Dimensions

Dimensions of the option card are as follows:



(Note) Signal line wiring is not permitted in the shaded areas.
The maximum component height is 15 mm.
The size of the external connector is limited by the dimensions of the upper and lower cases as shown at right.

APPENDIX

CONTENTS

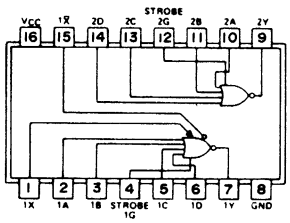
1. Table of Main ICs

Name	Part Code	Type	Location of Use	
			Q10SYM	Q10GMS
μPD416	X400104162	16K bit dynamic RAM		1B ~ 8B 2A ~ 9A
μPD449	X400004491	16K bit Static CMOS RAM	16M	
μPD765A	X400007650	Programmable Floppy Disk Controller	14H	
μPD780C-1	X400007801	8-bit Microprocessor	17J	
μPD4164	X400141640	64K bit dynamic RAM	6E ~ 9E 6F ~ 9F	1B ~ 8B 2A ~ 9A
μPD7220D	X400072200	Graphic Display Controller		10A
μPD2716	Y130801001	16K bit E-PROM	14M	
μPD2732A	*	32K bit E-PROM		2E (*)
μPD7201	X400072010	Multi-protocol Serial Controller		16B
μPD8237	X400082371	Programmable DMA Controller	19J, 21J	
μPD8253	X400082530	Programmable Interval Timer	14E, 16E	
μPD8255	X400082550	Programmable Peripheral Interface		18B
μPD8259	X400082591	Programmable Interrupt Controller	10E, 12E	
75188	X440751880	Line Driver (RS-232C level)	11B	
75189	X440751890	Line receiver (RS-232C level)	8B, 8C	
HD46818P	X400014680	Real-time Clock Plus RAM	21B	

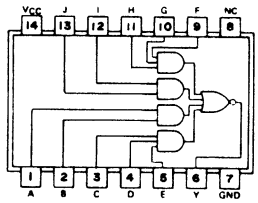
* Y130800701 P ROM QGA-1 (U.S.A)
  Y130800501 P ROM QGE-1(Europe)

2. ICs

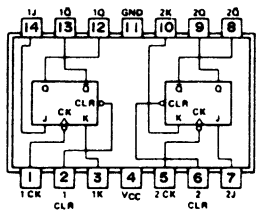
74LS23

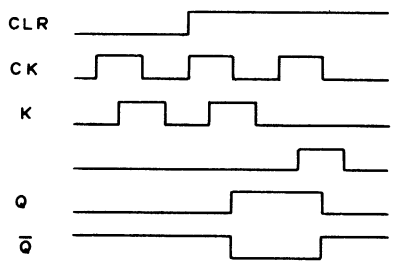


74LS54



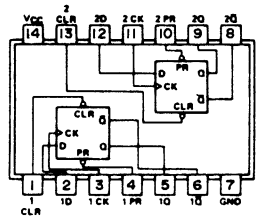
74LS73

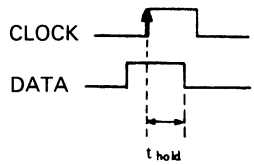




CLK	CK	K	J	Q	$\overline{Q}$
L	–	–	–	L	H
H	H/L	–	–	L/H	H/L
H	–Å	H	L	L → H H → L	H–L L–H
H	↓	L	H	L → H H → L	H → L L → H

74LS74

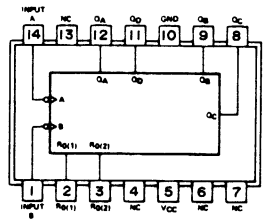


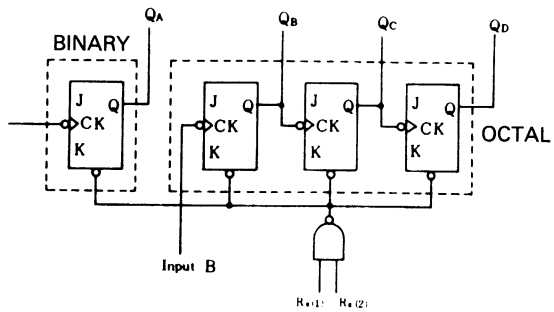


LOGIC

PR	CLR	CK	J	K	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↓	L	L	No change	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Reverse	

74LS93



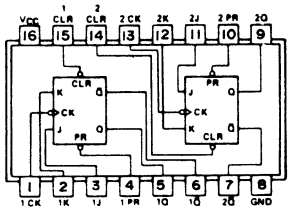


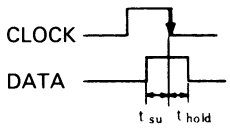
Function table

INPUT				OUTPUT		OPERATION
R_0	CK			Q_A	$Q_BQ_CQ_D$	
	A	B	PULSE			
L	CK to Q_A	CK to Q_D ≀ Q_B	0	L	LLL	COUNT
			1	H	HLL	
			2	L	LHL	
			3		HHL	
			4		LLH	
			5		HLH	
			6		LHH	
			7		HHH	
			8		LLL	
⊓	×	×	–	L	LLL	CLEAR

$R_0 = R_{0(1)} \cdot R_{0(2)}$

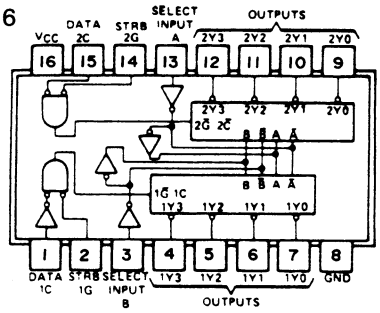
74LS112

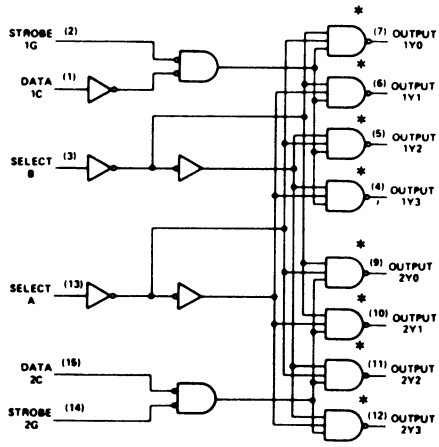




PR	CLR	CK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	No Change	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Reverse	

74LS156





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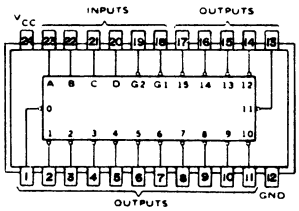
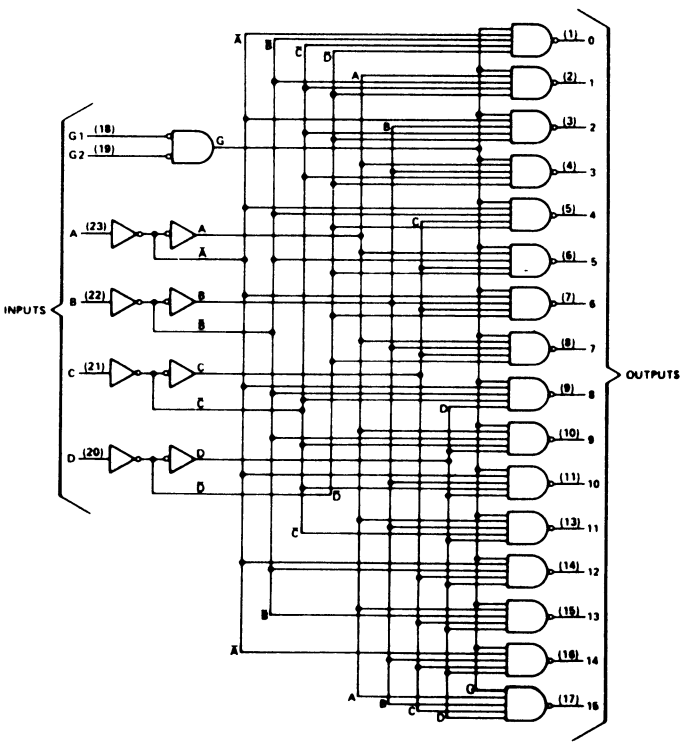


2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

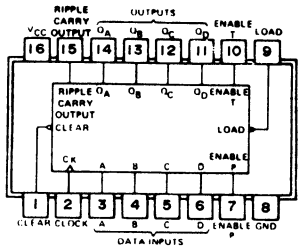
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H



3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

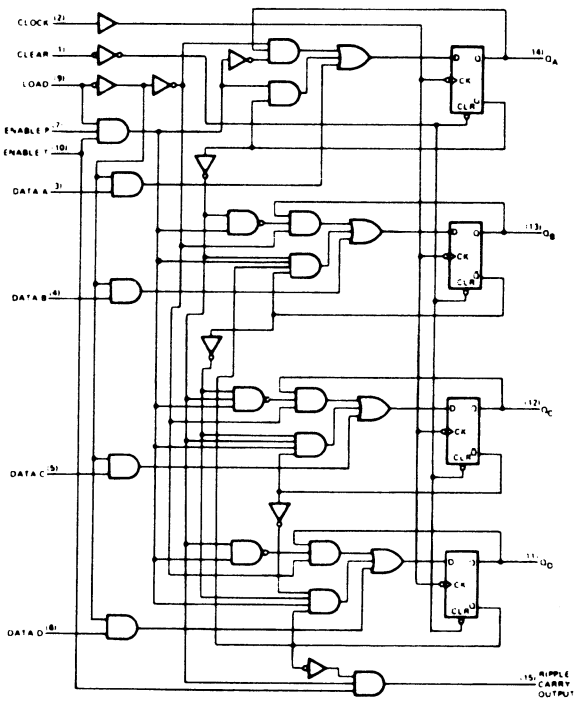
74LS161



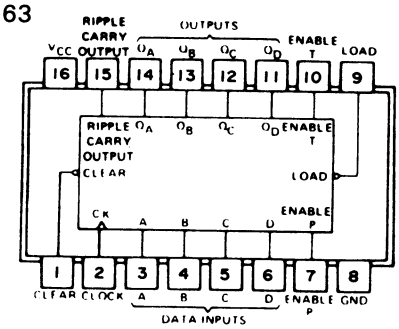
FUNCTION TABLE

INPUT					OUTPUT		OPERAITON
Clear	Load	CK	Enable P	Enable T	$Q_A Q_B Q_C Q_D$	Ripple Carry	
H	H	↑	H	H		—	COUNT
H	L	↑	X	X	$D_A D_B D_C D_D$	—	DATA SET
↓	X	X	X	X	L L L L		CLEAR
H	X	X	X	H	H H H H (H L L H)	⊓	—

( ) is at the time of 160



74LS163

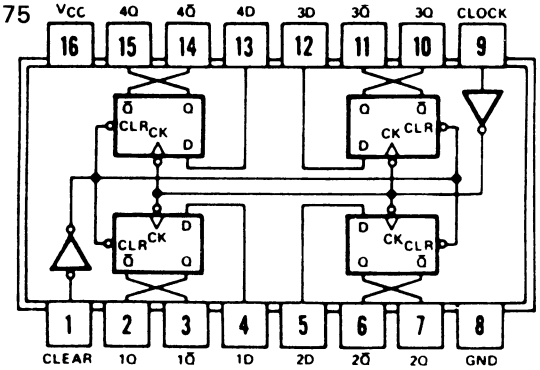


FUNCTION TABLE

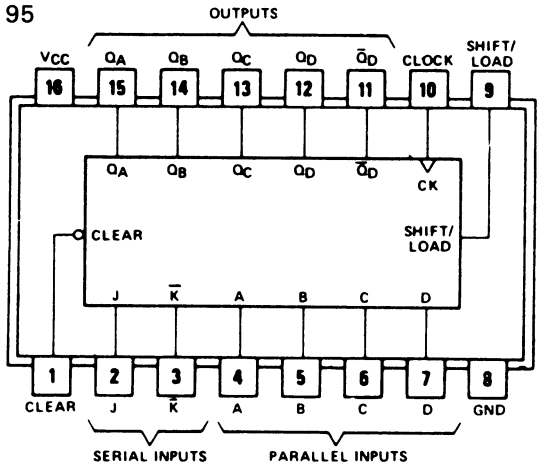
INPUT					OUTPUT		OPERATION
Clear	Load	C K	Enable P	Enable T	$Q_A Q_B Q_C Q_D$	Ripple Carry	
H	H	↑	H	H	——	–	COUNT
H	L	↑	X	X	$D_A D_B D_C D_D$	–	DATA SET
L	X	↑	X	X	L L L L	–	CLEAR
X	X	X	X	H	H H H H (H L L H)	⊓	——

( ) is at the time of 162

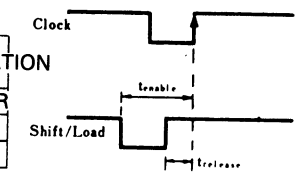
74LS175

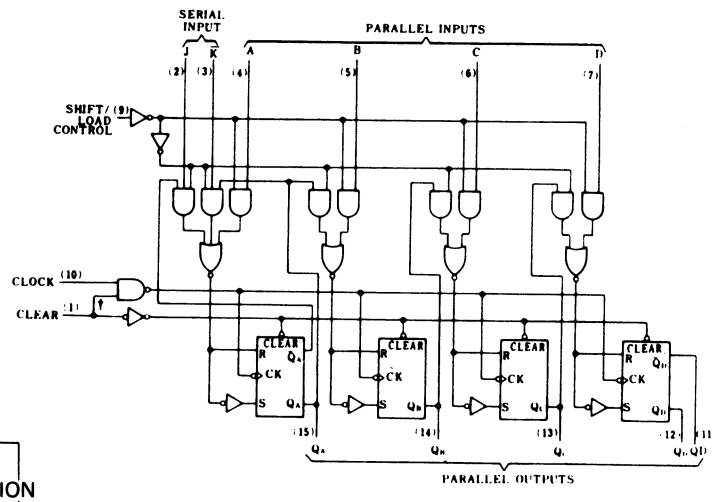


74LS195

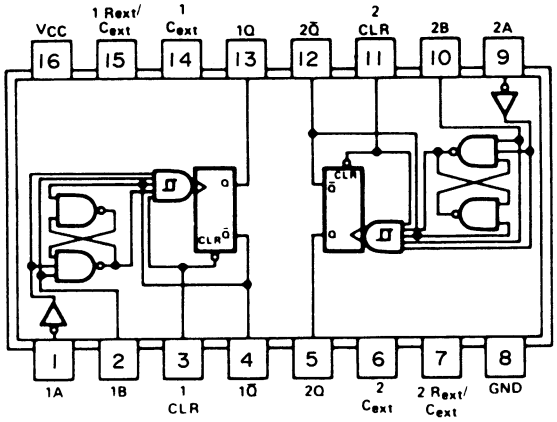


INPUT			OPERATION
Clear	Shift/Load	CK	
H	H	↑	SHIFT/R
H	L	↑	LOAD
↓	X	X	CLEAR





74LS221



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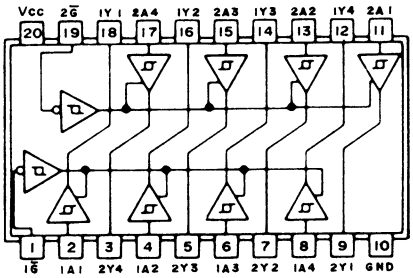
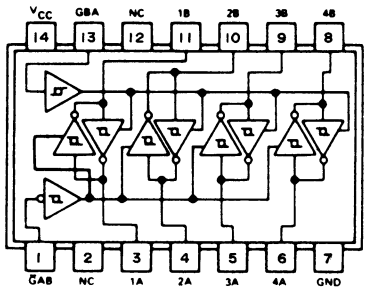
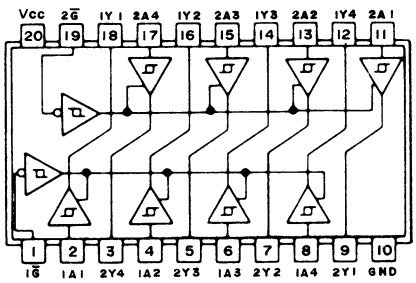


74LS242



GAB	GBA	OPEATION
H	H	A ← B
L	H	Not allowed
H	L	A OFF B
L	L	B ← A

74LS244



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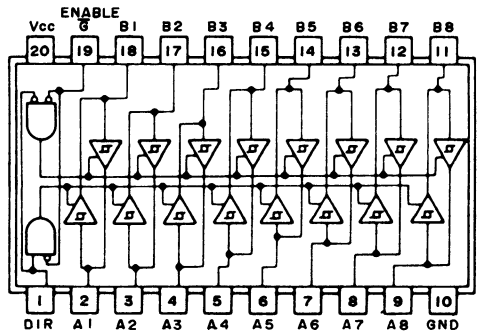

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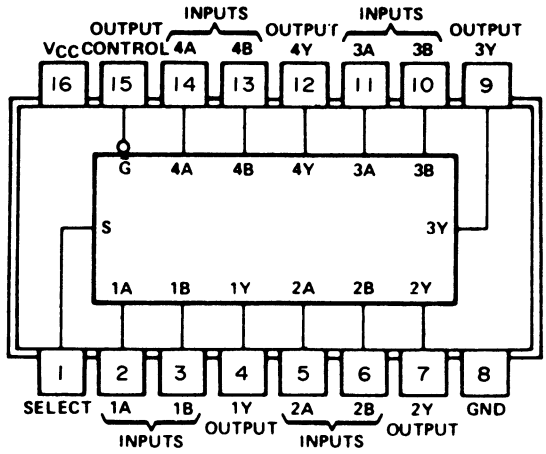
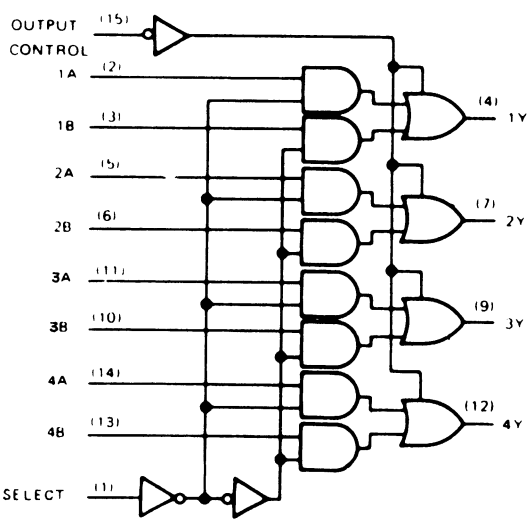


FUNCTION TABLE

INPUT		OUTPUT
Select	Output Control	Y
X	H	Z
L	L	A
H	L	B



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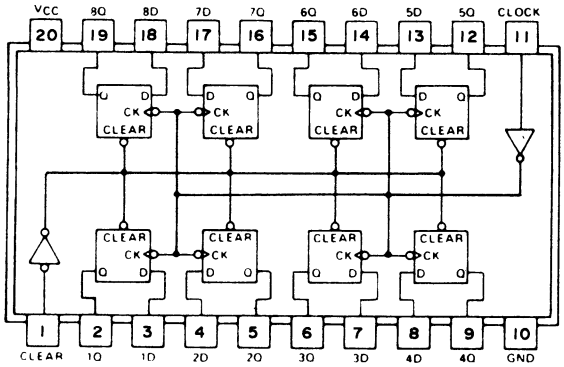

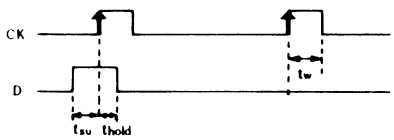

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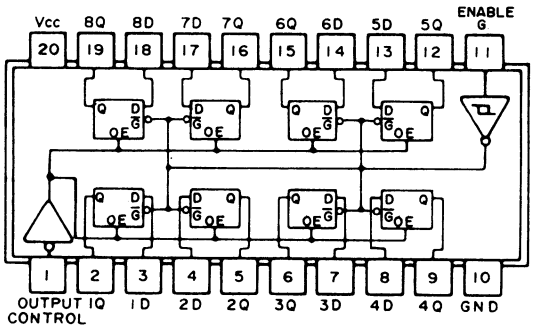

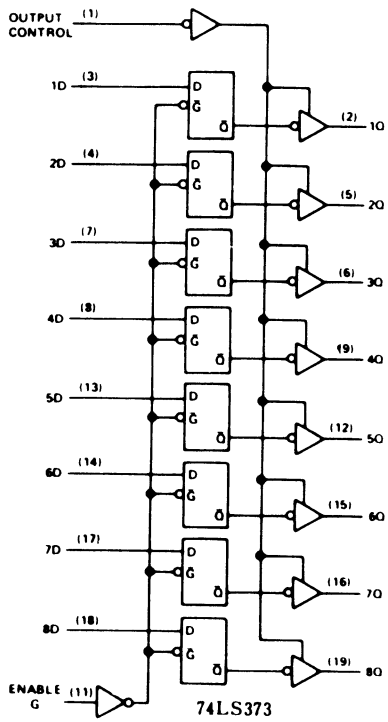

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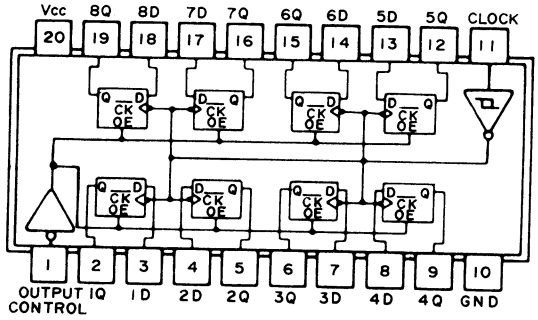
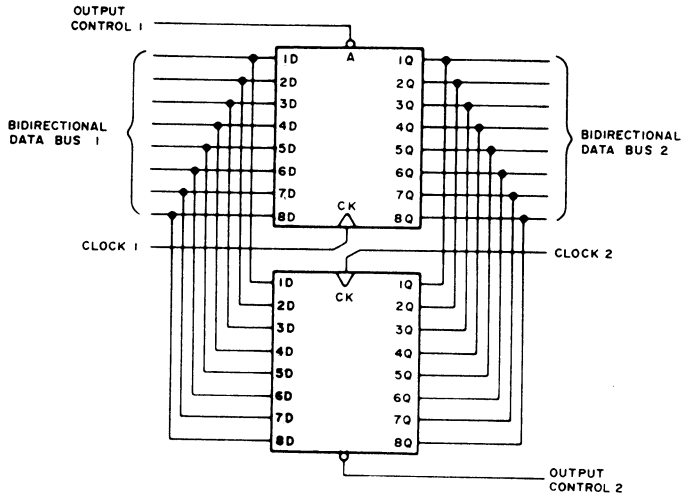
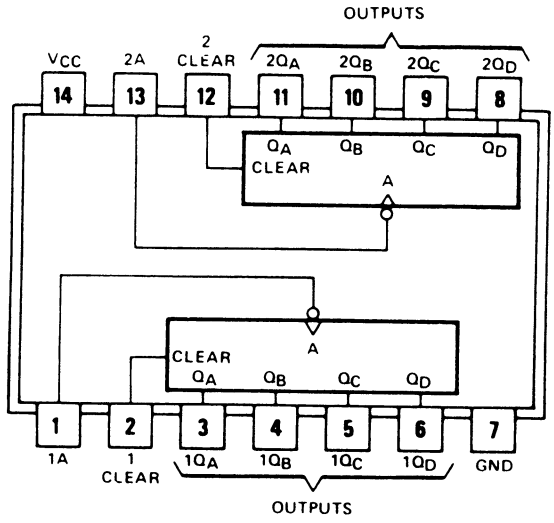
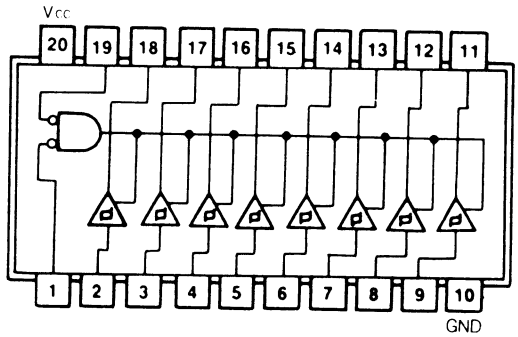




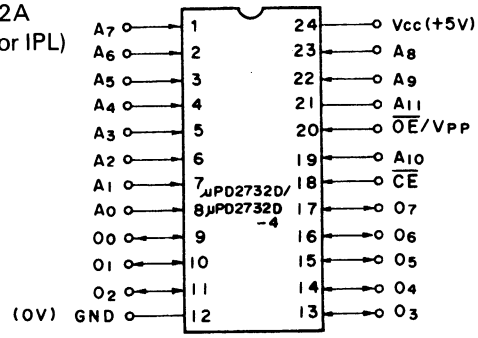
74LS393



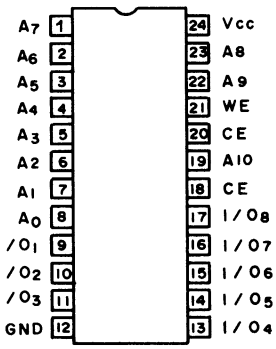
74LS541



μPD2732A
(PROM for IPL)



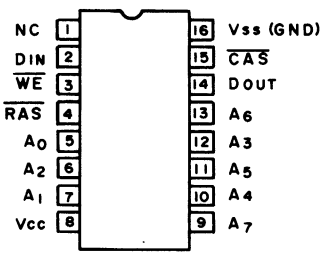
μPD449
(C MOS RAM)



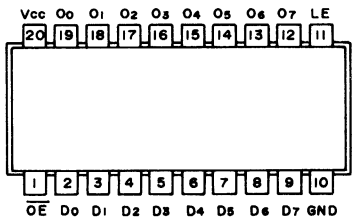
FUNCTION TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	CHIP	OUTPUT MODE	POWER CURRENT
×	H	×	Nonselected	High Impedance	I_{CCS}
H	L	×			
L	L	H	READ	D_{OUT}	I_{CCA}
L	L	L	WRITE	D_{IN}	

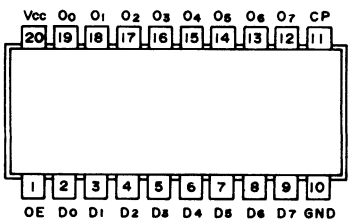
μPD4164
(Dynamic RAM)



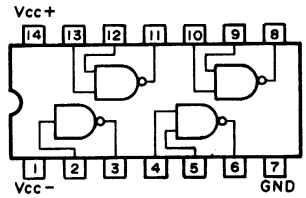
74LS573

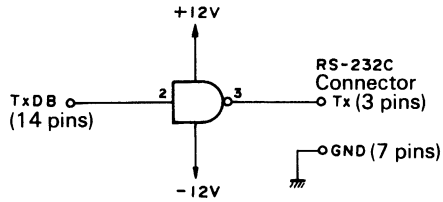


74LS574

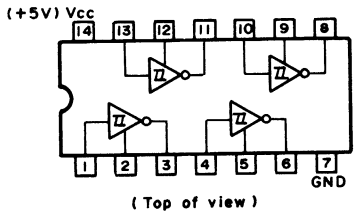


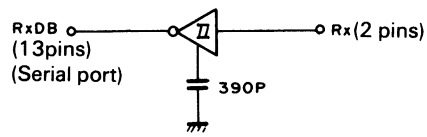
75188 (RS-232C for Interface)



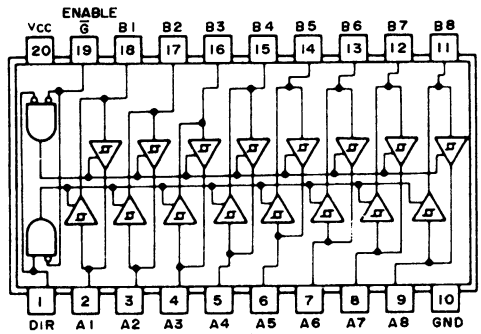


75189 (RS-232C for Interface)





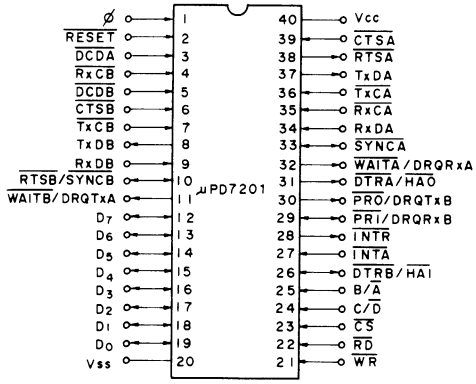
TYPES SN74LS245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



Function table

ENABLE G	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

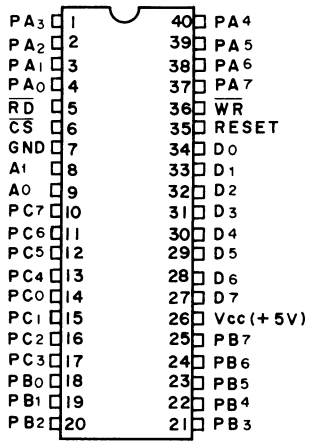
H = high level,
L = low level,
X = irrelevant



Pin (signal) name	I/O	Function
ϕ	I	3.9936 Hz clock (same as with the main CPU) is supplied.
C/$\overline{D}$	I	H: command/status L: transmitted/received data
B/$\overline{A}$	I	H: channel B L: channel A

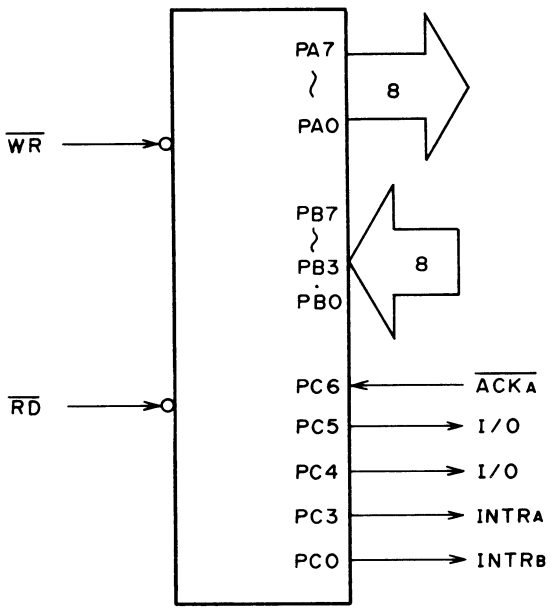
B/$\overline{A}$	C/$\overline{D}$	$\overline{WR}$	$\overline{RD}$	$\overline{CS}$	Function
0	0	0	1	0	Writes transmitted data
1					
0	0	1	0	0	Reads received data
1					
0	1	0	1	0	Writes in command/parameter register (WR 0 – 7)
1					
0	1	1	0	0	Reads from status/vector register (RR 0 – 2)
1					

$\overline{INTR}$	O	Interrupt request signal
$\overline{PRI}$ (priority output)	I	Kept at GND level in the QX-10 to indicate that no other devices of higher priority have service to interrupt offered.
$\overline{DTR}$ (data terminal ready)	I/O	Indicates to the communicating party that communication channel is ready.
$\overline{CTS}$ (clear to send)	I	Allows transmitter to send data (controls data transmission).
$\overline{DCD}$ (data carrier detect)	I	Allows receiver to receive data (control data reception).
$\overline{RTS}$ (request to send)	O	Indicates transmitter is requesting to transmit data.
RXD	I	Received data
TXD	O	Transmitted data
$\overline{RXC}$ (receive clock)	I	Received data are sampled at the rise of this signal.
$\overline{TXC}$ (transmit clock)	I	Transmitted data are output at the decay of this signal.
$\overline{INTA}$	I	Acknowledge interrupt request.

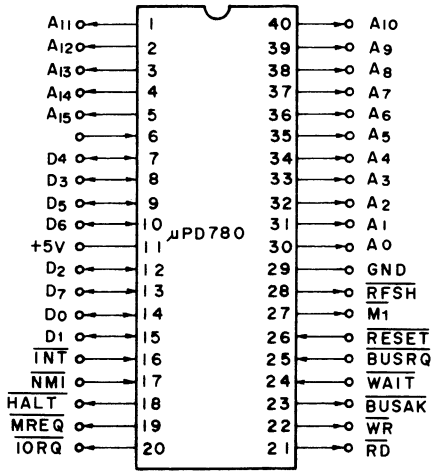


The μPD8255A (18B) is used in Mode 1 for the printer interface.

«Mode 1»

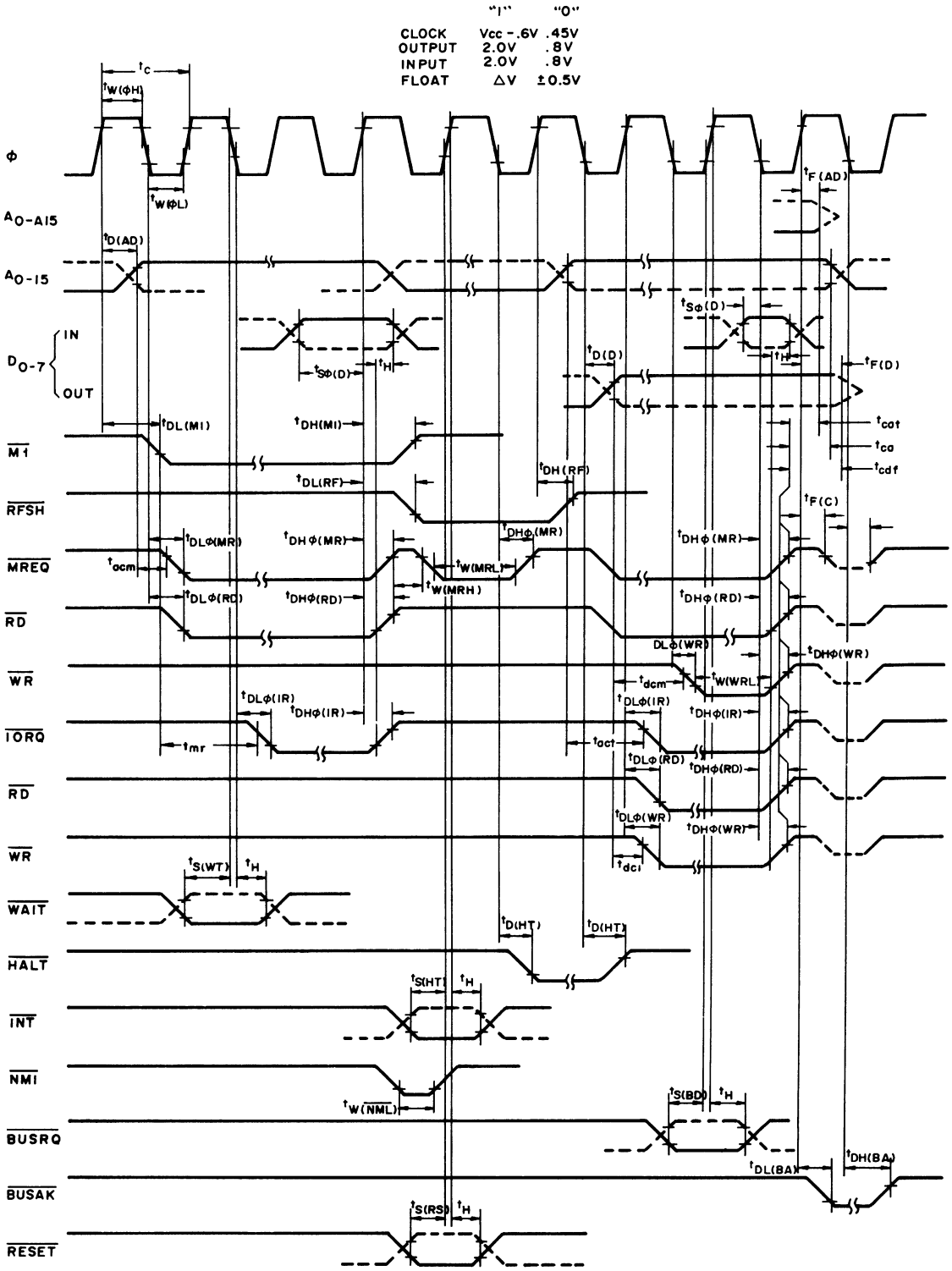


- $\overline{\text{ACKA}}$ (Acknowledge Input):
  Acknowledge signal to the reception of data from the CPU through port A
- INTR (Interrupt Request):
  Interrupt request signal (high) to the CPU



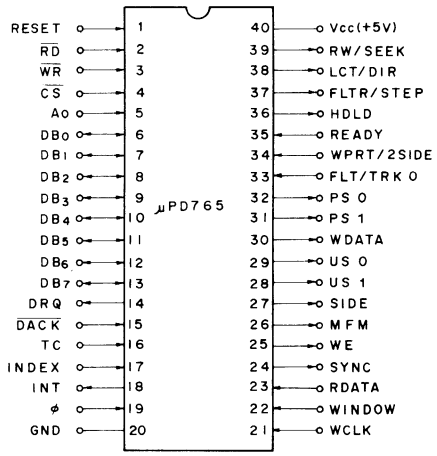
Pin (signal) name	I/O	Function
A0 – A15	O	Address bus
D0 – D7	I/O	Data bus
$\overline{M1}$	O	Indicates that the CPU is currently in operation code fetch cycle. with 2-byte instructions, $\overline{M1}$ is generated at the fetch time of each byte. In acknowledge-to-interrupt request cycle, $\overline{M1}$ is output along with $\overline{IORQ}$.
$\overline{MREQ}$	O	Indicates that address is entered on the address bus during memory read or write. During memory refresh time, this is also output for synchronization.
$\overline{IORQ}$	O	Indicates that a right I/O address is output to the address bus. If output together with $\overline{M1}$, this indicates acknowledge-to-interrupt request cycle.
$\overline{RD}$	O	Indicates the input status of the data bus.
$\overline{WR}$	O	Indicates the output status of the data bus.
$\overline{RFSH}$	O	Indicates that a refresh address is placed in the address bus lines of the least significant seven bits, so that dynamic RAM is refreshed, triggered by $\overline{MREQ}$ generated during this time.
$\overline{HALT}$	O	Indicates halt state.
$\overline{WAIT}$	I	The CPU remains in the wait state when $\overline{WAIT}$ is active, so that a low-speed memory or I/O device may be directly connected to the CPU.
$\overline{INT}$	I	Interrupt request
$\overline{NMI}$	I	Non-maskable interrupt request which is stable-high in the QX-10
$\overline{RESET}$	I	Initializes the CPU when: (1) Power on, Power off (2) Depression of reset switch (3) Resetting by an external I/O device
$\overline{BUSRQ}$	I	Puts the data bus, address bus, and 3-state output control line to high-impedance state, so that another device may use the buses. After receiving $\overline{BUSRQ}$, the CPU puts the buses to high impedance as soon as execution of the current machine cycle is completed.
$\overline{BUSAK}$	O	Indicates that the CPU has met the demand by $\overline{BUSRQ}$ and the buses are available to other devices.
ϕ	I	Single-phase clock. 3.9936 MHz is supplied in the QX-10.

► μPD780 Timing diagram



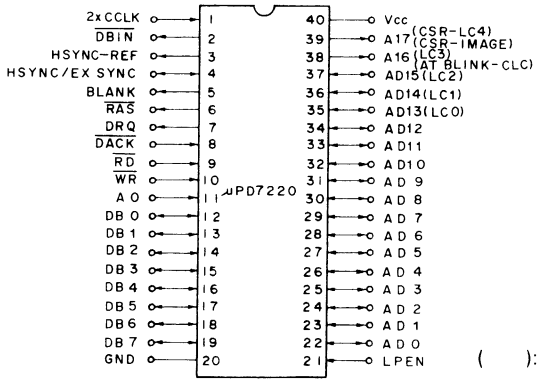
AC Characteristics (Ta = 0 ~ +70°C, Vcc = +5V ±5%)

			Z80A CPU			
Signal	**Symbol**	**Parameter**	**Min**	**Max**	**Unit**	**Test Condition**
ϕ	t_c	Clock Period	25		μsec	
	t_{w} (ϕH)	Clock Pulse Width, Clock High	110		nsec	
	t_{w} (ϕL)	Clock Pulse Width, Clock Low	110	2,000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
$A_0 - 15$	t_D (AD)	Address Output Delay		110	nsec	C_L = 50 pF
	t_F (AD)	Delay to Float		90	nsec	
	t_{acm}	Address Stable Prior to $\overline{MRFQ}$ (Memory Cycle)			nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)			nsec	
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$			nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float			nsec	
$D_0 - 7$	t_D (D)	Data Output Delay		150	nsec	C_L = 50 pF
	t_F (D)	Delay to Float During Write Cycle		90	nsec	
	$t_{S\phi}$ (D)	Data Setup Time to Rising Edge of Clock During M1 Cycle	35		nsec	
	$t_{S\bar{\phi}}$ (D)	Data Setup Time to Falling Edge of Clock During M2 to M5	50		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)			nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)			nsec	
	t_{cdf}	Data Stable From $\overline{WR}$				
	t_H	Any Hold Time for Setup Time		0	nsec	
$\overline{MREQ}$	$t_{DL\bar{\phi}}$ (MR)	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		85	nsec	C_L = 50 pF
	$t_{DH\phi}$ (MR)	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{DH\bar{\phi}}$ (MR)	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	t_{w} ($\overline{MRL}$)	Pulse Width, $\overline{MREQ}$ Low			nsec	
	t_{w} ($\overline{MRH}$)	Pulse Width, $\overline{MREQ}$ High			nsec	
$\overline{IORQ}$	$t_{DL\phi}$ (IR)	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		75	nsec	C_L = 50 pF
	$t_{DL\bar{\phi}}$ (IR)	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		85	nsec	
	$t_{DH\phi}$ (IR)	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		85	nsec	
	$t_{DH\bar{\phi}}$ (IR)	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		85	nsec	
$\overline{RD}$	$t_{DL\phi}$ (RD)	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		85	nsec	C_L = 50 pF
	$t_{DL\bar{\phi}}$ (RD)	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		95	nsec	
	$t_{DH\phi}$ (RD)	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		85	nsec	
	$t_{DH\bar{\phi}}$ (RD)	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		85	nsec	
$\overline{WR}$	$t_{DL\phi}$ (WR)	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		65	nsec	C_L = 50 pF
	$t_{DL\bar{\phi}}$ (WR)	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		80	nsec	
	$t_{DH\phi}$ (WR)	$\overline{WR}$ Delay From Falling Edge of Clock $\overline{WR}$ High		80	nsec	
	t_{w} ($\overline{WRL}$)	Pulse Width, $\overline{WR}$ Low				
$\overline{M1}$	t_{DL} (M1)	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		100	nsec	C_L = 50 pF
	t_{DH} (M1)	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		100	nsec	
$\overline{RFSH}$	t_{DL} (RF)	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		130	nsec	C_L = 50 pF
	t_{DH} (RF)	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		120	nsec	
$\overline{WAIT}$	t_s (WT)	$\overline{WAIT}$ SetupTime to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	t_D (HT)	$\overline{HALT}$ Delay Time From Falling Edge of clock		300	nsec	C_L = 50 pF
$\overline{INT}$	t_s (IT)	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	t_{w} ($\overline{NML}$)	Pulse Width, $\overline{NM1}$ Low	80		nsec	
$\overline{BUSRQ}$	t_s (BQ)	$\overline{BUSRQ}$ SetupTime to Rising Edge of Clock	50		nsec	
$\overline{BUSAK}$	t_{DL} (BA)	$\overline{BUSAK}$ Delay From Rising Edge of Clock $\overline{BUSAK}$ Low		100	nsec	C_L = 50 pF
	t_{DH} (BA)	$\overline{BUSAK}$ Delay From Falling Edge of Clock $\overline{BUSAK}$ High		100	nsec	
$\overline{RESET}$	t_s (RS)	$\overline{RESET}$ Setup Time To Rising Edge of Clock	60		nsec	
	t_F (C)	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80	nsec	
	t_{mr}	M1 Stable Prior to IORQ (Interrupt Ack.)			nsec	



Pin (signal) name	I/O	Function
φ	I	Single-phase clock. 4 MHz is supplied.
RESET	I	Makes FDC idle, drive interface outputs except PS0, PS1 and WDATA (planned), L level; outputs INT and DRQ L level; and DB to input state.
INT	O	Indicates that FDC is requesting service. This is output for every byte during non-DMA mode and, during DMA mode, on completion of command execution.
A0	I	0: Status register selected 1: Data register selected
DRQ	O	Data transfer request signal between FDC and memory by DMA
$\overline{\text{DACK}}$	I	Indicates that DMA cycle may be entered.
SYNC	O	Designates operating mode of VFO. "1" enables read and "0" inhibits it.
RW/SEEK	O	Distinguishes between read/write (RW) and seek (SEEK) drive interface signals. "0" designates RW and "1" SEEK.
HDLD	O	Loads the drive's read/write head.
SIDE	O	Selects head 0 or 1 of a double-sided disk drive. "0" selects head 0 and "1" head 1.
LCT/DIR	O	When RW/SEEK designates RW, this works as LCT to indicate that the drive's read/write head selects a cylinder beyond # 43. When RW/SEEK designates SEEK, this works as DIR to indicate seek direction (0: outward, 1: inward).
FLTR/STEP	O	When RW/SEEK designates RW, this works as FLTR to reset the fault state of the drive. When RW/SEEK designates SEEK, this works as STEP which is the seek step signal.
READY	I	Indicates drive is ready.
WPRT/2 SIDE	I	When RW/SEEK designates RW, this works as WPRT to indicate that the drive or disk is write-protected. When RW/SEEK designates SEEK, this works as 2 SIDE which indicates that a doublesided disk is mounted.
INDEX	I	Indicates the physical start of tracks on the disk.
FLT/TRK0	I	When RW/SEEK designates RW, this works as FLT to indicate that the drive is in fault state. When RW/SEEK designates SEEK, this works as TRK0 to indicate that the read/write head is positioned at cylinder 0.
TC	I	Indicates the end of read or write from the main system.
WDATA	O	Data to be written through the drive. This consists of clock and data bits.
WE	O	Enables the drive to write data.
WCLK	I	Write clock supplied to the drive. 500 kHz is used in FM mode and 1 MHz in MFM mode.
PS0 – PS1	O	Indicates to advance or delay the timing of writing WDATA In MFM mode as given below to provide read-time margin.
RDATA	I	Data read through the drive. This consists of clock and data bits.
WINDOW	I	Generated in VFO and used to sample RDATA. FDC synchronizes the data bits of RDATA with WINDOW in phase.

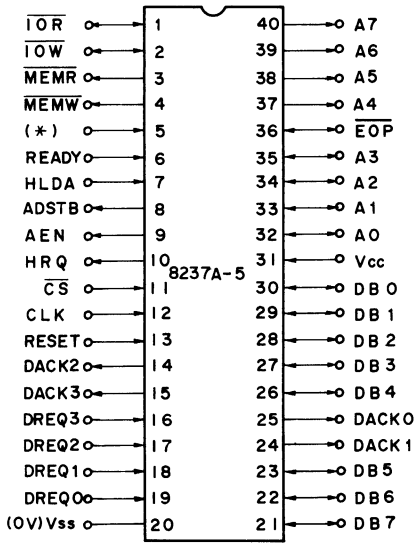
PS0	PS1	FM	MFM
0	0	Unchanged	Unchanged
0	1	–	LATE 225 ~ 250 ms
1	0	–	EARLY 225 ~ 250 ms
1	1	–	–



( ): Character display mode

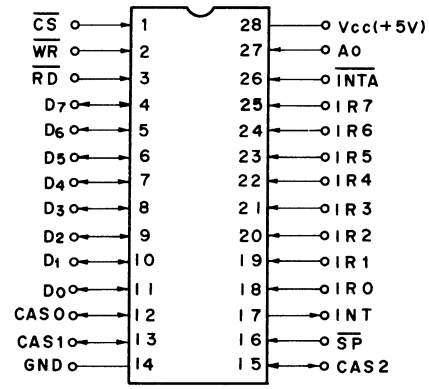
Pin (signal) name	I/O	Function
AD0 – AD12	I/O	Bidirectional address bus lines
AD13 (LC0) AD14 (LC1) AD15 (LC2)	I/O	During graphic and character-graphic mixed mode: address bus lines During character mode: line count
DB0 – DB7	I/O	Bidirectional data bus
$\overline{RAS}$	O	Memory control signal output from GDC to VRAM. $\overline{CAS}$ is generated from this. Also used as the timing signal to latch address.
$\overline{AT\ BLINK}$-$\overline{CLC}$	O	During blanking time (BLANK signal output): Clears the line counter. During tracing time (video signal ouput): Outputs attribute-blinking-timing signals
CSR-IMAGE	O	During blanking time (BLANK signal output): Outputs cursor mark During tracing time (video signal output): Outputs character/graphic area switching timing signal
A0	I	Connected to an address line of the CPU and used to designate data type
$\overline{DACK}$	I	Supplied from the DMA controller to enable the GDC to distinguish between read and write performed by DMA.
LPEN	I	Light pen strobe signal. H level signal enters when the light pen has detected light input.
DRQ	O	DMA request
$\overline{DBIN}$	O	Memory control signal output from the GDC to VRAM (timing signal used to put VRAM output to the data bus).
V.SYNC	O	Vertical sync signal
H. SYNC	O	Horizontal sync signal
BLANK	O	Blanking signal output during: (1) Horizontal retrace time (2) Vertical retrace time (3) Time between execution of SYNC and START commands (4) Draw execution time
2XCCLK	I	Supplied from an external dot clock generator. The clock frequency is determined by the relationship between the horizontal resolution in dots and the horizontal scanning time (4.1665 MHz in the QX-10).

A0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	READ STATUS FLAG
1	0	1	READ DATA
0	1	0	WRITE PARAMETER
1	1	0	WRITE COMMAND



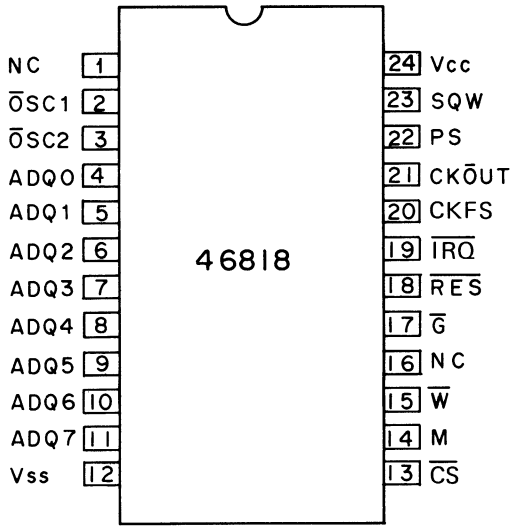
*: NC (unuse)

Pin (signal) name	I/O	Function
READY (ready)	I	Used to expand memory read/writer pulse output from 8237 to adapt to a low-speed memory or I/O device.
HLA (hold acknowledge)	I	Active-high signal indicating the CPU has left control of the system bus.
DREQ0 – DREQ3 (DMA request)	I	DMA request signals which peripheral devices use independently to receive DMA service through asynchronous channels. In a fixed-priority system, DREQ0 has the highest priority and DREQ3 the lowest. DREQ must be maintained until DMA becomes active.
DACK0 – DACK3 (DMA acknowledge)	O	Acknowledge signals to DMA request which inform specific peripheral devices of acceptance of DMA request.
ADEN (address enable)	O	Enables the latch, holding the most significant eight bits of address, to output them to the address bus.
ADSTB (address strobe)	O	Strobes an external latch for the most significant byte of address.
HRQ (hold request)	O	Hold request signal to the CPU. This requests control of the system bus.
$\overline{EOP}$ (end of process)	I/O	Information on completion of DMA service is available at this terminal. Signal $\overline{EOP}$ is generated internally or externally. This terminal must be connected to H level through a pull-up resistor to prevent entry of wrong signals.
DB0 – DB7	I/O	During DMA cycle, the most significant eight bits of address are output to the data bus and placed in an external latch, strobed by ADSTB.
A0 – A3 (address)	I/O	During idle cycle: Entered to address the control register loaded or read. During active cycle: Provides the least significant four bits of output address.
A4 – 7	O	Provides the most significant four bits of address, permitted only during DMA service.

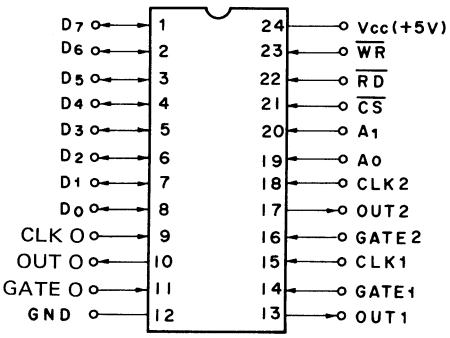


Pin (signal) name	I/O	Function
$\overline{CS}$	I	Signals $\overline{RD}$ and $\overline{WR}$ become valid when this is L level. Note that $\overline{INTA}$ is not affected by this signal.
D0 – D7	I/O	Through these terminals, 8-bit data of a status register or interrupt vector is output in read mode and, in write mode, a command is written in.
$\overline{SP}$	I	Determines whether the 8259 is to operate as a master ($\overline{SP}$ = 1) or a slave controller ($\overline{SP}$ = 0).
A0	I	Along with signals $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$, this is used to write commands or read contents of a register.
CAS0 – CAS2	I/O	Output terminals when the 8259 is used as a master ($\overline{SP}$ = 1) and input terminals when it is used as a slave ($\overline{SP}$ = 0). To control a system of more than one 8259, the CAS lines form the bus of the 8259's.
INT	O	When the 8259 requests interrupt, INT rises to H level and delivers an interrupt request to the CPU or master 8259.
$\overline{INTA}$	I	Permits output of interrupt vector data of the 8259. This operation is performed in the sequence of $\overline{INTA}$ generated by the CPU.
IR0 – IR7	I	IR0 has the highest interrupt priority assigned. These terminals are of asynchronous input.

HD146818P Real-time clock plus RAM RTC



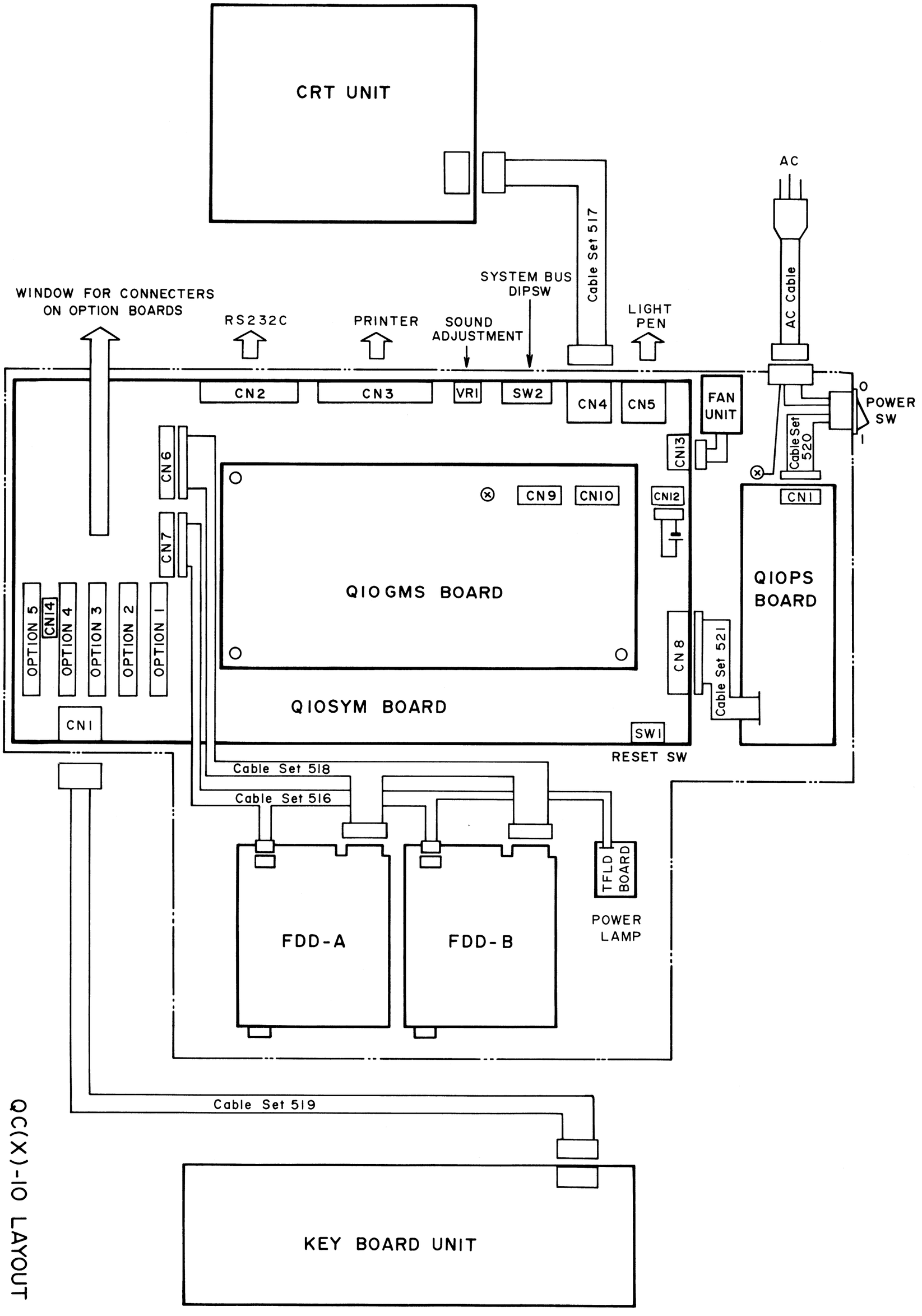
Pin (signal) name	I/O	Function
Vcc	–	Supply power
Vss	–	GND
OSC1	I	External clock signal (32.768 kHz)
OSC2	–	External clock signal (32.768 kHz). Open during input.
AD0 – AD7	I/O	Bidirectional bus lines through which the CPU transfers address to access the RTC then data. Address is transferred during the first half of the cycle and data transferred during the second half. The address signal level must be fixed at the decay of signal M. The data bus driver, 3-state output buffer, is at high impedance except when the RTC outputs data.
M	I	Strobe signal used to read address from the address bus. Address is read into the RTC at the decay of this signal.
$\overline{G}$	I	System clock input terminal. The CPU reads data from the RTC while $\overline{G}$ is H level or writes data at the decay of $\overline{G}$.
$\overline{W}$	I	Input terminal of signal R/W coming from the CPU. The CPU sets $\overline{W}$ at H level to read from the RTC and at L level to write data into the RTC.
$\overline{CS}$	I	Chip select
$\overline{IRQ}$	O	Active-low signal requesting interrupt to the CPU.
$\overline{RES}$	I	RTC reset signal. Operation proceeds to subsequent steps when $\overline{RES}$ turns to L level. $\overline{RES}$ does not affect clock, calendar, or RAM.
PS	I	The valid RAM and Times (VRT) bit is cleared to "0" when PS turns to L level. Then the CPU should initialize the RTC, then set the VTR bit to "1" to prepare for power failure.



Pin (signal) name	I/O	Function
D7 – D0	I/O	Connected to the QX-10's system data bus. Through these terminals, data are input or output according to a CPU instruction IN or OUT. The μPD8253-5 deals with three types of data "control word" and "count" input according to signal $\overline{WR}$, and "count data" output according to $\overline{RD}$.
$\overline{WR}$	I	Signal $\overline{IOWR}$ enters from the CPU and it is used to write in "control word" and "count". The control word and count are read from the data bus and written into the count register at the rise of $\overline{WR}$.
$\overline{RD}$	I	Signal $\overline{IORD}$ enters from the CPU and is used to read the contents of a counter of the μPD8253-5. When the CPU sets $\overline{RD}$ to "0", the count data which is being counted or latched in the storage register is output to the data bus.
$\overline{CS}$	I	The data bus (D7 – D0) is active when $\overline{CS}$ = 0 and at high impedance when $\overline{CS}$ = 1. $\overline{CS}$ is put to 0 when control word and count are to be written in or count data are to be read out. In the QX-10, I/O addresses 00-04H are assigned to IC 14E and 05H – 07H to IC 16E.
A1, A0	I	When writing count in the count register or reading count data, # 0, # 1, or # 2 is selected with A1A0 put to 00, 01, or 10. A1A0 is set to "11" when writing in control word. A1 – 0 are connected to the system address bus.
CLK N (N: 0 – 2)	I	Clock signal determining count rate of counter # N. After "count " is designated, the counter increments at the decay of CLK.
OUT N (N: 0 – 2)	O	Output of counter # N. This may be rate output, square wave output, or one-shot output depending on selected mode. This may also be used as an interrupt request signal.
GATE N (N: 0 – 2)	I	GATE N gates, triggers, or resets counter # N depending on selected mode. Counter # N operates according to the gate inputs as shown in Table.

Operation is as follows depending on the combination of the control signals.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Loads to counter # 0
0	1	0	0	1	Loads to counter # 1
0	1	0	1	0	Loads to counter # 2
0	1	0	1	1	Control word
0	0	1	0	0	Reads from counter # 0
0	0	1	0	1	Reads from counter # 1
0	0	1	1	0	Reads from counter # 2
0	0	1	1	1	No operation (high impedance)
1	X	X	X	X	Disabled (high impedance)
0	1	1	X	X	No operation (high impedance)



QC(X)-10 LAYOUT

Pin	416	4164
1	−5	Nc
8	+12	+5
9	+5	A7
16	GND	GND

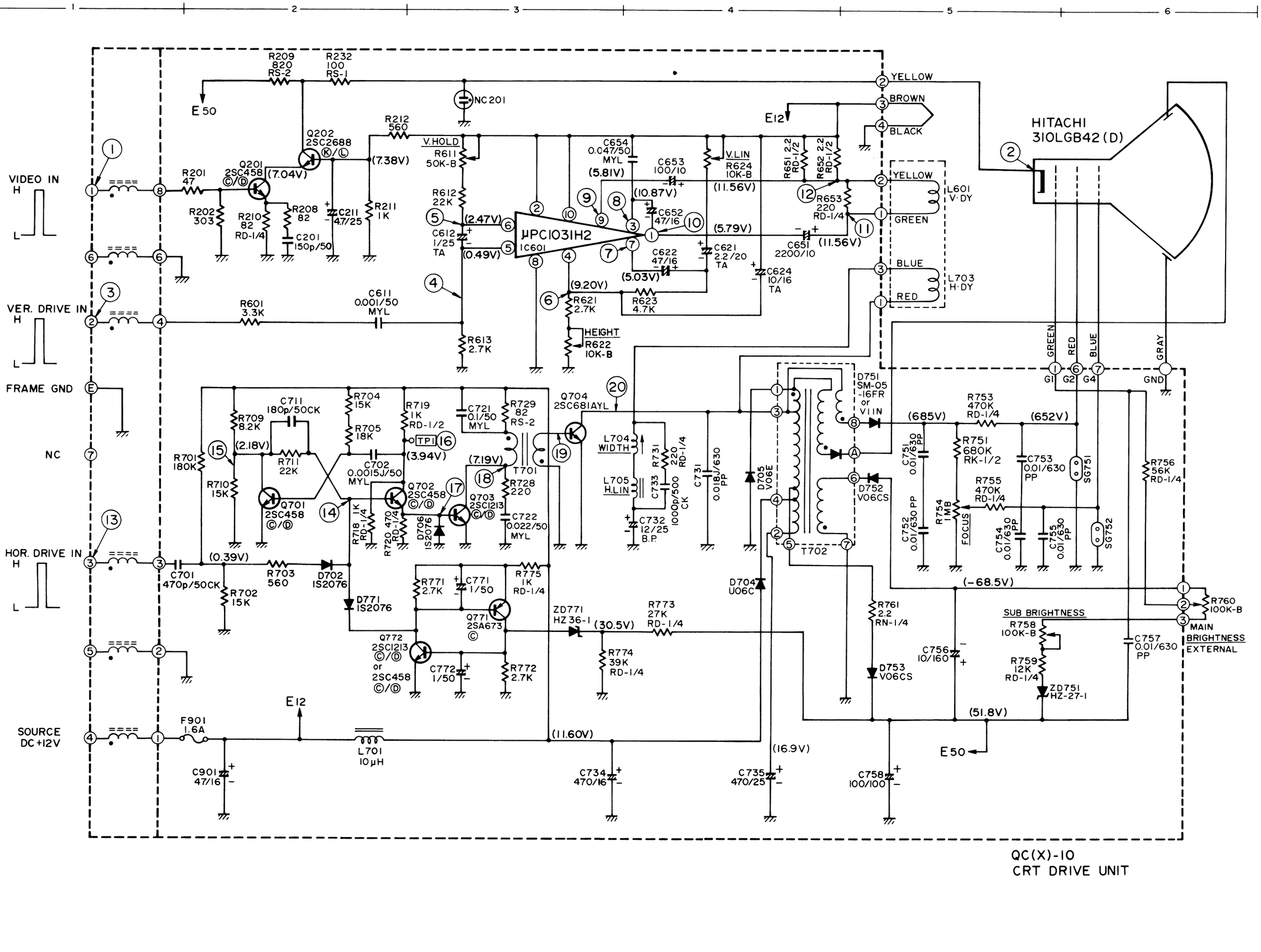
UNIT Y13020600000 (D RAM 416)
UNIT Y13020800000 (D RAM 4164)
QC(X)-10
Q 10 GMS BOARD Schematic Diagram

CAUTION : ∘ ( ) ····· AC198～264V

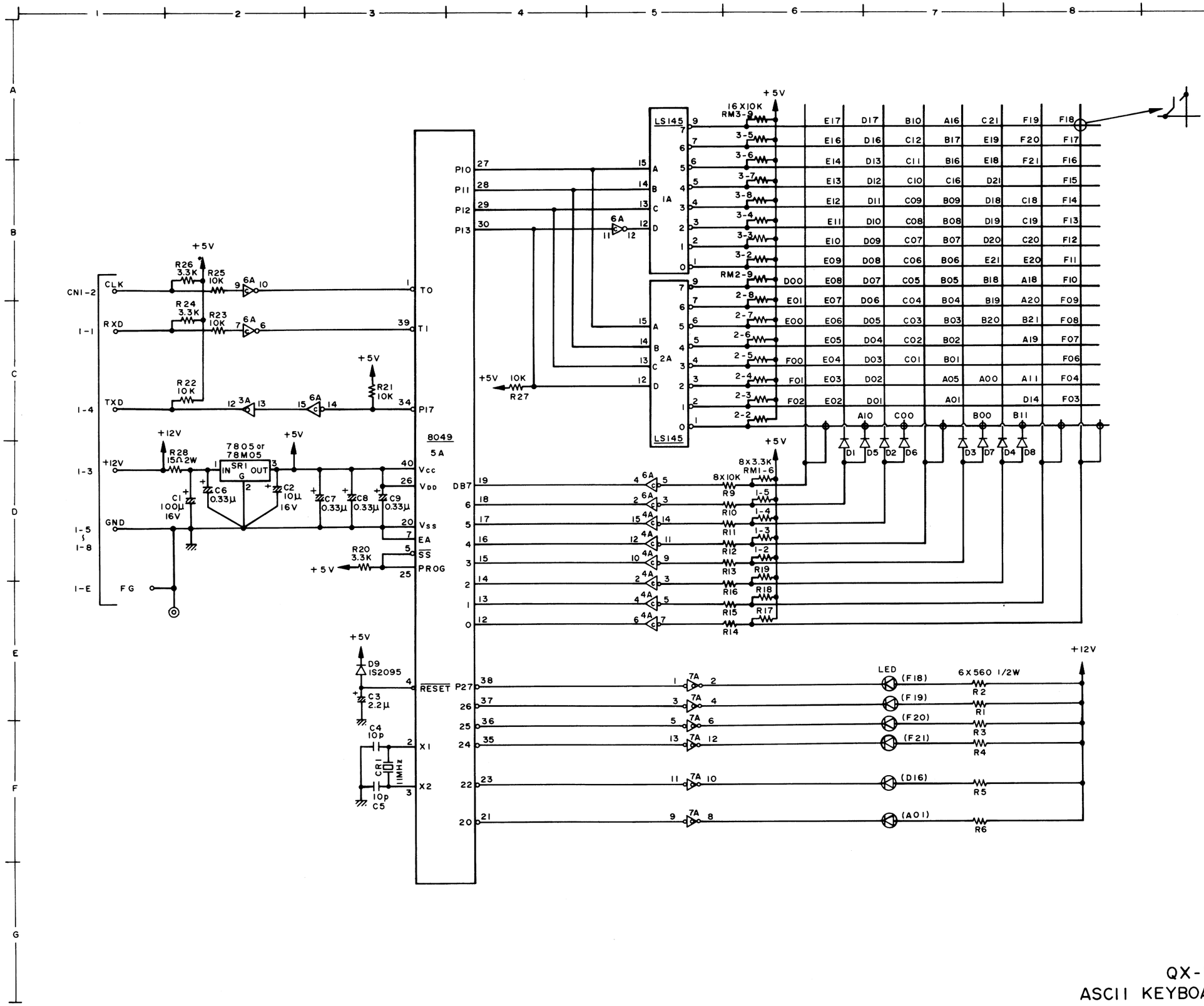
∘ J1 ON ···· AC90～132V
OFF ···· AC198～264V

∘ R3, R4 ···· FUSE RESISTANCE

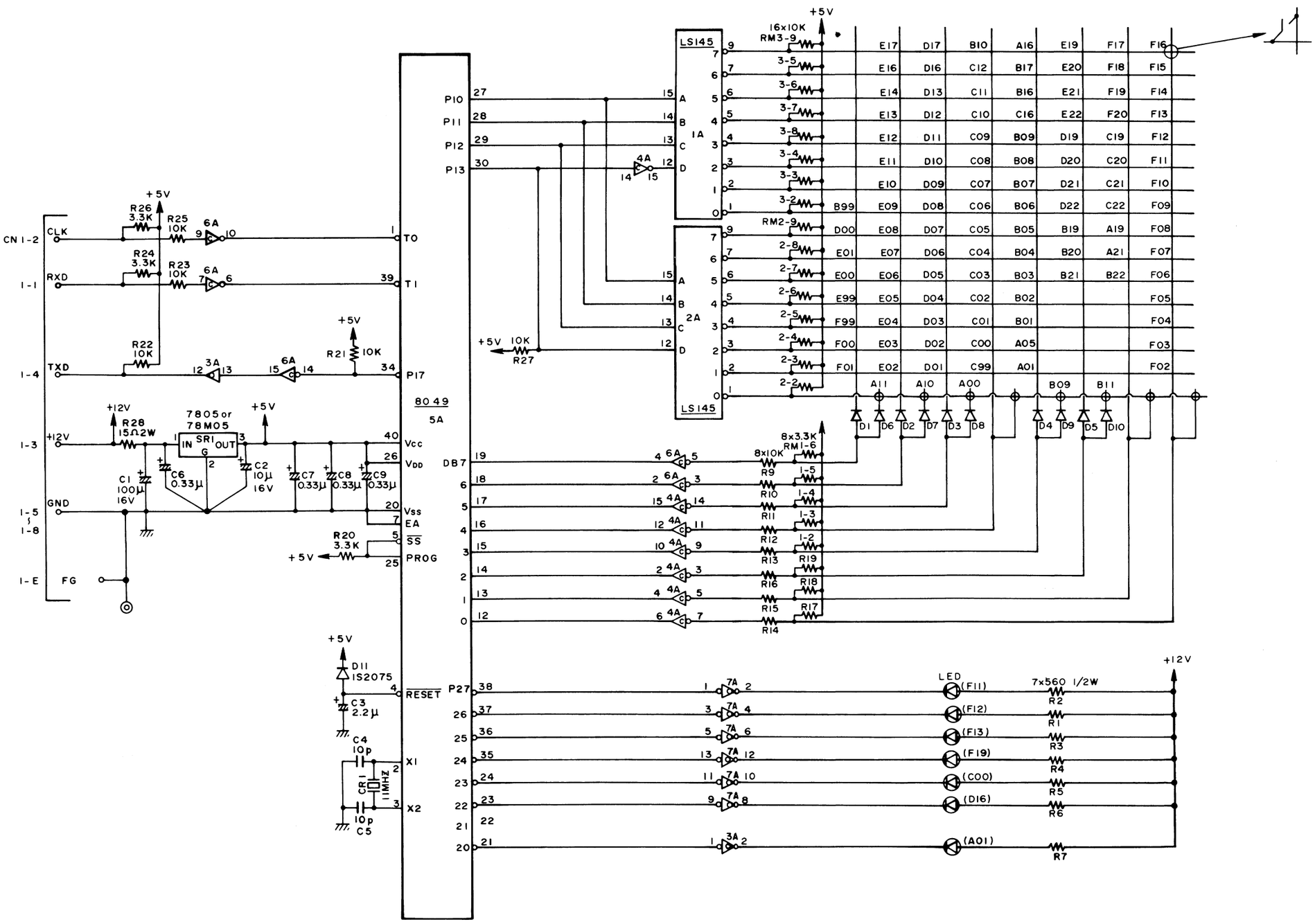
QC(X)-10
QIOPS BOARD



QC(X)-10
CRT DRIVE UNIT

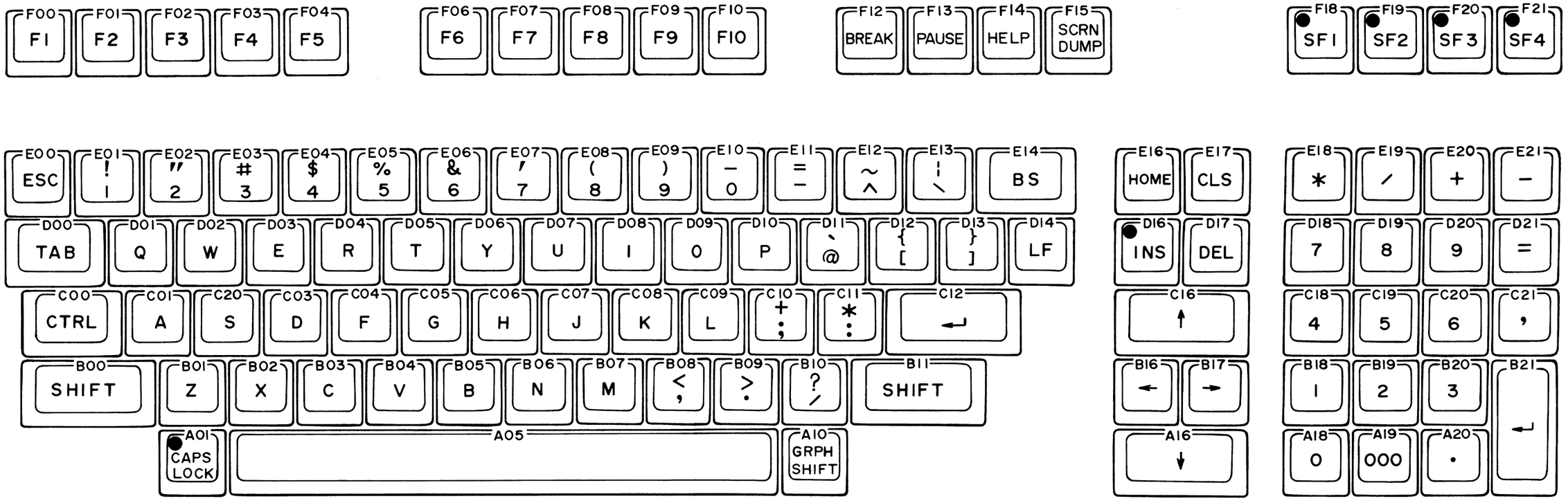


QX-10
ASCII KEYBOARD Schematic Diagram

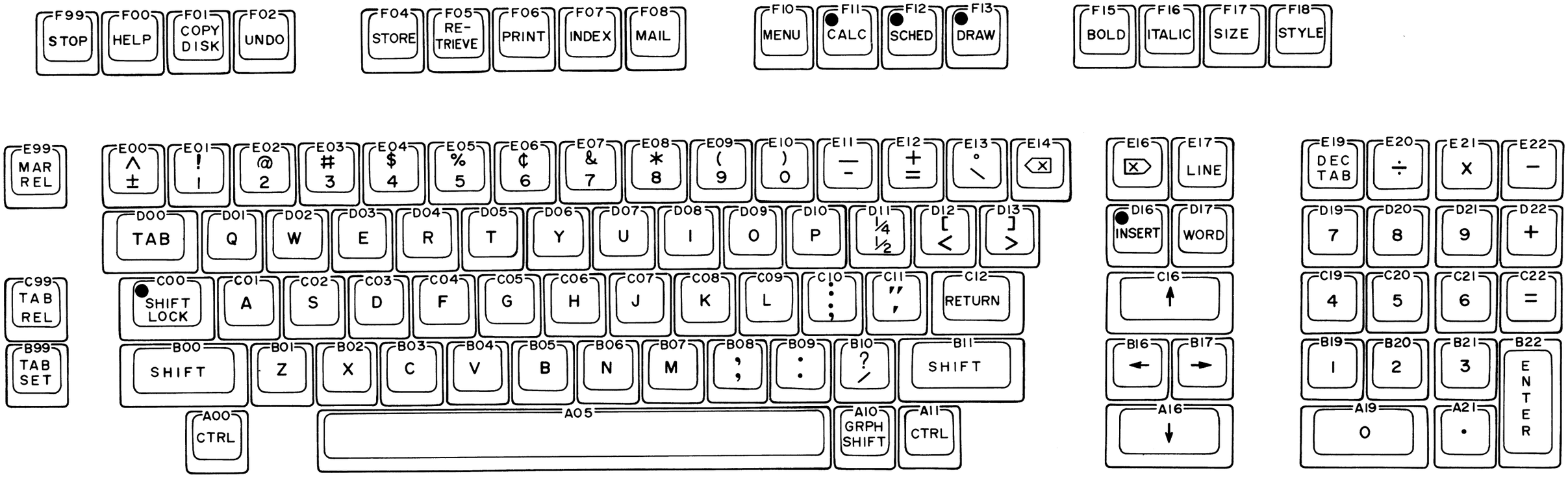


QX-10

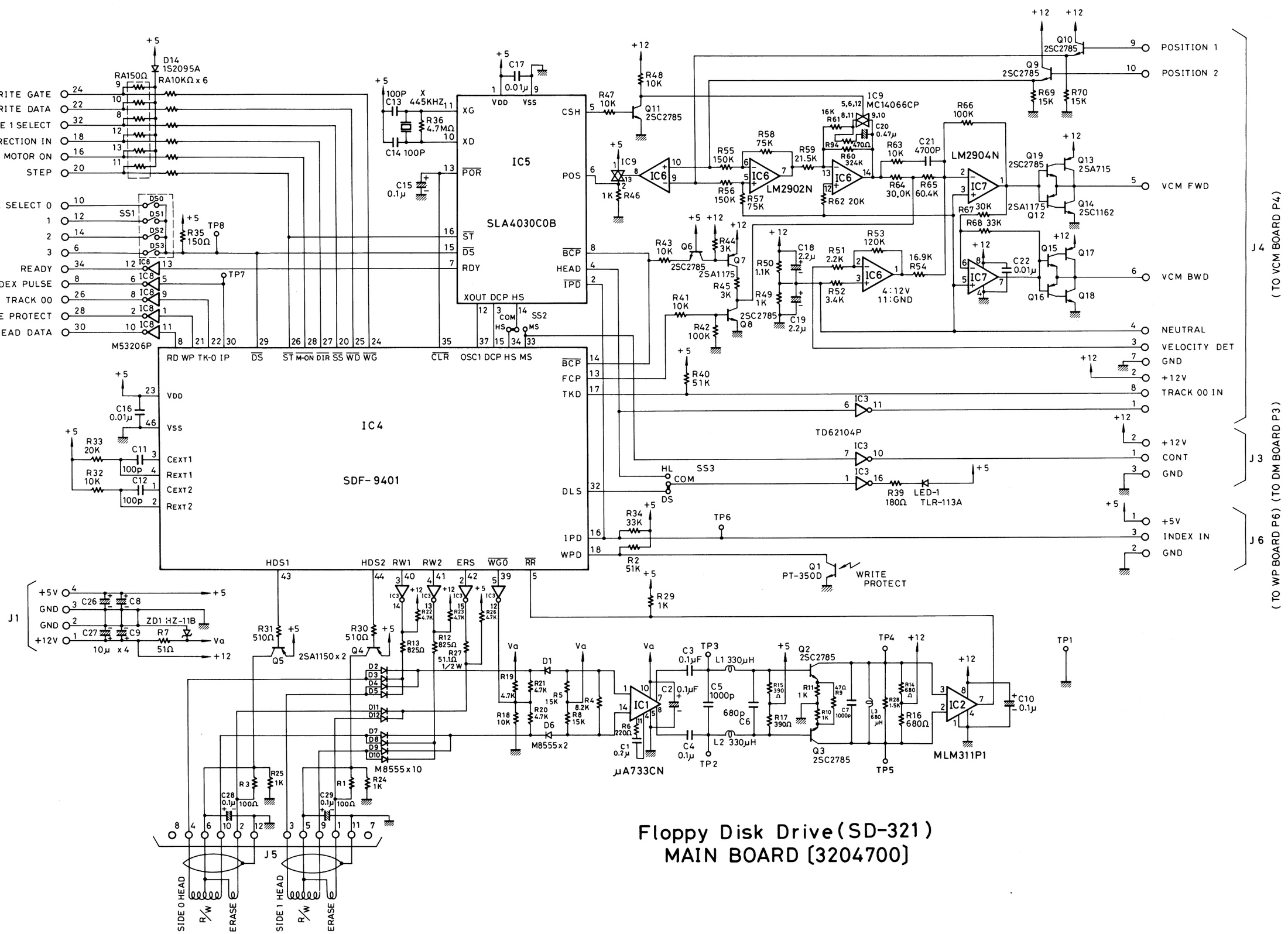
HASCI KEYBOARD Schematic Diagram



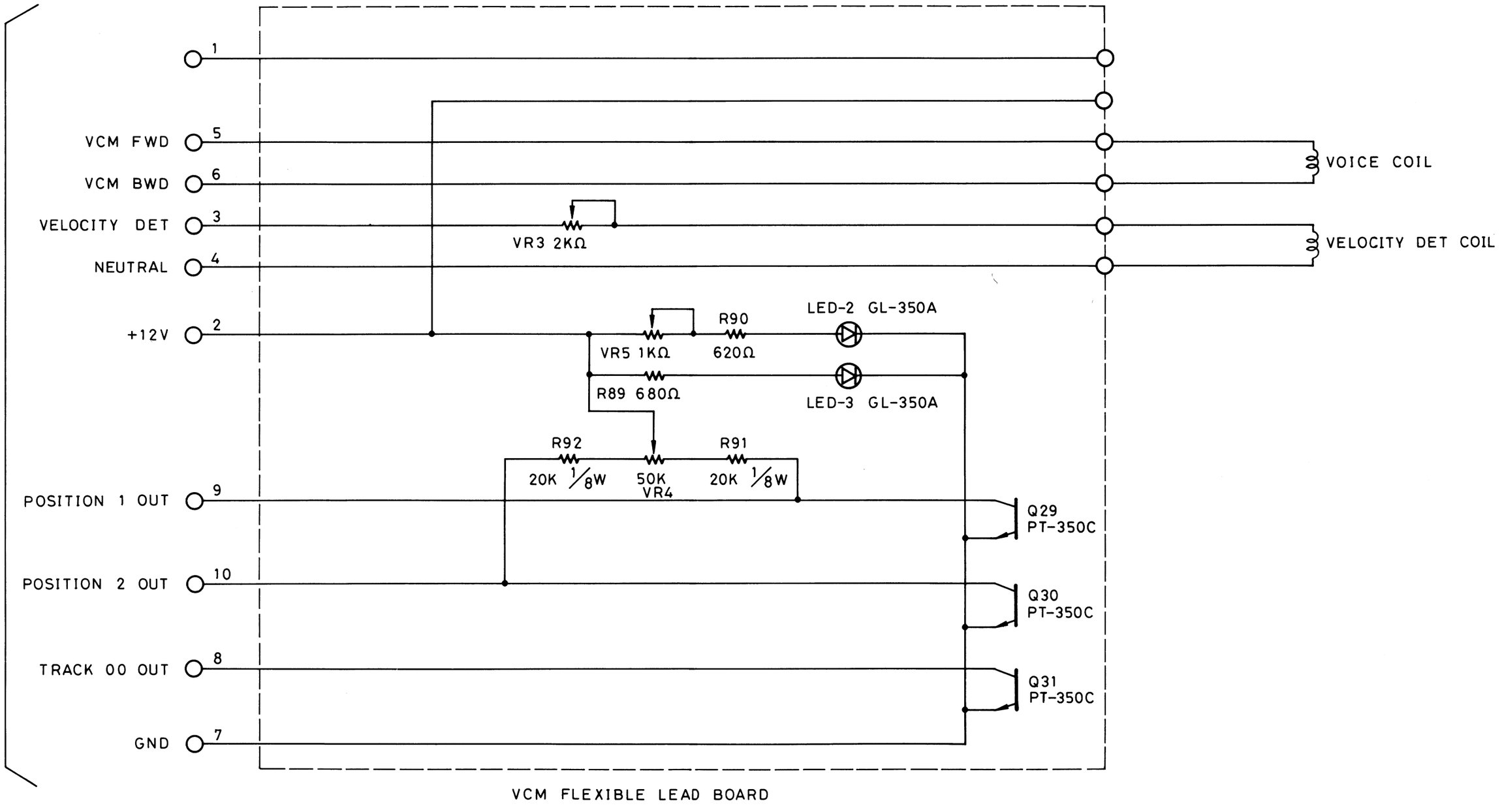
QX-10
ASCII KEYBOARD LAYOUT



QX-10
HASCI KEYBOARD LAYOUT



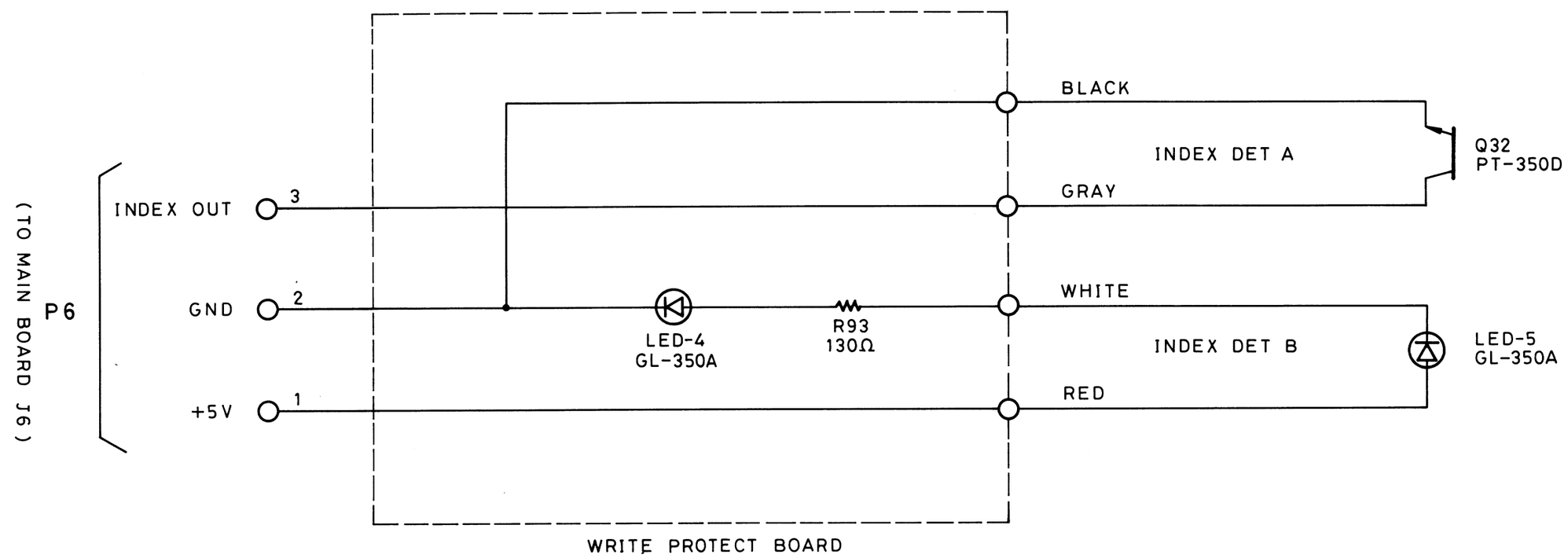
Floppy Disk Drive (SD-321)
MAIN BOARD (3204700)



(TO MAIN BOARD J4)

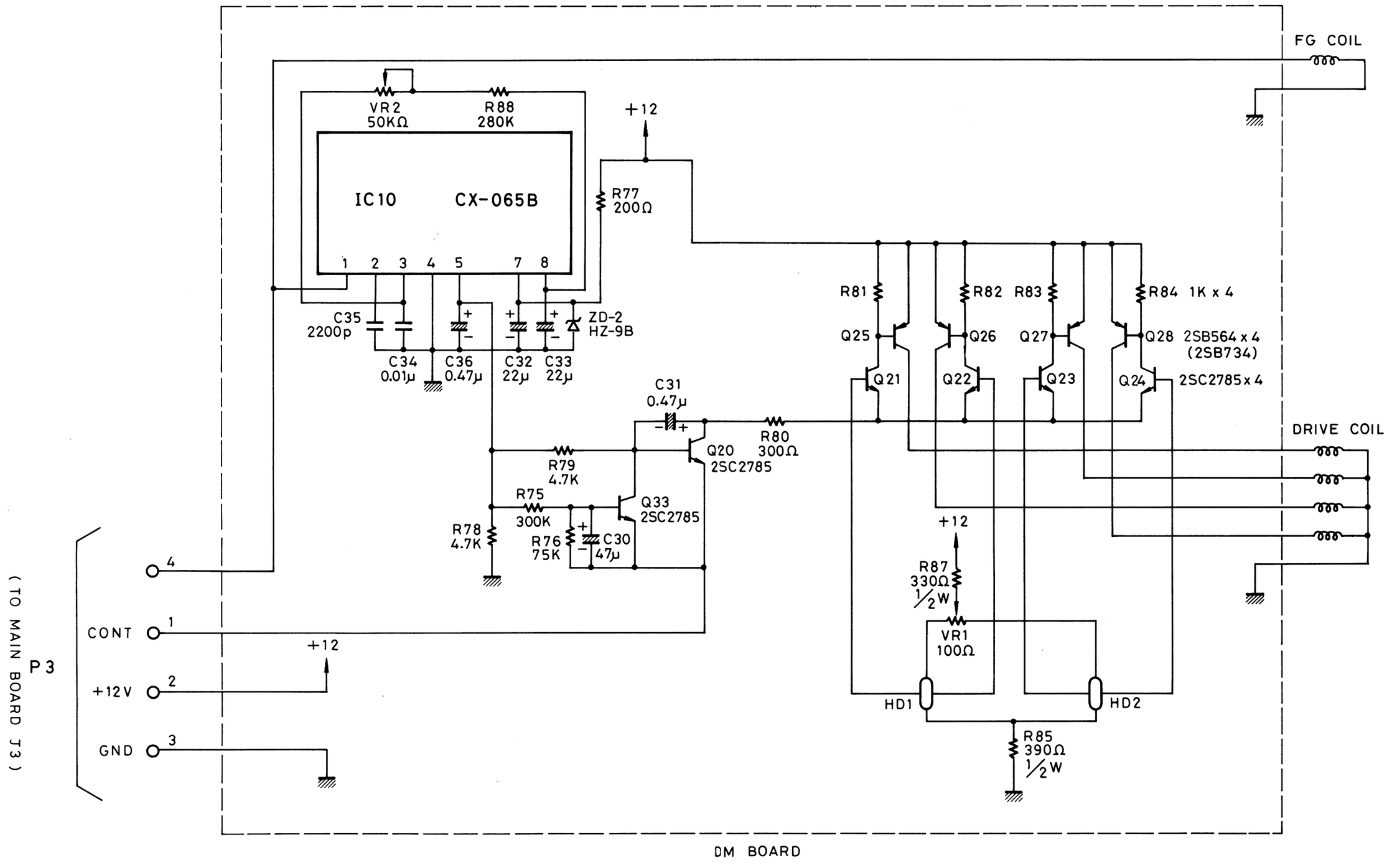
P4

Floppy Disk Drive (SD-321)
VCM BOARD



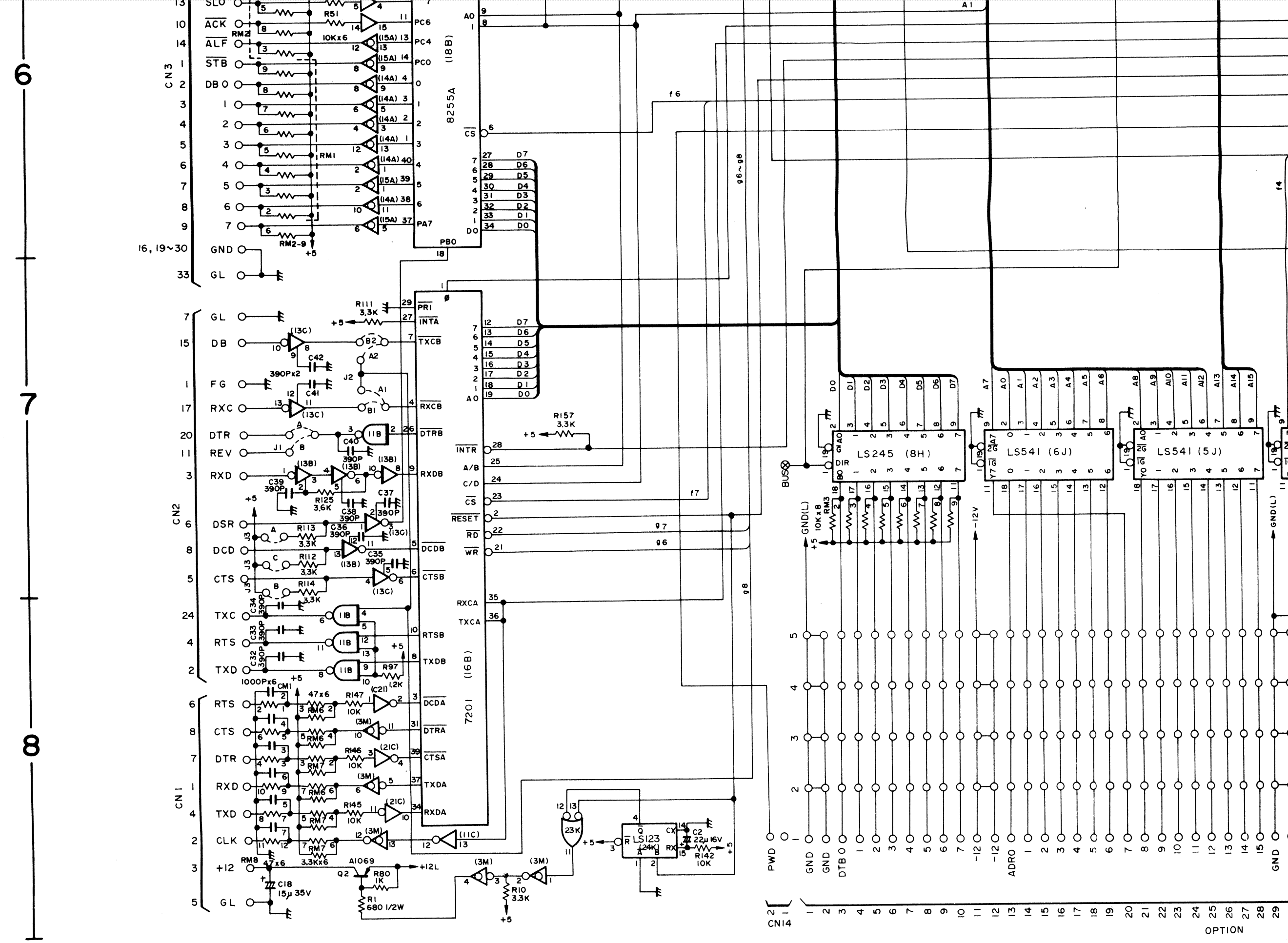
Floppy Disk Drive(SD-$\frac{320}{321}$)

WP BOARD

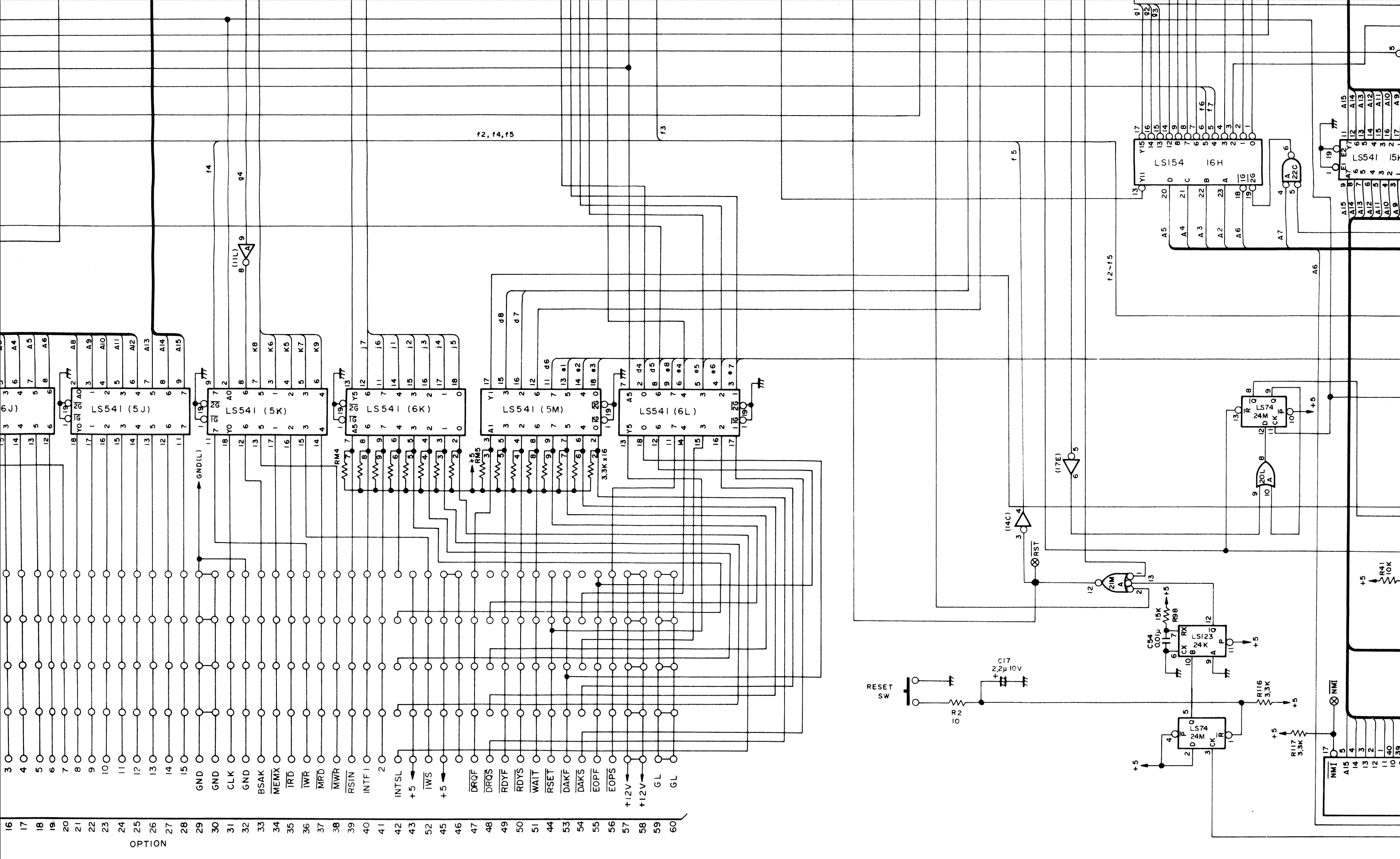


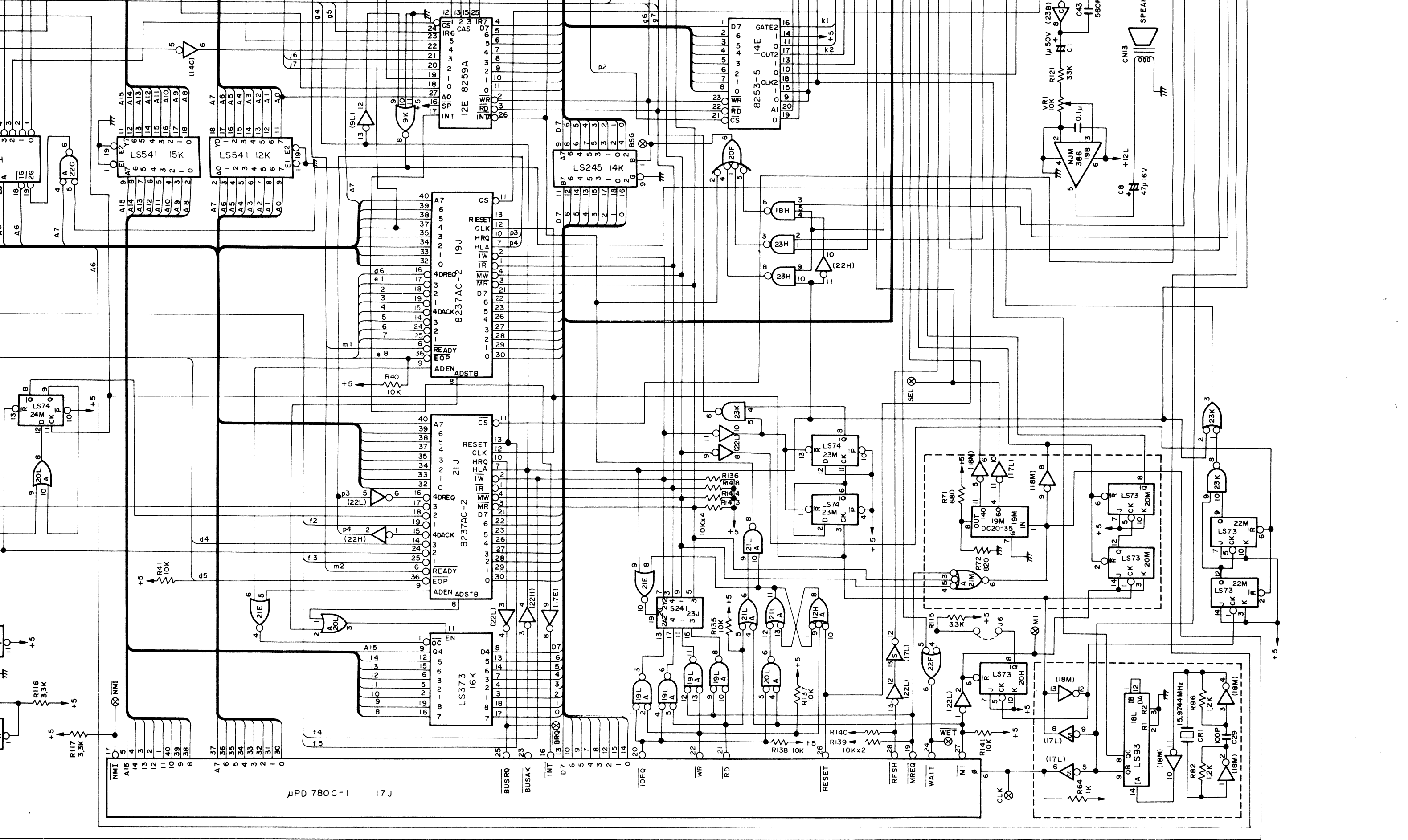
Floppy Disk Drive (SD-320/321)

DM BOARD

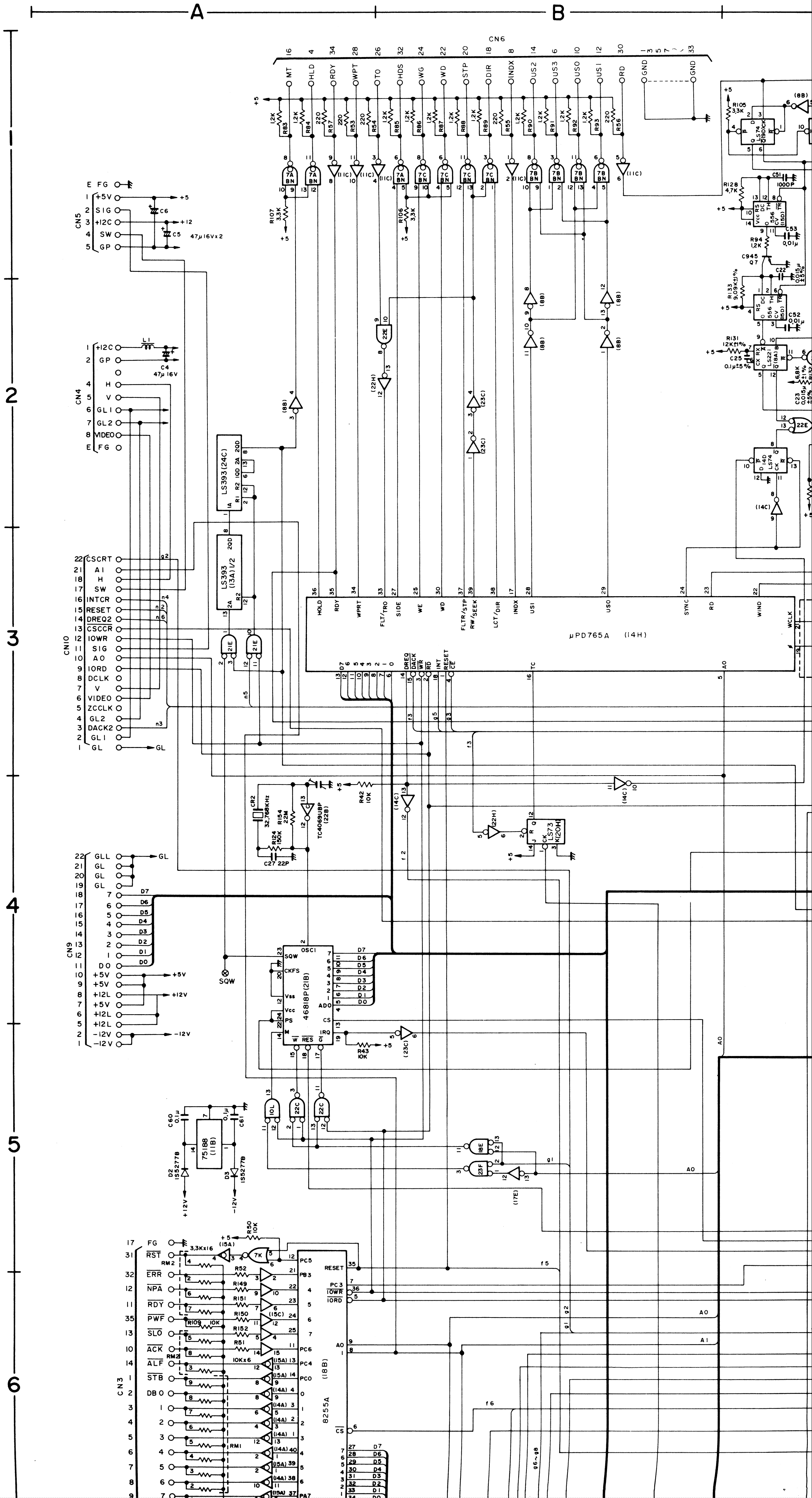


8255A (18B)
7201 (16B)
LS245 (8H)
LS541 (6J)
LS541 (5J)
LS123
CN1
CN2
CN3
CN14
OPTION
BUS
PWD
GND(L)

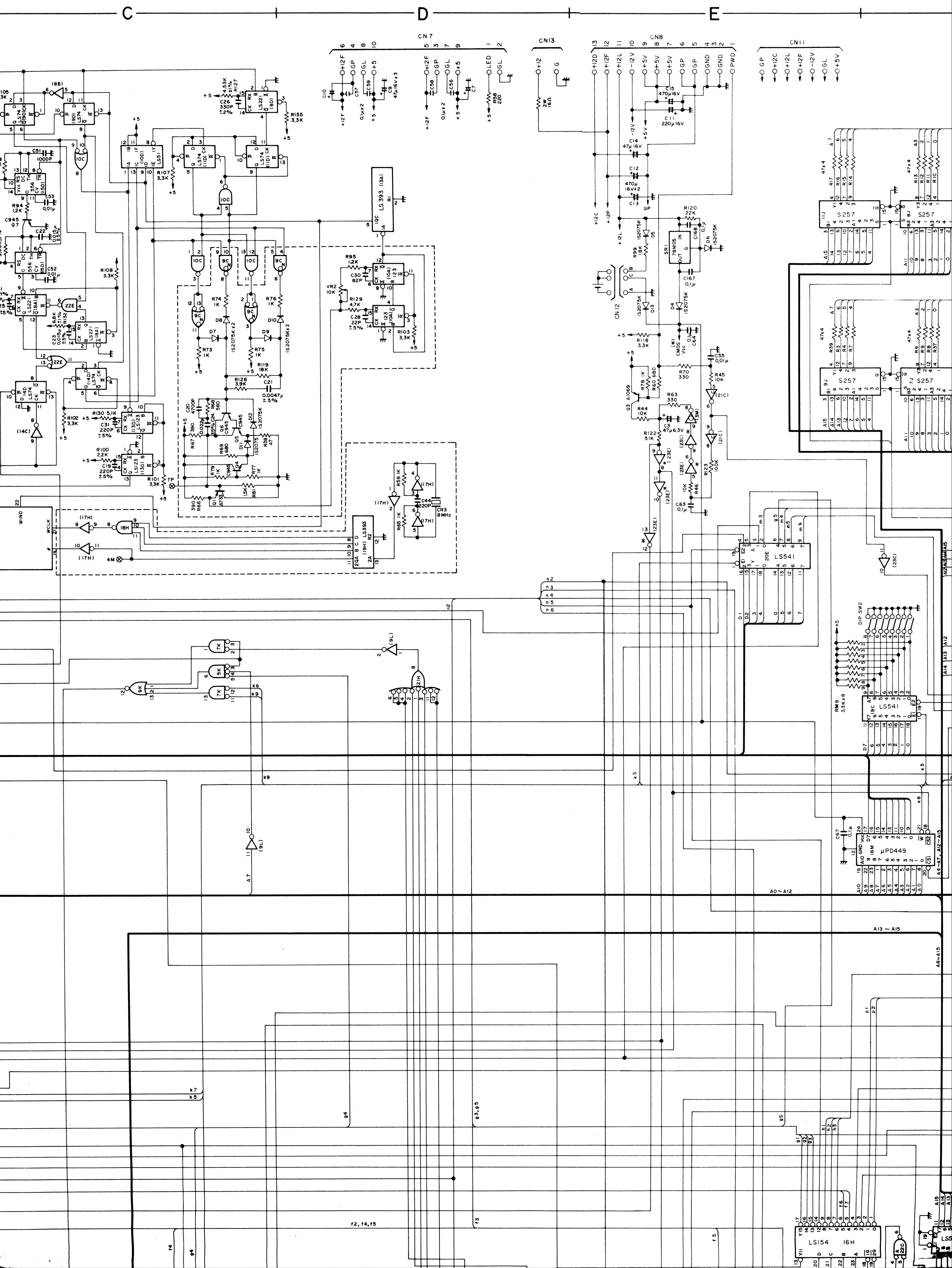

LS541 (5J)
LS541 (5K)
LS541 (6K)
LS541 (5M)
LS541 (6L)
LS154 16H
LS541 15H
LS74 24M
LS123 24K
RESET SW
OPTION
GND
CLK
BSAK
MEMX
IRD
IWR
MRD
MWR
RSIN
INTF I
INTSL
IWS
DRQF
DRQS
RDYF
RDYS
WAIT
RSET
DAKF
DAKS
EOPF
EOPS
+12V
GL
RST
NMI
3.3K x16



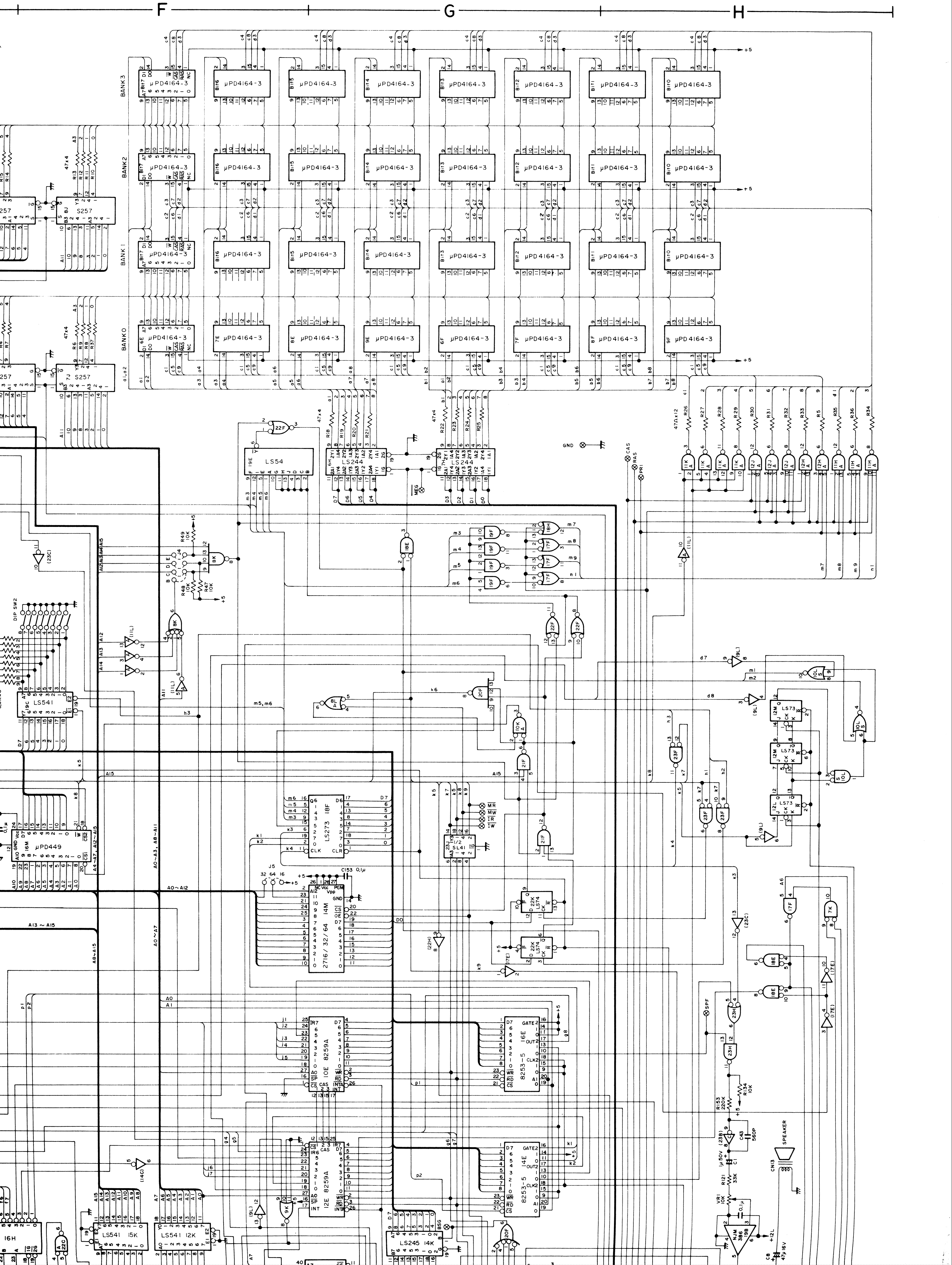
μPD 780C-1 17J
8237AC-2 19J
8237AC-2 21J
LS373 16K
LS245 14K
LS541 15K
LS541 12K
12E 8259A
8253-5 14E
LS93
LS74 24M
LS74 23M
LS73 20M
LS73 22M
LS73 20H
DC20-35 19M
S241 23J
NJM 386 19B
15.9744MHz
CN13
SEL
CLK
NMI
BUSRQ
BUSAK
INT
IOFQ
WR
RD
RESET
RFSH
MREQ
WAIT
M1



A
B
1
2
3
4
5
6
CN6
MT
HLD
RDY
WPT
TO
HDS
WG
WD
STP
DIR
INDX
US2
US3
US0
US1
RD
GND
CN5
E FG
+5V
SIG
+12C
SW
GP
47μ16Vx2
CN4
H
V
GL1
GL2
VIDEO
FG
L1
C4 47μ 16V
LS393(24C)
LS393 (13A)1/2
CN10
CSCRT
A1
INTCR
RESET
DREQ2
CSCCR
IOWR
A0
IORD
DCLK
ZCCLK
DACK2
GL
μPD765A (14H)
HOLD
WPRT
FLT/TRO
SIDE
WE
FLTR/STP
RW/SEEK
LCT/DIR
SYNC
WIND
WCLK
DREQ
DACK
WR
INT
CE
TC
CR2
32.768KHz
R154 22M
R124 150K
C27 22P
TC4069UBP (22B)
R42 10K
LS73 K(20H)
CN9
GLL
+12L
-12V
SQW
46818P(21B)
OSC1
CKFS
Vss
Vcc
PS
AD0
CS
IRQ
R43 10K
75188 (11B)
C60 0.1μ
C61
D2 1S5277B
D3 1S5277B
+12V
-12V
LS74 (19D)
R105 3.3K
556 (15D)
R128 4.7K
C51 1000P
C53 0.01μ
R94 1.2K
C945 Q7
R133 9.09K±1%
C22 0.015μ ±5%
C52 0.01μ
R131 12K±1%
LS221 (8A)
C25 0.1μ±5%
C23 0.015μ ±5%
6.8K ±1%
LS74 14D
CN3
FG
RST
ERR
NPA
PWF
SLO
ACK
ALF
STB
DB0
3.3Kx16
RM2
RM1
R50 10K
R52
R149
R151
R150
R152
R51
R109 10K
10Kx6
8255A (18B)
PC5
PB3
PC6
PC4
PC0
PA7
PC3
g6~g8



C
D
E
CN7
CN13
CN8
CN11
CN12
LS393 (13A)
LS541
µPD449
LS154 16H
S257
DIP SW2
A0 ~ A12
A13 ~ A15
A8 ~ A15
WIND
WCLK
CR3 8MHz
78M05


F
G
H
BANK3
BANK2
BANK1
BANK0
μPD4164-3
S257
LS541
μPD449
LS54
LS244
LS273 18F
2716/32/64 14M
8259A
8253-5
LS74
LS73
LS245 14K
DIP SW2
SPEAKER
GND
CAS
RAS
+5