PRODUCT DESCRIPTION

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1.1 OVERVIEW

The QX-16HD has the same specifications as the QX-16 except as noted in the following sections. In the QX-16HD, drive B houses the hard disk unit, which is connected to the APX-ISYM(HD) board via the APX-T interface board. Figure 1-1 shows the main unit configuration.

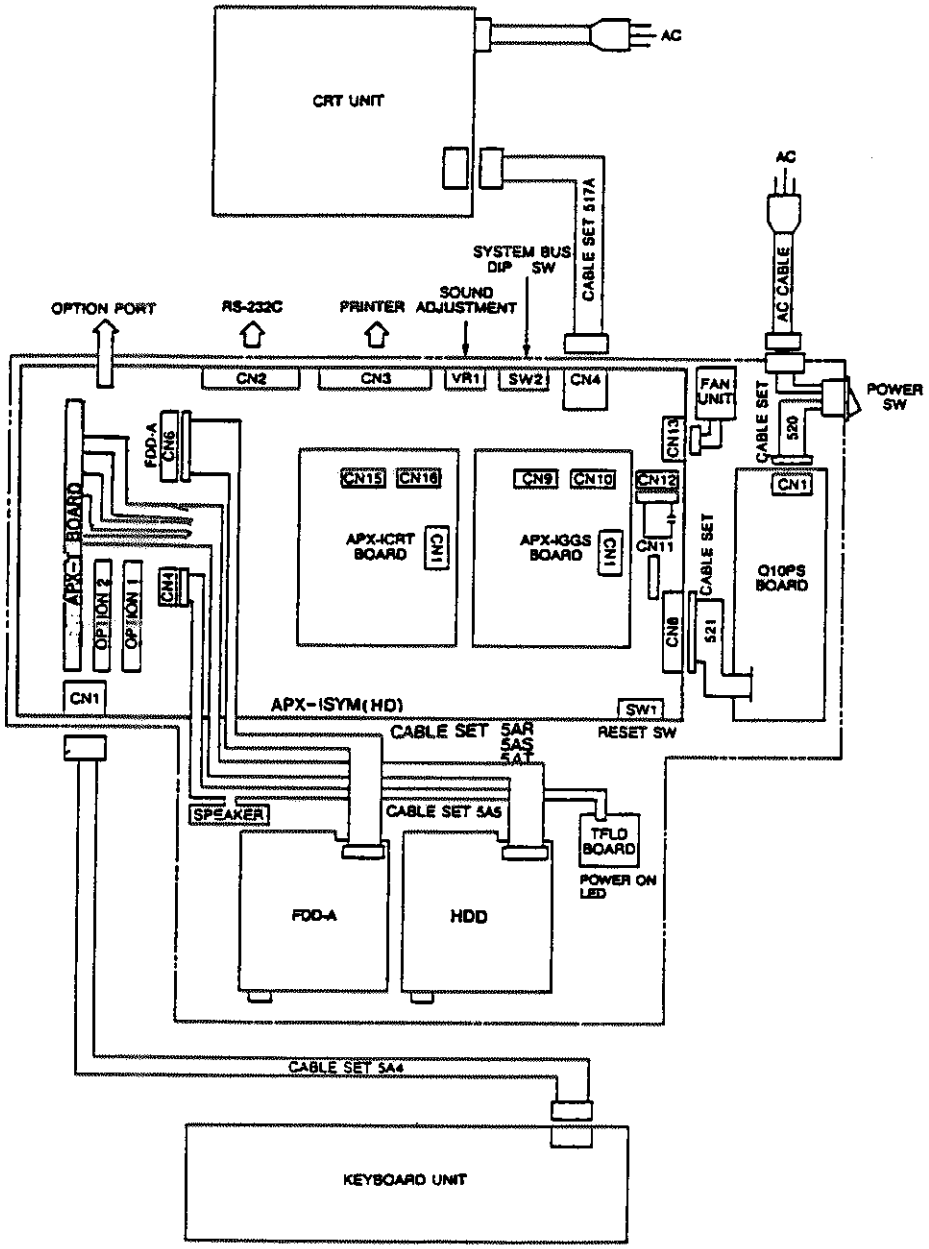

FIGURE 1-1. COMPONENT LOCATIONS

1.2 DIFFERENCES BETWEEN THE QX-16 AND THE QX-16HD

Hardware differences between the QX-16 and the QX-16HD are listed in Table 1-1.

TABLE 1-1. HARDWARE DIFFERENCES

		QX-16	QX-16HD
Control circuit board	ISYM	APX-ISYM circuit board	APX-ISYM(HD) circuit board (Modified APX-ISYM circuit board)
Disk Drives	Floppy Disk Drive (FDD)	SD-543 x 2	SD-543 x 1*
		FDD affixing plate B (for QX-16)	FDD affixing plate B (for QX-16HD)
		FDD screws (M3 x 8) x 8	FDD screws (M3 x 8) x 4
		QX-16 FDD protective plate	QX-16HD FDD protective plate
	Hard Disk Drive (HDD)	None	DK503-2 x 1
			HDD screws (M4 x 8) x 4
			One HDD insulating sheet
I/F Board		None	APX-T circuit board x 1
Case	Upper case	Upper case for QX-16	Upper case for QX-16HD
	Label	Unit label, manufacturer's plate and DRIVE label are different	Unit label, manufacturer's plate and DRIVE label are different
	Screw	Tightening screw for FDD protective plate and grounding plate 2 (M3 x 6) x 3	Tightening screw for FDD protective plate and grounding plate 2 (M3 x 4) x 3
Cable	HDD cable	None	Cable set #5AR
			Cable set #5AS
			Cable set #5AT

* QX-16 HD front is black.

1.3 MAIN UNIT

Figure 2-2 shows the QX-16HD logic block diagram. The APX-ISYM (HD) board is an APX-ISYM board modified (by a trace cut, an additional resistor, and an added jumper to connect the 12VC power to the option slots) to work with the hard disk. The QX-16HD uses one of the option slots to house the APX-T hard disk interface board.

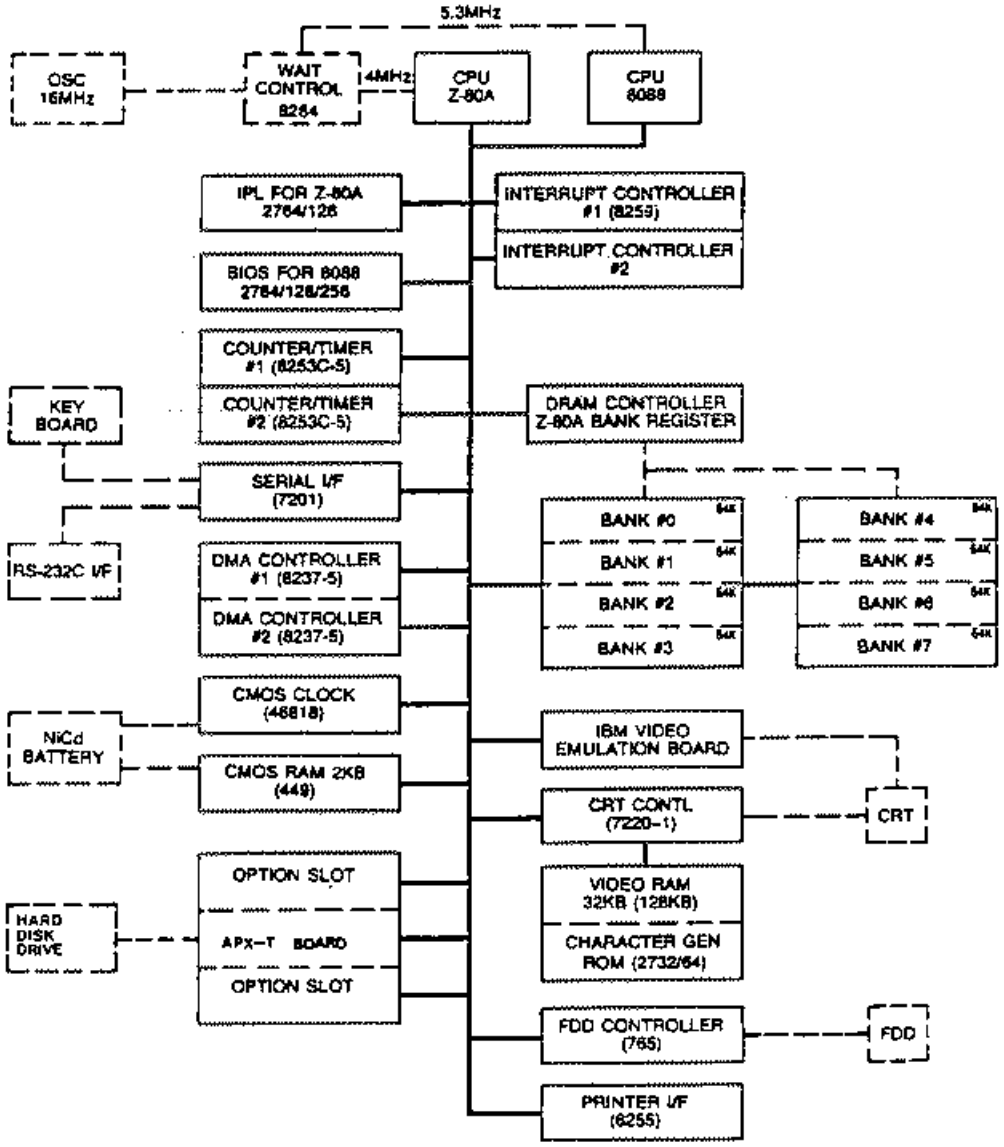

FIGURE 1-2. QX-16HD LOGIC BLOCK DIAGRAM

1.4 APX-T BOARD

The APX-T circuit board (Figure 1-3) is the hard disk drive control circuit board, which is utilized by inserting CN1 in one of three option slots of the QX-16HD. Three cable sets (5AR, 5AS, and 5AT) connect CN2, CN3, and CN4 with the hard disk drive; CN1 on the APX-ISYM(HD) board is not used.

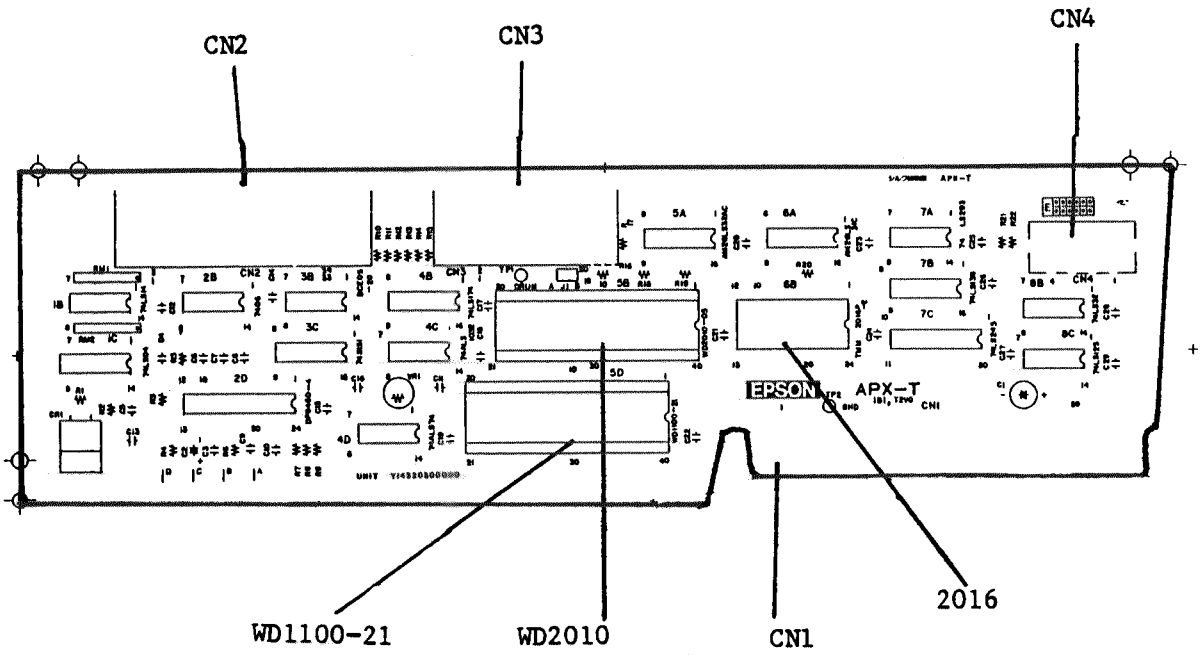

FIGURE 1-3. APX-T BOARD COMPONENTS

1.5 HARD DISK DRIVE

The DK503-2 hard disk drive is a half-height, sealed disk unit which utilizes a 5.25-inch magnetic disk and a Winchester light-load head. A high speed stepper motor system is used as its seek mechanism, and the drive has a large capacity and high reliability.

1.5.1 Environmental Conditions

	Operation	Storage
Temperature	5 C to 35 C	-20 C to 60 C
Humidity	20 - 80 %	10 - 90 %
Resistance to shock (1 msec)	max. 2 G	max. 20 G
Resistance to vibration (5-50 Hz)	0.25 G	2 G

1.5.2 HDD Specifications

Table 1-2 lists the HDD specifications.

TABLE 1-2. HARD DISK DRIVE SPECIFICATIONS

ITEM		SPECIFICATION
Total memory capacity	Unformatted	13.33 MB
	Formatted	10.49 MB
Capacity per area	Formatted	2.79 MB
Capacity per track	Formatted	8,704 B
Capacity per sector	Formatted	512 B
Sectors per track	(Soft sector)	17 Sectors
Number of disks		2 Disks
Number of heads		4 Heads
Number of cylinders		320 Cylinders
Number of tracks		1,280 Tracks

PRINCIPLES OF OPERATION 2

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2.1 APX-T CIRCUIT BOARD OVERVIEW

The APX-T circuit block diagram is shown below. An explanation of each block function is provided after Figure 2-1.

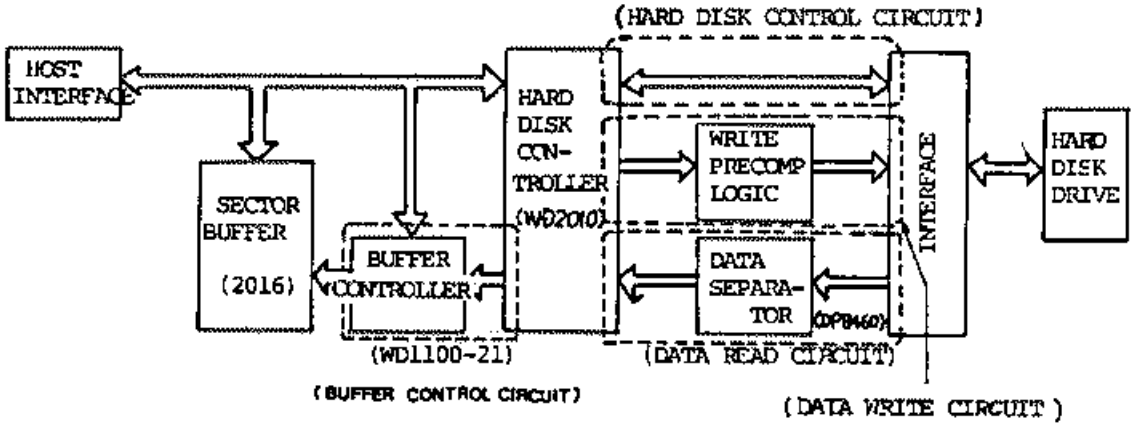

FIGURE 2-1. APX-T BLOCK DIAGRAM

Host Interface Logic

Performs APX-T board card select signal generation and I/O of commands and data from host CPU and status and data from HDC (Hard Disk Controller).

Sector Buffer

A 2-Kbyte 2016 is utilized as the sector buffer. HDD write and read data read by the HDC are stored once in the sector buffer.

Buffer Control Circuit

Sector buffer address incrementation, counter clearing, and generation of the sector buffer chip select signal are performed by this circuit. The main functions of the buffer control circuit are performed by the buffer controller (WD1100-21), which generates the hard disk head select signal and drive select signal, and performs sector buffer control.

Hard Disk Control Circuit

This circuit is incorporated in the hard disk controller (WD2010), with a signal inversion buffer circuit provided externally.

Data Write Circuit

This circuit is utilized when write data is sent to the hard disk. The write data signal timing is adjusted in this circuit to prevent the peak shift phenomenon.

Data Read Circuit

This circuit separates the hard disk drive MFM data read pulses into a read pulse and a clock pulse. The Vcoclk signal, generated by the data separator (DP8460), is sent to the data separator circuit in the hard disk controller (WD2010). Separation of MFM data is performed in the data separation circuit using the Vcoclk signal.

2.2 APX-T CIRCUIT BOARD I/O ADDRESS MAP

The APX-T circuit board I/O address map and each register built into the actual circuit elements are shown in Table 2-1. The functions of the registers are explained after Table 2-1. The CPU sets the data required for hard disk control with these registers.

TABLE 2-1. APX-T BOARD ADDRESS MAP

ADDRESS	READ	WRITE	
80H	Sector buffer	Sector Buffer	Sector Buffer (2016)
81H	Error register	Write Precomp Cylinder	Hard disk controller WD2010
82H	Sector Count Register		
83H	Sector Number Register		
84H	Cylinder Register Low		
85H	Cylinder Register High		
87H	Status Register		
86H	SDH Register		Hard disk controller WD2010 and Buffer controller WD1100-21

Error Register: Sets error data with command completion.

Write Preamp Cylinder: Sets cylinder number with which RWX signal is output (128 cylinders.)

Sector Count Register: Specifies the number of sectors accessed during multisector operation.

Sector Number Register: Enters the sector number accessed first. It is incremented by one during a multisector command.

Cylinder Register Low: Enters the cylinder number for the lower 8 bits.

Cylinder Register High: Enters the cylinder number for the upper three bits. The remaining 5 bits are ignored.

SDH Register: This register specifies the sector size, drive number, and head number.

Status Register: Sets status data.

Command Register: Loads commands to be executed. After a command is loaded, execution begins.

2.3 IC FUNCTIONS

The logic ICs on the APX-T circuit board are the hard disk controller (WD2010) and the buffer controller (WD1100-21), which are described in the following subsections:

2.3.1 Hard Disk Controller (WD2010)

The hard disk controller (WD2010) receives commands from the host CPU, writes and reads MFM data to/from the HDD, performs HDD control, and sends HDD status data to the host CPU.

The WD2010 adds exclusive code after writing MFM data to the HDD for each sector. The WD2010 performs check (read error or not) and automatic error correction during reading operation by using this code.

The hard disk controller operates in accordance with CPU instructions. The APX-ISYM(HD) circuit board CPU manages the hard disk. A description of the hard disk controller pins is provided in Table 2-2.

TABLE 2-2. WD2010 PIN DESCRIPTION

MNEMONIC	SIGNAL NAME	PIN NAME	I/O	FUNCTION
BCS	BUFFER CHIP SELECT	1	O	When active, it enables reading or writing the external Sector Buffer, as well as controlling bus switching.
BCR	BUFFER	2	O	BCR is active prior to read and write functions. It is high every time BCS changes state.
MR	MASTER RESET	5	I	When active, MR initializes all internal logic, except the Task File.
RE	READ ENABLE	6	I/O	Tri-state, bidirectional signal. RE is an input when reading the Task File, and an output when reading the Sector Buffer.
WE	WRITE ENABLE	7	I/O	Tri-state, bidirectional signal. Used as an input when writing to the WD2010 Task File. Used as an output when the WD2010 is writing to the Sector Buffer
CS	CHIP SELECT	8	I	CS must be high to read from or write to the WD2010 Task File.
A0 through A2	ADDRESS 0 through ADDRESS 2	9 through 11	I	Provides the address of the register within the Task File that is to transmit or receive on the data bus.
D7 through D0	DATA 7 through DATA 0	12 through 19	I/O	8-bit, tri-state, bidirectional bus used for the transfer of commands, status, and data.
BRDY	BUFFER READY	35	I	When active, the Sector Buffer is full or empty.
STEP	STEP PULSE	27	O	This signal is used for pulsing the stepper motor. It has a pulse width = 1.6 usec for a stepping rate of 3.2 msec per step, and 8.4 usec for all other stepping rates.
DRDY	DRIVE READY	28	I	DRDY must be high to execute any drive related commands.
INDEX	INDEX PULSE	29	I	The leading edge of this signal indicates that the index mark has been detected.

TABLE 2-2 WD2010 PIN DESCRIPTION

MNEMONIC	SIGNAL NAME	PIN NAME	I/O	FUNCTION
WF	WRITE FAULT	30	I	When high, WF indicates a write error at the drive. This will halt all write, read, and stepping commands.
TK000	TRACK 000	31	I	This signal is output when the read/write heads are positioned over track 0 (cyl.000). It is used to verify proper completion of a restore command.
SC	SEEK COMPLETE	32	I	The leading edge of SC indicates that the drive has settled down after stepping. It is static tested if the rising edge has not been received within 10 revolutions after the stepping pulses.
DIRIN	DIRECTION IN	26	O	This signal determines the direction of the read/write heads when stepped. A high signal moves them in, a low signal, out.
RO	READ DATA	37	I	MFM data clock pulses are received from the drive. The clock pulses and data are separated internally.
RG	READ GATE	38	O	RG is high when a search for an address mark is initiated. It remains high until the end of the ID or data field. (See drive interface.)
BCLK	READ CLOCK	39	I	This clock is generated by a VCO, phase locked to data read from the disk.
DRUN	DATA RUN	34	I	DRUN informs the WD2010 when a field of all ones or zeros has been detected. (See drive interface.)
LATE	LATE	22	O	This signal is used in the write precompensation circuitry along with EARLY to control the delay of WD.
EARLY	EARLY	23	O	This signal is used in the write precompensation circuitry along with LATE to control the delay of WD.
WG	WRITE GATE	24	O	WG is output when valid data is to be written. It enables write current to the head and is immediately brought low if a Write Fault (WF) is detected.
WCLK	WRITE CLOCK	25	I	A 5 MHz clock used internally to control WD.
RWC	REDUCE WRITE CURRENT	33	O	RWC can be programmed to reduce the write current starting at a selected cylinder. (See write precomp cylinder register.)
WD	WRITE DATA	21	O	WD is the MFM data to be written to the disk. The frequency is controlled internally by WC and should be stabilized further externally by a D flip-flop clocked by a 10 MHz clock. The output has an active pull-up and pull-down that can sink 4.8mA.
Vcc	+5V	40		+5 Volts
Vss	Ground	20		Ground

2.3.2 Buffer Controller (WD1100-21)

The buffer controller's main function is sector buffer address specification. The CPU and hard disk controller (WD2010) do not control the sector buffer address. The buffer controller also generates the drive select signal, head select signal, and the DRUN signal. The pin terminals of the buffer controller (WD1100-21) are explained in Table 2-3.

TABLE 2-3. WD1100-21 PIN DESCRIPTION

MNEMONIC	SIGNAL NAME	PIN NAME	I/O	FUNCTION
D0 through D6	DATA 0 through DATA 6	25 through 31	I	7-bit data bus used to write to the SDH Register.
WE	WRITE ENABLE	17	I	Must be active to write to the SDH Register. WE or RE must be active to increment the Buffer Address Counter.
RE	READ ENABLE	18	I	RE or WE must be high to increment the Buffer Address Counter.
A2 through A0	ADDRESS 2 through ADDRESS 0	22 through 24	I	A2 through A0 are used to address the SDH Register (A2-A0 = 6) and increment the Buffer Address Counter. (A2-A0 = 0).
CS	CHIP SELECT	16	I	Must be active to write to the SDH Register.
MR	MASTER RESET	10	I	When active, it initializes all internal logic, including the SDH Register.
BCLR	BUFFER CLEAR	32	O	When active, this signal indicates that the Buffer Address Counter has been cleared.
RCE	RAM CHIP ENABLE	33	O	Activated by BCS, or CS and A0 through A2 equal to zero. Used to enable access to the Data Buffer.
A10 through A15	BUFFER ADDRESS 10 through 15	34 through 39		Buffer Address Counter. Used to address the Data Buffer.
BCS	BUFFER CHIP SELECT	11	I	When active, this signal asserts RCE.
BCR	BUFFER COUNTER RESET	12	I	This signal resets the buffer address counter to zero, marking A10 through A15 = 0.
BRDY	BUFFER READY	14	O	This signal is output when the buffer counter (A10 through A15) has reached the sector size specified in the SDH Register (512).
DRH	DRIVE SELECT HIGH	5	I	Most significant bit of the drive select number. Must be encoded externally.
HD1	HEAD SELECT 1	8	I	Bit 1 of the head select number. Must be encoded externally.
HD0	HEAD SELECT 0	9	I	Bit 0 of the head select number. Must be encoded externally.
DRD1	READ DATA 1	1	I	This signal is data read from disk dirve 1. It is shaped and placed on output pin 13.

TABLE 2-3. WD1100-21 PIN DESCRIPTION (Continued)

MNEMONIC	SIGNAL NAME	PIN NAME	I/O	FUNCTION
DRTIM	DRUN TIMING	19	I	An external load used to adjust DRUN to a nominal pulse width of 250 nsec.
DRUN	DATA RUN	15	0	This signal is output when a field of ones or zeros has been detected.
Vss	Ground	20		Ground
Vcc	+5V	40		+5 Volts

2.4 OPERATION MODES

HDD write data and HDC read data are stored once in the sector buffer. Sector buffer reading and writing are performed by the CPU on the APX-ISYM(HD) circuit board. The CPU accesses the sector buffer as an I/O port.

APX-T circuit board operation is performed in the following two modes:

Read mode: Reads data from the hard disk and stores it in the sector buffer.
Write mode: Reads data from the sector buffer and writes it to the hard disk.

2.4.1 Read Mode

Commands required for hard disk operation are sent to the hard disk controller (WD2010) or buffer controller (WD1100-21) by the CPU. The signal lines and timing for this are shown in Figures 2-2 and 2-3.

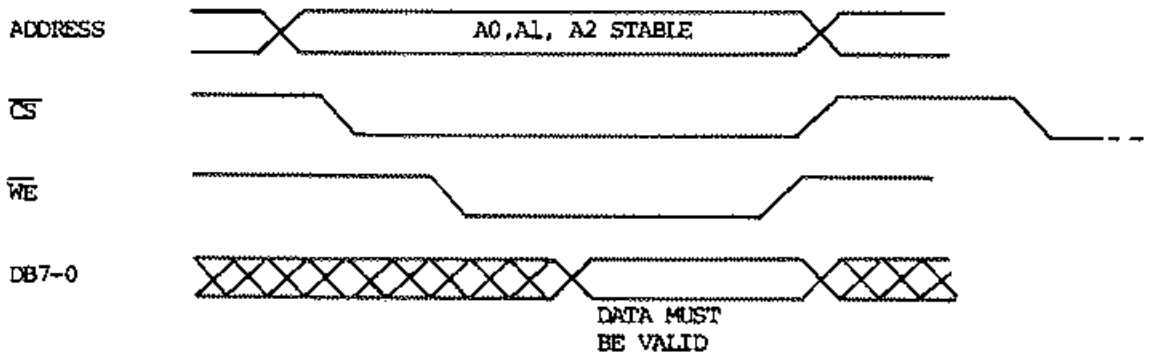

FIGURE 2-2. COMMAND WRITE (CPU TO TASK FILE)

When a command is executed, data read from the hard disk is output to terminals D0-D7 of the hard disk controller. The hard disk controller writes data in the sector buffer. When this occurs, the sector buffer address is specified by the buffer controller (WD1100-21). The signal lines used and signal timing are shown below.

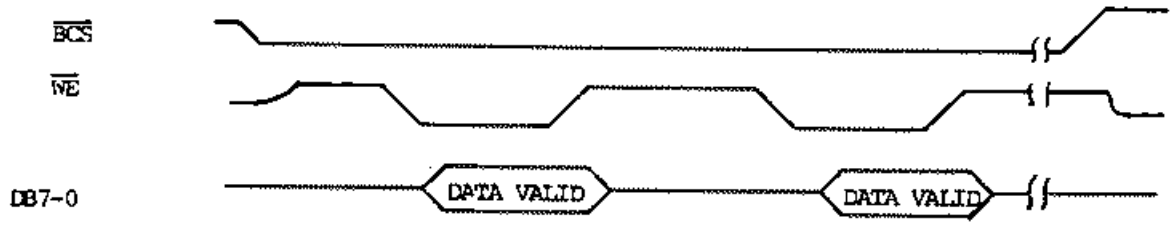

FIGURE 2-3. BUFFER WRITE TIMING (WD2010 TO SECTOR BUFFER)

2.4.2 Write Mode

Data to be written to the hard disk is sent to the sector buffer by the CPU. The buffer controller (WD1100-21) specifies the sector buffer address. During writing, the CPU specifies address 80H only. Commands requiring hard disk write operation are sent to the hard disk controller WD2010 or buffer controller , as in the Read Mode. (See Figure 2-2.) During hard disk data write, the hard disk controller operation is as shown in Figure 2-4; Figure 2-5 shows the buffer read timing.

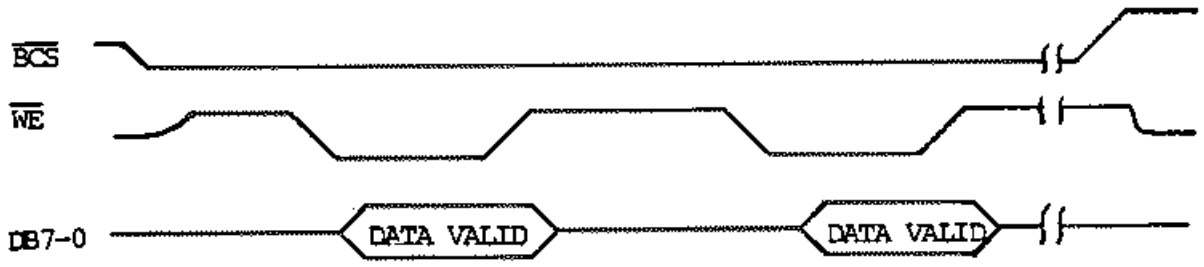

FIGURE 2-4. DATA WRITE TO HARD DISK

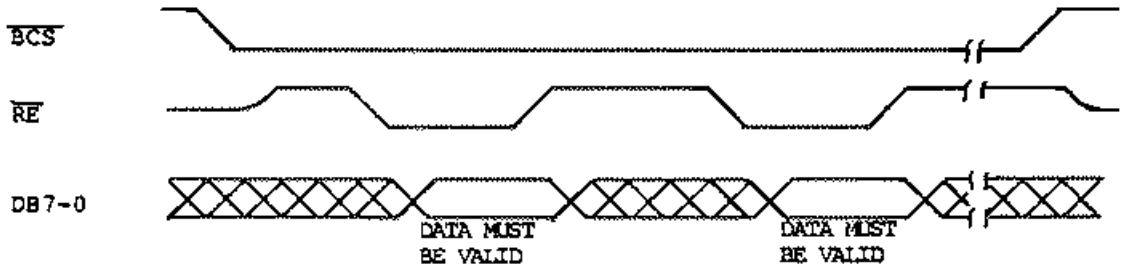

FIGURE 2-5. BUFFER READ TIMING (SECTOR BUFFER TO WD2010)

After read- or write-mode execution, status data and error data are stored in the register of the hard disk controller (WD2010). The CPU reads this data after command execution completion. Signal lines used during that time and signal timing are shown below in Figure 2-6.

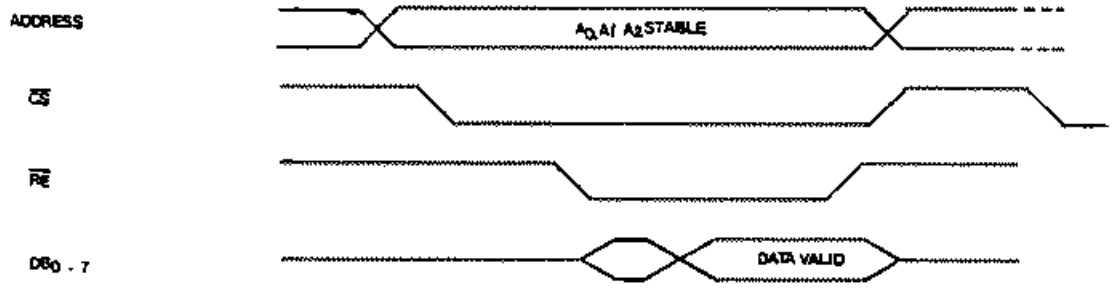

FIGURE 2-6. WD2010 REGISTER READ BY CPU (WD2010 TO CPU)

2.5 APX-T LOGIC CIRCUITRY

2.5.1 Host Interface Logic

The host interface circuit, Figure 2-7, consists of a circuit that records the I/O address of the APX-T circuit board and the bus direction conversion circuit of the LS245 bidirectional buffer on the data bus. The host interface circuit is shown below in Figure 2-7. Circuit operation is described following the figure.

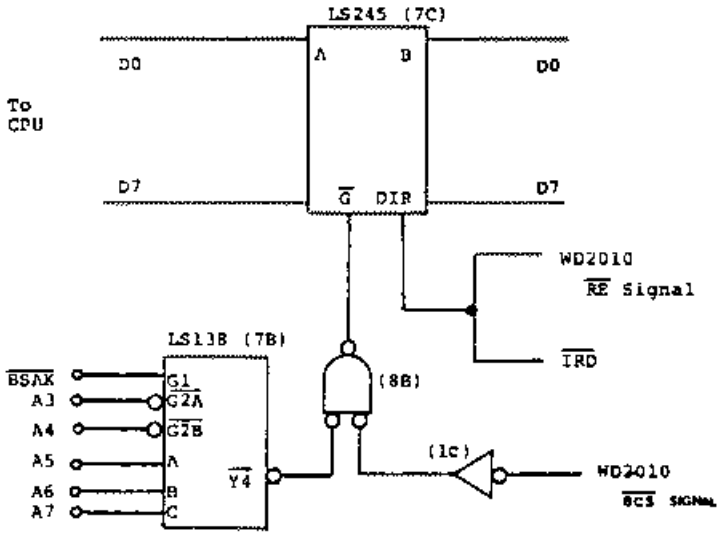

FIGURE 2-7. HOST INTERFACE LOGIC

2.5.1.1 APX-T Circuit Board Decoding (All of the following conditions must be satistied.)

Address signal lines A3-A7 show 8XH.

BSAK must be high. This indicates that the DMA (8237) on the APX-ISYM(HD) circuit board is not in use.

BCS of the WD2010 must be high. The WD2010 must not access the sector buffer.

2.5.1.2 LS245 Direction Determination

To A from B—IRD is active—The CPU is executing the I/O read cycle.

From A to B—IRD is inactive—The CPU is performing other than the I/O read cycle.
(RE of the WD2010 is a tri-state bidirectional terminal. RE is low sometimes. However, RCS is active at that time, which closes the LS245 gate so that the CPU is not influenced.)

2.5.2 Buffer Control Circuit

The buffer control circuit (Figure 2-8) consists of the buffer controller (WD1100-21) and a binary counter (LS293). The function of the buffer control circuit is as shown below.

Sector buffer address incrementation

Buffer counter clearance.

Sector buffer chip select signal generation.

These operations are executed by the hard disk controller (WD2010) or CPU.

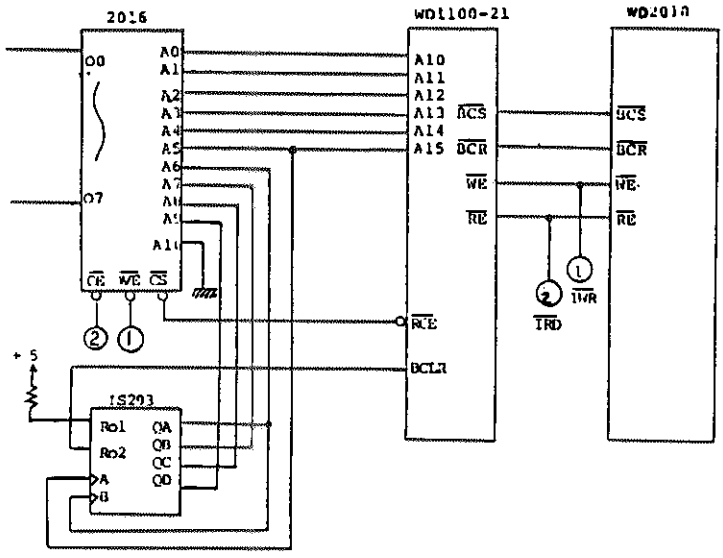

FIGURE 2-8. BUFFER CONTROL CIRCUIT

2.5.2.1 Sector Buffer Address Incrementation

The conditions for address incrementation are shown in Figure 2-9.

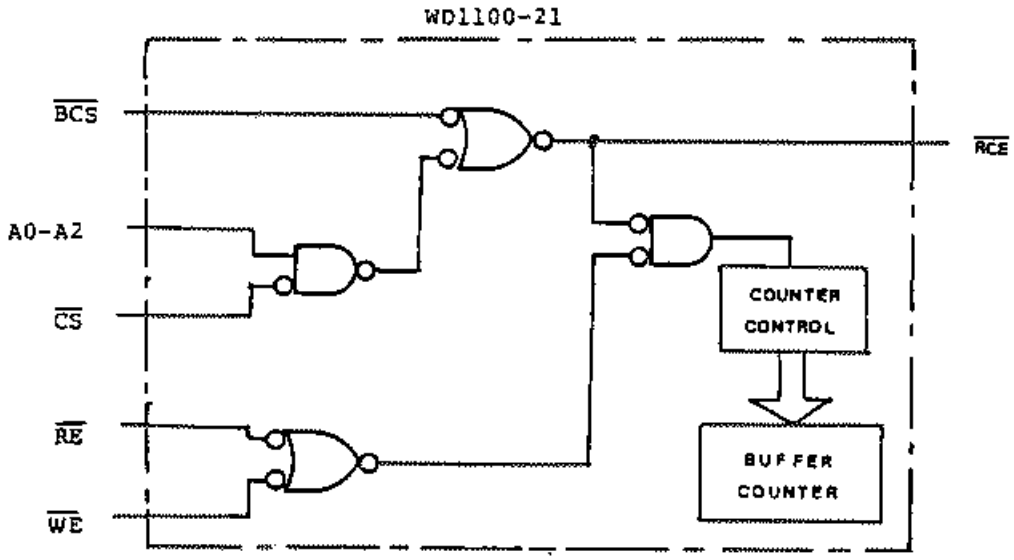

FIGURE 2-9 ADDRESS INCREMENTATION FOR SECTOR BUFFER

Buffer addresses A0-A5 are specified by the buffer controller (WD1100-21). Addresses A6-A9 are specified by the LS293.

Address specification by the LS293 is as shown in Figure 2-10. When the sector buffer address becomes 512 bytes, the WD1100-21 outputs BRDY to the WD2010.

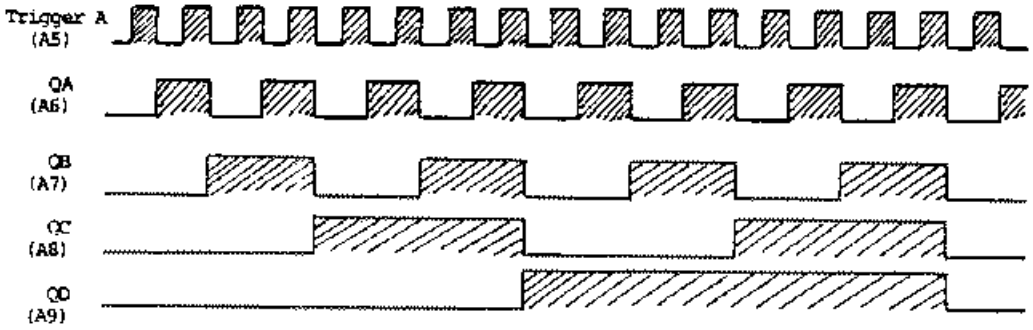

FIGURE 2-10 UPPER ADDRESS INCREMENTATION FOR SECTOR BUFFER

2.5.2.2 Buffer Counter Zero Clear

Buffer counter zero clear is executed when BCR, output by the hard disk controller (WD2010), is active. (BCR becomes active every time the status of BCB changes.) When BCR is active, the buffer controller (WD1100-21) clears address signal lines A10-A15 to zero. Also, when this occurs, the WD1100-21 makes BCLR high and all IC LS293 outputs low.

2.5.2.3 Sector Buffer Chip Select Signal Generation

The sector buffer chip select signal, CS, is output by RCE of the buffer controller (WD1100-21). Conditions for RCE output are shown in Figure 2-11.

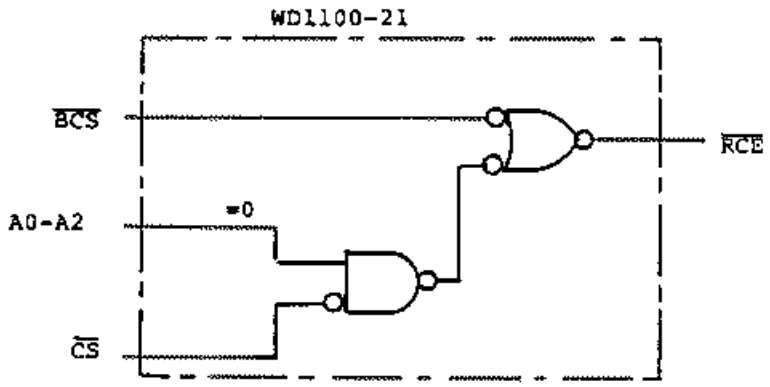

FIGURE 2-11. RCE SIGNAL GENERATOR CIRCUIT

2.5.3 Hard Disk Control Circuit

For the most part, the hard disk control circuit is built into the hard disk controller (WD2010). However, exceptions to this are the HDD drive select signal and the head delect signal which are output by the buffer controller (WD1100-21). Altogether there are 11 control signal lines. This section describes the generation of the HDD drive select signal and the head select signal by the buffer controller.

The buffer controller IC is provided with a SDH (Size, Drive, Head) register. The CPU writes head select and drive select signal data to this register. The SDH register address is 86H. The function of each SDH register bit is shown in Figure 2-12.

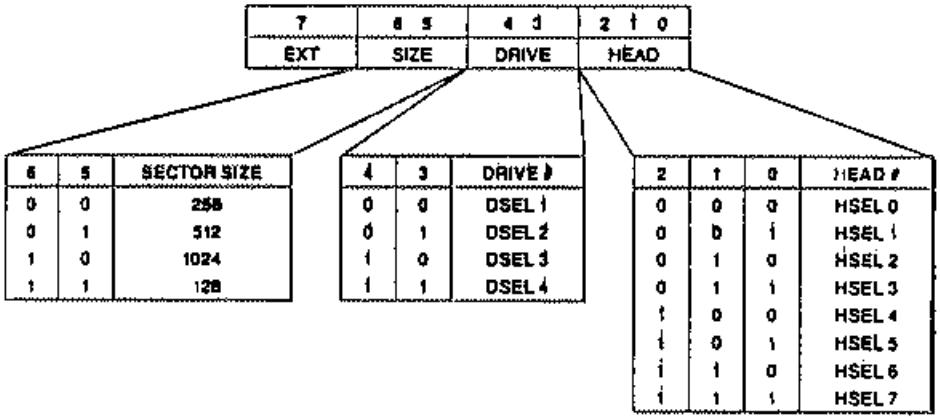

FIGURE 2-12 SDH REGISTER

The content of SDH register bits 0-1 are output to the WD1100-21 head select signal (HD0, HD1) pin. The content of SDH register bit 4 is output to the WD1100-21 drive select signal (DRH) pin.

2.5.4 Data Write Circuit

The write data (WD) output by the hard disk controller (WD2010) is converted to MFM data. However, it is not practical to send this data directly to a hard disk because peak shift occurs, which easily causes errors to occur. To prevent peak shift, the write data (WD) output timing is adjusted by the data write circuit, called a write precompensation circuit.

The hard disk magnetic inversion spacing is 200 ns, 300 ns, and 400 ns. The output waveforms, with which 1 pulse is written to disk, are as shown in Figure 2-13 (left). When 2 pulses are written with 200 ns spacing, each independent waveform interferes and the peak of the synthetic waveform is shifted from the write location as shown in Figure 2-13 (right). This is called peak shift. To eliminate this interference as much as possible, write compensation is performed. Since peak shift can be foreseen, write timing is shifted in a direction which automatically reduces the peak shift. Write compensation is performed past the cylinder 128 circumference with 13 ns as required compensation. This circuit is called a write precompensation circuit and is shown in Figure 2-14.

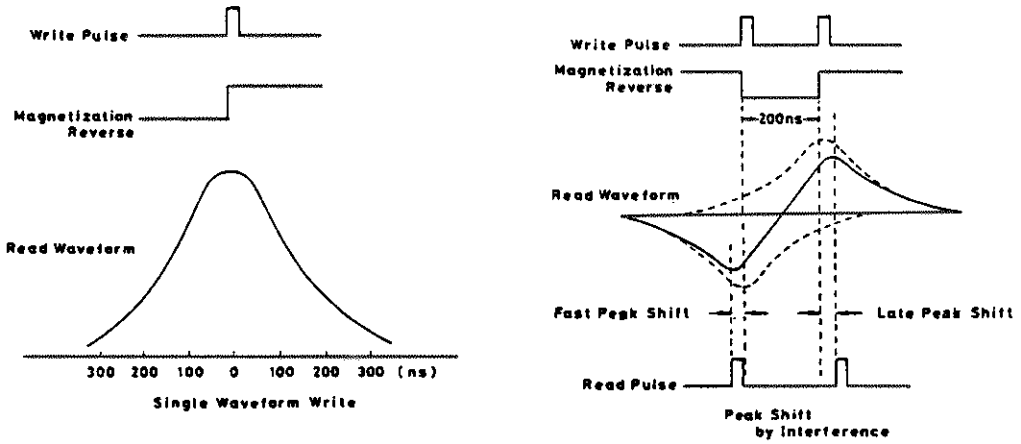

FIGURE 2-13. PRINCIPLE OF WRITE PRECOMPENSATION

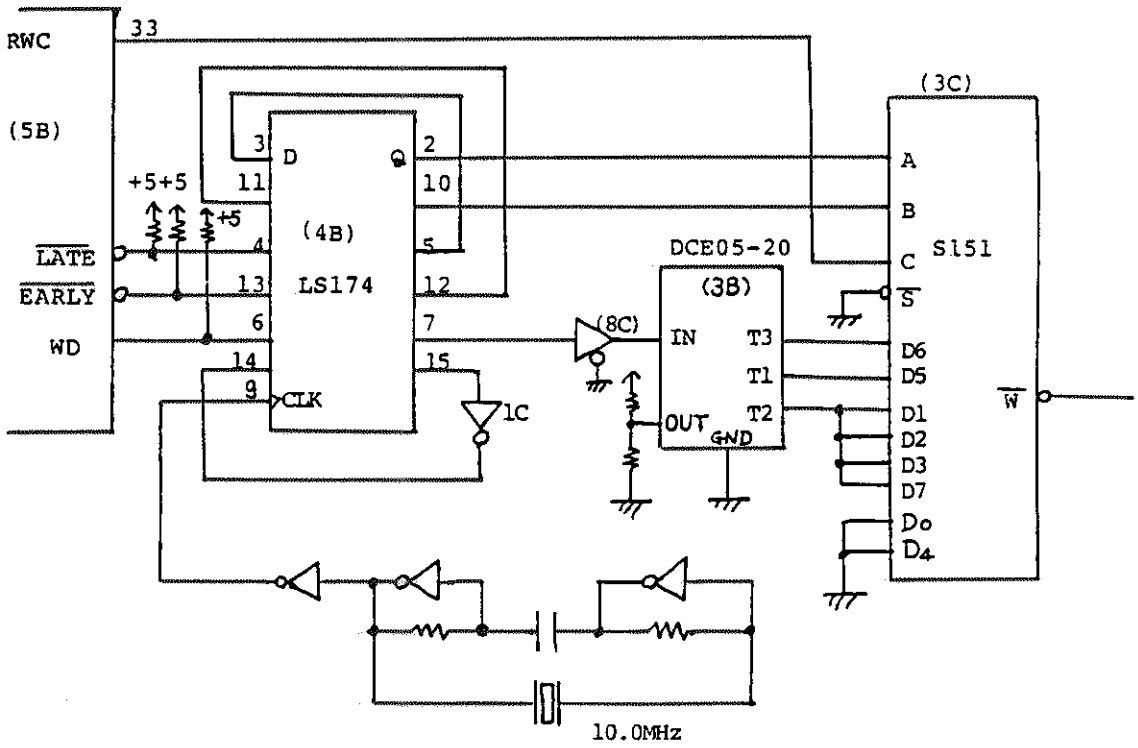

FIGURE 2-14. WRITE PRECOMPENSATION CIRCUIT

The signal timing of this circuit is shown in Figure 2-15. Hard disk controller (WD2010) terminal WD is the input terminal, and S151 terminal W is the output terminal. The hard disk controller signals (RWC, LATE, EARLY) control this circuit. RWC is active when the hard disk drive head position is past cylinder 128. LATE and EARLY are output with automatic timing provided by the hard disk controller. The WD signal output is synchronized with CLK by the LS174. The signal input to the delay element (DCE 05-20) terminal IN is converted to three signals (T1, T2, T3) as shown in Figure 2-15. S151 terminals A, B, and C are gate terminals. The D0-D7 input terminal signal output by terminal W is selected by this signal. THe LATE/EARLY signal output is synchronized with CLK by the LS174. These two signals are input to S151 terminals A and B after a 1 clock delay.

TABLE 2-4. S151 LOGIC

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	D0
L	L	H	L	D1	D1
L	H	L	L	D2	D2
L	H	H	L	D3	D3
H	L	L	L	D4	D4
H	L	H	L	D5	D5
H	H	L	L	D6	D6
H	H	H	L	D7	D7

If the RWC signal output is low, the W signal output is always signal T2. However, when A and B are both low, W output is still high. If RWC signal output is high, W signal output is determined by the status of the A and B terminals. When A is low, signal T3 is output to terminal W. When B is low, T1 is output to terminal W. When the signals of terminals A and B are simultaneously high, signal T2 is output; however, when A and B are low, terminal W output is still high. The 5MHz clock is input to terminal WCLK, which is used to control the write data (WD) output of the hard disk controller.

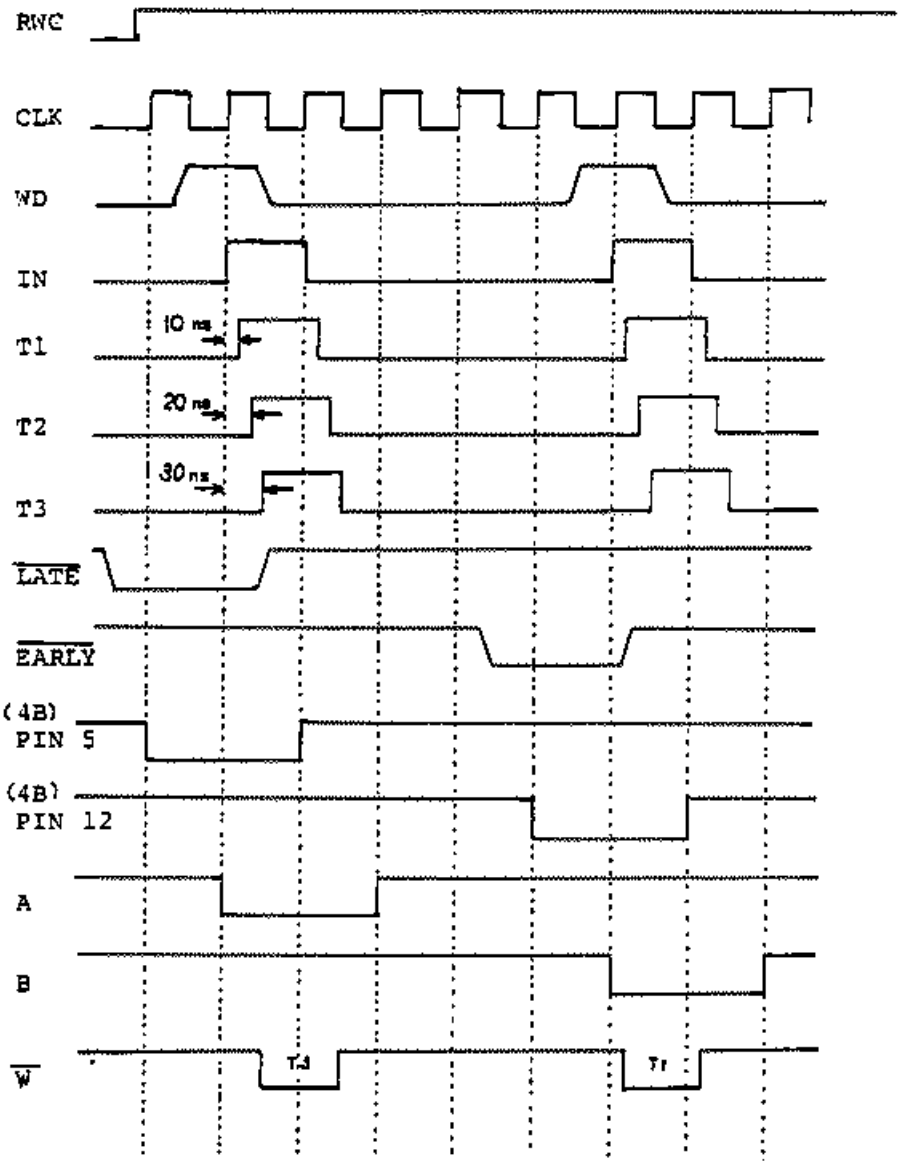

FIGURE 2-15. WRITE PRECOMPENSATION TIMING

2.5.5 Data Read Circuit

The data read circuit (Figures 2-16 through 2-18) separates MFM data read fromthe hard disk into a read pulse and a clock pulse. The Vcoclk signal, which separates the MFM data, is generated in the data read circuit. The data read circuit is composed of two functional blocks:

VFO circuit

Data separator

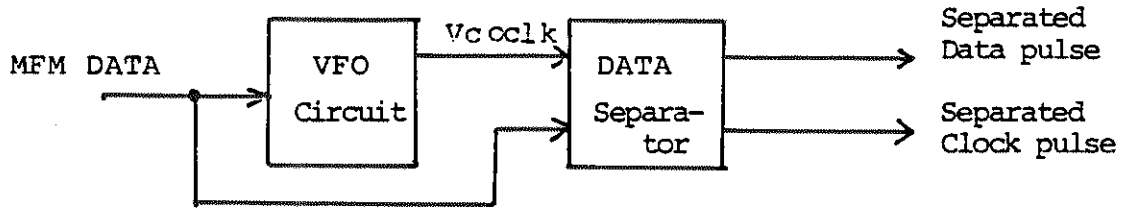

FIGURE 2-16. DATA READ CIRCUIT BLOCK DIAGRAM

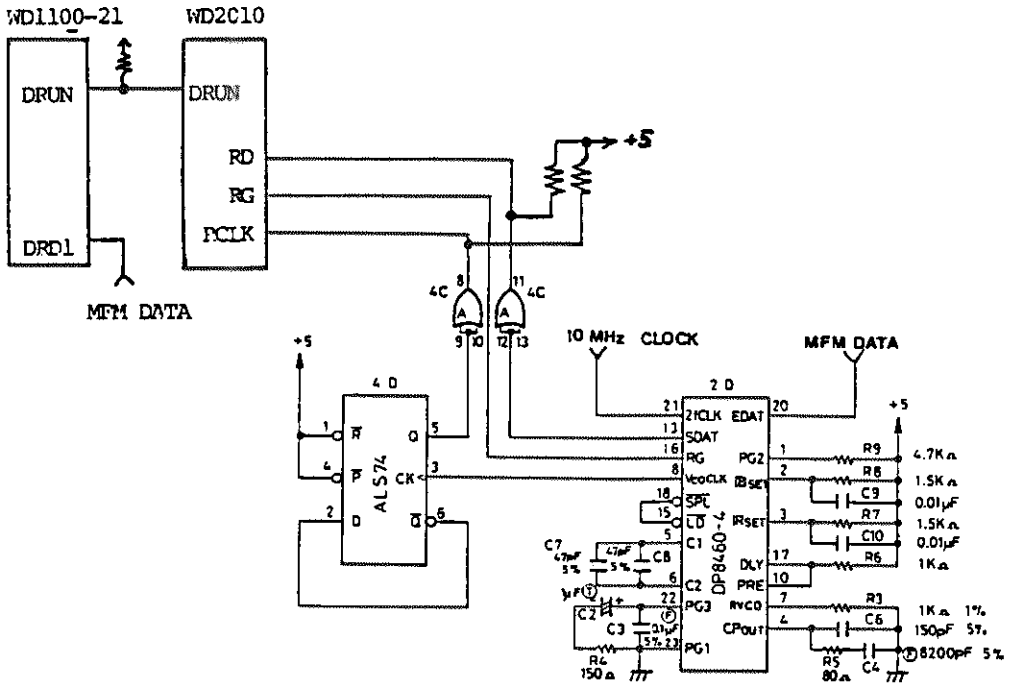

FIGURE 2-17. DATA READ CIRCUIT

Figure 2-18 shows the data read internal circuit.

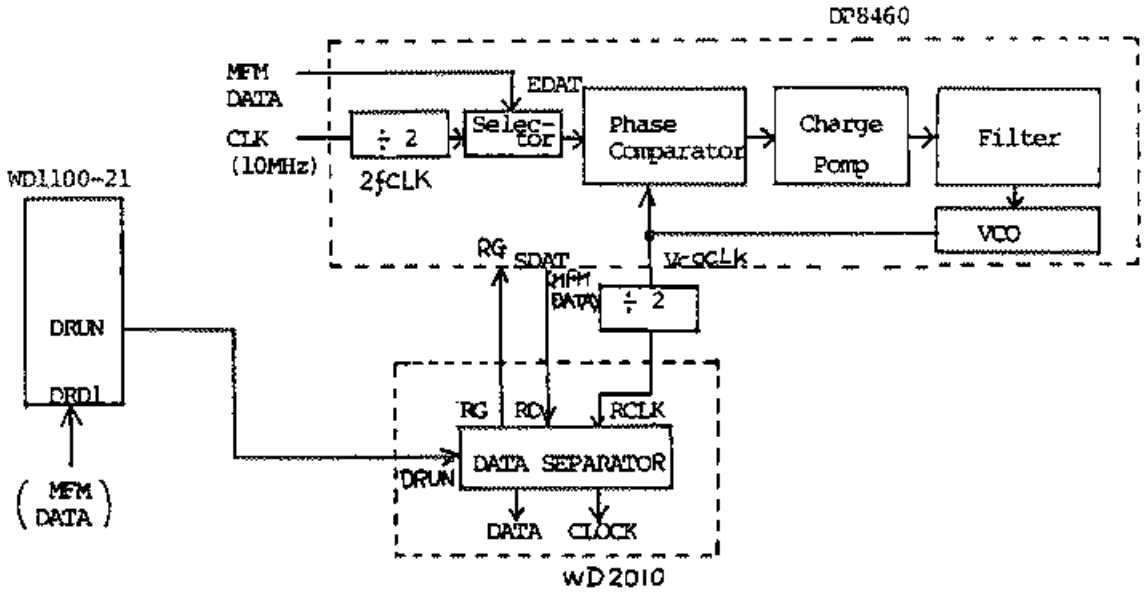

FIGURE 2-18. DATA READ INTERNAL CIRCUIT

DRUN Is active when terminal DRD1 detects a sync field (1*) called sync start. (MFM data is input to terminal DRD1.)

RG Becomes active several bytes after the sync field is detected. When this signal is low, the VFO circuit response speed is fast and the lock time (2*) is short. When it is high, the VFO circuit response speed is slow, which only follows a slow phase change, such as a rotary speed change. (Indicated during data read.)

*1 Sync field: Figure 2-19 shows the hard disk format. The sync field exists at the beginning of the ID field and data field which consist of "00".

*2 Lock time: Operates to match sync field signal timing. Lock time is the time period from sync start to synchronization.

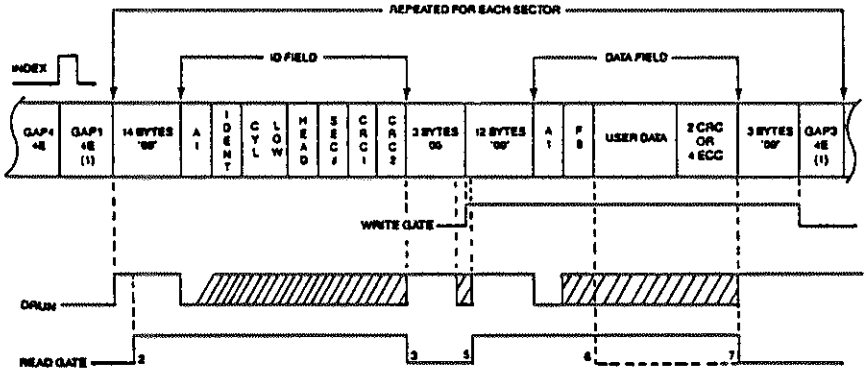

FIGURE 2-19. HARD DISK FORMAT

2.5.6 MRM Data Transmission and Reception Methods

To improve noise performance, the circuitry illustrated in Figures 2-20 through 2-22 is used for MFM data transmission and reception. The principle of noise performance is shown in Figure 2-23. When WG is inactive, +MFM WD and -MFM WD terminals have high impedance.

FIGURE 2-20. MFM DATA TRANSMISSION CIRCUIT

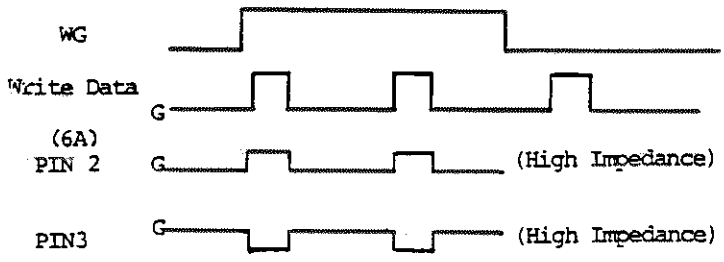

FIGURE 2.21. WRITE DATA TRANSMISSION LINE WAVEFORMS

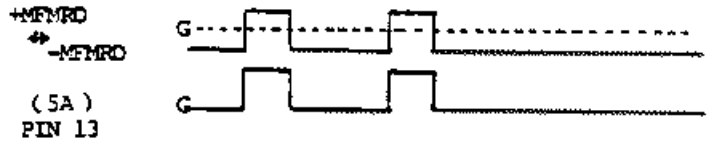

FIGURE 2-22. READ DATA TRANSMISSION LINE WAVEFORMS

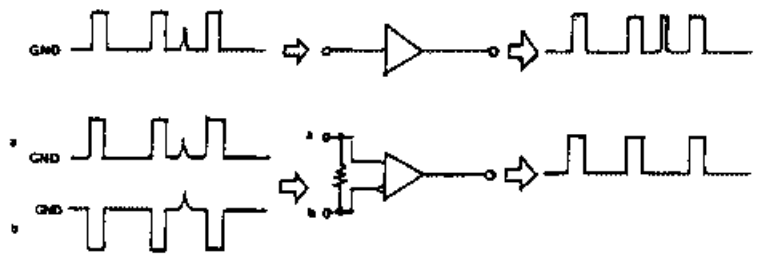

FIGURE 2-23. NOISE PERFORMANCE IMPROVEMENT

2.5.7 Index/Track Zero Sensors

2.5.7.1 Index Sensor

One index pulse is output for each spindle motor rotation by the detection of a gap engraved on the outer circumference of the spindle motor rotor by a magnetic sensor. To reduce the magnetic sensor is uneven response time and temperature dependence, the magnetic sensor output is differentiated once to provide an index pulse. The index pulse cycle is 16.67 nsec (3,600 RPM), with a pulse width of 200 usec (typ).

2.5.7.2 Track Zero Sensor

A shield plate affixed to the stepper motor shaft shields light transmitted to a photosensor for track zero detection. When the photosensor is off (light is shielded) and the stepper motor has A-phase excitation, Track 00 is detected. The shield plate location adjustment is based on the relationship between the response time of the photosensor and the shield plate shift speed, so that the photosensor is turned off (light is shielded) between cylinders 2 and 3. (C-D phase excitation location.)

2.6 HARD DISK DRIVE (DK503-2)

2.6.1 Main Components

The DK503-2 consists of the following five parts:

Data enclosure

Control circuit board

Index and track zero sensors

Frame

Front panel

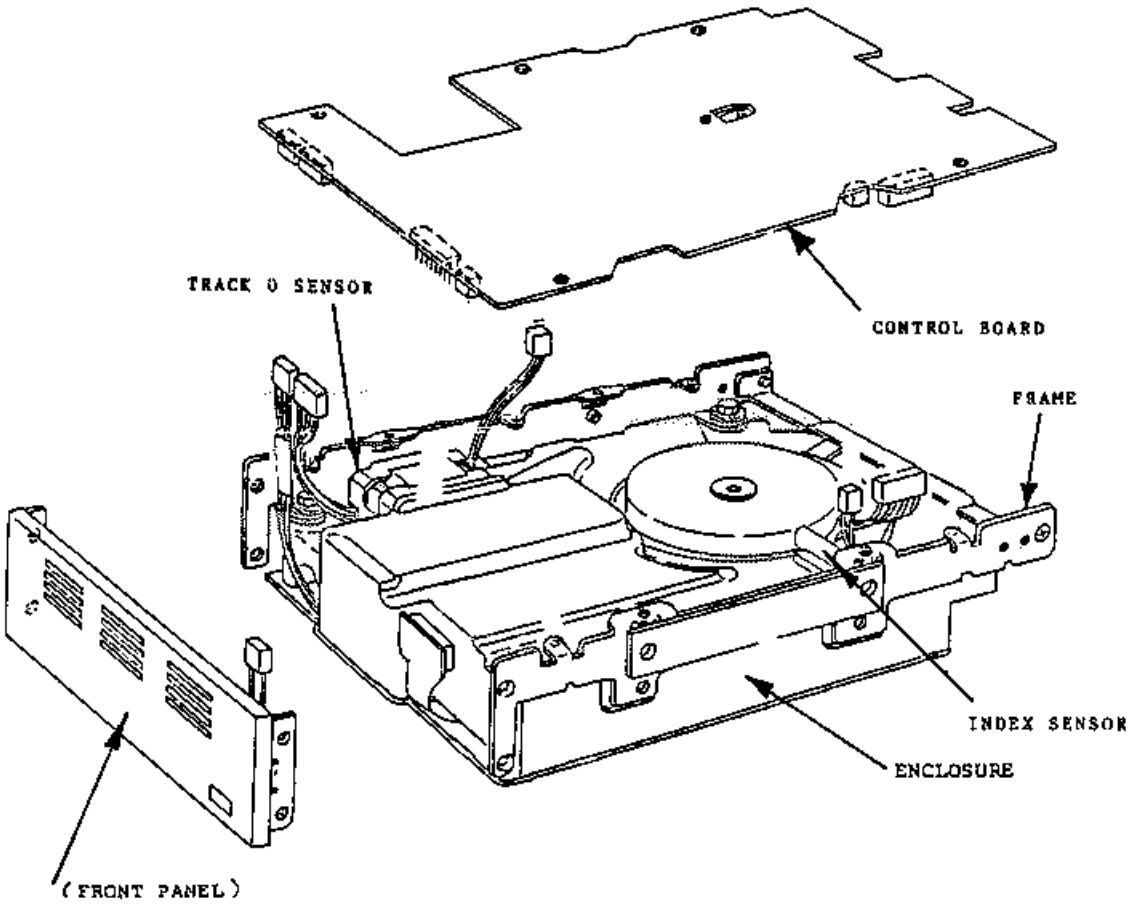

FIGURE 2-24. DK503-2 MAIN COMPONENTS

The sealed data enclosure consists of a magnetic head, magnetic disk, spindle motor actuator, and write/read amplifiers.

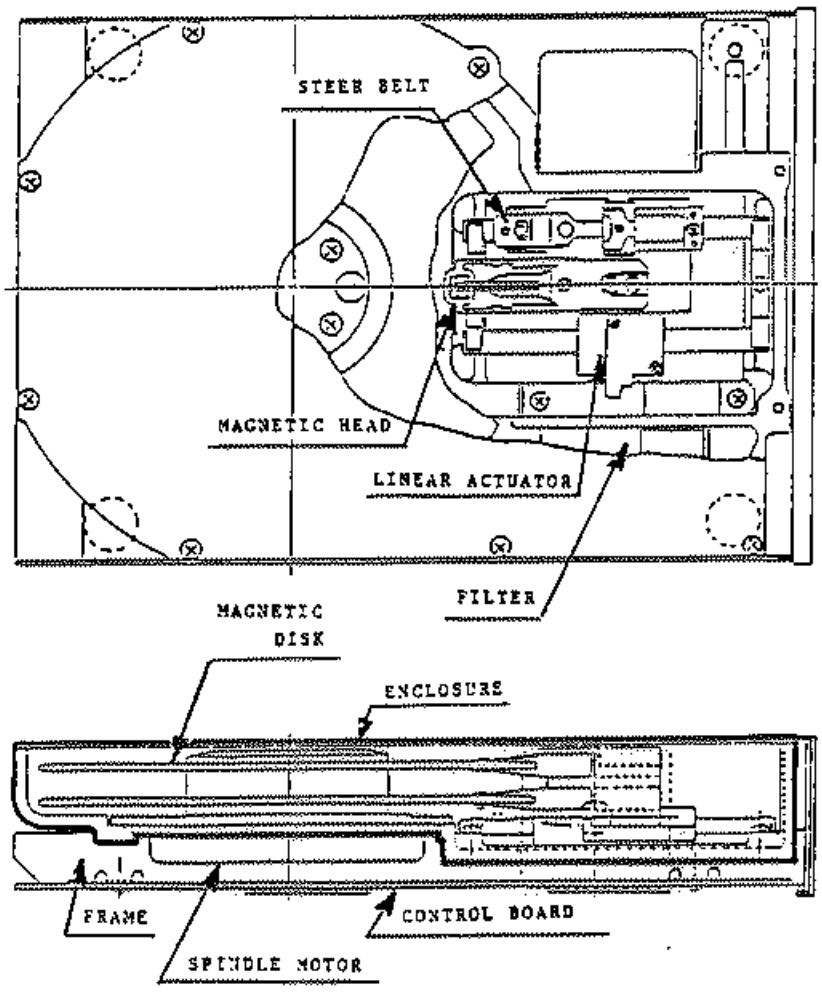

FIGURE 2-25. DATA ENCLOSURE

Magnetic head/disk: The DK503-2 incorporates two magnetic disks and four heads that perform data read and write on each corresponding disk face.

Spindle motor: To rotate the magnetic disks, a brushless DC motor is coupled directly to the spindle. The 3600 RPM rotation is controlled by a microcomputer on the control circuit board, and a drive circuit with 12VDC is used as a drive source. When the motor is off, the motor coil is shorted by a relay to provide a quick stop time.

Linear actuator: The linear actvator consists of a head arm, linear slider, steel belt, and a stepper motor The heads are shifted by an amount that corresponds to the rotary angle of the stepper motor.

Write amp/Read amp: The write amp performs data write while the read amp provides preamplification for the read signal. They are mounted on a flexible printed circuit board in the data enclosure.

2.6.2 Control Circuit Board

All DK503-2 hard disk drive control circuits are mounted on one printed circuit board.

Control circuits: Interface line driver, receiver circuit
Access control circuit
Read/write control circuit
Spindle motor dirve control circuit

Figure 2-26 provides a control circuit board block diagram.

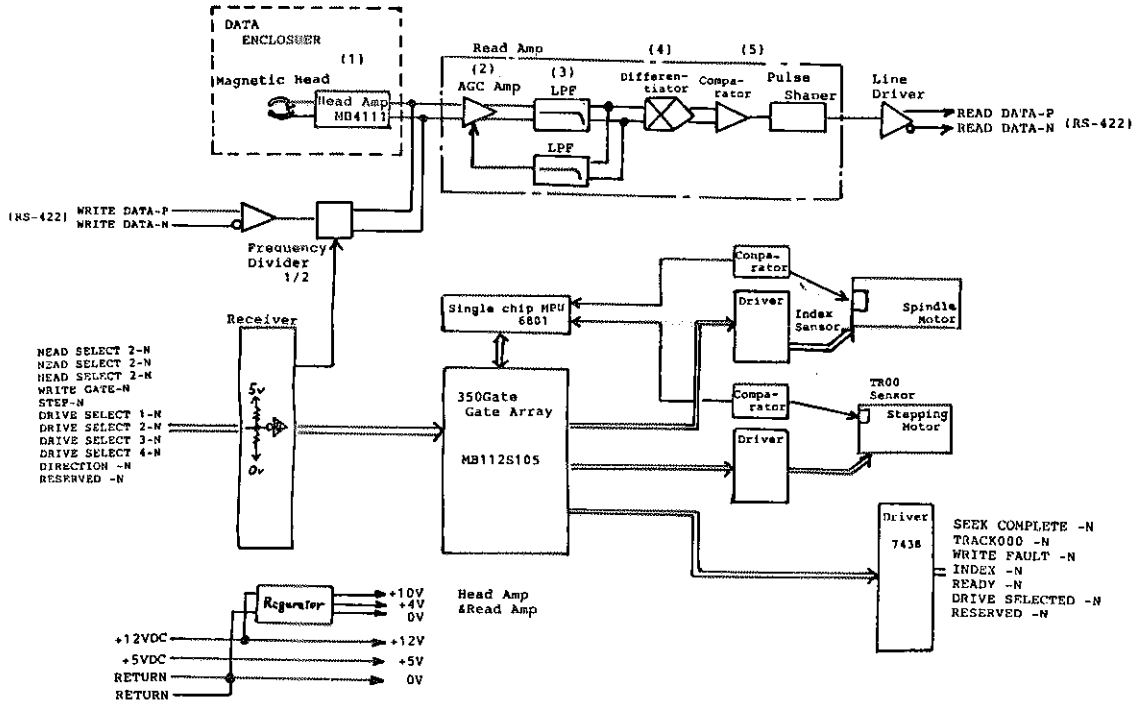

FIGURE 2-26. HARD DISK DRIVE CONTROL CIRCUIT BOARD

Preamp: The differential input/output preamp is mounted on the flexible printed circuit board in the data enclosure. The weak voltagbe from the head (1-2mVpp) is amplified about 40 times (typ.).

AGC amp: Gain is automatially controlled within a 5- to 10-fold range to compensate for differences in amplitude by amplifying the read signals between the inner and outer circumference of the disks.

Low pass filter: Removes high frequency noise that overlaps the AGC amp output signal.

Differentiation circuit: Differentiates the read signal.

Comparator, pulse circuit: Converts the differentiated read signal into a 50 nsec (typ.) TTL pulse.

TROUBLESHOOTING

3

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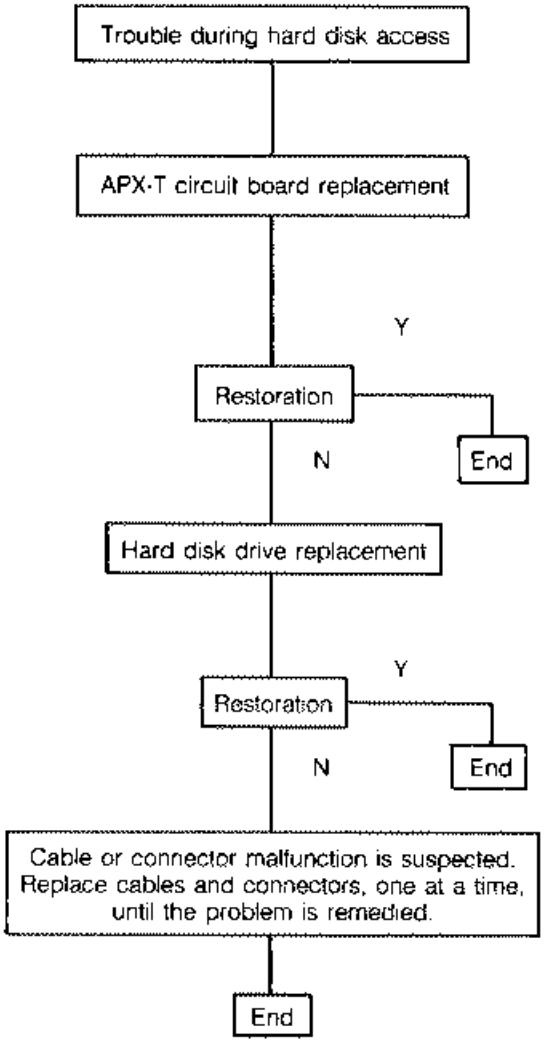
3.1 TROUBLESHOOTING BY UNIT REPLACEMENT

Since the APX-T circuit board and hard disk drive are CPU I/O ports, APX-T circuit board and hard disk trouble are not evident unless these ports are accessed by the CPU. A QX-16HD diagnotic disk is available to test the hard disk. A troubleshooting flowchart is provided below, in Figure 3-1.



Confirm that the power supply and voltage are normal. Also,use a test program to confirm that no trouble exists besides that of the APX-T board and hard disk drive.

FIGURE 3-1. TROUBLESHOOTING FLOWCHART

3.2 HARD DISK DRIVE TROUBLESHOOTING

The following replacement parts are commercially available. However, to ensure correct equipment performance, the replacement of other parts can only be performed at the factory.

1. Front panel (with LED display access)
2. Control circuit board
3. Index sensor

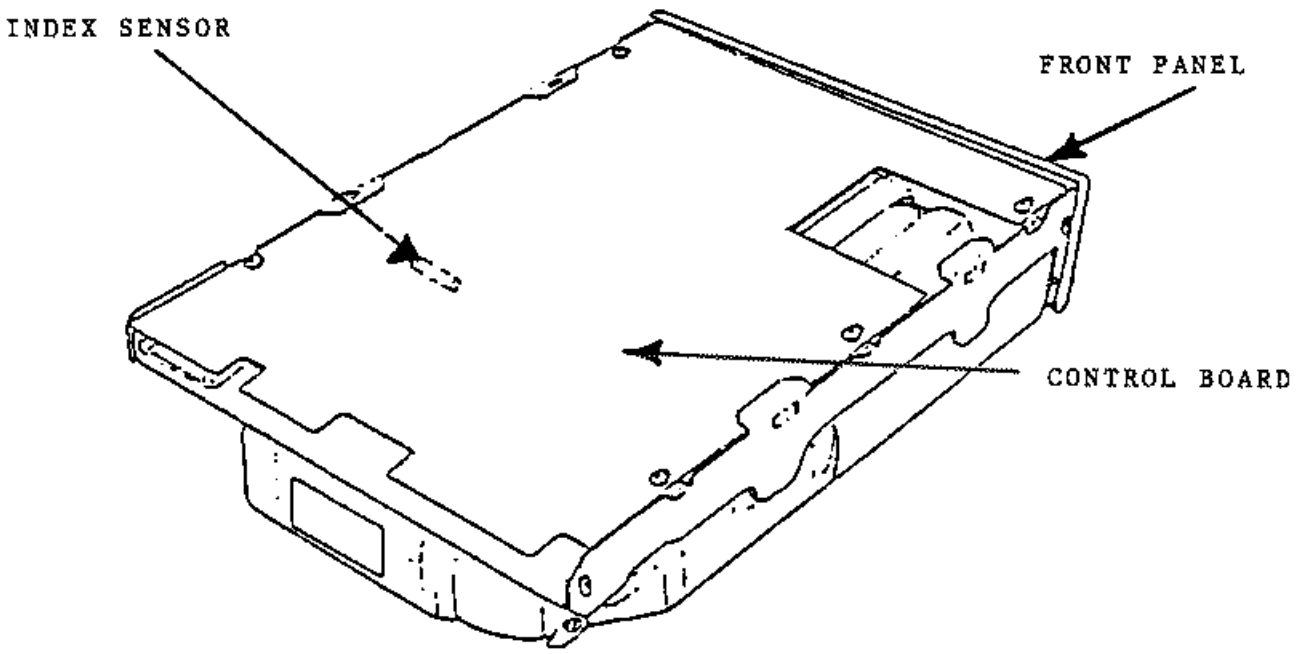


FIGURE 3-2 REPLACEMENT PARTS LOCATIONS

Before attempting troubleshooting, confirm that the terminator mounting and jumper setting are correct.

TABLE 3-1. TROUBLESHOOTING REFERENCE GUIDE

TROUBLE	CAUSE	REMEDY
Read or Read/Write error	Bad sector	Use the test program to verify whether or not the error sector is bad. After confirming that the error sector is a bad sector, register the bad sector using the test program. If the test program does not isolate the error, the error may be intermittent. Retest to verify.
	Control circuit board	Replace the control circuit board. (See Section 4.7.2)
	Enclosure	Replace the hard disk drive unit. (See Section 4.3)
Spindle motor does not rotate	Control circuit board	Replace the control circuit board. (See Section 4.7.2)
	Hard disk unit	Replace the hard disk drive unit. (See Section 4.3)
Rotation stops about 5 seconds after power supply output	Index sensor	Replace the index sensor. (See Section 4.7.5)
	Control circuit board	Replace the control circuit board. (See Section 4.7.2)
Does not seek	Control circuit board	Replace the control circuit board. (See Section 4.7.2)
	Enclosure	Replace the hard disk drive unit. (See Section 4.3)
READY signal is not active	Control circuit board	Replace the control circuit board. (See Section 4.7.2)
	Enclosure	Replace the hard disk drive unit. (See Section 4.3)
Access display LED does not light	Front panel	Replace the front panel. (See Section 4.7.1)
	Control circuit board	Replace the control circuit board. (See Section 4.7.2)

DISASSEMBLY AND ASSEMBLY

4

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4.1 OPTION COVER AND UPPER CASE REMOVAL

1. Remove two screws (A) from the option cover (Figure 4-1) and lift the cover from the main unit. Remove the option port shield (B) if present.
2. Use a flat-blade screwdriver to lift two caps (C) from the upper case, then remove four screws (D).
3. Remove cable (E) from disk drive A; remove cables (F) from the hard disk drive; remove speaker connector CN14 (G); then lift the case to remove.
4. Remove ground wire (H).

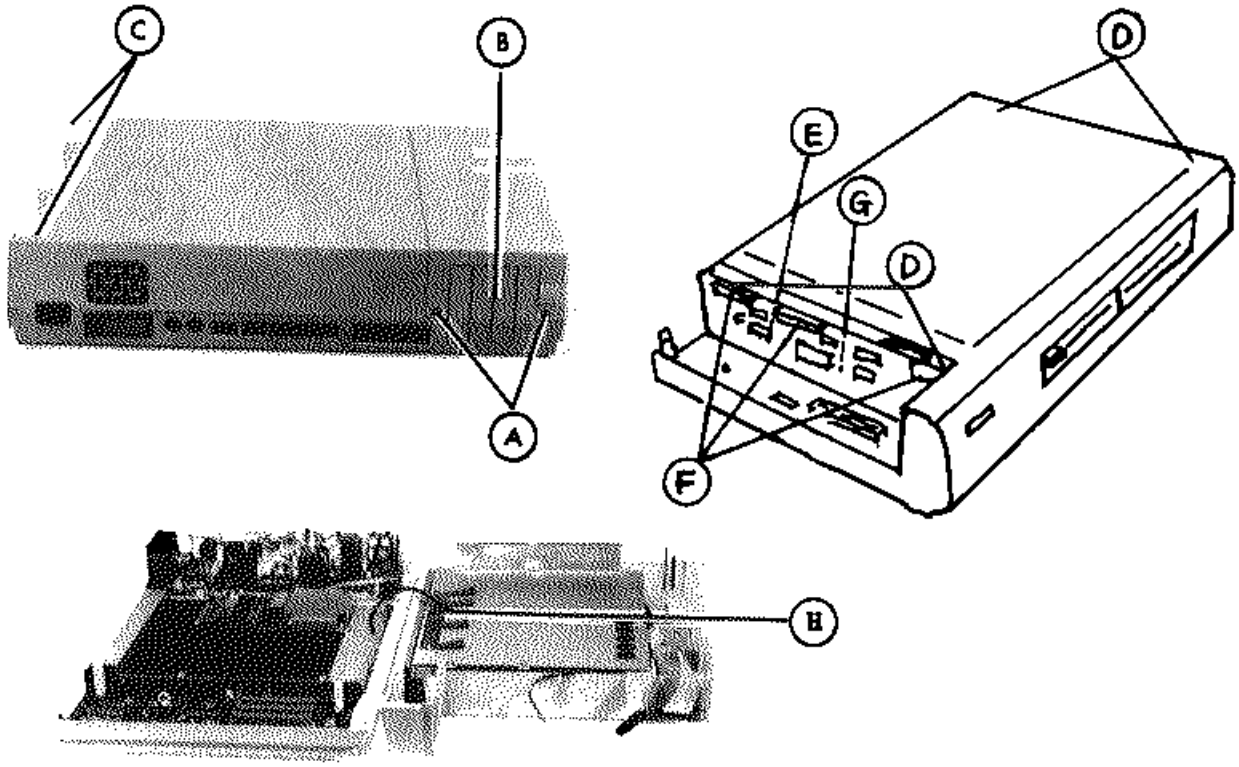

FIGURE 4-1. UPPER CASE REMOVAL/REPLACEMENT

4.2 OPTION COVER AND UPPER CASE REPLACEMENT

1. Install connector (E) to disk drive A (Figure 4-1); connect (F) to the hard disk drive; install connector CN14 (G), to the speaker; connect ground wire (H); then position the upper case on the lower case assembly.

NOTE: *Make sure the FDD cable and the hard disk drive cables are not pinched between the grounding tabs on the video board and the case top.*

2. Install the four Phillips screws (D) and two caps (C).
3. Install the option port shield (B) and the option cover; secure the cover with two screws (A).

4.3 FDD AND HARD DISK DRIVE (HDD) REMOVAL

1. Remove the upper case (Section 4.1).
2. Remove four screws (A), Figure 4-2, from grounding plate (B).
3. Remove two screws (C) to remove drive A; remove two screws (D); and remove the insulation plate to remove the hard disk drive. Slide the drive through the opening in the front case of the main unit to remove.

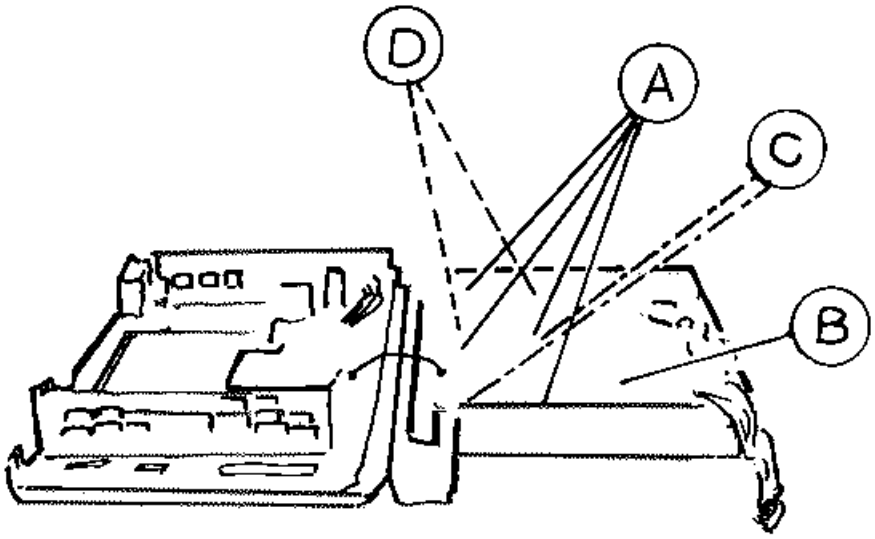

FIGURE 4-2. FDD AND HDD REMOVAL/REPLACEMENT

4.4 FDD AND HDD UNIT REPLACEMENT

1. Slide the drive through the opening in the front case (Figure 4-2). Install two screws (C) to secure drive A, and install the insulation plate and two screws (D) to secure the HDD.
2. Position grounding plate (B), then install four screws.

Make sure to use the screw (D) with M3 * 4.

4.5 APX-T BOARD REMOVAL

1. Remove the option cover (Section 4.1).
2. Remove cables (A), Figure 4-3, from the APX-T board.
3. Remove the APX-T board by lifting it straight up.

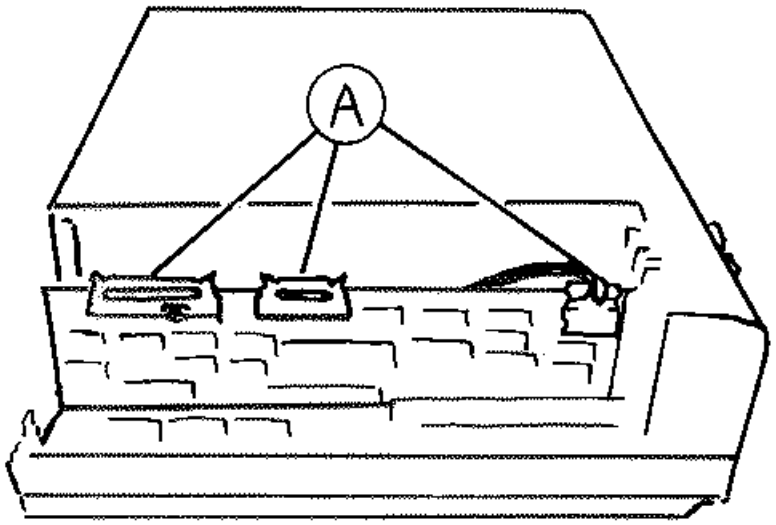

FIGURE 4-3. APX-T BOARD REMOVAL/REPLACEMENT

4.6 APX-T BOARD REPLACEMENT

1. Install the APX-T board (Figure 4-3) in any option slot.
2. Install connectors (A) to the APX-T board.
3. Install the option cover (Section 4.2).

4.7 HDD DISASSEMBLY AND ASSEMBLY

Refer to Figures 4-4 and 4-5 when performing the procedures listed in Sections 4.7.1 through 4.7.6.

4.7.1 Front Panel Removal

1. Remove screws (1) from four locations on the front panel.
2. Remove connector J8, which connects the front panel's LED to the control board.
3. Remove the front panel by drawing if forward.

4.7.2 Front Panel Replacement

1. Mount the front panel.
2. Attach connector J8, which connects the front panel to the control board.
3. Secure screws (1) at four locations on either side of the front panel.

4.7.3 Control Board Removal

1. Remove the front panel.
2. Remove screws (2), which secure the control board at five locations.
3. Remove screw (3), which secures the control board and drive mechanism ground leads.
4. Detach the connector which connects the control board with the drive mechanism.
5. Remove the control board, taking care not to damage it.

4.7.4 Control Board Replacement

1. Mount the board on the drive mechanism and connect all connectors.
2. Secure the ground leads for the control board and drive mechanism.
3. Tighten the screws securing the control board at five locations.
4. Connect the connector between the front panel LED and control board.
5. Install the front panel.

4.7.5 Index Sensor Removal

1. Remove the front panel.
2. Remove the control board.
3. Remove screw (4), which secures the index sensor.
4. Remove the index sensor, taking care that it does not contact the spindle motor.

4.7.6 Index Sensor Replacement

1. Mount the index sensor and tighten it slightly using the mounting tool.
2. Adjust the clearance between the tip of the index sensor and the rotor of the spindle motor to 0.2-0.3 mm, then tighten the screw (See Figure 4.5)
3. Mount the control board.
4. Mount the control panel.

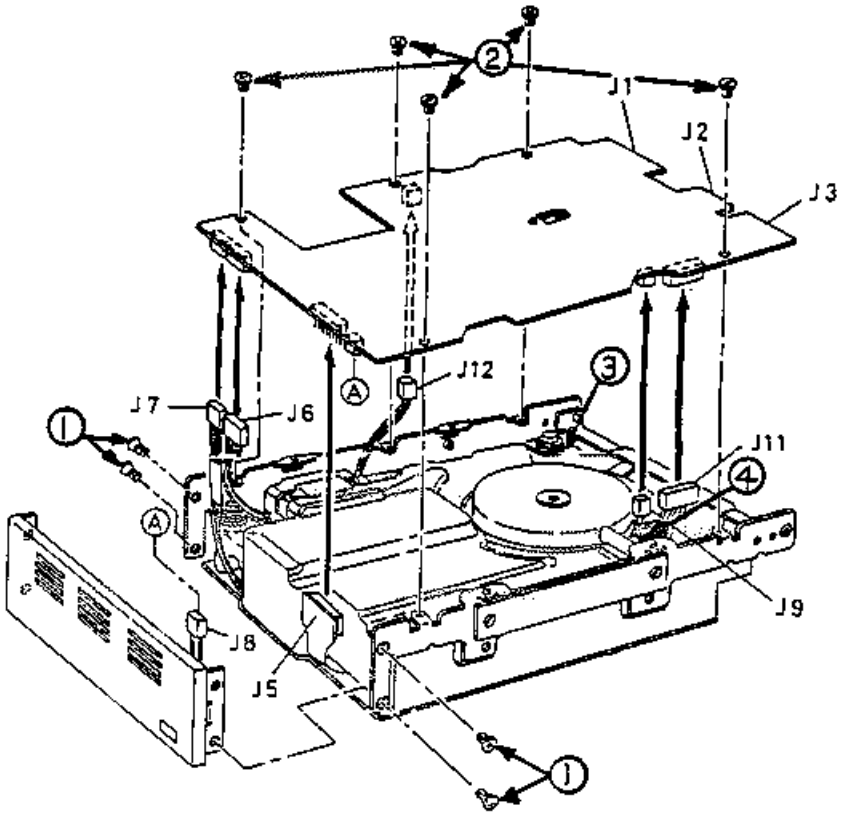

FIGURE 4-4. HARD DISK DRIVE DISASSEMBLY/ASSEMBLY

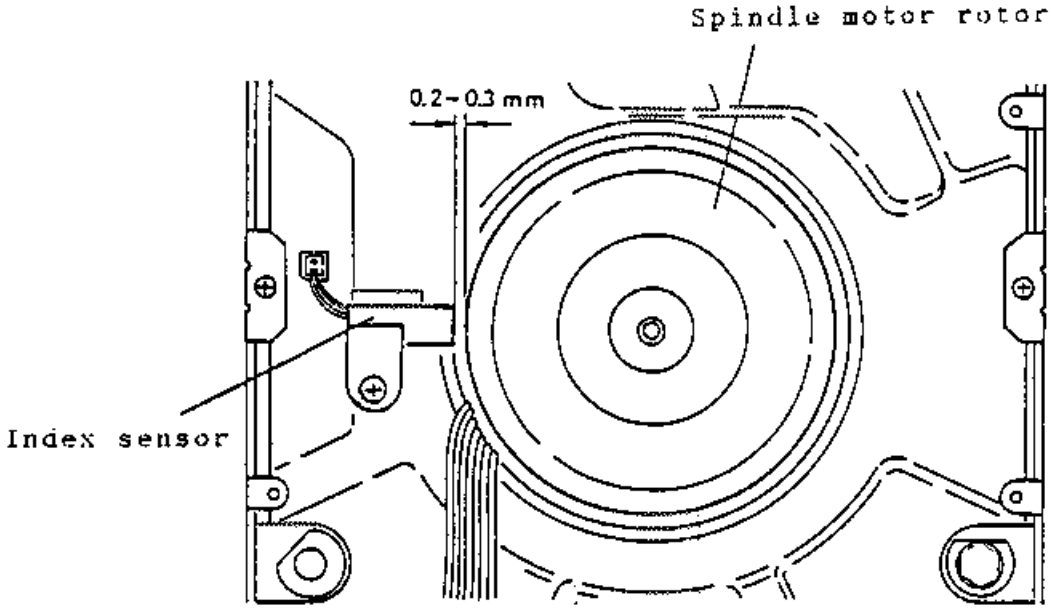

FIGURE 4-5. INDEX SENSOR POSITION

REFERENCE MATERIALS

5

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5.1 DISCRIMINATION OF A BAD SECTOR

The sectors which are recorded on the hard disk drive enclosure should be registered, via software, as bad sectors, using the following procedure:

Step 1. Make a backup copy of the system disk. (See Section 5.2 for details on how to make a backup copy.)

Step 2. Execute the "Read after write" test of the test program.

Step 3. If an error is reported in Step 2, judge the error sector a bad sector.

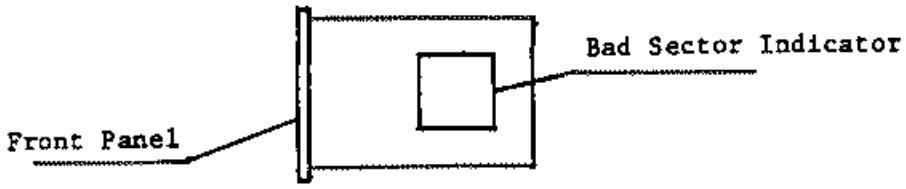


FIGURE 5-1. BAD SECTOR LABEL LOCATION

TABLE 5-1. LABEL CONTENTS

CYL. NO. (Cylinder)	Decimal
HD. NO. (Head)	Decimal
SEC. NO. (Sector)	Decimal

5.2 MAKING A BACKUP COPY

CP/M

HARD DISK DRIVE ⟶ FLOPPY DISK DRIVE

```
A   PIP A:*.* C:
          or
          D:
```

Source drive
Destination drive

FLOPPY DISK DRIVE ⟶ HARD DISK DRIVE

```
A   PIP C:*.* A:
          or
          D:
```

MS-DOS

HARD DISK DRIVE ⟶ FLOPPY DISK DRIVE

```
A   COPY C:*.*.A
```

Destination drive
Source drive

FLOPPY DISK DRIVE ⟶ HARD DISK DRIVE

```
A   COPY A:*.*. C:
```

5.3 HARD DISK DRIVE JUMPER, TERMINATOR, AND DIP SWITCH SELECTION

The HDD unit comes in two configurations (Figure 5-2): a DE-35 control board with a WI30668 enclosure, or a DE-36 control board with a WI30669 enclosure. The control boards are not interchangeable.

The DE-35 board jumper settings and terminator location are illustrated in Figures 5-3 and 5-4, respectively, and Table 5-2 describes the functions of the jumpers.

The DE-36 board has DIP switches instead of the jumper/terminator configuration. Figures 5-5 and 5-6 show the correct settings for these switches.

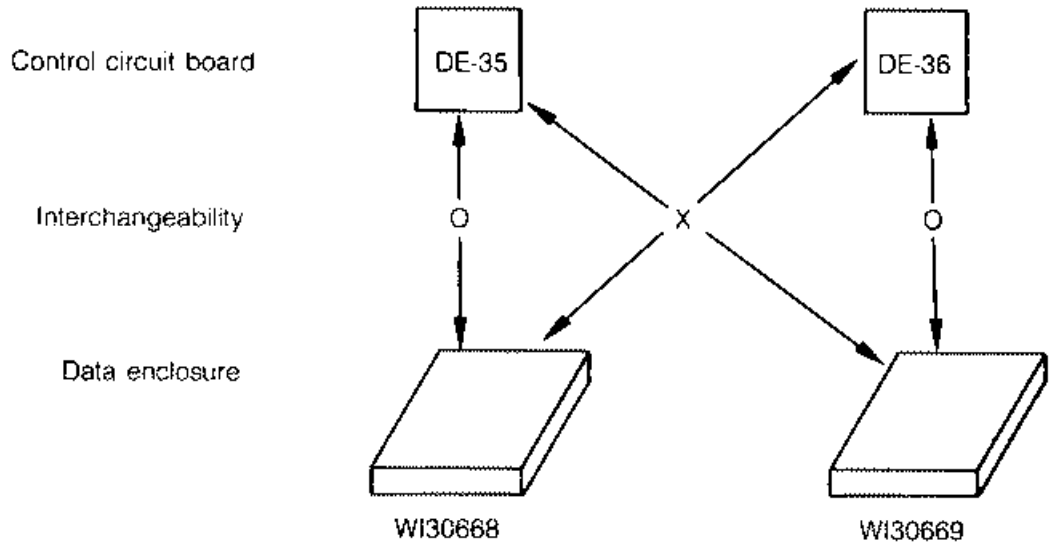


FIGURE 5-2. CONTROL BOARD/ENCLOSURE COMPATIBILITY

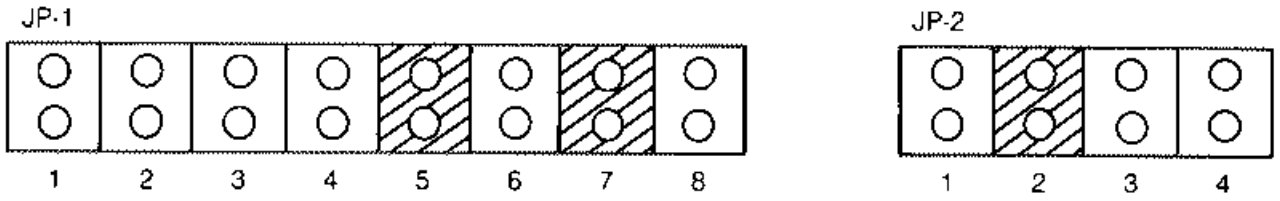


FIGURE 5-3. JUMPER SELECTION—DE-35 BOARD

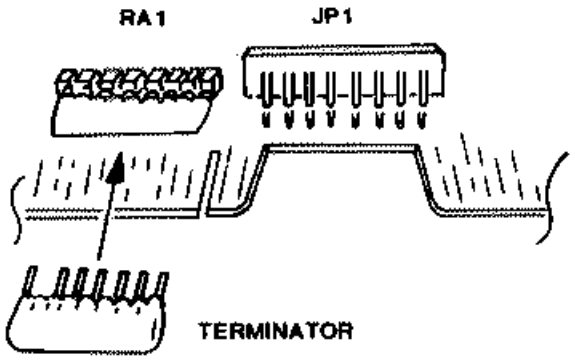
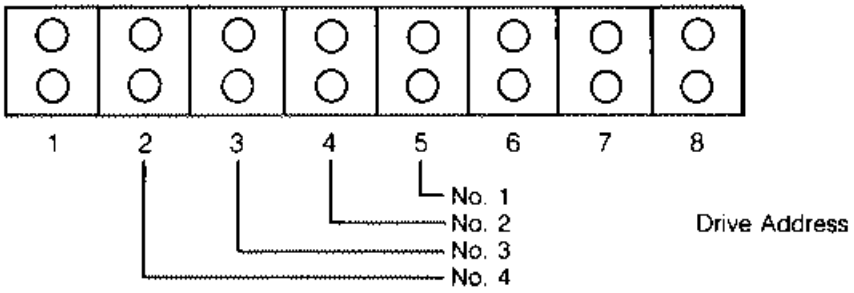


FIGURE 5-4. INSTALLATION OF TERMINATOR—DE-35 BOARD

TABLE 5-2. JUMPER FUNCTIONS

PIN NO.		FUNCTION
JP-1	1 6 8	Utilized when optional functions built into the hard disk control circuit are utilized.
JP-2	1 to 4	
JP-1	2 to 5	Specifies a drive address. Control signal I/O is enabled in the unit only when controller drive select and the drive address specified by a jumper are in accord.

JP-10 JP-1



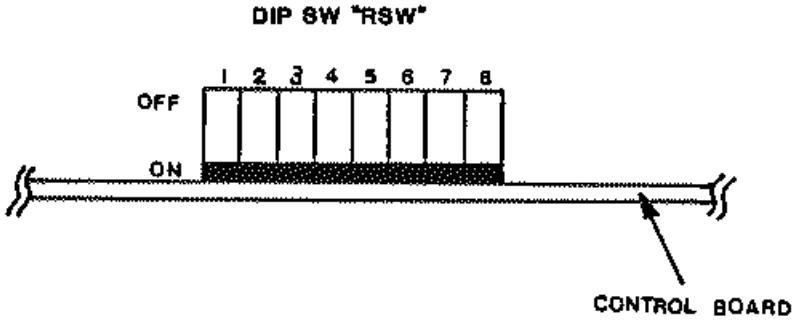


FIGURE 5-5. DIP SWITCH RSW SETTING—DE-36 BOARD

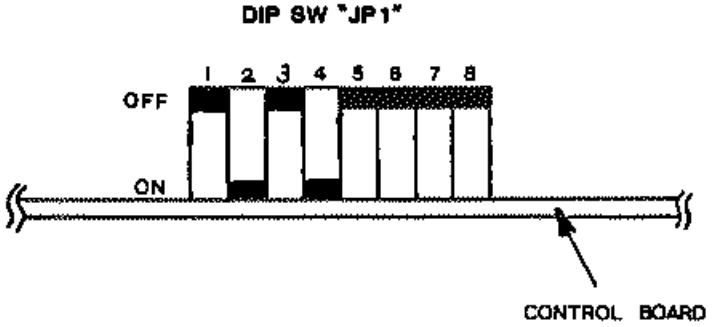


FIGURE 5-6. DIP SWITCH JP1 SETTING—DE-36 BOARD

5.4 HDD (DK503) CONNECTOR SIGNAL NAMES AND FUNCTIONS

Figure 5-7 shows the hard disk drive connector locations, while Tables 5-3 through 5-5 provide the signal names and functions.

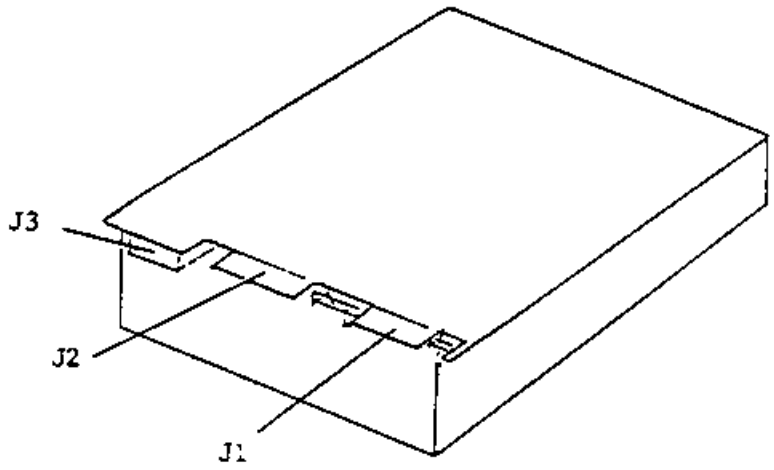


FIGURE 5-7. CONNECTOR LOCATIONS

TABLE 5-3. CONNECTOR J1 PIN FUNCTION

PIN NO.	SIGNAL NAME	I/O	FUNCTION
6	WG	I	Data is written to the disk through the selected head by this signal.
8	SC	O	Indicates that a stepper motor seek operation has been completed. Read/Write enable only occurs when this signal appears.
10	TK000	O	Indicates that a head is positioned at the outermost cylinder. When power is turned on the heads are automatically positioned at this location.
12	WF	O	Output when a drive abnormality is detected and recorded data might be destroyed.
14	HD0	I	Selects head 0.
18	HD1	I	Selects head 1.
20	INDEX	O	Occurs once per disk rotation to indicate track start. Cycle is 16-67 ms t/p.
22	READY	O	Indicates normal disk operation to enable seek.
24	STEP	I	Determines the head seek track number. Head seek occurs in FWD/REV directions by step pulse numbers combined with the DIRIN signal.
26	DS0	I	Selects drive 0.
34	DIRIN	I	Selects seek direction, FWD/REV.
1,3,5	GND	—	—

TABLE 5-4. CONNECTOR J2 PIN FUNCTION

PIN NO.	SIGNAL NAME	I/O	FUNCTION
13	+MFM WD	I	Data to be written to diskette.
14	+MFM WD	I	
17	±MFM RD	O	Data to be read from diskette.
18	+MFM RD	O	
2,4,6,8, 11,12,15, 16,19,20	GND	—	—

5.5 TRANSPORTATION

For safe hard disk transport, shift the heads to cylinder 319 (shipping zone). However, if dedicated transport packing is used, the heads can be at any position during transport.

Cylinder 319 Shifting

Set up: Check the program.

Method: Activate the check program and select "9". SEEK 319 from initial screen, then turn the main frame power supply off.

TABLE 5-5. CONNECTOR J3 PIN FUNCTION

PIN NO.	SIGNAL NAME	I/O	FUNCTION
1	+12 V	I	—
2	+12 V GND	O	—
3	+5 V GND	O	—
4	+5 V	O	—