QX-10

OPTION CARDS

TECHNICAL MANUAL

Q8490026-0

EPSON

INTRODUCTION

This Technical Manual provides technical information on the principles of operation of the QX-10 options and on trouble-shooting. Major technical modifications, if made in the future, will be notified through Service Bulletins, and the Technical Manual should be revised accordingly.

The details of the Manual are subject to change without notice. All the information given in the Manual concerns the QX-10 options, and we are not responsible for any problems with the industrial copyright of a third party that might arise from your application of the Manual to other products or from the connection of the QX-10 options to others.

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CHAPTER 1 GENERAL

1.1. Outline of Options

1.2. Precautions on FCC Regulations

1.3. Maintenance

The QX-10 has five option card slots including the 8-bit parallel data bus. The following option cards are available for user support.

Name	Application
Q10K1	ROM card including JIS 1st level kanji character generator
Q10K2	ROM card including JIS 2nd level kanji character generator
Q10MF	ROM card including 16 kinds of proportional characters
Q10RS	2-channel RS-232C interface card
Q10IE	IEEE-488 interface card
Q10OF	Optical fiber interface card
Q10AD	8-bit A/D-D/A converter
Q10CMS	Color monitor subboard
Q10UC	Universal card usable optionally by user
Q10LP	Light pen

Table 1-1

1.2. Precautions on FCC Regulations

1) The FCC regulations require each option card to meet the regulated values when mounted in the QX-10 system. All EPSON brand option cards satisfy these regulations. However, when option cards are produced by the universal card (Q10UC) and sold under the EPSON brand, each of these option cards must be approved by FCC.
In such a case, samples of these cards shall be submitted to EPSON, System Design Section 1 for recognition by EPSON.
Application by the foreign corporation of EPSON or EPSON CORPORATION to FCC (FTZ) shall be considered each time the application is made.

2) Precautions on designing option cards to meet FCC Regulations

   (1) Use C-MOS IC as far as possible in option cards. If C-MOS IC cannot be used, use LS or normal TTL. Never use TTL of S, ALS.

   (2) Use thick GND and power supply pattern, and make the power supply impedance sufficientyly small.

   (3) Make the clock frequency as low as possible, and make the waveform as dull as possible in the leading and trailing edges.

   (4) When a connector is needed for external connection, use a connector with metallic case and connect FG (Frame Ground) to the metal plate on the rear panel of QX-10.

1.3. Maintenance

The following tool and test program are available for maintenance of option cards.

Tool: Q10 Extension Card (Y135211001)

As shown in Fig. 1-1, this card is inserted in the option slot to raise the option card position for ease of waveform observation and repair.

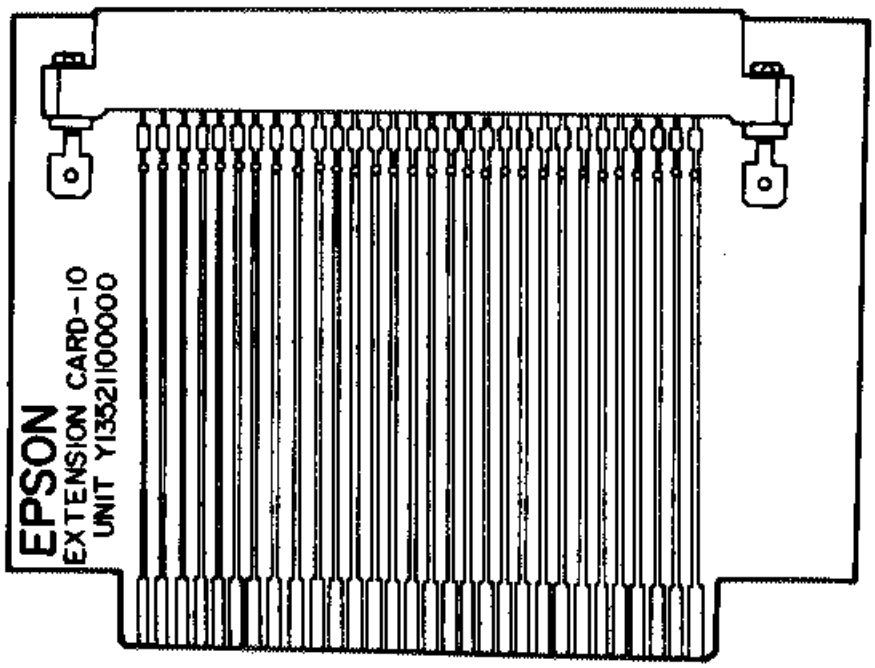


Fig. 1-1

Test Program: The test program is used for checking operation of option card.

CHAPTER 2 SPECIFICATIONS OF OPTION SLOT SIGNALS

2.1. Location of Option Connector Signals

As shown in Fig. 2-1, there are five option slots on the Q10SYM circuit board under the option cover. Signal lines of 60 pins including the system data bus, address bus and power supply line are output to these slots. Each slot is different in interrupt level, etc. Pay attention to this point when using the slots.
The Table 2-1 shows the location of these option connector signals.

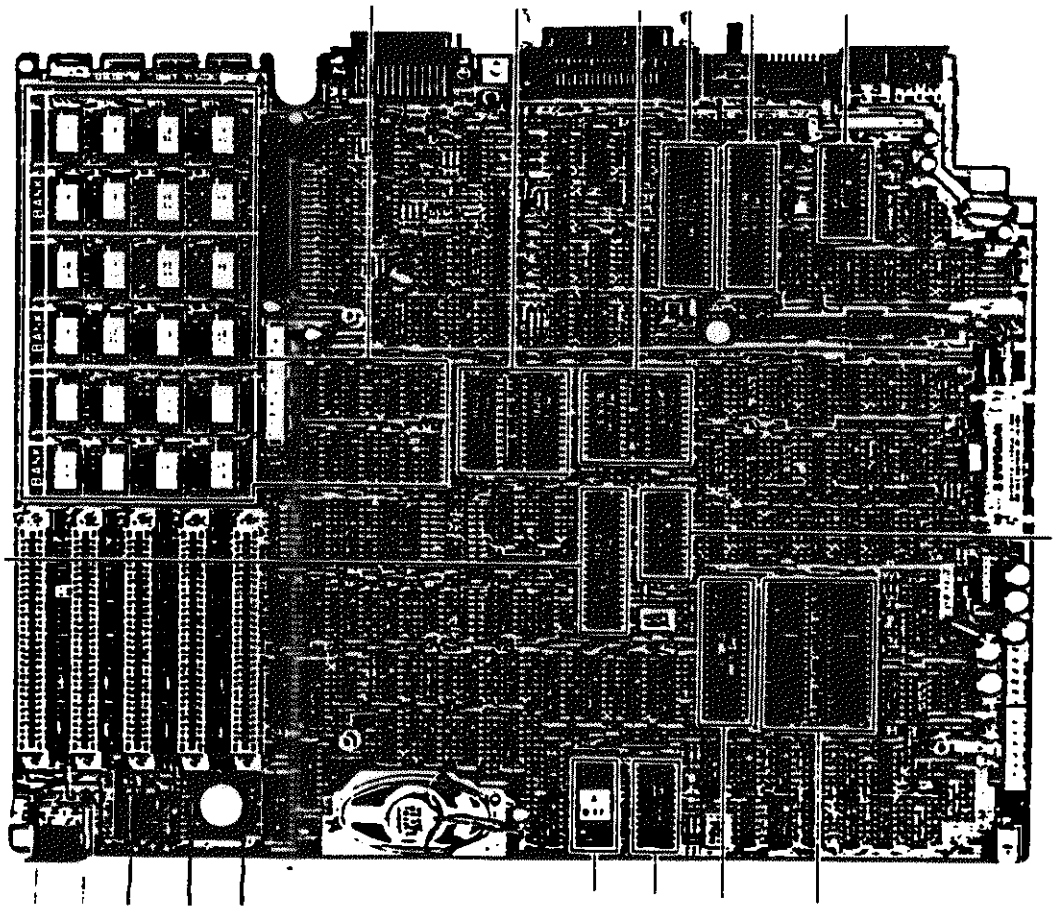


Fig. 2-1 Location of option slots

Pin No.	Signal Symbol	Signal Direction	Description of Signal
1 - 2	GND	——	Ground
3 - 10	DTBO-7	IN/OUT	Data bus
11 - 12	-12 V	——	-12 V
13 - 28	ADRO-15	OUT	Address bus
29 - 30	GND	——	Ground
31	CLK	OUT	System clock
33	$\overline{\text{BSAK}}$	OUT	Bus acknowledge
34	$\overline{\text{MEMX}}$	OUT	External memory select
35	$\overline{\text{IRD}}$	OUT	I/O read
36	$\overline{\text{IWR}}$	OUT	I/O write
37	$\overline{\text{MRD}}$	OUT	Memory read
38	$\overline{\text{MWR}}$	OUT	Memory write
39	$\overline{\text{RSIN}}$	IN	Reset input
40	INT(H)1	IN	High-priority external interrupt
41	INT(H)2	IN	High-priority external interrupt
42	INT(L)	IN	Low-priority external interrupt
43	+5 V	——	+5 V
44	$\overline{\text{RSET}}$	OUT	Reset output
45 - 46	+5 V	——	+5 V
47	$\overline{\text{DRQ(F)}}$	IN	DMA request
48	$\overline{\text{DRQ(S)}}$	IN	DMA request
49	$\overline{\text{RDY(F)}}$	IN	DMA ready
50	$\overline{\text{RDY(S)}}$	IN	DMA ready
51	$\overline{\text{WAIT}}$	IN	Wait

Pin No.	Signal Symbol	Signal Direction	Description of Signal
52	$\overline{\text{IWS}}$	OUT	I/O write short
53	$\overline{\text{DAK(F)}}$	OUT	DMA acknowledge
54	$\overline{\text{DAK(S)}}$	OUT	DMA acknowledge
55	$\overline{\text{EOP(F)}}$	OUT	End of process
56	$\overline{\text{EOP(S)}}$	OUT	End of process
57 - 58	+12 V	——	+12 V
59 - 60	GND	——	Ground

2.2. Description of Signals

Signal	Pin No.	Description
GND	1, 2, 29, 30, 32, 59, 60	Potential 0V. Return lines of respective power supplies (+5, +12, -12). All pins are connected to the signal ground on the main board.
DTB 0 | DTB 7	3 - 10	DATA BUS. Input/Output signals. These are buffered by the bidirectional buffer on the main board. All of these are output signals except for data input from the option slot.
ADR 0 | ADR 15	13 - 28	ADDRESS BUS. Output signals. These signals designate memory addresses and an input/output device.
CLK	31	SYSTEM CLOCK. Output signal. It is the main system clock (3.9936 MHz). The phase is the same as that supplied to the CPU.
$\overline{\text{BSAK}}$	33	BUS ACKNOWLEDGE. Output signal. This is a bus acknowledgement signal for CPU. When LOW, this signal indicates that the DMA is operating.
$\overline{\text{MEMX}}$	34	EXTERNAL MEMORY SELECT. Output signal. When LOW, this signal indicates that memory at the option slot has been selected.
$\overline{\text{IRD}}$	35	I/O READ. Output signal. Set to LOW for data input from an I/O device; the CPU receives data at the rising edge of the signal.
$\overline{\text{IWR}}$	36	I/O WRITE. Output signal. Set to LOW for data output to an I/O device.
$\overline{\text{MRD}}$	37	MEMORY READ. Output signal. Set to LOW for data input from memory; the CPU receives data at rising edge of the signal.

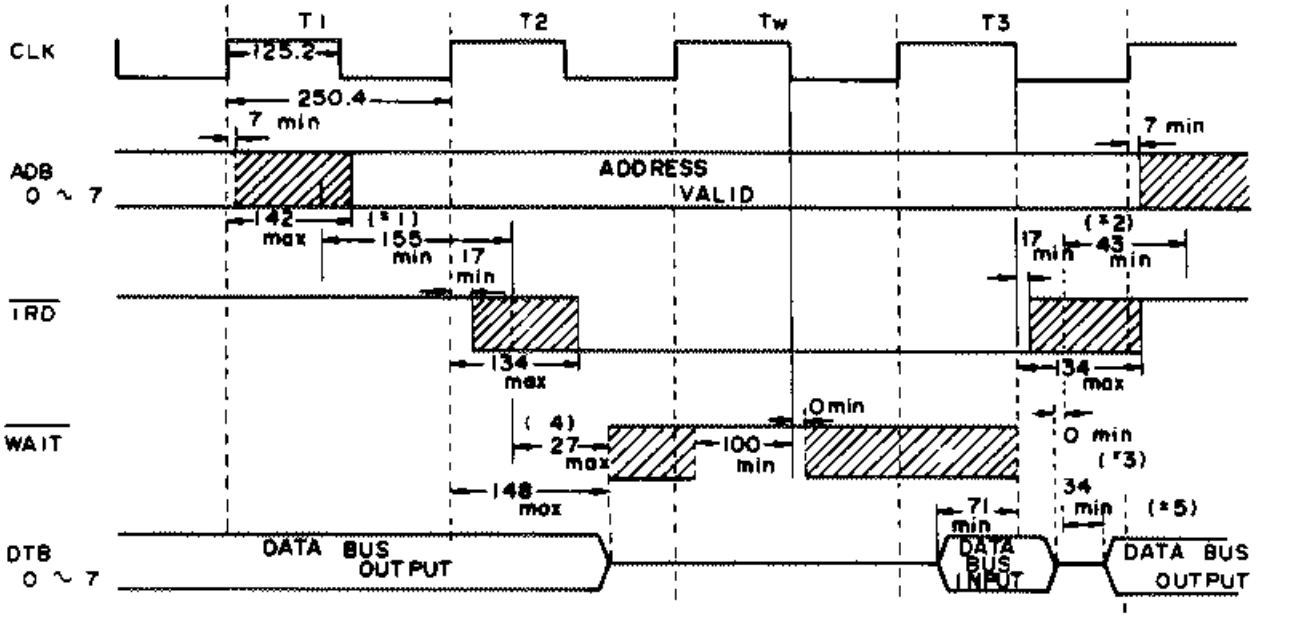
Signal	Pin No.	Description
$\overline{\text{MWR}}$	38	MEMORY WRITE. Output signal. Set to LOW level for data output to memory.
$\overline{\text{RSIN}}$	39	RESET IN. Input signal. Input of this signal from the option side resets the CPU when the signal goes LOW, while the reset operation ends when the signal is set to HIGH.
INT(H) 1 INT(H) 2	40 41	HIGH PRIORITY EXTERNAL INTERRUPT. Input signals. High priority interrupts applied when signals are set to HIGH. These signals are connected to the 8259 on the main board.
INT(L)	42	LOW PRIORITY EXTERNAL INTERRUPT. Input signal. This signal is used in the same manner as INT(H), but the priority of the interrupt is low.
$\overline{\text{RSET}}$	44	RESET. Output signal. This signal initializes the device at the option slot. When the system is in the reset condition, this signal is set to LOW.
$\overline{\text{DRQ(F)}}$ $\overline{\text{DRQ(S)}}$	47 48	DMA REQUEST. Input signals. These signals are set to LOW to request DMA transfer from a device at the option slot. DRQ(F) has a higher DMA request level than DRQ(S).
$\overline{\text{RDY(F)}}$ $\overline{\text{RDY(S)}}$	49 50	DMA READY. Input signals. WAIT can be applied to the DMA controller by setting these signals to LOW. RDY(F) and RDY(S) correspond to DRQ(F) and DRQ(S), respectively.
$\overline{\text{WAIT}}$	51	WAIT. Input signal. CPU operation can be interrupted by setting this signal to LOW.

Signal	Pin No.	Description
$\overline{\text{IWS}}$	52	I/O WRITE SHORT. Output signal. Used when the IWR signal does not provide sufficient time to write data from an external memory to an I/O device during a DMA transfer.
$\overline{\text{DAK(F)}}$ $\overline{\text{DAK(S)}}$	53 54	DMA ACKNOWLEDGE. Output signals. When the DMA controller receives DRQ, these signals are set to LOW when the DMA is started. DAK(F) and DAK(S) correspond to DRQ(F) and DRQ(S), respectively.
$\overline{\text{EOP(F)}}$ $\overline{\text{EOP(S)}}$	55 56	END OF PROCESS. Output signals. These signals indicate the end of 1 block during a DMA transfer. They are set to LOW together with DAK when the last byte is sent. EOP(F) and EOP(S) correspond to DRQ(F) and DRQ(S), respectively.
+5 V	43, 45, 46	+5 V power supply lines. (Up to 2 A.)
+12 V	57, 58	+12 V power supply lines. (Up to 0.2 A.)
-12 V	11, 12	-12 V power supply lines. (Up to 0.04 A.)

2.3. I/O Port Access Timing

(1) I/O Read Timing

[Unit: nsec]



(*1) Address stabilization prior to $\overline{IRD}$.

(*2) Address holding time after $\overline{IRD}$.

(*3) Data holding time after $\overline{IRD}$.

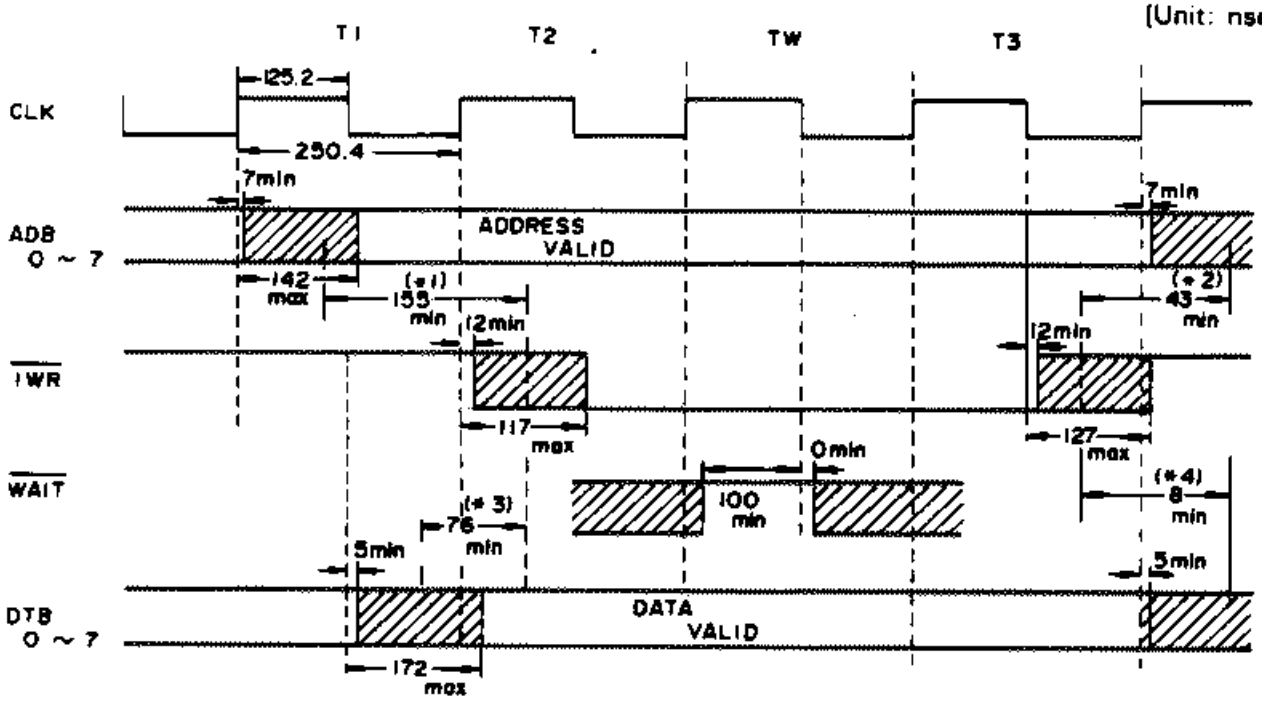
(*4) Delay before float after $\overline{IRD}$.

(*5) Floating hold time after $\overline{IRD}$.

Note: The data bus is normally in the output state, and serves as an input terminal only when data is output from the option side.

(2) I/O Write Timing

[Unit: nsec]



(*1) Address stabilization prior to $\overline{IWR}$.

(*2) Address holding time after $\overline{IWR}$.

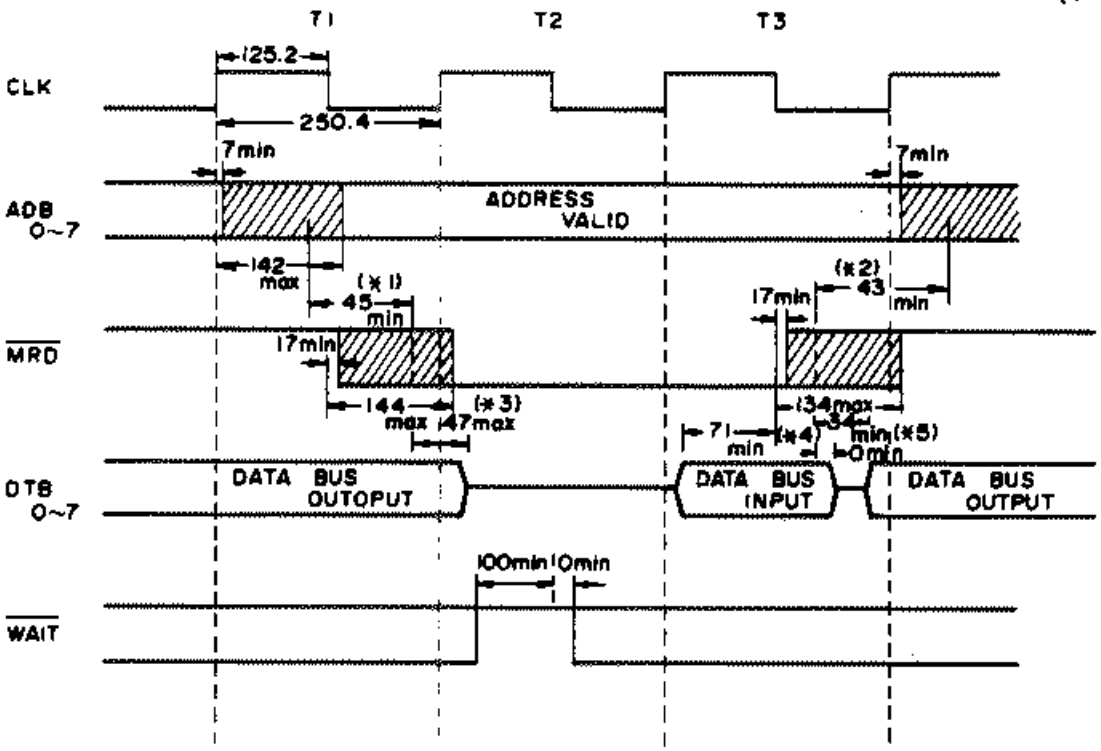
(*3) Data stabilization after $\overline{IWR}$.

(*4) Data holding timing prior to $\overline{IWR}$.

2.4. Memory Access Timing

(1) Memory read timing

(Unit: nsec)



(*1) Address bus stabilization time preceding the falling edge of $\overline{MRD}$.

(*2) Address bus holding time following the rising edge of $\overline{MRD}$.

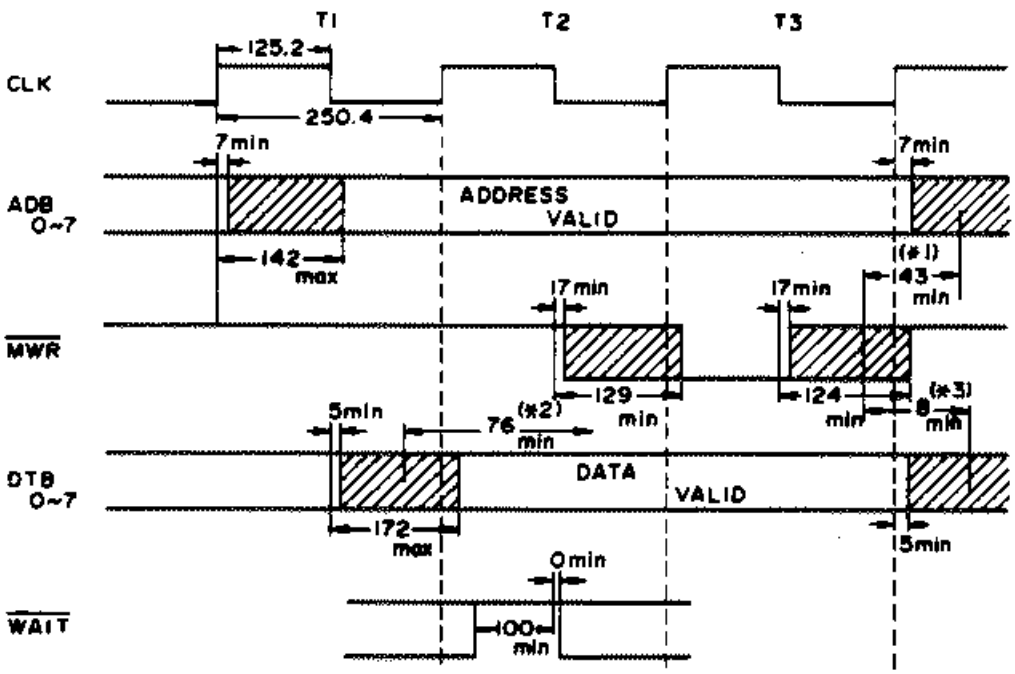
(*3) Time following the falling edge of $\overline{MRD}$ before the data bus starts floating.

(*4) Data bus holding time following the rising edge of $\overline{MRD}$.

(*5) Data bus floating time following the rising edge of $\overline{MRD}$.

(2) Memory write timing

[Unit: nsec]



(*1) Address bus holding time following the rising edge of $\overline{MWR}$.

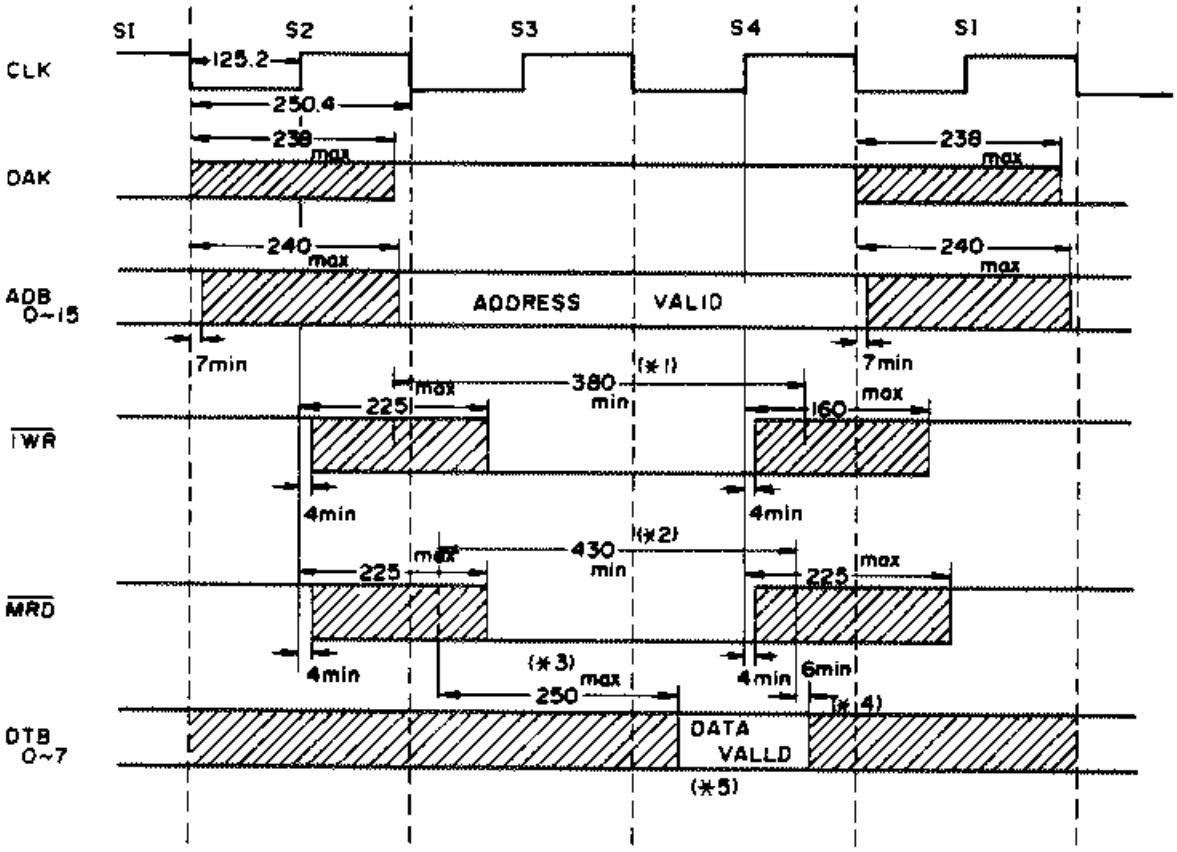
(*2) Data bus stabilization time preceding the falling edge of $\overline{MWR}$.

(*3) Data bus holding time following the rising edge of $\overline{MWR}$.

2.5. DMA Access Timing

(1) Memory read, I/O write timing

[Unit: nsec]



(*1) Low level pulse width of $\overline{IWR}$.

(*2) Low level pulse width of $\overline{MRD}$.

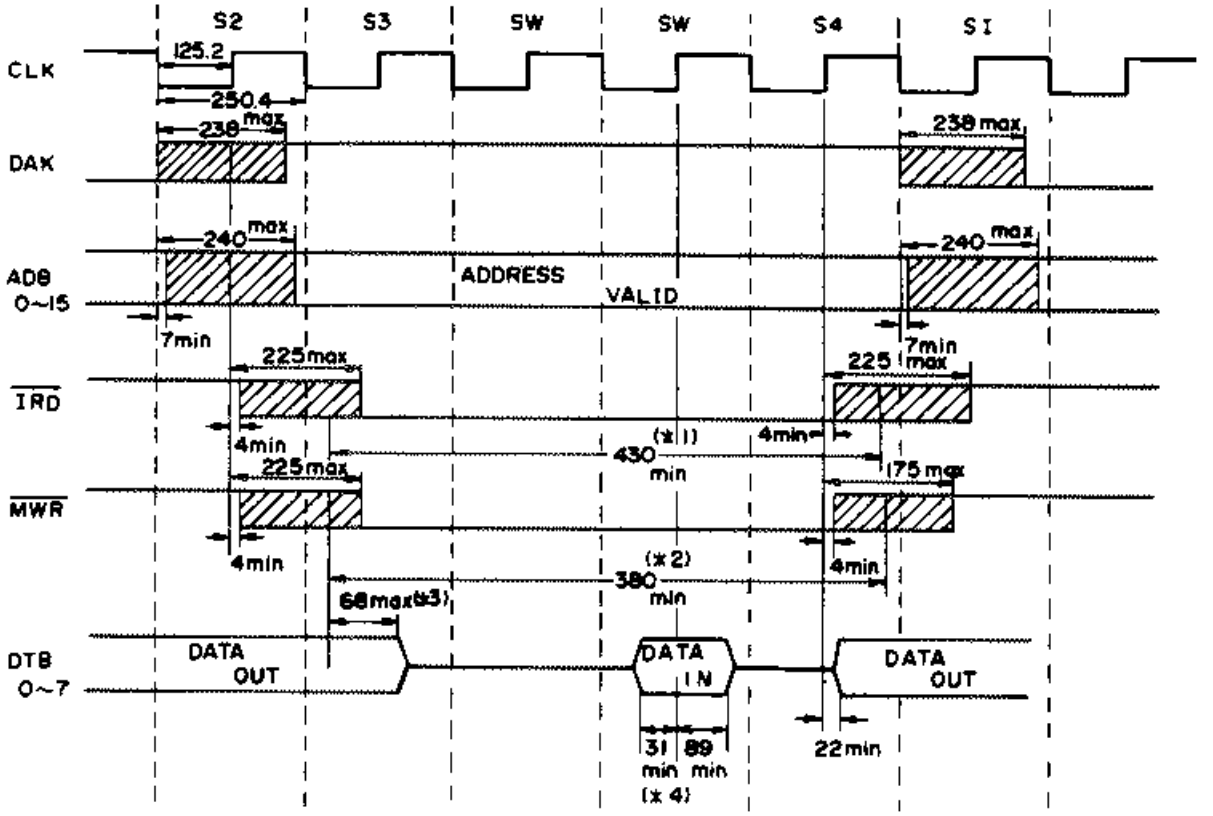
(*3) Data bus stabilization time following the falling edge of $\overline{MRD}$.

(*4) Data bus holding time following the rising edge of $\overline{MRD}$.

(*5) Data from internal memory to I/O in DMA.

(2) I/O read, memory write timing

[Unit: nsec]



(*1) Low level pulse width of $\overline{IRD}$.

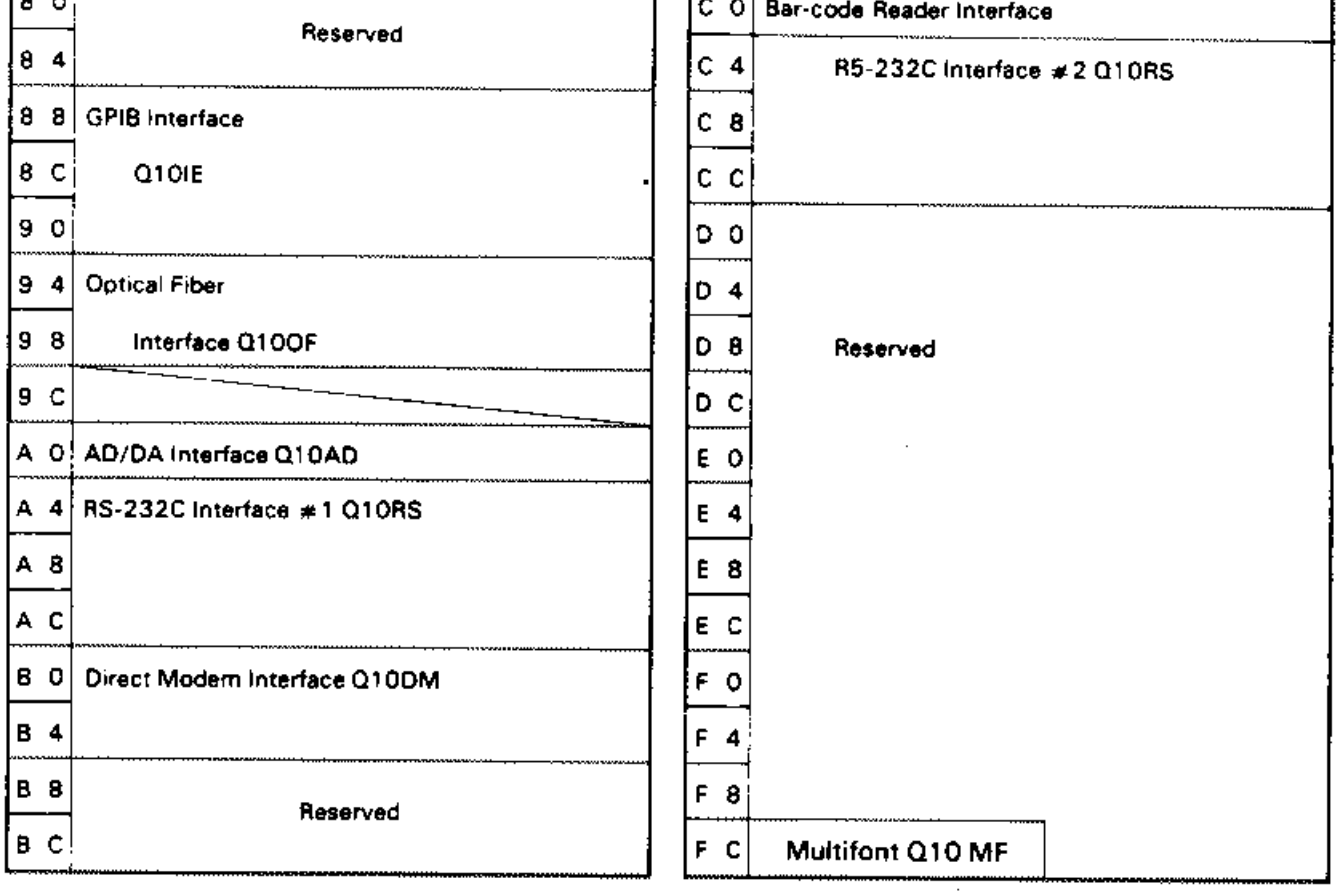
(*2) Low level pulse width of $\overline{MWR}$.

(*3) Time following the falling edge of $\overline{MWR}$ before the data bus starts floating.

(*4) Limitation of input data from I/O to internal memory.

2.6. I/O Port Address Map for Options

The addresses of I/O ports allocated for options are from 80H to FFH. Of these, some are already assigned to existing interface cards. Therefore, when other option cards are prepared, contact the Electronic Instruments Design Dept. of the EPSON Corporation for confirmation that the addresses are free. (This precaution must be observed to prevent the same port from being allocated to more than one option.)


8 0
Reserved
8 4
8 8
GPIB Interface
8 C
Q10IE
9 0
9 4
Optical Fiber
9 8
Interface Q10OF
9 C
A 0
AD/DA Interface Q10AD
A 4
RS-232C Interface #1 Q10RS
A 8
A C
B 0
Direct Modem Interface Q10DM
B 4
B 8
Reserved
B C
C 0
Bar-code Reader Interface
C 4
RS-232C Interface #2 Q10RS
C 8
C C
D 0
D 4
D 8
Reserved
D C
E 0
E 4
E 8
E C
F 0
F 4
F 8
F C
Multifont Q10 MF

2.7. Precautions on Making Interface

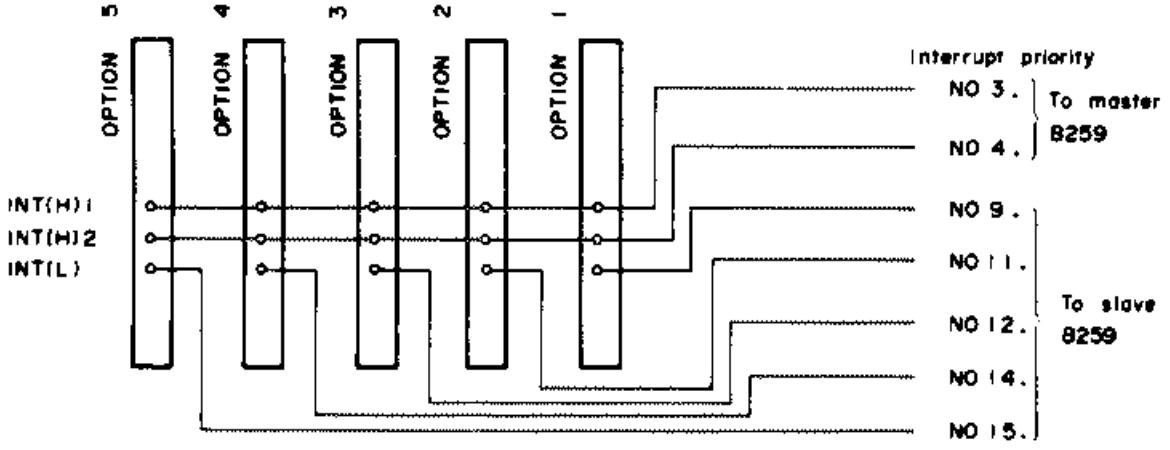
Take note of the following when preparing option cards.

(1) $\overline{\text{RSIN}}$ (Reset signal)

$\overline{\text{RSIN}}$ is the input signal for system reset. Since this signal is directly input to the CPU reset terminals with no particular synchronization, it is recommended that it be synchronized with the rising edge of the read/write pulse and that the pulse width be held to less than 1 mS when D-RAM data is to be saved, however, note that the pulse width must be greater than three clocks.

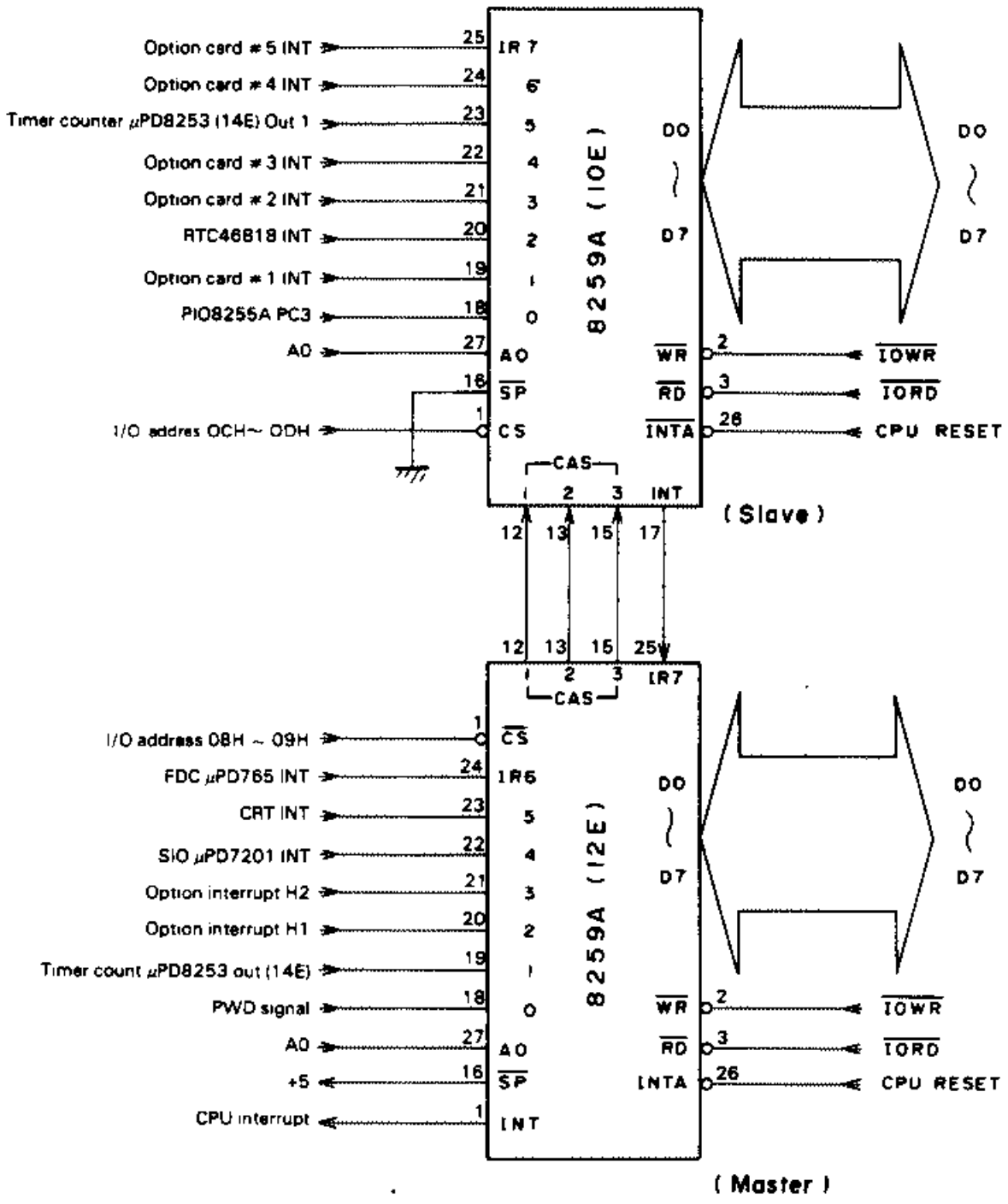
(2) Difference between INT(H) and INT(L) (Interrupt request signals)

Although there are three types of interrupt request signals (INT(H) 1, INT(H) 2, and INT(L)) for each option connector, INT(H) 1 and INT(H) 2 are common to all of the connectors. Therefore, only one card which utilizes INT(H) 1 or 2 can be used at any given time. However, since INT(L) is assigned to the various connectors individually, it can be used with several cards simultaneously. Connection of the INT(H) and INT(L) interrupts on the main board is shown below.



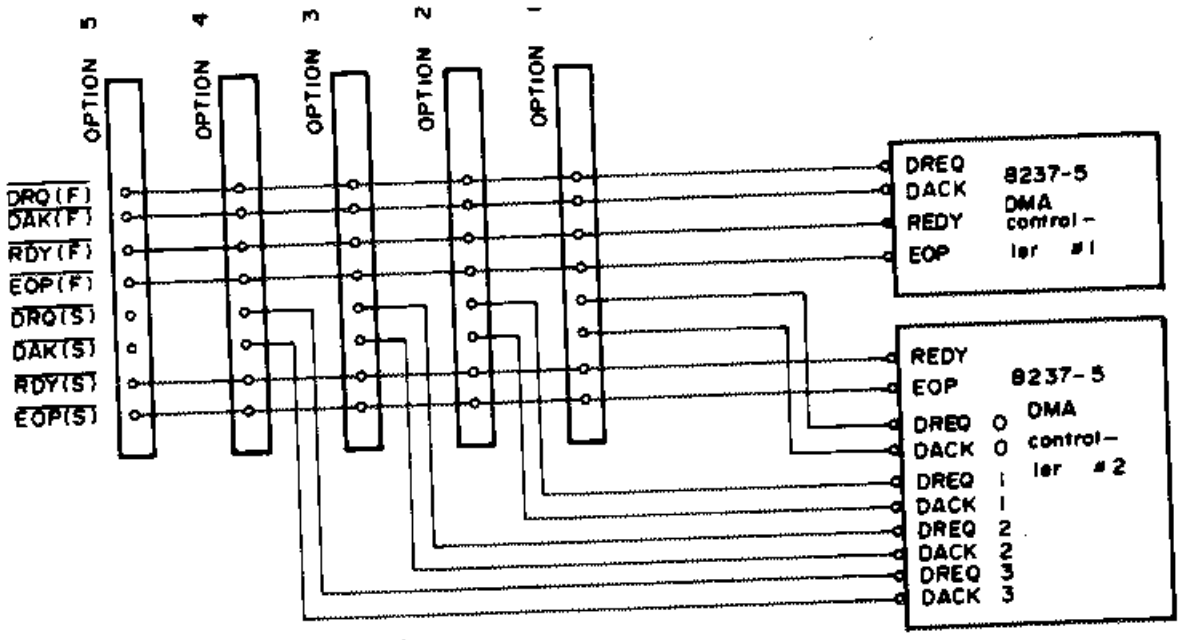
Connection		Relative address	Interrupt cause	
Master	IR0	0000	Power down detection interrupt	High-order
	IR1	0004	Software timer # 1 interrupt	
	IR2	0008	External (option) interrupt INTF 1	
	IR3	000C	External (option) interrupt INTF 2	
	IR4	0010	Keyboard/RS-232C interrupt	
	IR5	0014	CRT/light pen interrupt	
	IR6	001B	Floppy controller interrupt	
				Priority
Slave	IR0	0020	Printer interrupt	
	IR1	0024	External (option) interrupt # 1	
	IR2	0028	Calendar clock interrupt	
	IR3	002C	External (option) interrupt # 2	
	IR4	0030	External (option) interrupt # 3	
	IR5	0034	Software timer # 2 interrupt	
	IR6	0038	External (option) interrupt # 4	
	IR7	003C	External (option) interrupt # 5	Low-order

Interrupt addresses


Option card # 5 INT
Option card # 4 INT
Timer counter μPD8253 (14E) Out 1
Option card # 3 INT
Option card # 2 INT
RTC46818 INT
Option card # 1 INT
PIO8255A PC3
A0
I/O addres OCH~ ODH
25
24
23
22
21
20
19
18
27
16
1
IR 7
6
5
4
3
2
1
0
A0
SP
CS
8259A (10E)
DO
D7
WR
RD
INTA
2
3
26
IOWR
IORD
CPU RESET
CAS
1
2
3
INT
(Slave)
12
13
15
17
12
13
15
25
IR7
I/O address 08H ~ 09H
FDC μPD765 INT
CRT INT
SIO μPD7201 INT
Option interrupt H2
Option interrupt H1
Timer count μPD8253 out (14E)
PWD signal
A0
+5
CPU interrupt
1
24
23
22
21
20
19
18
27
16
1
CS
IR6
5
4
3
2
1
0
A0
SP
INT
8259A (12E)
DO
D7
WR
RD
INTA
2
3
26
IOWR
IORD
CPU RESET
(Master)

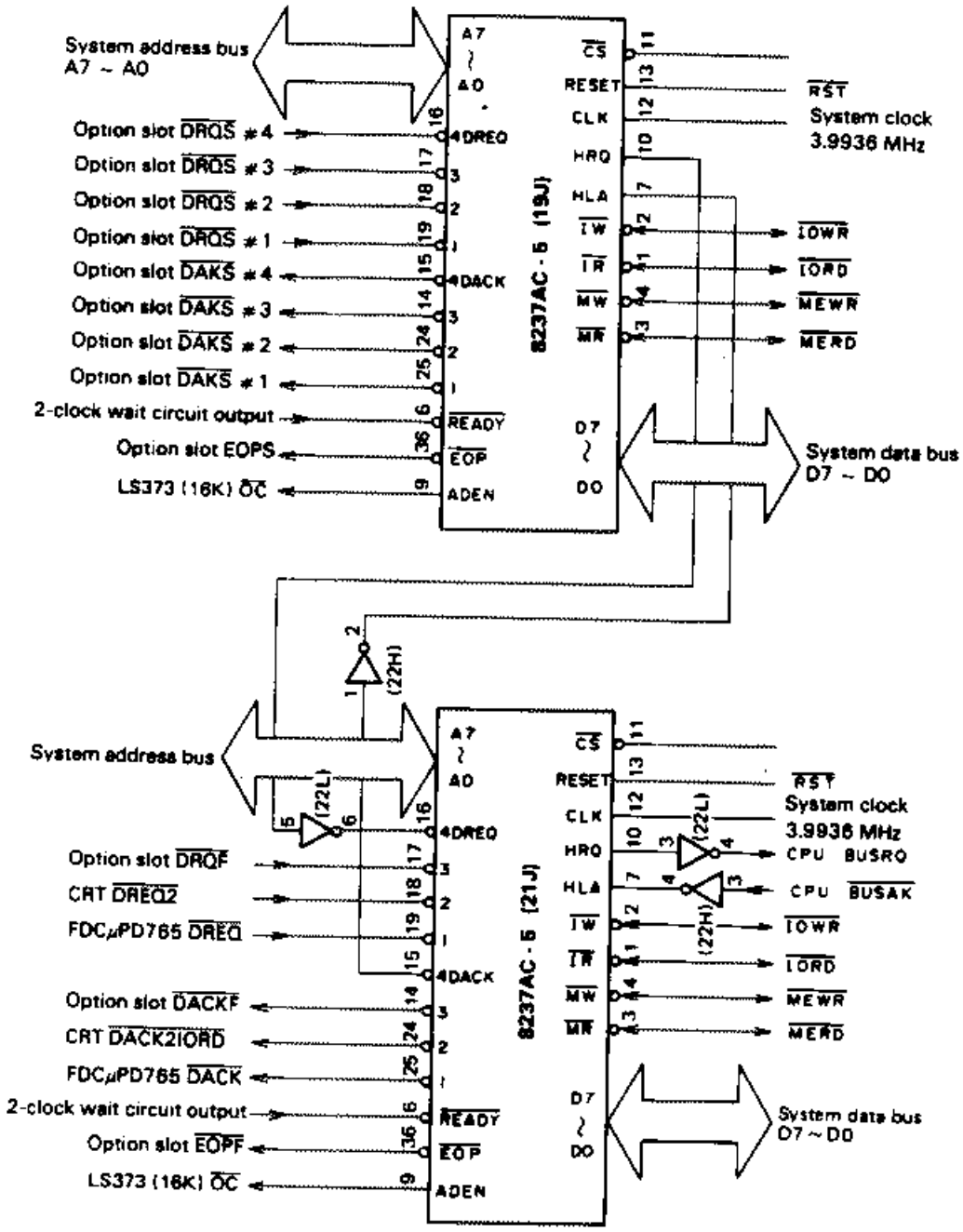
(3) Difference between $\overline{DRQ(F)}$ and $\overline{DRQ(S)}$

There are also two types of DMA request signals for each option connector, $\overline{DRQ(F)}$ and $\overline{DRQ(S)}$. $\overline{DRQ(F)}$ is common to all of the connectors, while $\overline{DRQ(S)}$ is assigned individually. However, $\overline{DRQ(S)}$ and $\overline{DAK(S)}$ are not connected to option connector 5.
Also, $\overline{RDY(F)}$ and $\overline{EOP(F)}$ corresponding to $\overline{DRQ(F)}$ and $\overline{DRQ(S)}$ are common to all of the connectors, as are $\overline{RDY(S)}$ and $\overline{EOP(S)}$.
This is because all the $\overline{DRQ(S)}$ signals use the same DMA controller. Finally, $\overline{DAK(S)}$ is individually assigned to all of the connectors in the same manner as $\overline{DRQ(S)}$.
These relationships are shown in the figure below.



Channel		Connection	
Master	1	Floppy disk	High
	2	Monitor	
	3	Option slots (One of OP # 1 through OP # 5)	
			Priority
Slave	1	Option slots (OP # 1)	
	2	Option slots (OP # 2)	
	3	Option slots (OP # 3)	
	4	Option slots (OP # 4)	Low

DMA request level



DMA.controller μPD8237

(4) Difference between $\overline{\text{BSAK}}$ and $\overline{\text{DAK}}$

Both of these signals are active during DMA operation, but whereas $\overline{\text{BSAK}}$ is active during all DMA operations (i.e., the signal is output even when the CPU is stopped), $\overline{\text{DAK}}$($\overline{\text{DAK(F)}}$ or $\overline{\text{DAK(S)}}$) becomes active only when the corresponding $\overline{\text{DRQ}}$ is accepted and that DMA is operating. For this reason, it is recommended that these two signal types be used as follows.

a. $\overline{\text{BSAK}}$ should be ANDed upon I/O port address decoding and the I/O port non-selected when it is LOW. (This is because the address bus contains a memory address when $\overline{\text{BSAK}}$ is LOW.)

b. Use $\overline{\text{DAK}}$ for chip selection of the I/O port outputting the corresponding $\overline{\text{DRQ}}$.

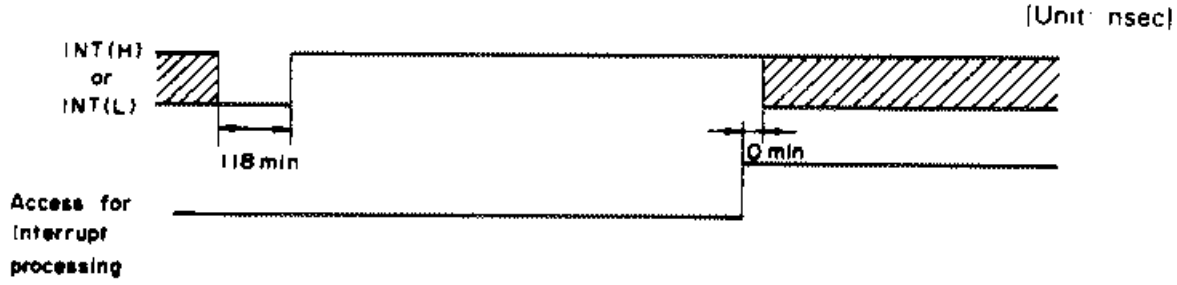
It is particularly important that $\overline{\text{BSAK}}$ is used as described, since incorrect operation will result (regardless of whether the DMA is used) if this processing is not performed.

(5) External memory select

$\overline{\text{MEMX}}$ is required when the option card includes memory. This signal becomes LOW when bit 3 in the memory bank register is 1 and neither P-ROM, C-MOS RAM, nor the common area are selected. Thus, programming considerations are necessary when external memory (on the option card) is to be used. In other words, when external memory is to be selected, bit 3 in the memory bank register must be set to 1 and bits 7 - 4 (the internal memory bank) must be set to 0 so that memory on the main board is not selected. Note must also be taken of the fact that the resident RAM area cannot be placed on external memory.

(6) Interrupt processing

Interrupts from the option slots are controlled by the INT(H) or INT(L) signals. An 8259A is used as the interrupt controller in the main system, and the INT signals are connected directly to the IR terminal of this 8259A. When the INT signal goes from LOW to HIGH, it must be kept HIGH from its rising edge until the $\overline{\text{INTA}}$ from the CPU has been accepted by the 8259A; however, since the $\overline{\text{INTA}}$ signal is not output to the option connector, the INT signal must also be kept HIGH until interrupt processing is started for that device. Finally, since a rising edge is necessary, be sure to observe the rules concerning the duration of the LOW level for the INT signal. These considerations are outlined in the figure below.

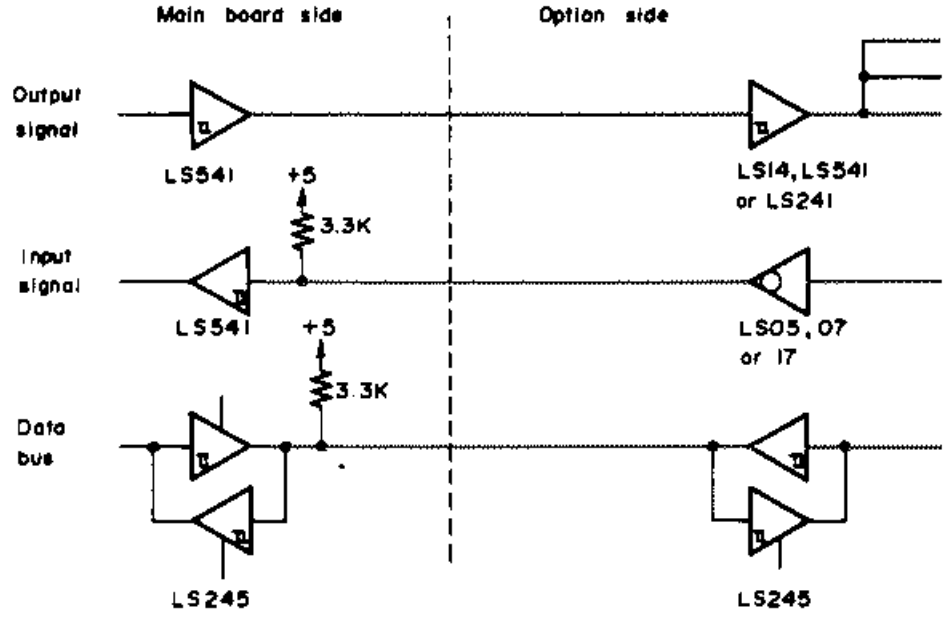


(7) Notes concerning inclusion of options in the OS

When option cards are prepared, some additional circuit must be provided to make it possible for the OS to determine whether previously reserved options are present, and to allow it to automatically control interrupt tables and so forth. The OS must use the following sequence to determine whether the various options are connected to the option connectors.
First, data is output to the ports designated for each option (with a different port for each option); depending on the option, the content of the data may also be designated. If the applicable option is connected, an interrupt is generated, causing INT(H) or INT(L) to go HIGH. In the case of an INT(L) interrupt, the main system is able to determine the slot to which the card is connected from the interruption address, which differs according to slot number. If the option card is not connected, the OS recognizes the fact because no interrupt is generated.
Therefore, a circuit must be provided so that an interrupt is applied when data is written into one of the port addresses assigned to options controlled by the OS, and to clear the interrupt when that same port is read out.

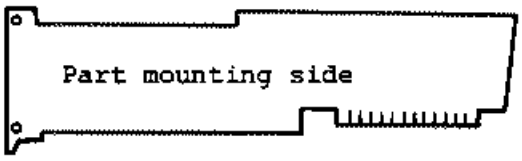
(8) I/O signal interface

All input signals fed to the main board from the option side are pulled up by 3.3K ohm resistors. These signals (other than bidirectional data bus signals) are received by the 74LS541, and therefore should be controlled by an open collector circuit. The 74LS541 is also used for driving output signals (other than data bus signals) which are fed to the option side from the main board.
The option side should be provided with a one-stage buffer for connection of multiple options.
I/O switching for the data bus must be controlled by the 74LS245 bidirectional bus buffer on the main board, as well as on the option side. This is to prevent data conflicts.
Signal lines which are not used must be left open.
The recommended I/O interface circuit is shown below:

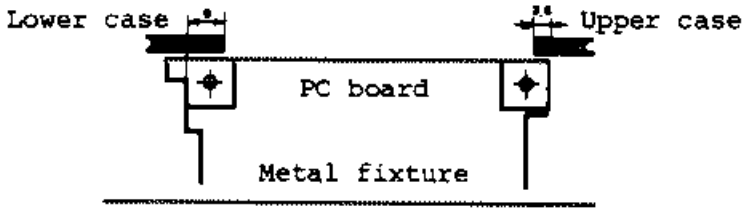


2.8. Mounting of parts

° Parts should be mounted only on the part mounting side of PC board (the side at the front when the slot connector is located right below) taking care to set the height of part to within 15 mm from the PC board surface, and not to make contact between the part and PC board surface or between parts.



° All parts, except for the external interface connector, should be mounted inside the PC board contour.
When mounting the external interface connector, refer to the following drawing as the connector position and size are restricted by the case cover.

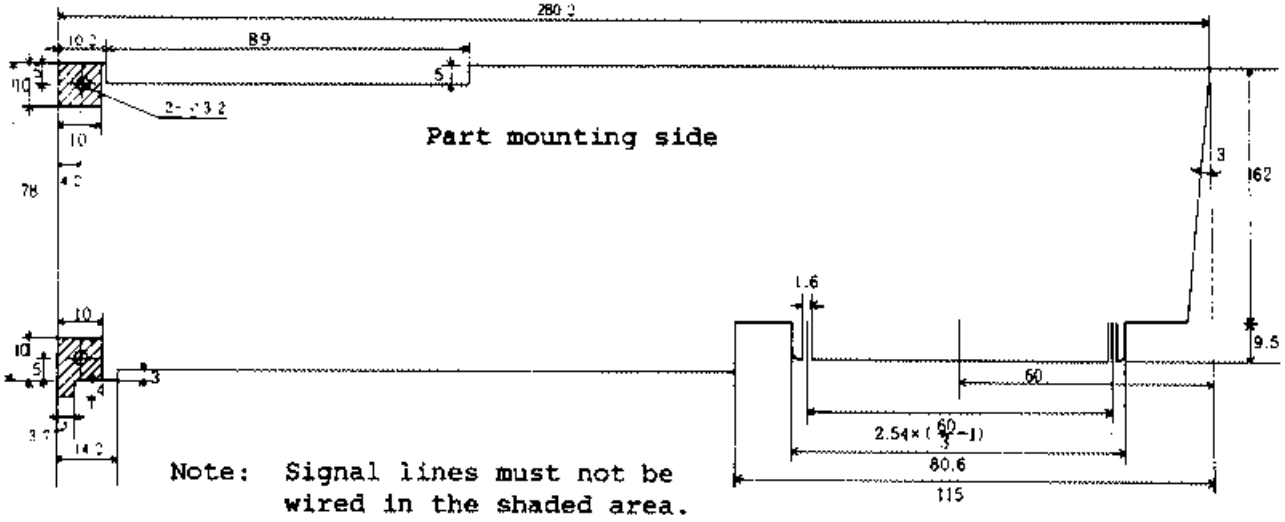


° Wiring should be as short as possible on the PC board, and be fixed as required.

° Lead wires (lead wires of IC resistor, etc.) on the soldered side (rear side of part mounting side) should be 1 - 2 mm high from the PC board surface and arranged so as not to make a shortcircuit with the other lead wires.

2.9. Outer Dimensions of Option Card

Unit: mm



Note: Signal lines must not be wired in the shaded area.