Chapter 16 Extension Units

The capability of the MAPLE can be extended easily by connecting various extension units via the system bus. These extension units are accessible through I/O addresses 80H through 0FFH. (80H through 0DFH are reserved for EPSON-supplied extension units. I/O addresses 0E0H through 0FFH are available for user-supplied extension units.)

This chapter describes the following extension units with focus mainly given on their specifications and functions as viewed from the software standpoint:

1. Nonintelligent RAM disk unit
2. Intelligent RAM disk unit
3. Direct modem unit
4. Multi Unit 64
5. Multi Unit II

The Japanese-language processing unit may also be attached addition to the above units. Details on the Japanese language processing unit are discussed in a separate manual.

16.1 Nonintelligent RAM Disk Unit

The nonintelligent RAM disk unit is classified as two types according to their RAM capacity: 64K- and 128K-byte RAM versions. The nonintelligent RAM disk unit is not available as a stand-alone extension unit but is located on the following extension units:

- Japanese-language processing unit 64 (Model H105A)
  64K RAM disk + Japanese-language processing unit
- Japanese-language processing unit 128 (Model H106A)
  128K RAM disk + Japanese-language processing unit
- Japanese-language processing unit 64 (Model H110A)
  64K RAM disk + Touch-type Japanese-language processing unit
- Japanese-language processing unit 128 (Model H111A)
  128K RAM disk + Touch-type Japanese-language processing unit
- Multi Unit 64 (Model H108A)
  64K RAM disk
  ROM capsule
  Direct modem
- Multi Unit II (Model H115A)
  64K RAM disk

ROM capsule

Synchronous communication unit

RAM file hardware

(1) Memory access method

This unit is allocated in some I/O addresses of the MAPLE main unit. All operations on this unit can be controlled by issuing I/O instructions.

Data in memory can be read from or written into this unit by reading or writing the access port after loading the correct address in the address register.

The address register is automatically incremented as an access is made to memory. However, the highest eight bits of the address register are not incremented because only the lowest eight bits work as a counter. This limits the number of data bytes to 256 that can be transferred to or from RAM in a single read or write operation.

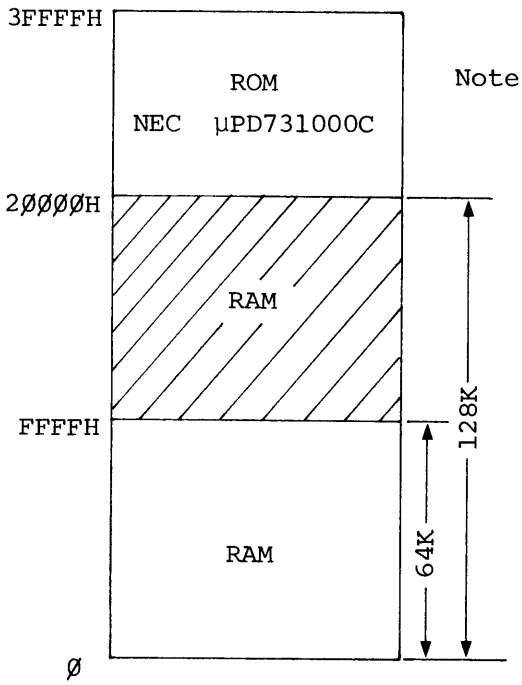
Since the RAM file is closed in the normal state for saving power, an open command (described later) must be executed before an attempt is made to access the file.

(2) Address map

RAM is allocated in memory as illustrated below.

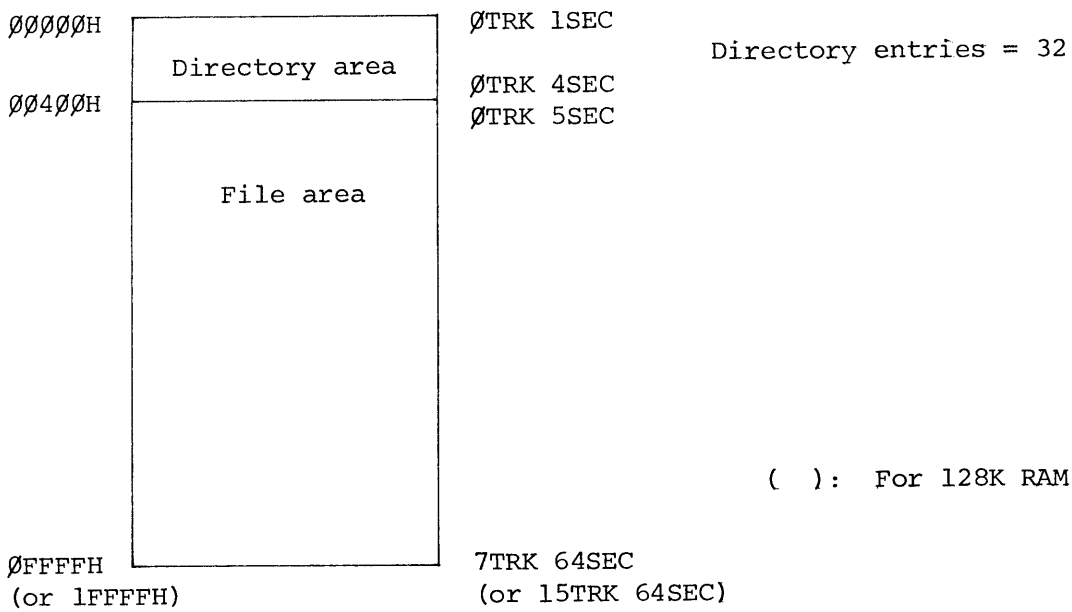
This starting address must be loaded in the address register when accessing the RAM file.

(2) Address map



Note: MPD731000 Chip Select pin must be programmed to low active.

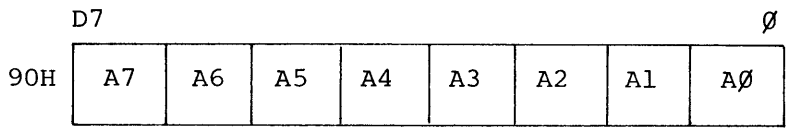
Memory structure



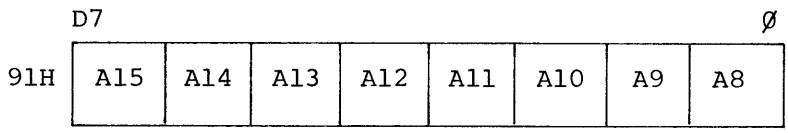
The first 1K bytes of RAM makes up the directory area and the rest is used as the file area. Data (directory and file) is stored in RAM in the same format as it is on FD.

(3) RAM/ROM file register format

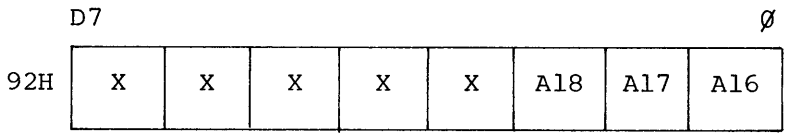
① Address register 1 WRITE ONLY



② Address register 2 WRITE ONLY

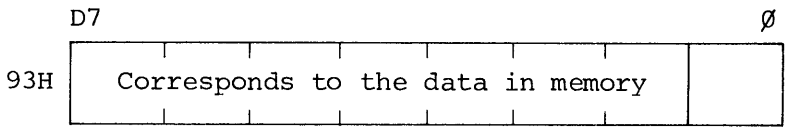


③ Address register 3 WRITE ONLY

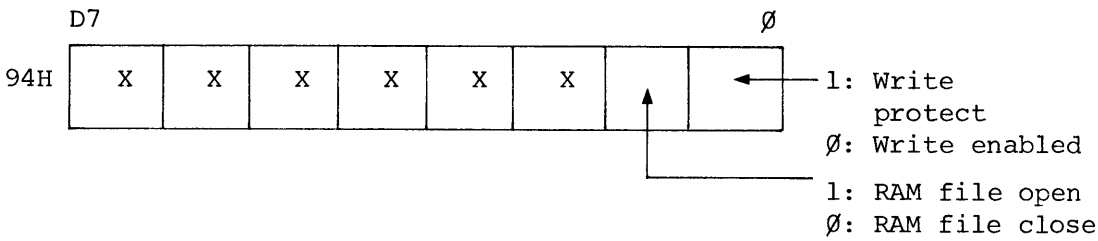


X: No care

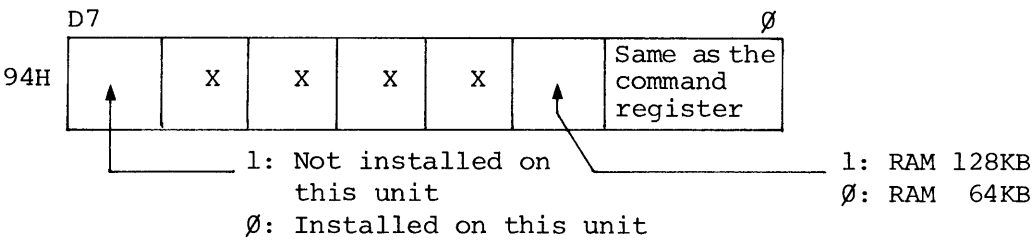
④ Access port WRITE/READ



⑤ Command register WRITE

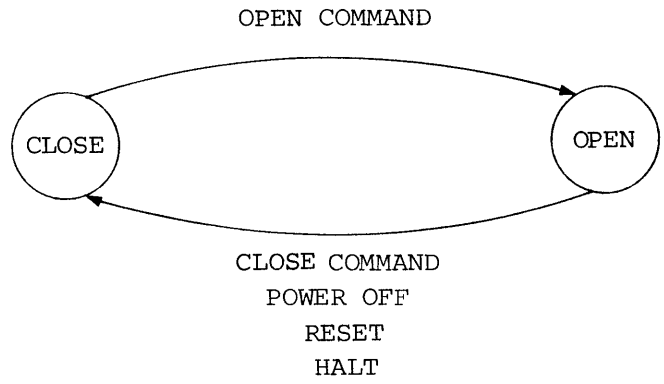


⑥ Status register READ



(4) Opening/closing a RAM file

It is recommended that the RAM file be opened only when accessed to save electric power. The state transitions for file opening and closing processing is shown below.



As illustrated above, an OPEN command must be executed before accessing the RAM file. RAM is self-refreshing when the file is closed and so must not be accessed in the closed state. The address register does not increment while the file is closed.

The file may be destroyed if RESET is made active while it is in the open state.

Note: No OPEN command is required when accessing the file ROM.

(5) Write protect

Write protect is enabled (write protected) after a power on or reset. In the write protect mode, RAM is disabled for write and can only be read. The address register does not increment in this mode.

16.2 Intelligent RAM Disk Unit

The MAPLE can control writes and reads to and from the intelligent RAM disk simply by sending commands as is the case with the FDD. The RAM disk capacity is 60K or 120K bytes.

(Although an intelligent RAM disk unit contains 64K- or 128K-byte RAM, 4K or 8K bytes are reserved for the unit program; that is, the user can actually use 60K or 120K bytes of RAM, respectively.)

The following options are available:

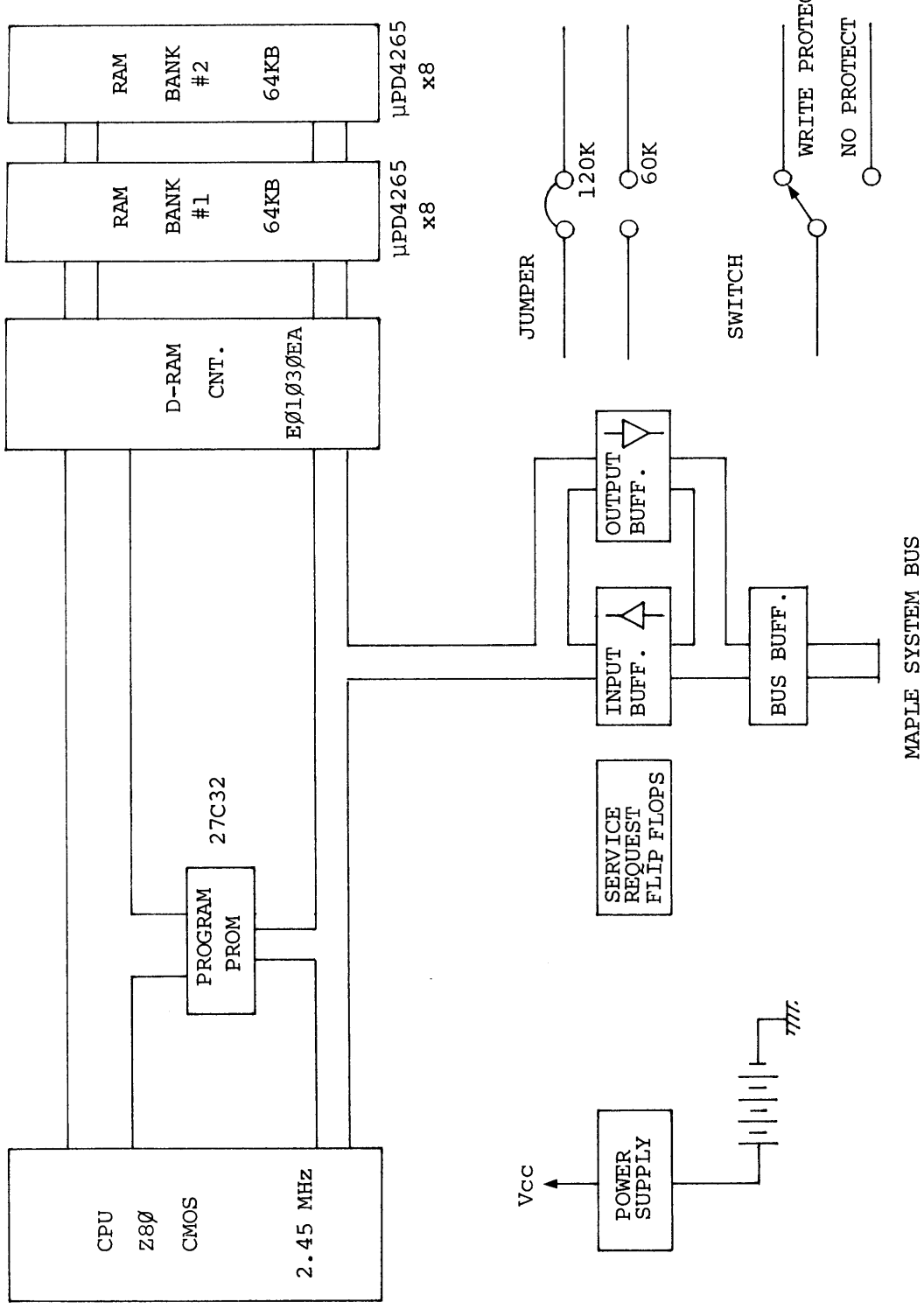
- RAM DISK UNIT 60 (Model H102A)

  60K-byte RAM disk

-RAM DISK UNIT 120 (Model H103A)

  120K-byte RAM disk

(1) Block diagram



- Jumpers

The RAM disk unit has two jumper pins on its main board. The firmware determines the memory capacity by checking the state of these pins.

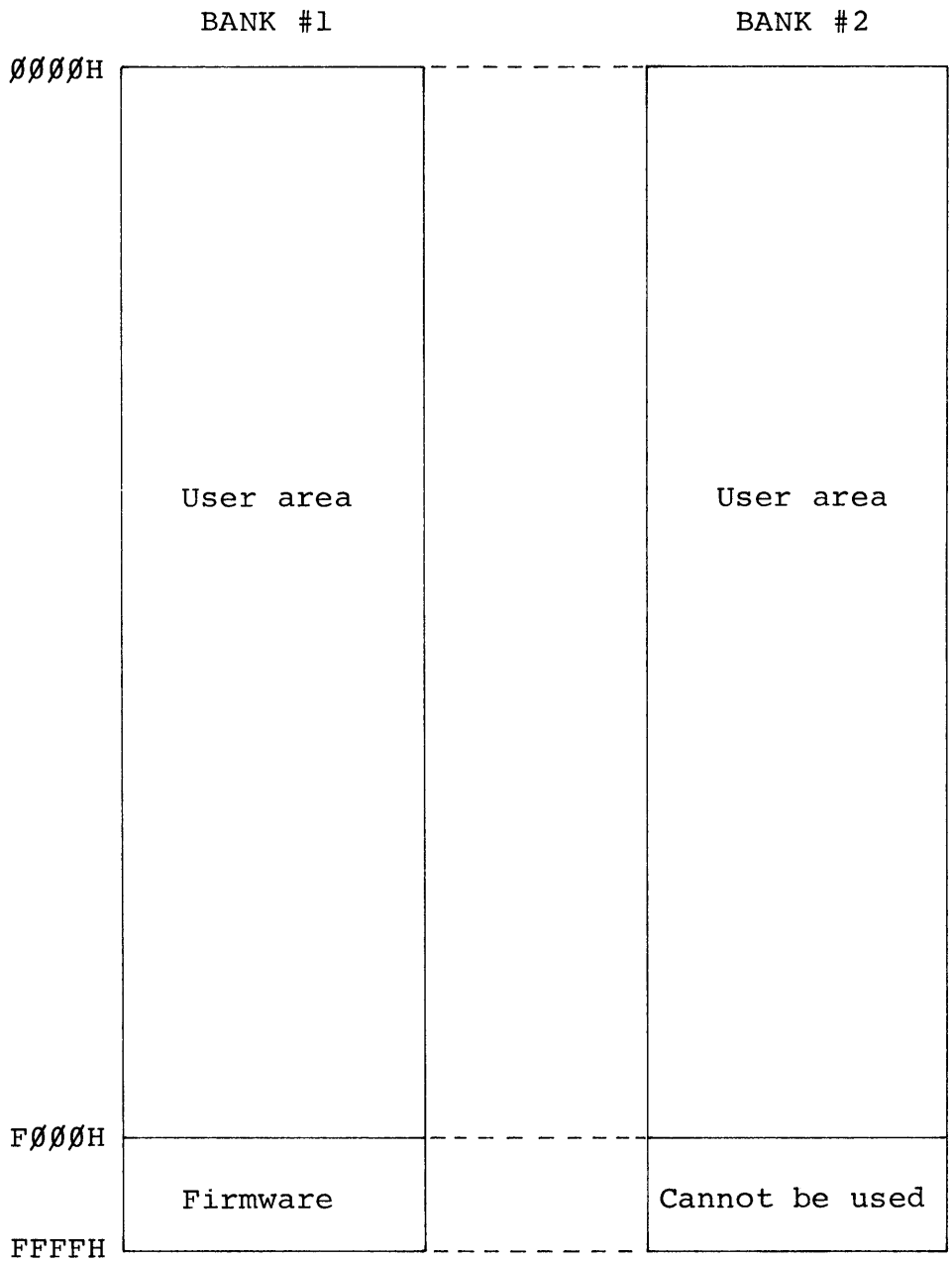
The jumper pins are labeled 60K and 120K with silk printing, respectively. Install the jumper for 60K when eight RAM chips are used and for 120K when 16 RAM chips are used.

- Switch

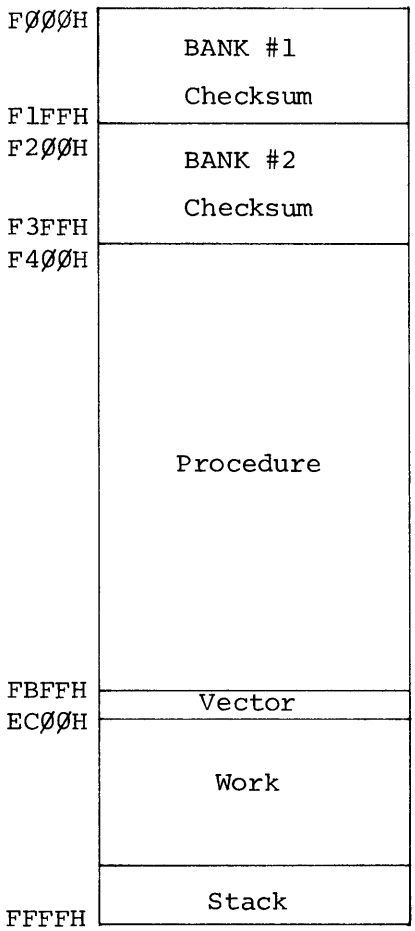
The RAM disk unit has a switch on its main board. This switch can be controlled externally and used as a write protect switch. When the switch is set to on, RAM is disabled for write and enabled only for read.

(2) Memory map

1. Memory map



3. Firmware memory map



Disk format

The RAM disk unit is formatted as shown below.

Track Ø	Sector Ø		BANK #1			Sector 3F
1	Ø			#1		3F
2	Ø			#1		3F
3	Ø			#1		3F
4	Ø			#1		3F
5	Ø			#1		3F
6	Ø			#1		3F
7	Ø	#1	1F	2Ø	#2	3F
8	Ø		BANK #2			3F
9	Ø			#2		3F
A	Ø			#2		3F
B	Ø			#2		3F
C	Ø			#2		3F
D	Ø			#2		3F
E	Ø			#2		3F

Up to track 7, sector 1FH can be addressed for 64K RAM disk.

(3) I/O map as viewed from the MAPLE

The MAPLE communicates with the RAM disk unit through two I/O addresses 80H and 81H. The MAPLE functions for communicating with RAM disk units are listed below.

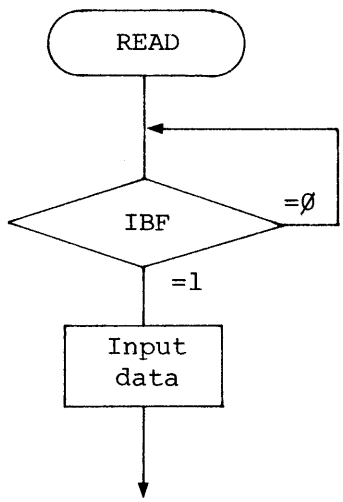
Address	Read/ write	MAPLE operation
80H	R	Read data status
	W	Write data
81H	R	Read handshake information
	W	Write command

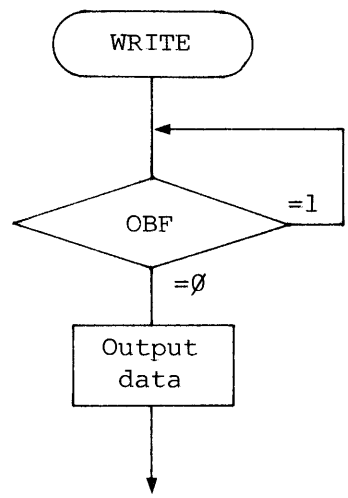
The MAPLE can check whether a RAM disk unit is installed by reading I/O address 81H. Its highest two bits are set to 00 when a RAM disk unit is installed.

(4) Communication with the RAM disk unit

1. Communication sequence

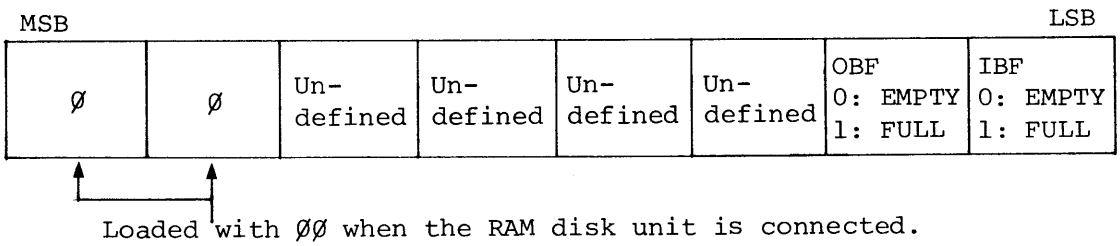
The MAPLE must always check the IBF and OBF bits (handshake information) when communicating with a RAM disk unit.





2. Handshake information

Handshake information (81H)



Note: The application program must always check the handshake information when sending or receiving a command, data, or status to or from the RAM disk unit.

OBF Ø: Command or data transfer from MAPLE is enabled.

1: Command or data transfer from MAPLE is disabled.

IBF Ø: Receive data is present.

1: Receive data is not present.

(5) RAM disk commands

The RAM disk unit processes the following six commands:

- RESET (ØØ) Reset
- READ (Ø1) Read Sector
- READB (Ø2) Read Byte
- WRITE (Ø3) Write Sector
- WRITEB (Ø4) Write Byte
- CKSUM (Ø5) Check Entire Memory

Note 1: The RAM disk ignores commands other than the above as well as invalid data.

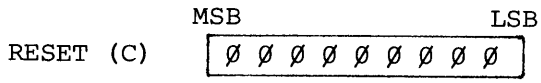
Note 2: If a new command is issued before completion of the current command, the RAM disk starts the protocol sequence of the new command ignoring the old command.

Note 3: When the write protect switch is set to ON, the RAM disk unit returns an error code without changing the RAM contents.

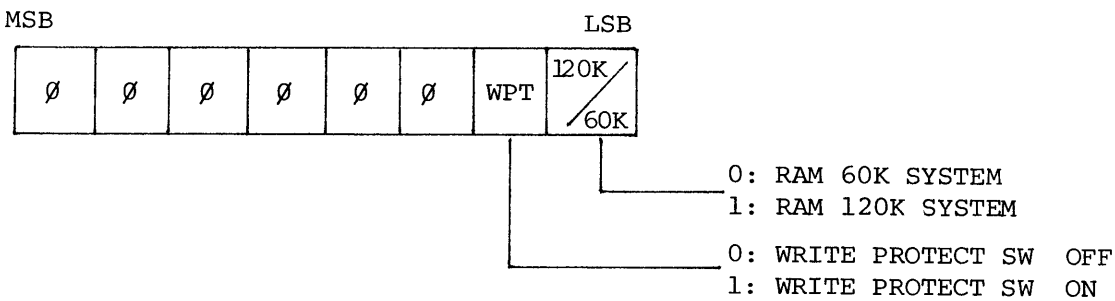
Note 4: The RAM disk contents are preserved even when MAPLE power is turned off.

(5-1) RESET (ØØH)

Resets the RAM disk unit and returns its status.



Subsequently, the following 1-byte status information is returned from the RAM file:



(5-2) READ (Ø1H)

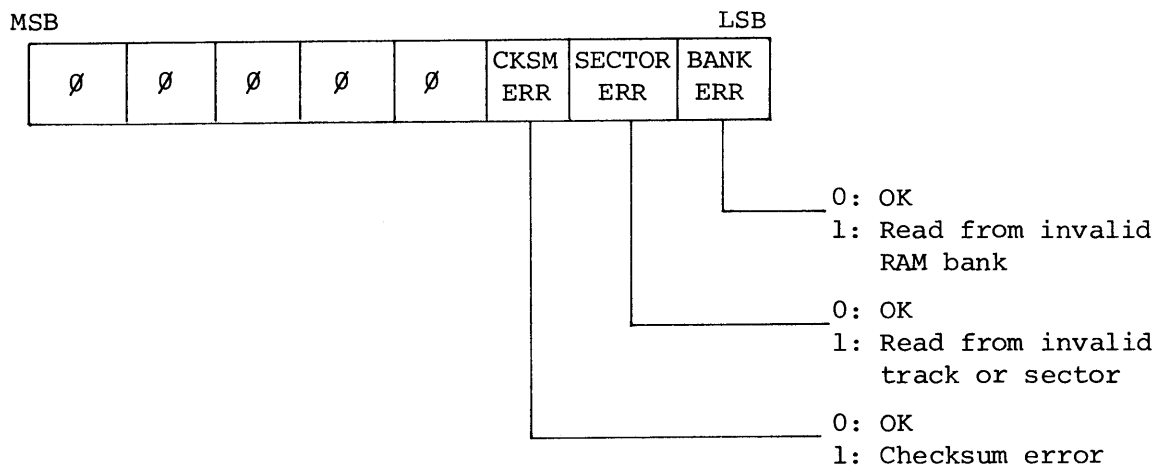
Causes the MAPLE to read a sector from the RAM disk unit.

		MSB							LSB	
READ	(C)	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	
TRACK	(D)									Ø - ØEH
SECTOR	(D)									Ø - 3FH

Subsequently, a 1-byte status information and 128 byte of data are returned from the RAM disk unit in that order.

128-byte data is returned even if the status byte indicates an error condition (in this case, the validity of the data is not guaranteed).

Status information



(5-3) READB (Ø2H)

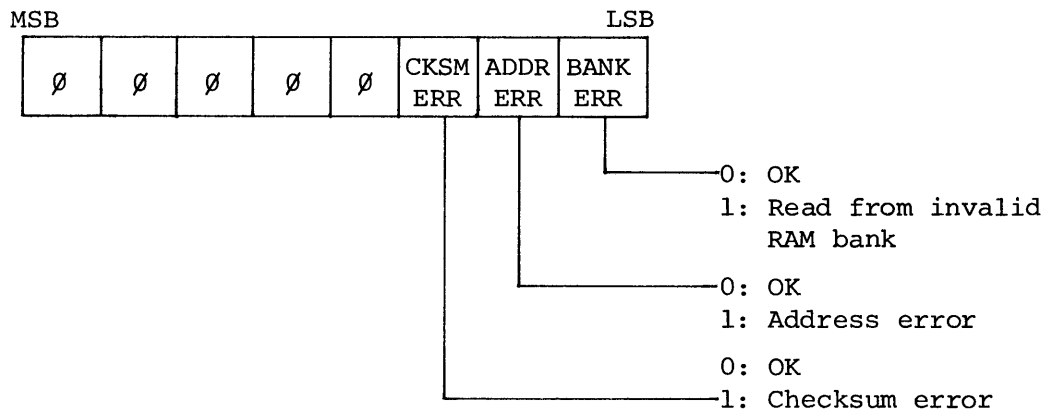
Causes the MAPLE to read a byte from the RAM disk unit.

READB	(C)	Ø Ø Ø Ø Ø Ø 1 Ø	
BANK	(D)		1 or 2 (2 may be specified only when there are two banks.)
ADDRH	(D)		Ø - ØEFH } Address ØFØØØH and higher are invalid.
ADDRL	(D)		Ø - ØFFH }

Subsequently, a 1-byte status information and 1-byte data are returned from the RAM disk unit in that order.

Data is returned even if the status byte indicates an error condition (in this case, the validity of the data is not guaranteed).

Status information



(5-4) WRITE (Ø3H)

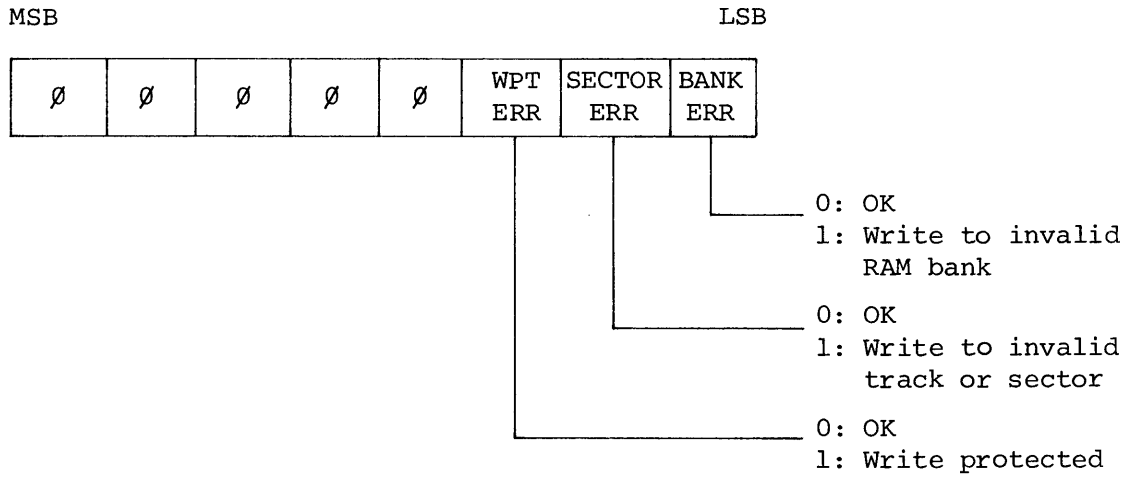
Causes the MAPLE to write data onto a sector in the RAM disk unit.

WRITE	(C)	Ø Ø Ø Ø Ø Ø 1 1	
TRACK	(D)		Ø - ØEH
SECTOR	(D)		Ø - 3FH

Subsequently, 128-byte data is sent to the RAM disk unit. A 1-byte status information is returned from the RAM disk unit after the data is written.

The status byte contains a nonzero value if an error is detected. In this case, the RAM disk unit discards the data.

Status information



(5-5) WRITEB (ØH)

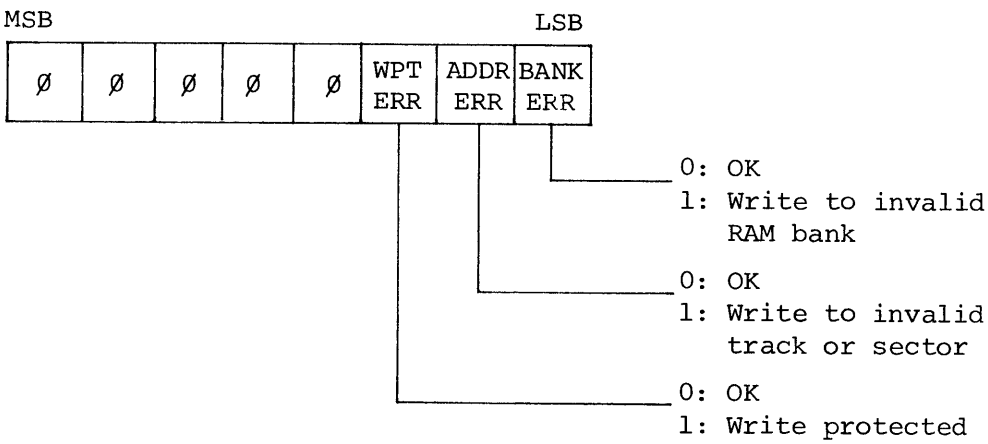
Causes the MAPLE to write a byte onto the RAM disk unit.

WRITEB	(C)	Ø Ø Ø Ø Ø 1 Ø Ø	
BANK	(D)		1 or 2 (2 may be specified only when there are two banks.)
ADDRH	(D)		Ø - ØEFH } Address ØFØØØH and higher
ADDRL	(D)		Ø - ØFFH } are invalid.

Subsequently, 1-byte data is sent to the RAM disk unit. A 1-byte status information is returned from the RAM disk unit after the data is written.

The status byte contains a nonzero value if an error is detected. In this case, the RAM disk unit ignores the byte.

Status information



(5-6) CKSUM (Ø5H)

Causes the MAPLE to perform a checksum test on the entire RAM on the RAM disk unit.

	MSB							LSB
CKSUM (C)	Ø	Ø	Ø	Ø	Ø	1	Ø	1

Subsequently, a 1-byte status information is returned from the RAM disk unit.

Status information

MSB							LSB
Ø	Ø	Ø	Ø	Ø	Ø	BANK2 ERR	BANK1 ERR

BANK1 ERR
0: Normal
1: Checksum error on bank 1

BANK2 ERR
0: Normal
1: Checksum error on bank 2

16.3 Direct Modem Unit

The direct modem is installed in the expansion units shown below. It is available only in the U.S.A.

- Modem Unit

  Consists of a direct modem unit only.

- Multi Unit 64

  Consists of a direct modem unit, 64K RAM disk, and a ROM capsule.

The pages that follow explain the specifications for and functions of the direct modem unit.

1. Outline

The direct modem unit has the following features:

(1) Modem communication function

BELL103 (ORIG/ANS) compatible. Full duplex communication at speeds up to 300 bps is possible using a telephone line.

(2) Can be connected to a telephone line directly or through an acoustic coupler. The standard direct modem unit is provided with a telephone line interface certified by FCC. It is also connectable using an optional acoustical coupler unit.

(3) Communication function

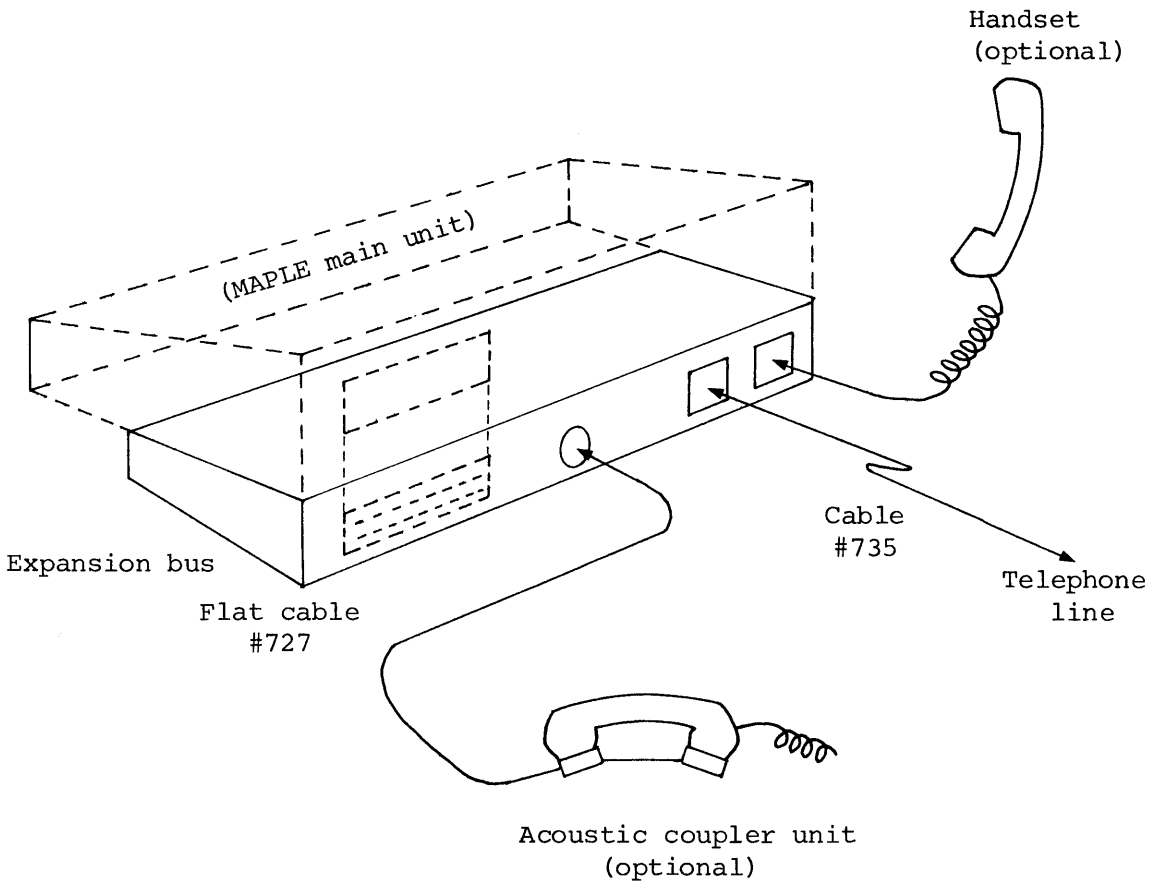
Audio communication using the optional handset is possible.

(4) Monitoring function

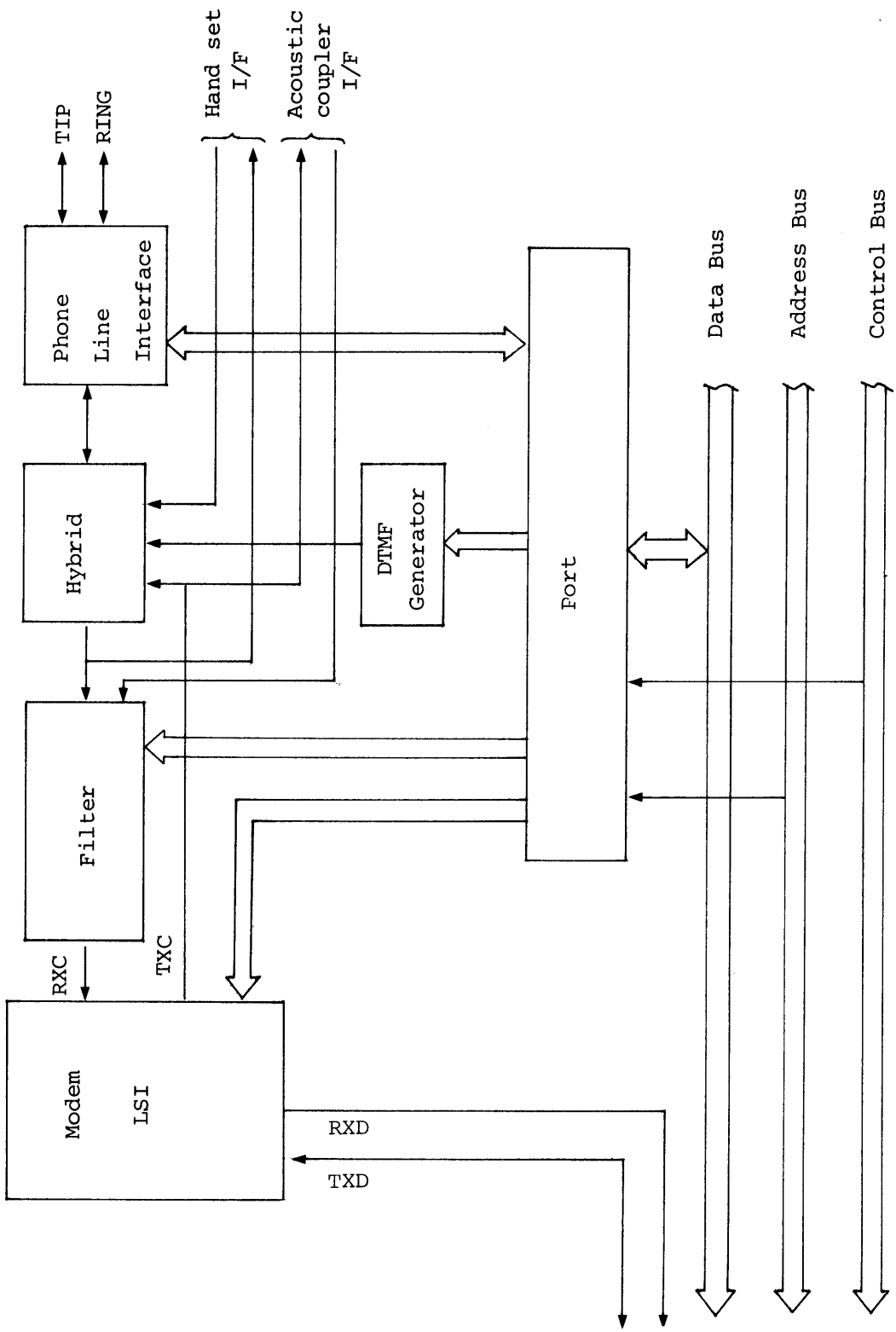
The line status can be monitored through the speaker in the MAPLE main unit.

(5) Automatic dialing and answering

Both pulse or tone dialing are possible. Automatic answering is possible using a telephone ring detection circuit.



< MAPLE rear panel >



< Block diagram >

2. Basic hardware specifications

2.1 Modem

Compatibility --------- BELL103

Originate or answer mode

Data rate ------------- 0 - 300 bps

Modulation ------------ FSK

Handset sensitivity -- -8 - -43 dBm

Transmitter output level

--- B -12±3 dBm

Carrier frequencies

Mode		Mark	Space
Originate	Transmission	1270 Hz	1070 Hz
	Receive	2225 Hz	2025 Hz
Answer	Transmission	2225 Hz	2025 Hz
	Receive	1270 Hz	1070 Hz

2.2 Telephone line interface

(1) FCC Part 68 certification No.: BKM9A8-12717-DT-E

(2) Ringer equivalence: 0.5B

(3) Connector: RJ11C, RJ11W

(4) Impedance

On-hook, DC: 20M ohms or more (across TIP and RING electrodes and ground, 200VDC bipolar)

On-hook, AC: 20K ohms or less across TIP and RING electrodes.

Off-hook, DC: 200 ohms ± 20 % across TIP and RING electrodes.

Off-hook, AC: 600 ohms ± 20 % across TIP and RING electrodes.
(when measured at least two seconds after off-hook.)

(5) Insulation:

1000 volts r.m.s across TIP and RING and the other electrodes.

(6) Surges:

Must withstand surges with a peak voltage of 1500V, a rise time shorter than 10 μsec and a fall time shorter than 160 μsec. Surge voltage is measured between TIP and RING and between these terminals and ground.

(7) Ring detection

Detection frequency:	16 to 68 Hz
Voltage:	40 to 150 volts r.m.s

2.3 Acoustic coupler

The MAPLE can serve as an acoustic coupler when furnished with an optional acoustic coupler unit.

Sound output: +5 dB max. ($1N/m^2$ = 0 dB)

2.4 Power consumption

	Typ.	Max.
1) MAPLE power off time	3 μA	10 μA
2) MAPLE power on time (when no modem is used)	0.4 mA	1 mA
3) Modem power on (line not connected w/t coupler)	50 mA	60 mA
4) Modem power on (line connected)	65 mA	80 mA

3.1 Telephone line interface

Certified by FCC Part 68.

This interface can be connected to a RJ11C or RJ11W type modular jack via the attached modular cable.

3.2 Handset interface

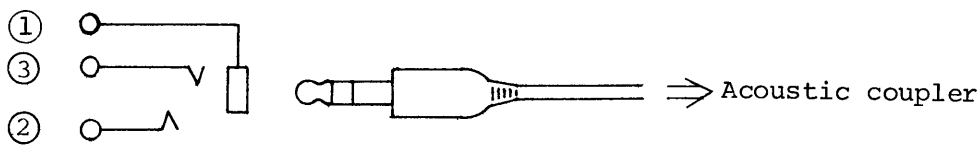
The MAPLE can be used as a telephone when equipped with an optional handset unit.

The handset interface can be enabled or disabled by the MAPLE controlling a dedicated output port. The connector is of modular jack type which is commonly used in U.S.A. for receivers. Electrically, however, the MAPLE is designed for connection to an EPSON-supplied receiver unit.

3.3 Acoustic coupler interface

This interface connects the optional acoustic coupler unit to the MAPLE.

Connector to be used: HSJ0863-01-440 (HOSHIDEN)



① : GND
② : ACMI (microphone)
③ : ACSP (speaker)

4. I/O Ports

4.1 Outline

The H107A is controlled directly by the MAPLE main CPU via I/O ports.

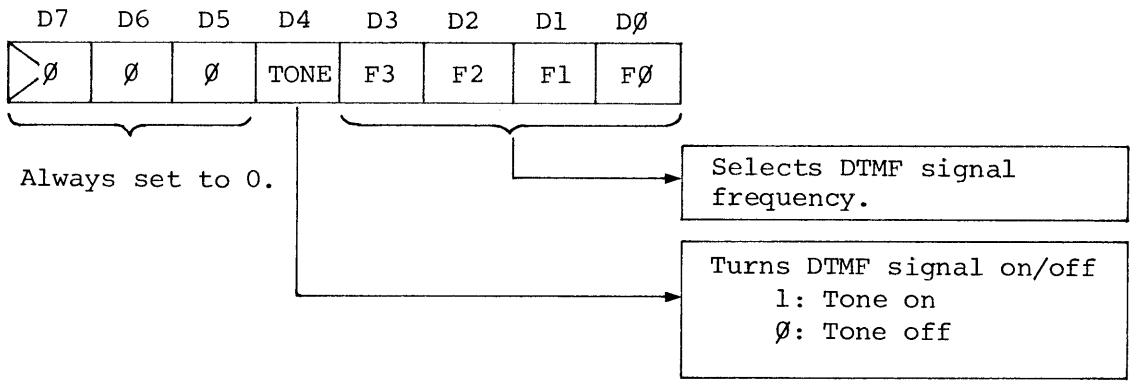
The H107A is assigned the following I/O ports:

Address	Input port	Output port
84H	Inhibited	Tone dialer control
85H	Inhibited	Model control
86H	Modem status	Inhibited
87H	Inhibited	Port mode

4.2 Address 84H

I/O: Output only

Use: For tone dialer control



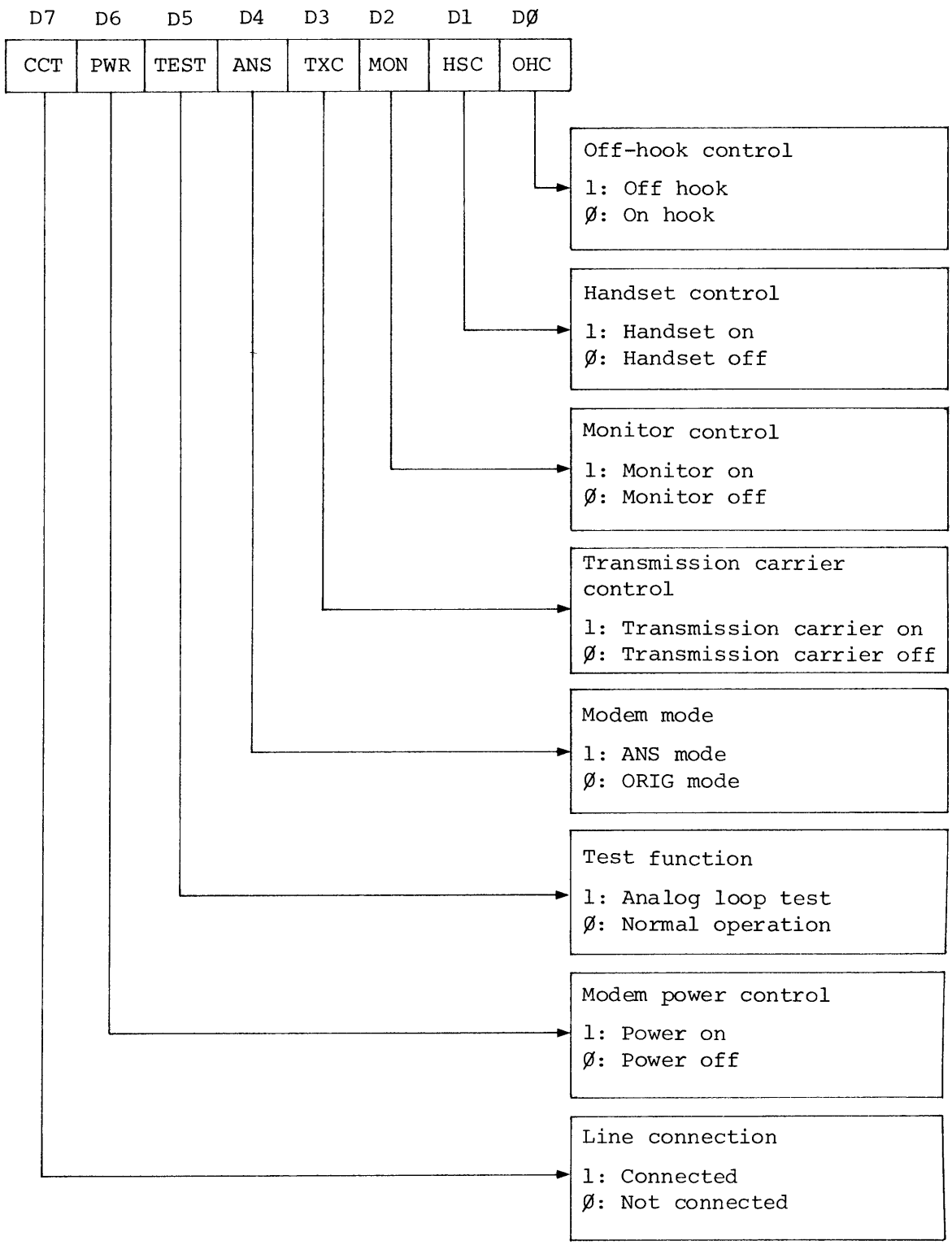
ØØØØ**** = Tone off

ØØØ1$F_3F_2F_1F_Ø$ = Tone on with the frequency specified by FØ through F3.

4.3 Address 85H

I/O: Output only

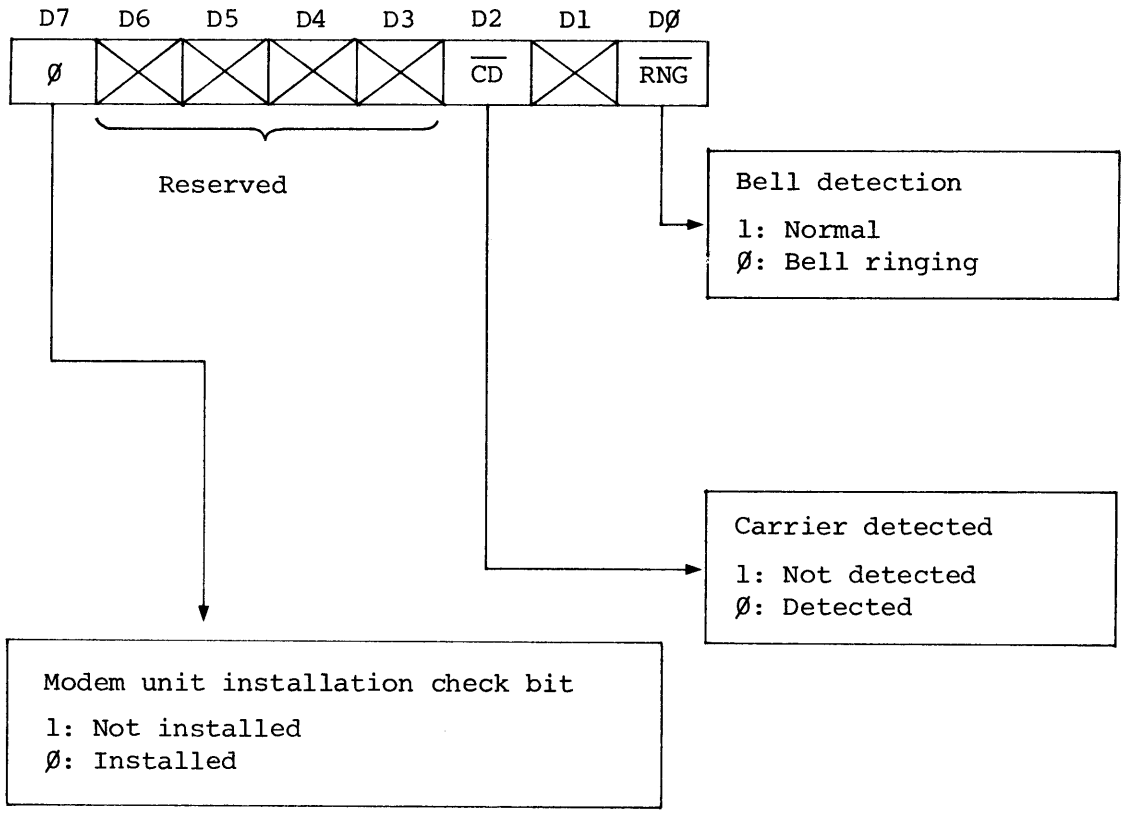
Use: For modem control



4.4 Address 86H

I/O: Input only

Use: For modem status read



Note: All bits are Ø when modem power is off. Read the status at least 1ØØ ms after power is turned on.

4.5 Address 87H

I/O: Output only

Use: <Input> Inhibited

<Output> For port (8255 mode) setting

Note: When the auto shut-off function of the MAPLE main unit is activated, power to logic electronics is turned off and all modem unit functions are stopped. Consequently, the mode setting procedure described below must also be performed when recovering the MAPLE from the shut-off state. Generally, the auto shut-off function should be disabled while the modem unit is in operation.

<Output>

Sets up the 8255 operating mode. The following data must be output to this port after the MAPLE is powered or reset:

Data to be output: 89H

Example:

```
    .
    .
  LD    A, 89H
  OUT   (87H), A
    .
```

- 8255 setup -

Port A = output

Port B = output

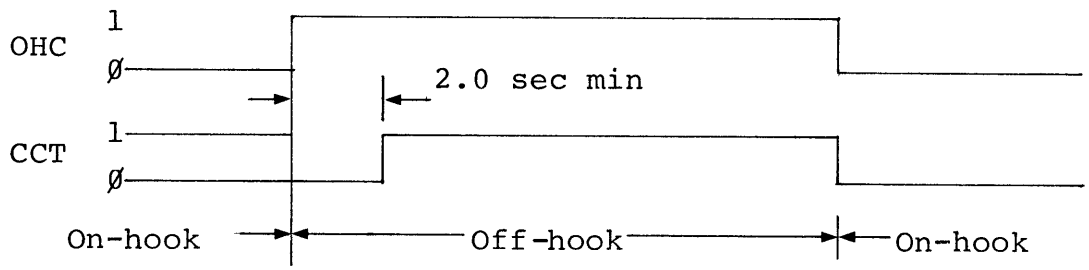
Port C = input

Mode = Ø

5. Operating Specifications

5.1 Connection to a communication line

The direct modem enters the off-hook state the OHC (Off-Hook Control) bit is set to 1. At least a 2-second delay is required between the off-hook state and the time when the connection to the line is established. Set the OHC bit to 1 and wait for two or more seconds before setting the CCT bit (Coupler Cut Through) to 1.



5.2 Modem operation

(i) Selecting ORIG or ANS mode

The mode is controlled by the ANS bit of the output port (85H).

Ø = ORIG mode

1 = ANS mode

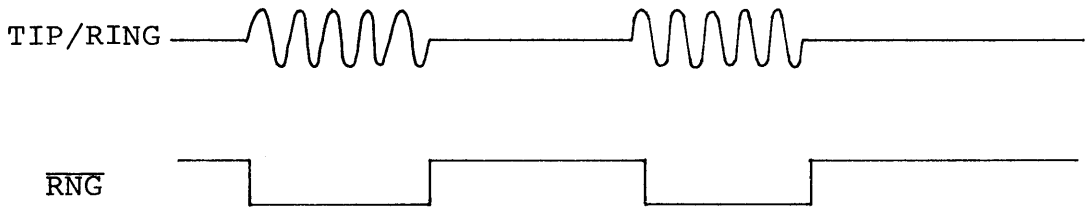
(ii) Transmission

The carrier is turned on or off in accordance with the 1/Ø state of the TxC bit of the modem control port (85H). When the TxC bit is 1, the carrier is present all the time in the ANS mode and generated only when the counterpart carrier is being received in the ORIG mode.

5.3 Receiving a call

The direct modem unit generates outputs a *RNG signal when it detects a ringing bell. The *RNG signal can be read through the input port (86H) as a modem status flag. *RNG is a level signal and held low while the bell is ringing.

—— Timing ——



5.4 Dial operation

(a) Pulse dialing

Pulse dialing is made possible by controlling the OHC bit of the modem control port.

(1) Procedure

<Step>	<Action>
1	Set OHC to 1.
2	Wait for at least two seconds.
3	Supply dial pulses to the OHC.
4	Set CCT to 1 with at least two-second delay after the last pulse.
5	Set OHC and CCT to Ø to disconnect the line.

6 To dial again, return to step 1 after holding OHC low for longer than 3.5 seconds.

(2) Dial pulses

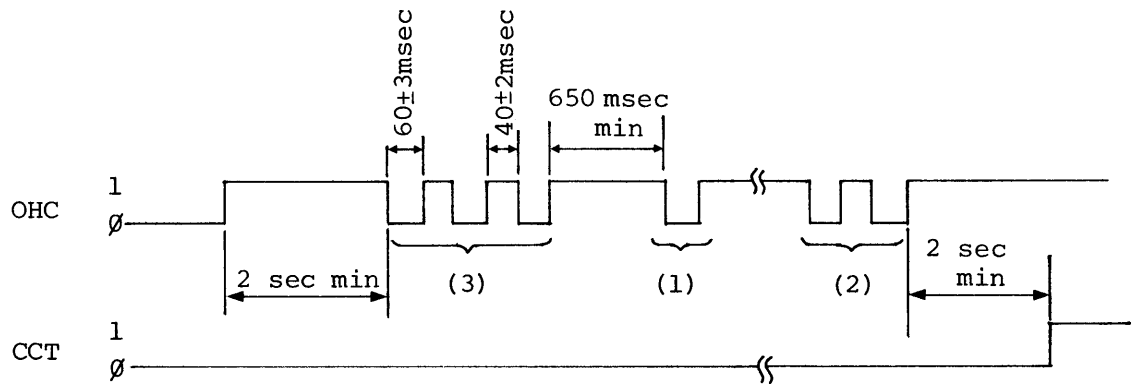
- One pulse consists of 60 ± 3 msec on-hook and 40 ± 2 msec off-hook states.
- Correspondence between digits and number of pulses are as follows:

Digit	Number of pulses
1 - 9	1 - 9
0	10

- Digit interval

  650 msec. min. and 3 sec. max

(3) Timing



(b) Tone dialing

Dialing using the DTMF signal is enabled by controlling the output port (84H).

(1) Procedure

The same as pulse dialing except step 3. Set CCT to 1 and use the output port (84H) instead of controlling CHC.

(2) Data to the output port (84H)

The correspondence between the digits and bits FØ through F3 is listed below.

	F3	F2	F1	FØ
1	Ø	Ø	Ø	Ø
2	Ø	Ø	Ø	1
3	Ø	Ø	1	Ø
4	Ø	1	Ø	Ø
5	Ø	1	Ø	1
6	Ø	1	1	Ø
7	1	Ø	Ø	Ø
8	1	Ø	Ø	1
9	1	Ø	1	Ø
Ø	1	1	Ø	1
*	1	1	Ø	Ø
#	1	1	1	Ø
A	Ø	Ø	1	1
B	Ø	1	1	1
C	1	Ø	1	1
D	1	1	1	1

} Usually not used.

FØ through F3 determine the tone frequency. Whether dial tone is to be turned on or off is controlled by the tone bit.

(3) Frequency

The table below lists the frequency of the tones derived from the clock (3.579545 MHz). (Deviation limit is ±1.5%.)

	Standard DTMF in Hz	Tone output in Hz	Deviation from standard (%)
f1	697	7Ø1.3	+Ø.62
f2	77Ø	771.4	+Ø.19
f3	852	857.2	+Ø.61
f4	941	935.1	-Ø.63
f5	12Ø9	1215.9	+Ø.57
f6	1336	1331.7	-Ø.32
f7	1477	1471.9	-Ø.35
f8	1633	1645.Ø	+Ø.73

(4) Level

- Nominal level per tone: -6 to -4 dBm
- Minimum level: Low frequency group: -1Ø dBm
  High frequency group: -8 dBm
- Maximum level: Low frequency group + High frequency group = ØdBm
- Level difference between low and high frequency group tones:

  ØdB <= (High frequency group) - (Low frequency group) <= 4dB

(5) Timing

- Tone duration: 50 msec. min.
- Tone interval: 45 msec. min. to 3 sec. max.
- Cycle: 100 msec. min.

The procedure and timing are controlled by a system program.

(6) Correspondence between digits and output frequencies

High frequency group (Hz) / Low frequency group (Hz)	1209	1336	1477
697	1	2	3
770	4	5	6
852	7	8	9
941	*	0	#

16.4 Multi-Unit 64

The Multi-Unit 64 (Model H108A) contains the following units (the unit is available only in U.S.A.):

- 64K RAM disk (described in 16.1)
- Direct modem (described in 16.3)
- ROM capsule

This section describes the specifications and functions of the ROM capsule incorporated in the Multi-Unit 64.

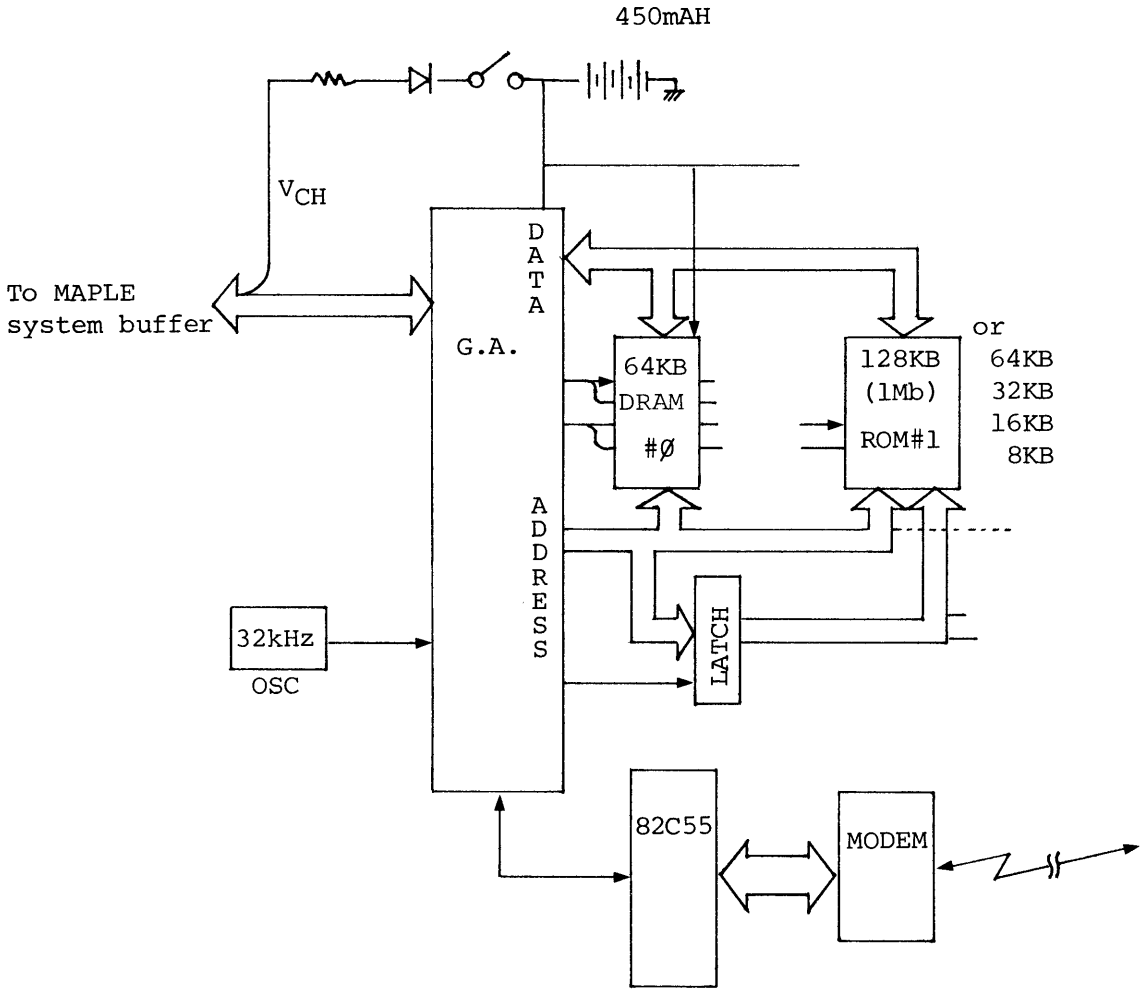
The basic specifications for the ROM capsule are identical to those for the ROM capsule installed in the main unit. Consequently, the ROM used for the main unit may also be used on the Multi Unit 64 simply by switching the ROM select jumpers.

The major differences from the ROM capsule in the main unit are as follows:

- Either 512K-bit (64K-byte) or 1M-bit (128K-byte) ROM may be used.
- Non-CMOS type ROM cannot be used.

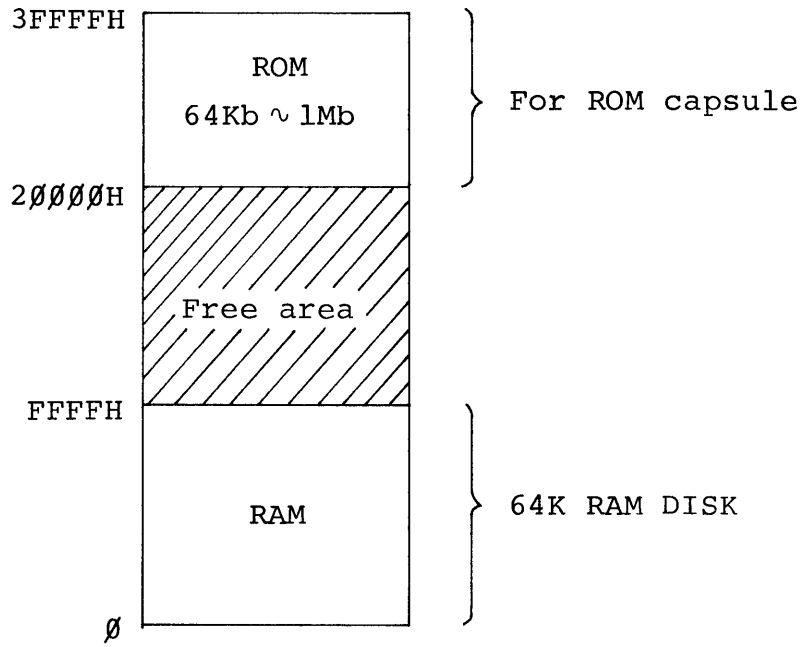
See Section 15.2 for the file structure in ROM.

(1) Block diagram



(2) Address map

The ROM capsule is allocated in RAM as shown below. Load the starting address of ROM in the address register.



(3) ROM file

1) The ROM file block can be accessed in the same way as the RAM file block. Each ROM socket has 28 pins, so not only 1M-byte ROM devices but also 64K-, 128K-, 256K, and 512K-byte CMOS mask EPROM devices may be used.

Switch settings must be changed as follows according to the type of ROM devices used:

ROM	SW2	SW3
64Kb	K	B
128Kb	K	B
256Kb	K	B
512Kb	1M	B
1Mb	1M *	A *

*: Settings as shipped from factory

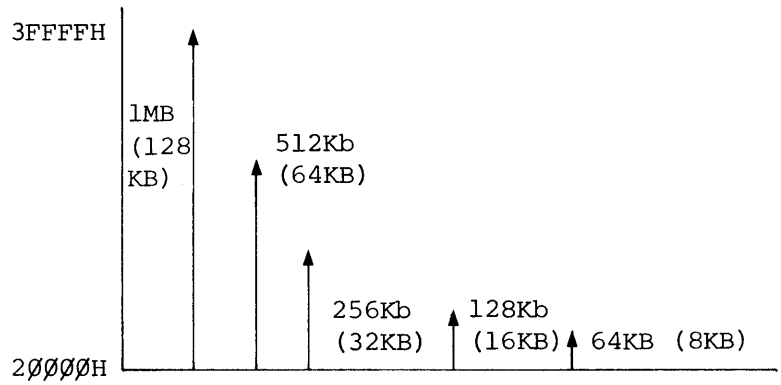
Note: 512K-byte ROM is not released at present.

2) NMOS ROM cannot be used because power to ROM is supplied from the battery through a switch. Normal operation will not be guaranteed if NMOS is used. NMOS ROM would consume more power and thus decreasing life of the MAPLE battery.

3) The ROM capsule in the MAPLE main unit may be installed on this board. To maintain compatibility, the OS must support the ROM capsule on this board. (Overseas OS versions B and up support this ROM capsule.)

4) Address map

The address relationship for different ROM device types (address to be loaded in the address register) are shown below.

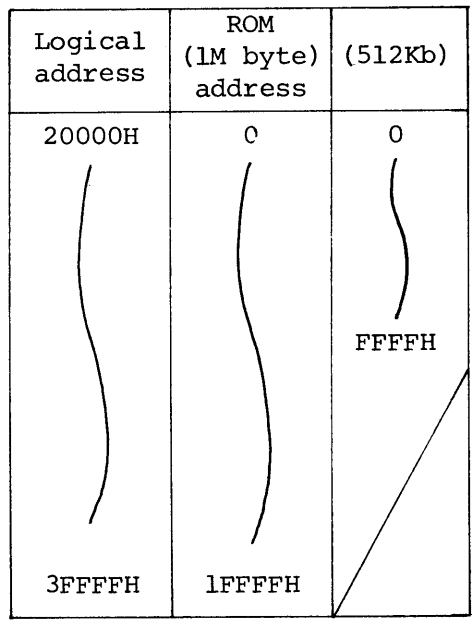


5) Writing data into ROM

Data is written into ROM in the same way as into the ROM capsule in the main unit if ROM devices smaller than 256K bytes are used.

Logical address	ROM address		
	64Kb	128Kb	256Kb
20000H ⌇ 23FFFH 24000 ⌇ 27FFFH	0 ⌇ 1FFFH	0 ⌇ 3FFFH	4000H ⌇ 7FFFH 0 ⌇ 3FFFH

The correspondence between the logical and physical addresses for 1M- and 512K-byte ROM is shown below.



6) Applicable ROM devices

1M bytes	Hitachi	HN62301 or equivalent
256K bytes	SUWA SEIKO	SMM6326 or equivalent
	Fujitsu	27C256 or equivalent
128K bytes	Fujitsu	27C128 or equivalent
64K bytes	Fujitsu	27C64 or equivalent

16.5 Multi-Unit II

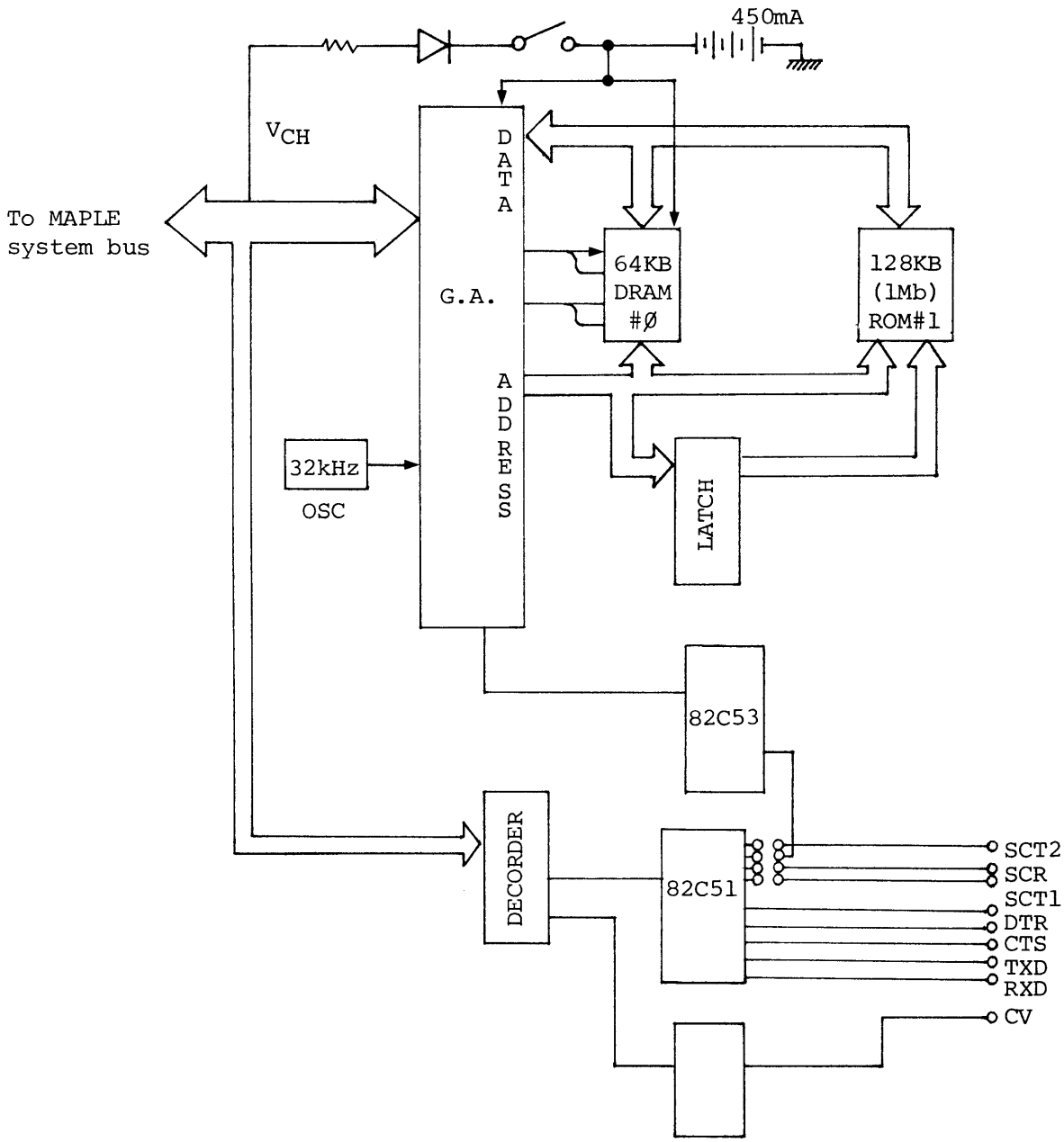
The Multi-Unit II (Model H115A) contains the following:

- 64K RAM disk (described in 16.1)
- ROM capsule (described in 16.4)
- RS-232C interface

The Multi-Unit II contains the same components as the Multi-Unit 64 except the RS-232C interface that is employed instead of the direct modem. This feature allows the Multi-Unit II to have a capability to communicate with the MAPLE asynchronously or synchronously. The interface on the main unit can be used only in the asynchronous mode because of an inadequeate number of connectors on the main unit.

This section describes the specifications for and functions of the RS-232C interface on the Multi-Unit II.

(1) Block diagram



(2) RS-232C hardware

The RS-232C interface is composed of an 8251A (serial interface) Programmable Communication Interface and a 8253 Programmable Interval Timer.

(3) RS-232C control

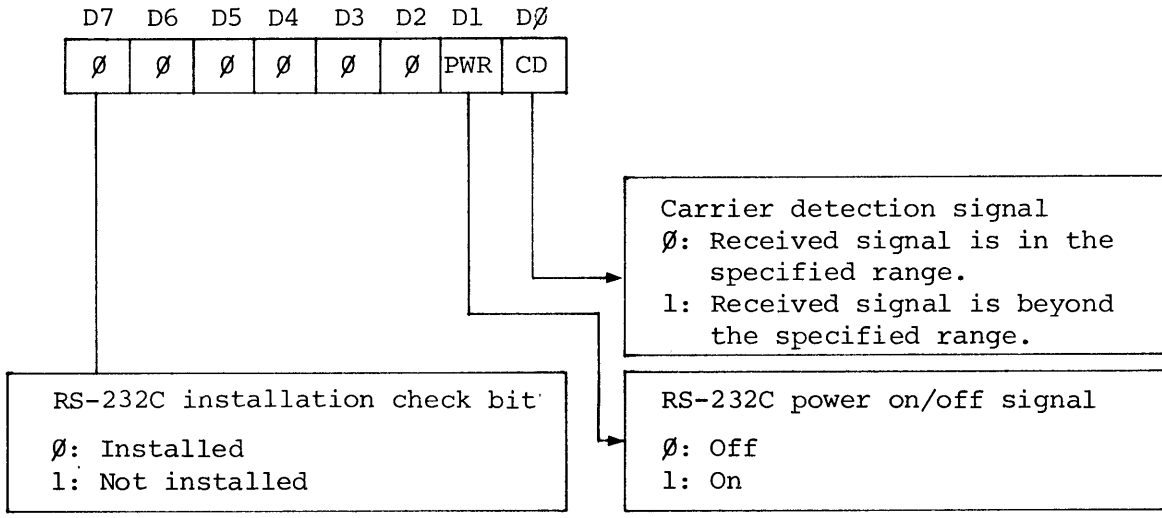
The MAPLE controls the RS-232C interface through the following I/O ports:

A0H: #0 (Count register)	82C53
A1H: #1 Unused	
A2H: #2 Unused	
A3H: Counter mode	
A4H: Data	82C51
A5H: Control/status	
A6H: Carrier detection signal	
A7H: RS-232C power on/off	

(4) Address A6H

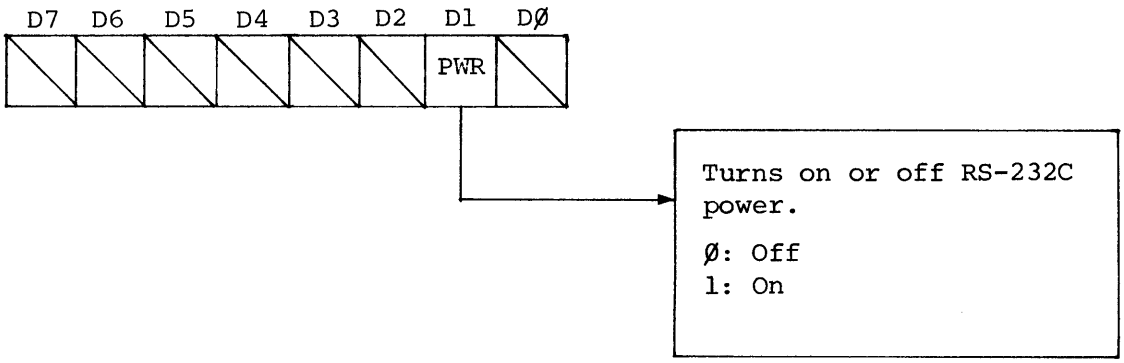
I/O= Input only

Use: For carrier detection



(5) Address A7H

I/O= Output only



RS-232C power refers to the power to the RS-232C driver and receiver.

Note: When the auto shut-off function of the MAPLE main unit is activated, power to logic electronics is turned off and all RS-232C functions are stopped and placed into the reset state. Consequently, it is necessary to set the operating mode of the 8251 when recovering the MAPLE from the auto shut-off state.

It is necessary to supply a mode definition to the 8251 after the MAPLE is powered on or reset.

(6) 8251 serial interface

(See related manuals of 8251 for detail.)

The system clock input to the 8251 is 2.4576 MHz.

There are two 8251 control word formats:

1. Mode instruction format
2. Command instruction format

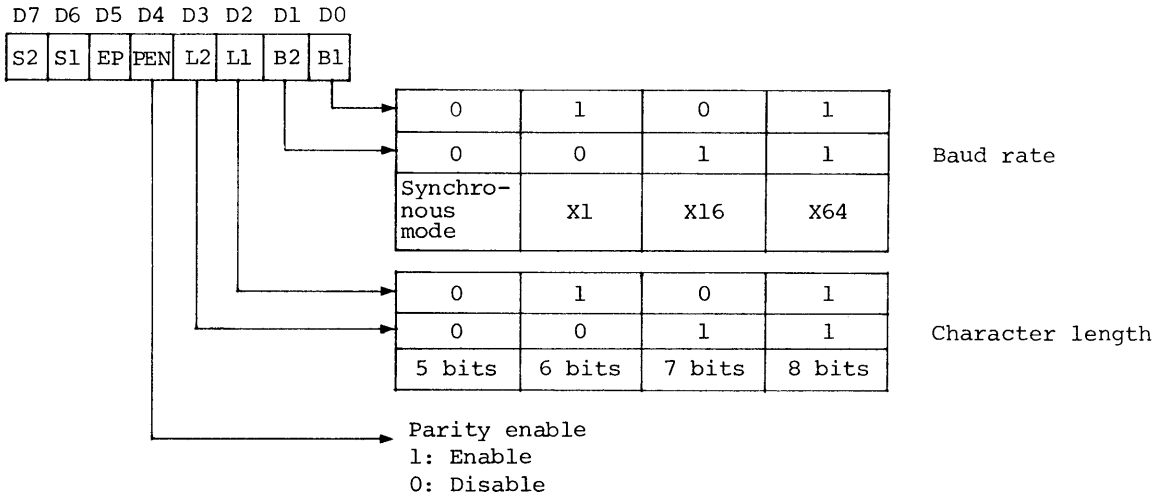
Mode instruction format

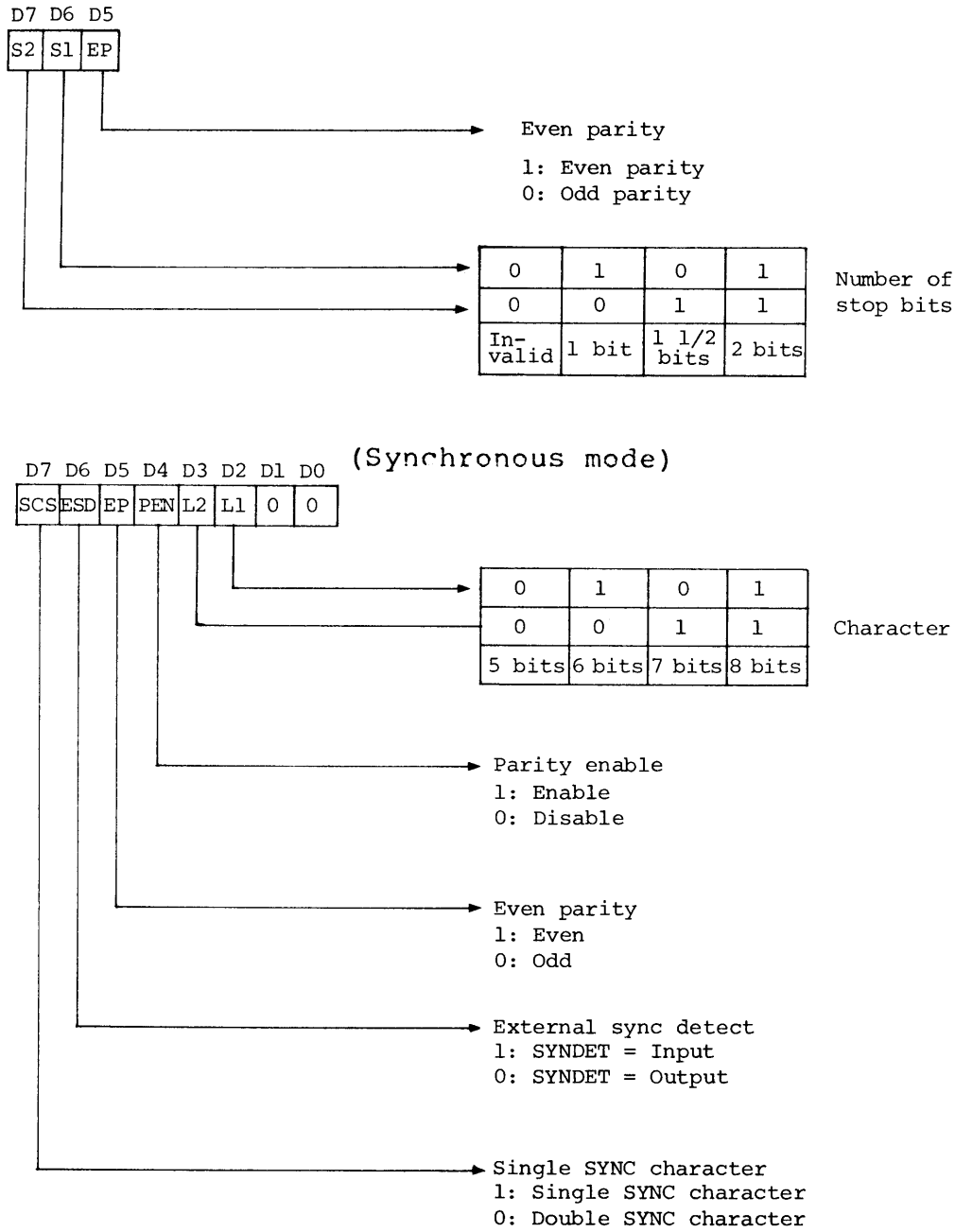
A word in this format must follow an 8251 reset (internal or external). Once the mode instruction is written into the 8251 from the CPU, the 8251 is ready for receiving SYNC character(s) or a command instruction.

Command instruction format

The first command instruction must follow a mode instruction or SYNC characters. The command instruction may be written at any time throughout the operation of the 8251. The 8251 can be reset into the state in which it is ready to receive a mode instruction by setting the D_6 bit (IR) in the command instruction word.

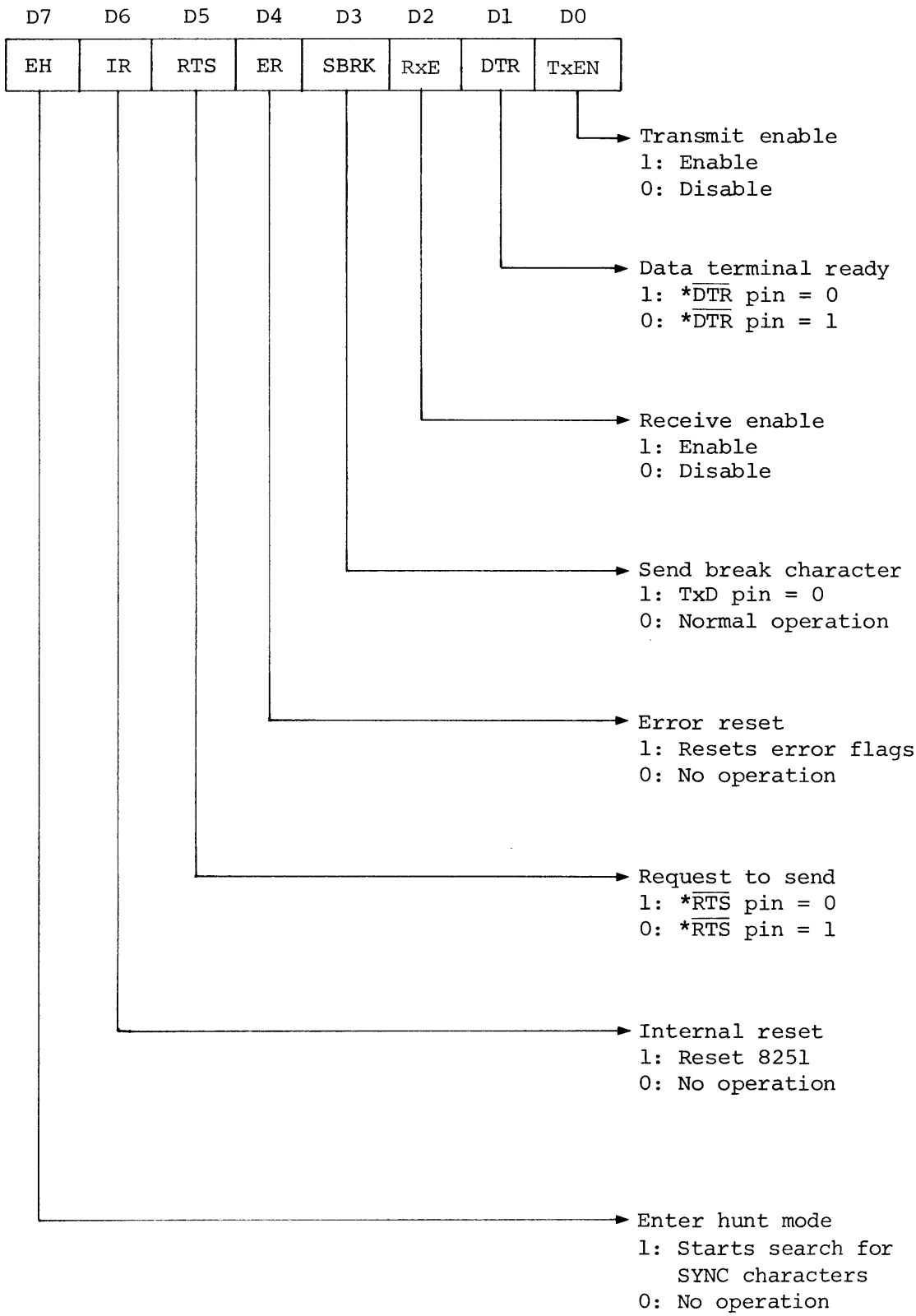
* Address A5H (Mode instruction format in the asynchronous mode)





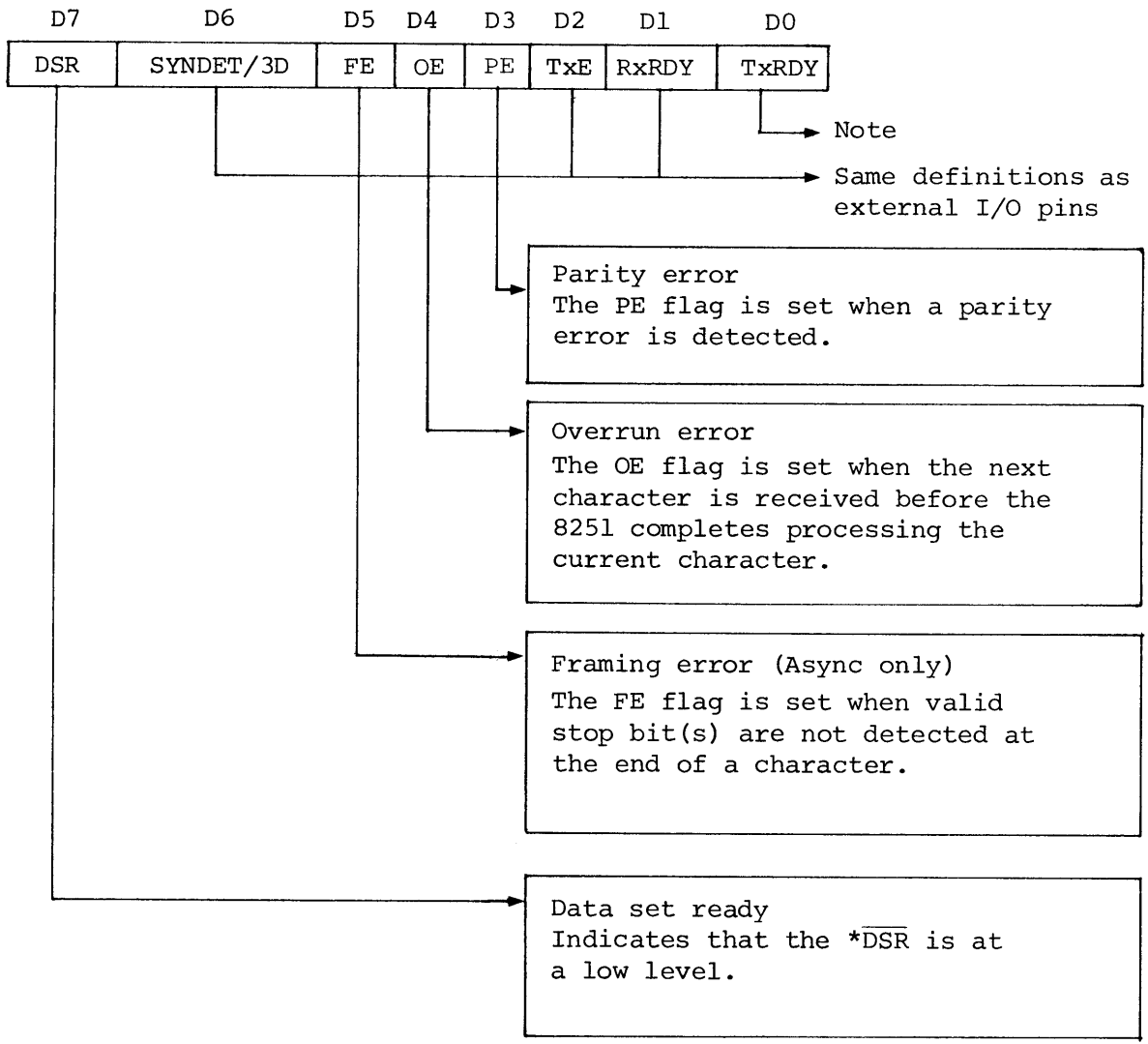
Switching between synchronous and asynchronous modes is controlled by setting bits D1 and D2 of the mode instruction.

Command instruction format (Address A5H)



Status format (Address A5H)

The CPU reads the status of the 8251 by setting C/*D bit to 1 (C1H).



Baud rates

1) Asynchronous mode

Baud rate	(X1)	(X16)	(X64)
150 bps	4ØØØH	Ø4ØØH	Ø1ØØH
200	3ØØØH	Ø3ØØH	ØØØØH
300	2ØØØH	Ø2ØØH	ØØ8ØH
600	1ØØØH	Ø1ØØH	ØØ4ØH
1200	Ø8ØØH	ØØ8ØH	ØØ2ØH
2400	Ø4ØØH	ØØ4ØH	ØØ1ØH
4800	Ø2ØØH	ØØ2ØH	ØØ8ØH
9600	Ø1ØØH	ØØ1ØH	————
19200	ØØ8ØH	ØØØ8H	————

Load a counter value in the above table into the 8253.

2) Synchronous mode

1200 bps Ø8ØØH

2400 bps Ø4ØØH

4800 bps Ø2ØØH

9600 bps Ø1ØØH

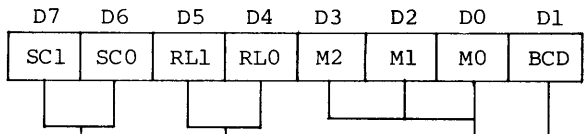
Sample program (Synchronous mode, 4800 bps)

```
LD   A, 36H        ; Load control word
OUT  (A3H), A
LD   A, ØØH        ; Load lowest 8 bits of counter value
OUT  (AØH), A
LD   A, Ø2H        ; Load highest 8 bits of counter value
OUT  (AØH), A
```

(7) 8253 programmable interval timer

(See related manuals of 8253 for detail.)

Address A3H (Control word)



BCD	
0	Binary count (16 digits)
1	BCD count (4 digits)

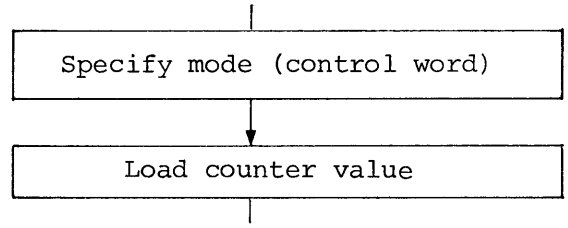
M2	M1	M0	Mode	
0	0	0	Mode 0	
0	0	1	Mode 1	
X	1	0	Mode 2	
X	1	1	Mode 3	*
1	0	0	Mode 4	
1	0	1	Mode 5	

RL1	RL0	Read/Load
0	0	Count latch operation
0	1	Read/load LSB
1	0	Read/load MSB
1	1	Read/load LSB and MSB in that order.

SC1	SC0	Select counter
0	0	Counter #0
0	1	Counter #1
1	0	Counter #2
1	1	————

* Use the 8253 in mode 3.

Program sequence for starting the 8253



(8) Interrupts

An RS-232C interrupt is generated when either RxRDY or TxRDY of the 8251 is set to 1. Both RxRDY and TxRDY are connected to the INT5 (INTEXT) of the MAPLE main unit.

(9) Switching between RS-232C external and internal synchronous modes

DIP switches are used to switch between RS-232C internal and external synchronous modes.

Procedure for checking whether the Multi-Unit II is installed