Chapter 15 I/O and Peripheral Devices

This chapter discusses the following tops:

1. I/O address space
2. Physical file structure
3. EPSP protocol
4. DIP switches

15.1 I/O Address Space

The MAPLE I/O address space listed below.

I/O address	Read	Write
00H	ICRL (Input Capture Register Low)	CTLR1 (Control Register 1)
01H	ICRH (Input Capture Register High)	CMDR (Command Register)
02H	ICRL.B (ICRL Bar code Trigger)	CTLR2 (Control Register 2)
03H	ICRH.B (ICRH Bar code Trigger)	
04H	ISR (Interrupt Status Register)	IER (Interrupt Enable Register)
05H	STR (Status Register)	
06H	SIOR (Serial I/O register)	SIOR (Serial I/O register)
0CH	8251 Data Read	8251 Data Write
0DH	8251 Status Read	8251 Command Write
0EH	SED 1320 PSR	SED 1320 PDIR
0FH	SED 1320 PDOR	SED 1320 PDIR

I/O addresses between 00H and 7FH excluding the above addresses are not used.

I/O addresses 80H through 0FFH are used to access optional units over the system bus. Since addresses 80H through 0DFH are assigned to EPSON optional units addresses 0E0H through 0FFH must be used for user-supplied options.

Currently used I/O addresses

I/O address	Optional unit
8ØH	Intelligent RAM disk
81H	
82H	
83H	
84H	Direct modem
85H	
86H	
87H	
88H	Japanese-language processor
89H	
8AH	
8BH	
8CH	
8DH	
8EH	
8FH	

I/O address	Optional unit
9ØH	Nonintelligent RAM disk
91H	
92H	
93H	
94H	
95H	
96H	
97H	
98H	
99H	
9AH	
9BH	
9CH	
9DH	
9EH	
9FH	

AØH	Synchronous communication unit
A1H	
A2H	
A3H	
A4H	
A5H	
A6H	
A7H	

See Chapter 16, "Extension Units" for use of I/O addresses.

(1) I/O address ØØH

[Read] ICRL

The CPU reads the lower 8 bits from the current FRC (16-bit counter running at 614.4 KHz clock) through this I/O port address. Since the contents of the FRC are loaded into port addresses ØØH and Ø1H immediately once this port is read, the higher 8 bits from the FRC can also read from address Ø1H immediately.

Addresses ØØH and Ø1H must be read in that order.

[Write] CTLR1

CTLR1 bits are assigned as follows:

Bit	Name	Function
7	BRG3	Sets the clock rate for the 8251 (see section 12.2).
6	BRG2	
5	BRG1	
4	BRG0	
3	SWBCD	Indicates the state of the bar code bar code connector power switch (5V). 1: ON, 0: OFF
2	BCD1	Sets the bar code reader interrupt trigger (see section 10.7)
1	BCD0	
0	BANK	Specifies the memory bank. 0: BANK0 0000H - 07FFFH = ROM 8000H - 0FFFFH = RAM 1: BANK1 0000H - 0FFFFH = RAM

Any data to be written into this I/O address must also be saved into work area labeled CTLR1.

```
LD    A, (CTLR1)
```

Set necessary bits of A reg. to 1.

```
LD    (CTLR1), A
OUT   (00H), A
```

CTLR1 --- Overseas version = ØFØBØH

Japanese-language version =ØED9ØH

(2) I/O address Ø1H

[Read] ICRH

The CPU reads the higher 8 bits from the current FRC through this port address. The contents of the FRC is latched immediately when address ØØH is read. Consequently, the contents of ØØH and Ø1H must be read in that order.

[Write] CMDR

CMDR bit assignments are as follows:

Bit	Name	Function
7 6 5 4 3		Unused Always set to 0.
2	RESOVF	1: Resets OVF interrupt INTR signal generated by FRC overflow. 0: Does nothing. The interrupt INTR signal must be reset by the OVF interrupt processing routine before OVF interrupts are to be enabled.

1	RESRDYSIO	1: Resets RDYSIO signal used for communicating with the 7508 (the signal indicates whether the 7508 is ready). 0: Does nothing. See Chapter 11, "7508 CPU" for the use of this bit.
0	SETRDYSIO	1: Sets RDYSIO signal used for communicating with the 7508. 0: Does nothing. This bit is not used by applications.

Set only the necessary bit (bit 1 or 2) to 1 before sending data to this I/O address.

(3) I/O address Ø2H

[Read] ICRL.B

This address contains the lower 8 bits from the FRC latched on a transition in the state of the signal from the bar code reader (positive or negative trigger). A transition in the signal state can be recognized through the ICF interrupt processing routine or by checking I/O address Ø4H, bit 3 (INT3 signal).

The higher 8 bits can be read from I/O address Ø3H.

I/O addresses Ø2H and Ø3H must be read in that order.

[Write] CTLR2

CTLR2 bit assignments are as follows:

Bit	Name	Function
7 6		Unused
5	AUX	1: Specifies that the 8251 is to be connected to the RS-232C connector. 0: Specifies that system bus lines TxDE and *RxDE are to be used to control 8251 handshaking. This bit is set to 0 immediately after the RESET switch is pressed.

Bit	Name	Function
4	INHRS	Used to prevent generation of garbage data when power to the RS-232C drivers is turned on or off. Set this bit to 1 when turning on or off the driver power.
3	SWRS	1: Indicates that RS-232C power (±8 V) is on. 0: Indicates that RS-232C power (±8 V) if off.
2	LED2	1: Indicates that keyboard LED2 is set to on. 0: Indicates that keyboard LED2 is set to off.
1	LED1	1: Indicates that keyboard LED1 is set on. 0: Indicates that keyboard LED1 is set to off.
0	LED0	1: Indicates that keyboard LED0 is set to on. 0: Indicates that keyboard LED0 is set to off.

Write data into this I/O address using the following procedure:

```
LD   A, (CTLR2)
```

Set necessary bits of A reg. to 1.

```
LD   (CTLR2), A
OUT  (02H), A
```

CTLR2 --- Overseas version = 0F0B2H

Japanese-language version =0ED92H

(4) I/O address Ø3H

[Read] ICRH.B

This address contains the higher 8 bits from the FRC latched by a transition in the state of the signal from the bar code reader (positive or negative trigger). Transition in the signal state can be recognized through the ICF interrupt processing routine or by checking I/O address Ø4H, bit 3 (INT3 signal).

The INT3 signal (interrupt signal from the bar code reader) is reset when this I/O address is read.

Addresses Ø2H and Ø3H must be read in that order.

[Write]

None.

(5) I/O address 04H

[Read] ISR

The bits in I/O address 04H indicate the associated interrupt status as shown below:

Bit	Name	Function
7 6		Unused
5	INT5 (EXT)	Indicates the (EXT) external interrupt (system bus external interrupt) status.
4	INT4 (OVF)	Indicates the status of the OVF interrupt caused by FRC overflow. This bit is reset by setting I/O address 01H, bit2.
3	INT3 (ICF)	Indicates the bar code reader interrupt status. This bit is reset by when I/O address 03H is read.
2	INT2 (CD)	Complement of RS-232C CD signal. (When CD is set low, INT2 is set high, generating a CD interrupt.)

1	INT1 (8251)	Indicates the status of the 8251 interrupt generated when RxRDY is set. This bit is reset when receive data is read from the 8251.
0	INT0 (7508)	Indicates the 7508 interrupt status. This bit is reset when the 7508 status is read.

Each of the above statuses can be read if the corresponding interrupt is masked.

[Write] IER

The IER bits enable or disable the corresponding interrupt. All interrupts are disabled when the RESET switch is pressed.

Bit	Name	Function	
7		Unused	
6			
5	IER5	EXT interrupts	1: Enabled 0: Disabled
4	IER4	OVF interrupts	
3	IER3	ICF interrupts	
2	IER2	CD interrupts	
1	IER1	8251 interrupts	
0	IER0	7508 interrupts	

Write data into this I/O address using the following procedure:

```
LD   A, (IER)
```

Set necessary bits of A reg. to 1.

```
LD   (IER), A
OUT  (04H), A
```

IER --- Overseas version = 0F0B3H

Japanese-language version =0ED93H

(6) I/O address 05H

[Read] STR

The bits in I/O address 05H indicate the I/O status as follows:

Bit	Name	Function
7		Unused
6		
5		
4		
3	RDYSIO	Indicates the state of the control signal for the serial bus that serves as an interface to the 7508. 1: 7508 accessible 0: 7508 inaccessible See Chapter 11, "7508 CPU" for to to access the 7508.
2	RDY	Indicates the state of the RDY input line from the 7508. This line is not used.
1	BRDT	Indicates the state of the data input signal from the bar code reader.

Bit	Name	Function
0	BANK	Indicates the current BANK status. 0: BANK0 0000H - 7FFFH = ROM 8000H - 0FFFFH = RAM 1: BANK1 0000H - 0FFFFH = RAM

(7) I/O address ØH

[Read]

The Z8Ø CPU reads this I/O address when receiving data from the 75Ø8.

[Write]

The Z8Ø CPU reads this I/O address when sending a command or data to the 75Ø8.

See Chapter 11, "75Ø8 CPU" for how to access the 75Ø8.

(8) I/O address ØCH

[Read]

The Z8Ø CPU reads this I/O address when receiving RS-232C receive data from the 8251.

[Write]

The Z8Ø CPU reads this I/O address when sending RS-232C send data to the 75Ø8.

(9) I/O address ØDH

[Read]

The Z8Ø CPU reads this I/O address when reading the 8251 status.

[Write]

The Z80 CPU reads this I/O address when sending a command to the 8251.

See Chapter 12, "Using 8251" or consult technical reference manuals on 8251 for I/O addresses 0CH and 0DH.

(10) I/O address ØEH

[Read]

The Z8Ø CPU reads this I/O address when reading the 63Ø1 status.

[Write]

The Z8Ø CPU reads this I/O address when sending data to the 63Ø1.

(11) I/O address ØFH

[Read]

The Z8Ø CPU reads this I/O address when receiving data from the 63Ø1.

[Write]

The Z8Ø CPU reads this I/O address when sending a command to the 63Ø1.

The user cannot read I/O addresses ØEH and ØFH directly. Use the slave BIOS call (WBOOT + 72H) to access the 63Ø1.

15.2 Physical File Structure

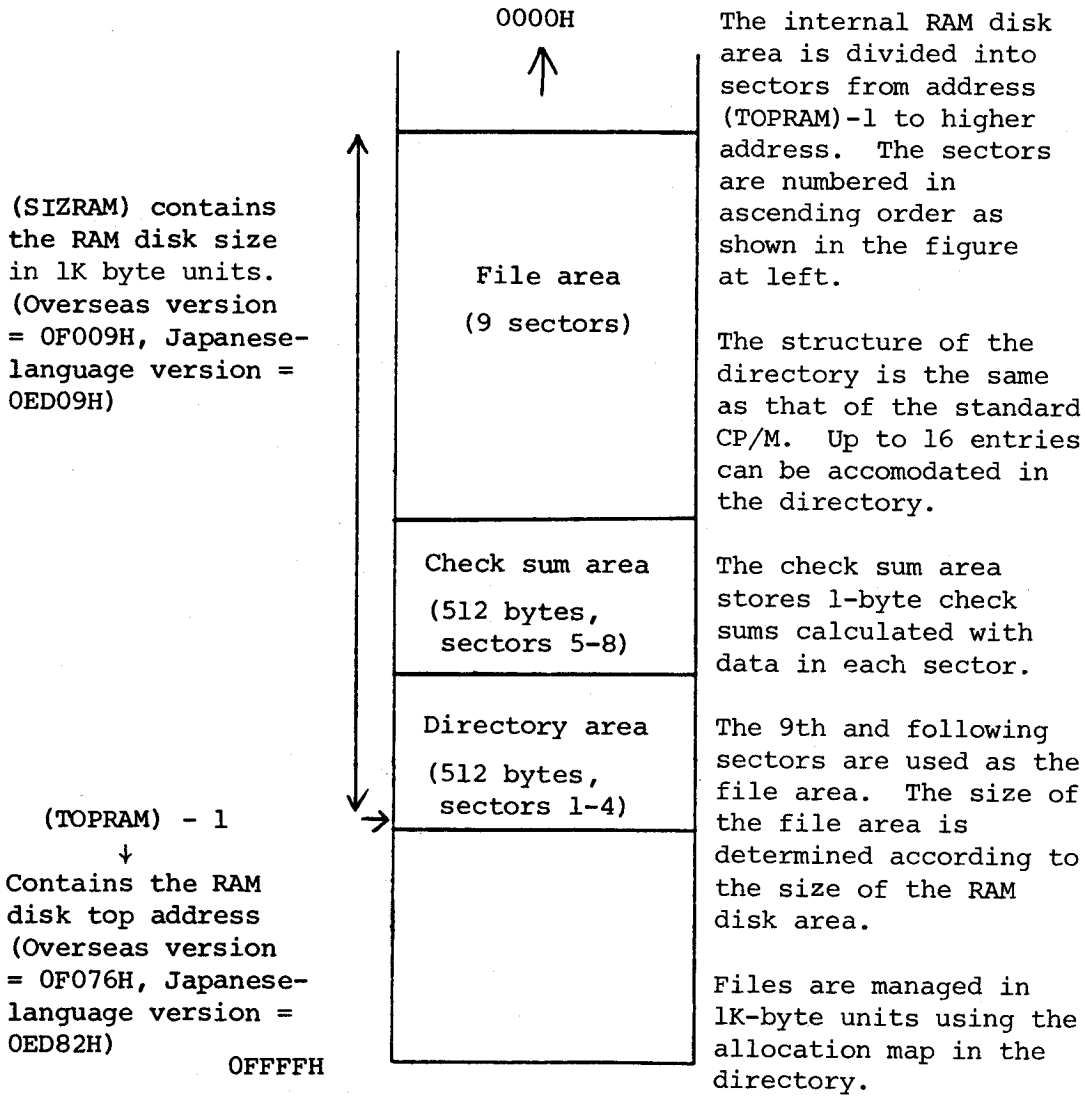
This section describes the structure of the MAPLE files stored on the MAPLE drives. The MAPLE drives use various types of storage media. The storage drives and media are summarized below.

1. Drive A: Internal RAM disk
   See Chapter 16, "Extension Units" for the extension unit RAM disk which is also assigned to drive A:.
2. Drive B: and C: ROM capsule
3. Drive D:, E:, F: and G: Floppy disk
4. Drive I: Extension unit ROM capsule

See Chapter 14, "MTOS and MIOS" for MCT files in drive H:.

(1) Internal RAM disk

The internal RAM disk format in main memory is shown below.



(2) ROM capsule

(2-1) Types of ROM

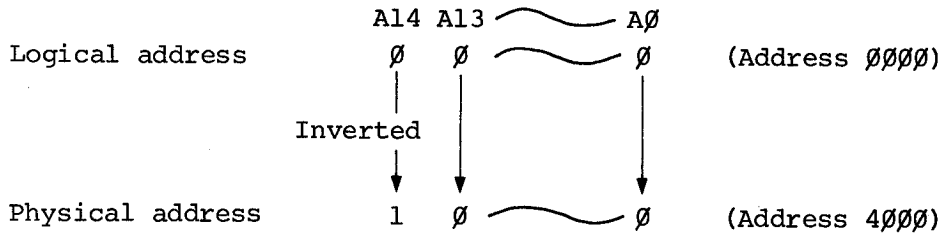
2764, 27128, and 27256 can be used as MAPLE ROM devices.

(2-2) Addresses

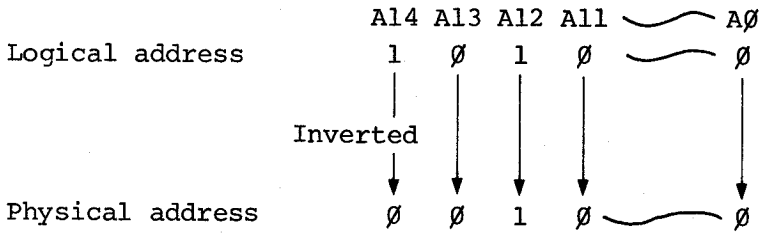
Addresses as viewed from the OS (logical addresses) have a one-to-one correspondence with actual ROM addresses (physical addresses) on 2764 and 27128. On 27256, the relationship between the logical and physical addresses is reversed at address 4000H. This is because the meaning of pin A14 is different for 2564, 27128 and 27256. On 2764 and 27128, this pin must always be set high and, therefore, the signal at pin A14 is inverted by hardware. On 27256, however, pin A14 is used for addressing. This means that address 0 is mapped into address 4000H because accessing address 0 sets A14 pin high.

Example:

- When accessing address ØØØØ:



- When accessing address 5ØØØH



Physical address viewed from the OS	Actual ROM address		
	2764	27128	27256
Ø Ø Ø Ø H	Ø Ø Ø Ø H	Ø Ø Ø Ø H	4 Ø Ø Ø H
1 F F F H	1 F F F H		
2 Ø Ø Ø H			
3 F F F H		3 F F F H	7 F F F H
4 Ø Ø Ø H			Ø Ø Ø Ø H
7 F F F H			3 F F F H

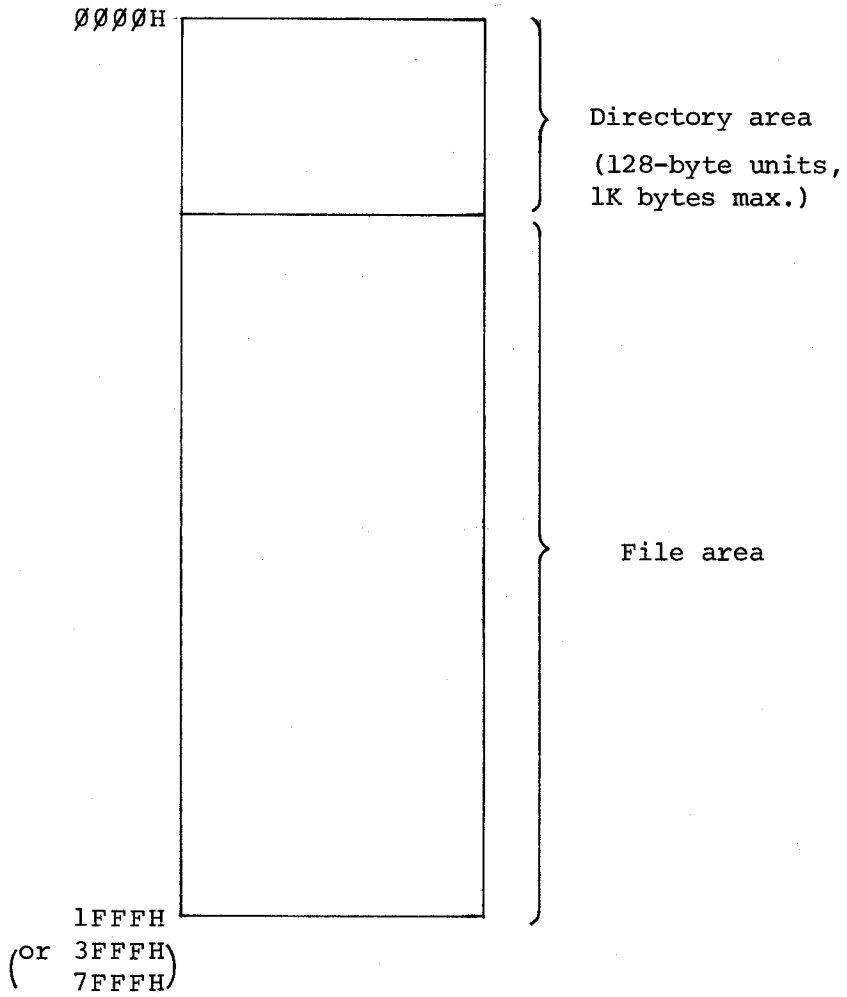
(2-3) ROM capsule memory map

The addresses referred to in the following description are all logical ones. Care must be taken when using 27256 ROM devices.

(For example, address 1000H corresponds to address 5000H in 27256 ROM.)

i) General

ROM is divided into directory and file areas.

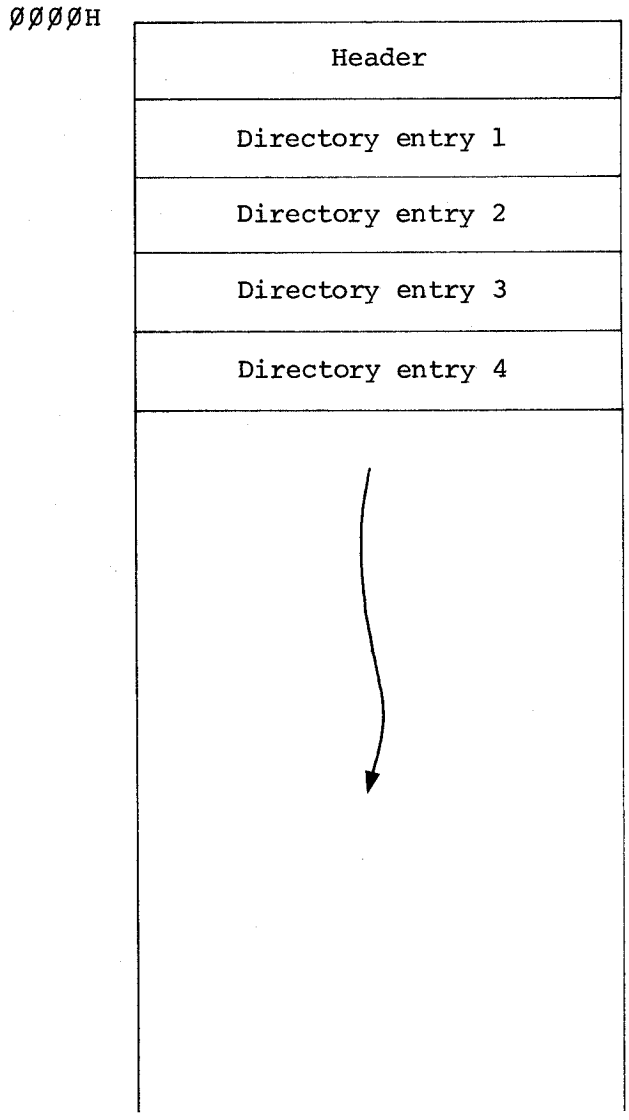


ii) Directory area

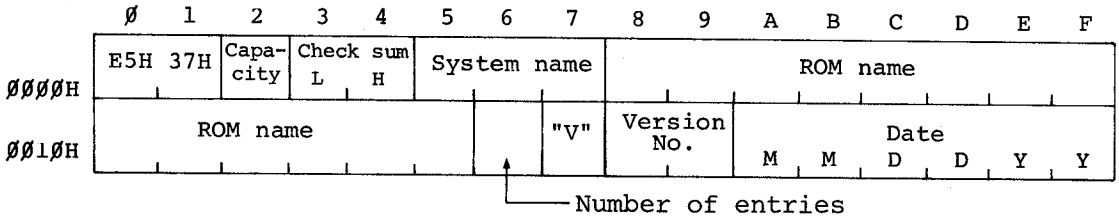
1) The directory area is divided into two sections: a header (first 32 bytes) and a directory entry area.

2) Each directory entry is 32 bytes wide and the directory can hold a maximum of 31 directory entries.

3) The directory area is allocated in 128-byte increments up to 1K bytes.



iii) Header format



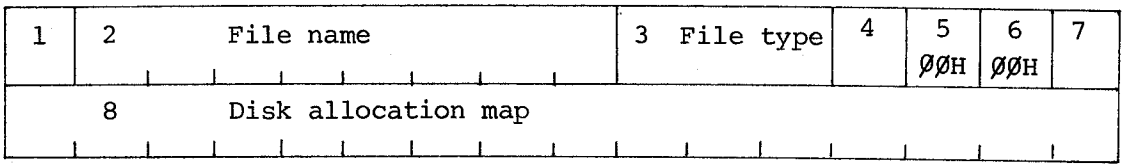
No.	Address	Description
1	0000H - 0001H	Is the ROM identifier. Always set to 0E5H and 37H.
2	0002H - 0002H	Contains the ROM capacity in 1K bytes in binary form. 2764 --- 08H 27128 -- 10H 27256 -- 20H
3	0003H - 0004H	Contains the lowest two bytes of the size of the ROM file area from the beginning of the file area to the end of ROM. 0003H contains the low-order byte and 0004H contains the high-order byte.
4	0005H - 0007H	Contains the user-specified system name.
5	0008H - 0015H	Contains a user-specified ROM name.

No.	Address	Description
6	0016H - 0016H	Contains the number of 32-byte directory entries. The number is either 04H, 08H, 0CH, 14H, 18H, 1CH, or 20H since the directory area is allocated in 128-byte units up to 1K bytes.
7	0017H - 0017H	Set to "V".
8	0018H - 0019H	Contains the ROM version number.
9	001AH - 001FH	Contains the date on which ROM is implemented (latest version).

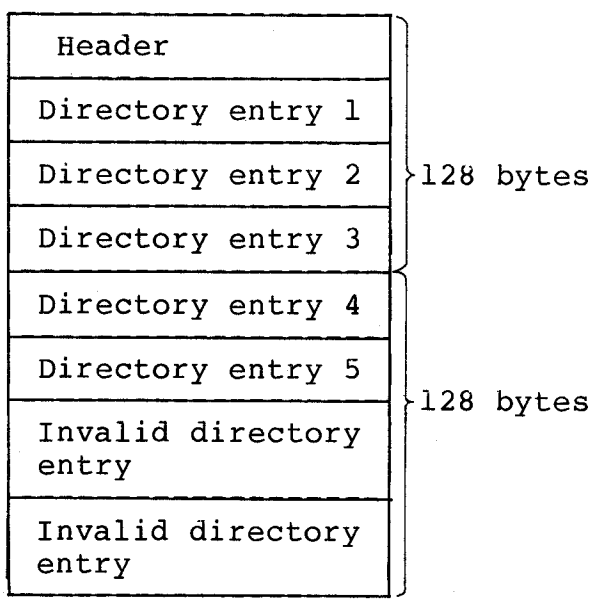
Fields 1, 2, and 6 must be supplied by the user. The other fields are supplied by the system. (The third field (CHECK SUM) should be filled with correct data though the OS makes no check on that field.)

iv) Directory entry format

The format of the directory entries in memory is the same as that of the directory entries on the disk.



No.	Address	Size (Byte)	Description
1	0H - 0H	1	Contains 00H for a valid directory entry and 0E5H for an invalid directory entry. Invalid entries refer to free entries in a 128-byte unit directory area. In the example below, the 128-byte directory contains five valid entries and two invalid entries (64 bytes).

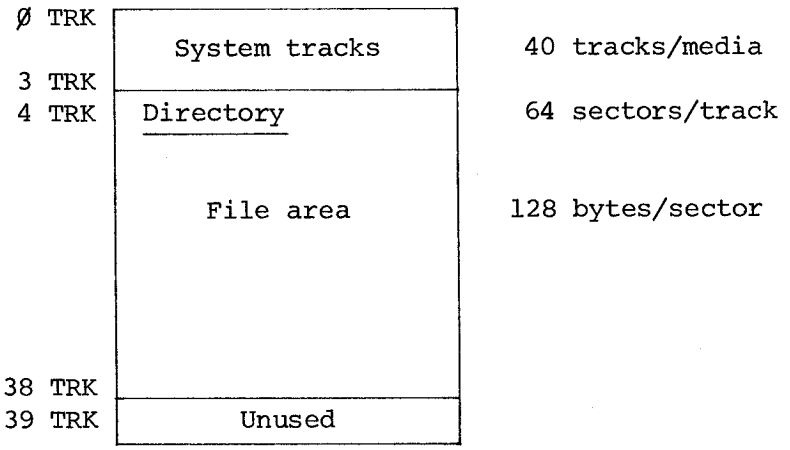


No.	Address	Size (Byte)	Description
2	1H - 8H	8	Contains a 1- to 8-character name.
3	9H - BH	3	Contains a 1- to 3-character file type.
4	0CH - 0CH	1	The logical extent number of the current directory entry (00H - 1FH). As described later, one directory entry can manage a file extent of up to 16K bytes. Therefore, two or more directory entries are required for a file larger than 16K bytes. The logical extent number identifies a 16K-byte extent. It starts at 00H.
5	0DH - 0DH	1	Set to 00H.
6	0EH - 0EH	1	Set to 00H.
7	0FH - 0FH	1	Number of records controlled by the directory entry. (0 - 128, in binary). A record is a unit of data accessed by CP/M at a time

No.	Address	Size (Byte)	Description
			and 128 byte long. Since one directory entry can manage up to 16K bytes of data, it can manage a maximum of 128 records.
8	10H - 1FH	16	Disk allocation map. A file is actually controlled in 1K-byte block units in the file area. The block number of the block currently used by the file is indicated here. (Block numbers begin at 1 and are assigned to 1K-byte blocks sequentially from the first block. The file top location differs depending on the directory area size. The file top is indicated in the header.

(3) FD

The structure of the floppy disk is shown below:



Tracks Ø through 4 contain the boot program for the TF-2Ø floppy disk drive. Sectors 1 through 16 on track 4 are reserved for the directory. The directory can contain up to 64 entries.

The file area starts at sector 17 on track 4 and ends at sector 64 on track 38.

Track 39 is not used so that the MAPLE is compatible with the QC-1Ø/QX-1Ø which does not use track 39. The actual file area size can be calculated as follows:

1 track = 8K bytes

File area = ((40 - 4 - 1) x 8) - 2 = 278K bytes

↑ Total number of tracks
↑ System tracks
↑ Unused track
↑ Track size
↑ Directory size

(4) Extension unit ROM capsule

Overseas MULTI UNIT 64 and MULTI UNIT II can install a ROM capsule of up to 1M bit (128K bytes). Overseas OS version B and up support a ROM capsule as drive I:.

Applicable ROM types are as follows:

i) 64K bits (8K bytes)

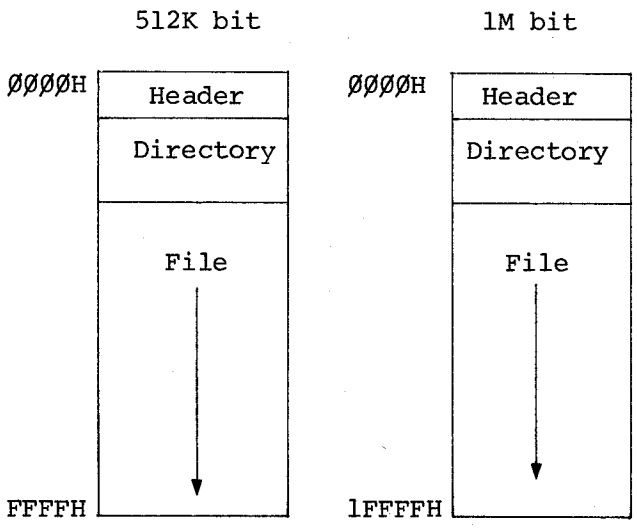
ii) 128K bits (16K bytes)

iii) 256K bits (32K bytes)

iv) 512K bits (64K bytes)

v) 1M bits (128K bytes)

The the format of the extension unit ROM capsule made up of 64K- to 256K-bit ROM devices is identical to that of the ROM capsule described in (2). The format of the 512K- and 1M-bit ROM capsules is also the same except that provide larger address space.



The capacity field at the second byte of the header contains different values for different ROM types.

512K-bit ROM = 40H (64K bytes)

1M-bit ROM = 80H (128K bytes)

15.3 EPSP Protocol

The MAPLE can connect to external disks of the type listed below via a serial interface. Up to two external units (four drives maximum) can be connected in daisy cain configuration.

TF-20 (5.25 inches, 2 drives)
TF-15 (5.25 inches, 1 or 2 drives)
PF-10 (3.5 inches, 1 drive)

CP/M can access these disks as drive D:, E:, F:, and G:. The physical characteristics of the serial interface to external disks are identical to those of the RS-232C interface as shown below.

Level: ±8V
Baud rate: 38,400 bps
Data length: 8 bits/word
Start bit: 1
Stop bit: 1
Parity: None.

Logically, CP/M accesses external disks by

communicating with the external disks using the EPSON Serial Communication Protocol (EPSP). There are six OS commands which are used to access external disks (described on the following pages).

Application programs can access external disks directly by calling the slave BIOS call (WBOOT + 72H) with necessary parameters specified.

4) Commands for drives are summarized below.

FMT	DID	STD	FNC	SIZ	Text data No.	Function and text contents
						Reset terminal floppy.
ØØ	SS	MM	ØD	ØØ	ØØ	XX
Ø1	MM	SS	ØD	ØØ	ØØ	Return code ØØ
						Format disk.
ØØ	SS	MM	7C	ØØ	ØØ	Drive code (1 or 2)
Ø1	MM	SS	7C	Ø2	ØØ	High-order byte of the track number of the currently formatting track
					Ø1	Low-order byte of the track number of the currently formatting track [Ø - 39 FFFF: end]
					Ø2	Return code (BDOS error or Ø)
						Read disk direct.
ØØ	SS	MM	77	Ø2	ØØ	Drive code (1 or 2)
					Ø1	Track No. (Ø - 39)
					Ø2	Sector No. (1 - 64)
Ø1	MM	SS	77	8Ø	ØØ 〉 7F	Read in data (128 bytes)
					8Ø	Return code (BDOS error or Ø)
						Write disk direct.
ØØ	SS	MM	78	83	ØØ	Drive code (1 or 2)
					Ø1	Track No. (Ø - 39)
					Ø2	Sector No. (1 - 64)
					Ø3	Contents of C reg. (write type) (Ø - 2)*1
					Ø4 〉 83	Write data (128 bytes)
Ø1	MM	SS	78	ØØ	ØØ	Return code (BDOS error or Ø)

FMT	DID	STD	FNC	SIZ	Text data No.	Function and text contents
						Flush buffer.
ØØ	SS	MM	79	ØØ	ØØ	XX
Ø1	MM	SS	79	ØØ	ØØ	Return code (BDOS error or Ø)

						Disk volume.
ØØ	SS	MM	7A	ØØ	ØØ	Drive code (1 or 2)
Ø1	MM	SS	7A	Ø2	ØØ	High-order byte of the track number of the currently copying track
					Ø1	Low-order byte of the track number of the currently copying track [Ø - 39 FFFF: end]
					Ø2	Return code (BDOS error or Ø)

The command 7AH (Copy All disk) is used not by the OS but used by the disk utility program COPYDISK. The function is not supported for one-drive disk systems (PF-1C, for example).

Command Descriptions

FMT: Identifies the header block type.

ØØH: Indicates message transmission from the main unit (MAPLE).

ØlH: Indicates message transmission from the FDD.

(All values in FMT through SIZ is in hexadecimal.)

DID: Destination device ID. This identifies the drive to which the current message (command) is to be sent when two FDDs are connected in daisy chain configuration.

31H: First drive (Drive D: or E:)

32H: Second drive (Drive F: or G:)

The device of address of the FDDs (TF-2Ø, for example) is determined by DIP switches.

SID: Source device ID

Identifying the source of the current message (command). This field contains 22H if the message (command) is from the MAPLE.

FNC: Command for FDD.

SIZ: Indicates the text block length (ØØH - ØFFH). The value in this field is the length of the actual text block minus 1.

Text block: A block of data necessary for executing the command. This block can contain 1 to 256 data bytes.

1) Reset Terminal Floppy (RESET)

Causes the FDD to initialize itself and wait for an ENQ block. The FDD returns return code ØØ to the system.

2) Format Disk (FORMAT)

Causes the FDD to format two tracks and return the corresponding track number (logical numbers) and a return code to the system. The FDD continues formatting in two track units and sets the logical track number in the return message to ØFFFFH when it completes formatting.

3) Read Disk Direct (READ)

Causes the FDD to transfer the data (128 bytes) to the system from the disk sector on the specified logical track at the specified sector number and a return code to the system. Deblocking technique (physical to logical conversion of tracks and sectors) is adopted to speed up this processing.

4) Write Disk Direct (WRITE)

Causes the FDD to write the specified data (128 bytes) to the location on the disk addressed by the specified logical track and sector numbers. Actually, this command only places the specified data into the 1K-byte host buffer because of the

blocking technique (logical to physical conversion of tracks and sectors).

5) Flush Buffer (WRITEHST)

Causes the FDD to flush the contents of the 1K-byte buffer filled by the WRITE command onto the disk.

6) Copy Volume

Causes the FDD to copy the entire diskette on the specified drive onto another diskette. This command is not available if the system has only one drive.

7) Return codes

Return code (hex)	Meaning	
00	Normal termination	
FA	BDOS error	Read error
FB		Write error
FC		Drive select error
FD		Write protect
FE		

*1: The third byte of the data block for FNC=78H indicates the write mode:

ØØH: Standard write (The FDD blocks data before write.)

Ø1H: Flush buffer (The FDD immediately writes data on the FD without blocking.)

Ø2H: Sequential write

ØØH is used when writing ordinary files. Ø1H is used only when writing directories.

Other commands

The FDD supports some other commands in addition to the six commands used by the MAPLE. Refer to FDD manuals for further information on these commands. They can also be activated easily by calling the slave BIOS function (WBOOT + 72H).

15.4 DIP Switches

The table below lists the uses of the DIP switches on the main unit back panel.

Uses of DIP switches

SW	Overseas version	Kana and Japanese-language version
1	Identifies the keyboard type.	Identifies the keyboard type. Ø = Kana keyboard 1 = Japanese-language keyboard or touch type keyboard
2		Not used.
3		Not used.
4		Not used.
5	Specifies whether the check sum is to make a check at power-on time when the RAM disk unit 6Ø or 12Ø is connected.' Ø = No check made 1 = Check made	⟸
6	Specifies the range of code conversion to be used during screen dump. Ø = Converts ØØH - 1FH, 7FH, or ØFFH to a space. 1 = Converts ØØH - 1FH or 7FH - ØFFH to a space.	Not used.
7	Not used.	Not used.
8	Not used.	Not used.