CHAPTER 7
APPENDIX

7.1 Main CPU (Z80)

The main CPU is a CMOS-based, 8-bit microprocessor that controls the whole system. It directly controls DRAM, the RS-232C interface and the expansion interface (CN8), and sends and received commands and data both to and-from sub-CPUs 7508 and 6303 through the gate arrays.

Part No. X400260000 is currently used for the main CPU; however, jumper J1 has been incorperared on the MAPLE board so that in the future, other CPUs, which will expand the systems capabilities, can also be used.

7.1.1 Operation

The main CPU operates at a clock rate of 2.45 MHz, making the instruction cycle approximately 1.6μs.

1 state : $1/(2.45 \times 10^8) = 408\mu s$
1 cycle : 408×4(4 states) = Approx. 1.6μs

Fig. 7-1 shows a block diagram of the main CPU. Registers consist of general-purpose registers, accumulator registers, and flag registers.

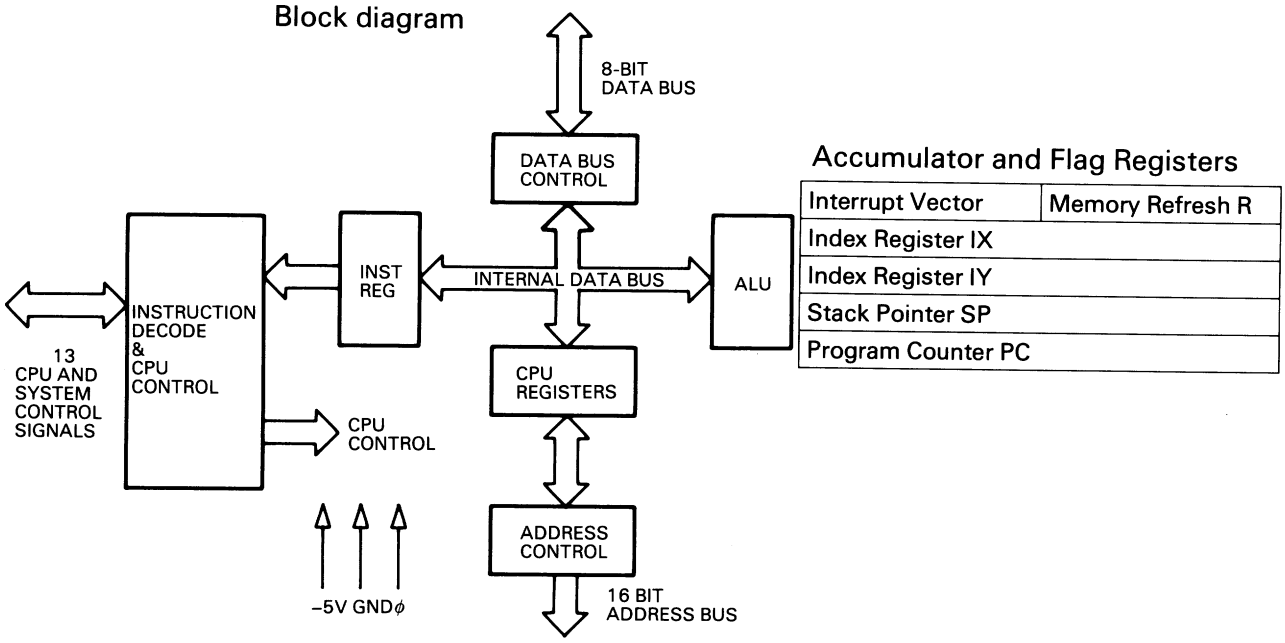


Fig. 7-1

7.1.2 Functions of Major Registers

1. Program counter (PC): 16 bits
   Holds address of next instruction.
2. Stack pointer (SP): 16 bits
   Holds address of the top of the stack memory in DRAM.
3. Index register (IX and IY): 16 bits
   Used for index addressing.
4. Memory refresh register (R): 8 bits
   Holds refresh address of DRAM. Lower seven bits are automatically incremented on execution of op code fetch cycle.
5. Interrupt page address register (I): 8 bits
   Holds high-order 8 bits of the indirect address used for interrupt mode 2.

7.1.3 Timing

An instruction is normally executed in combination with one of the following three basic machine cycles:

(1) Instruction op code fetch (MI cycle)
(2) Memory read/write cycle
(3) Input/output cycle

* The relation between clock, state and machine cycle is as follows.

1 state = 1 clock
1 machine cycle = 3 to 6 states
1 instruction cycle = 2 to 6 machine cycles

7.1.4 Interrupt Function

The $\overline{\text{NMI}}$ (non maskable interrupt) line of the main CPU cannot be used because it is always pulled up by resistor R94. Therefore, only the maskable interrupt $\overline{\text{INTR}}$ line is valid in this machine. The interrupt function operates in one of the following three modes:

Mode 0: Executes the instruction (normally RST or CALL) read in MI (mode condition after reset).
Mode 1: Saves the content of the program counter and automatically causes a branch to 0038H.
Mode 2: Executes an indirect CALL instruction according to the content of the index registor and the data which has been read.

* These interrupts may not be accepted when the $\overline{\text{BUAK}}$ signal is low. (I.C., that period when the CPU is keeping the bus open).

70008 Main CPU

1. Location: MAPLE board, 4A
2. Pin Assignments

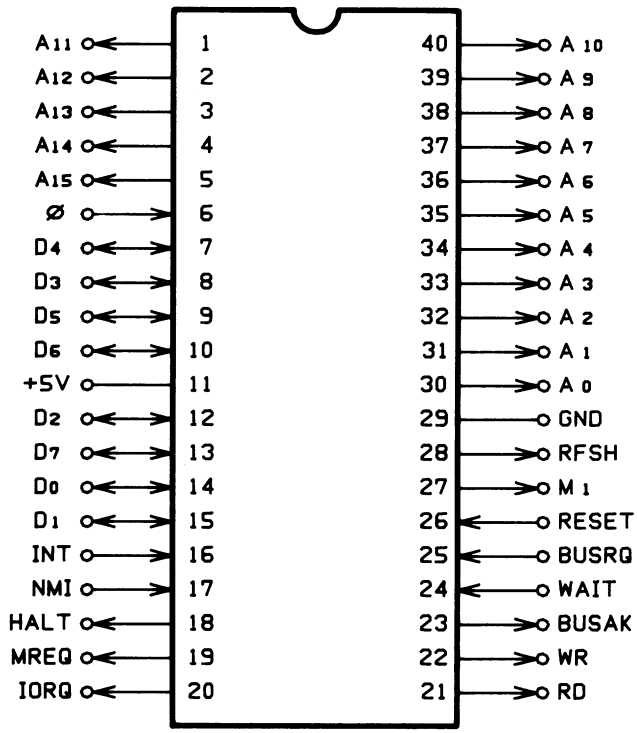


Table 7-1 70008 MAIN CPU Pin Assignments

Pin No.	Signal Name	In/Out	Function
–5 30–40	AB0–15 (Address Bus)	Tri-state output active high	A 16-bit address bus which outputs a memory address or I/O device number. It outputs the lower 7 bit D-RAM address for memory refresh.
7–10 12–15	DB0–15 (Data Bus)	Tri-state input and output active high	An 8-bit data bus which is used for data transfer between memory or an I/O device and main CPU.
27	$\overline{M_1}$ (Machine Cycle one)	Output active low	A signal which indicates that the starting machine cycle is the OP code fetch cycle.
19	$\overline{MRQ}$ (Memory Request)	Tri-state output: active low	A signal which indicates that the address information required for the memory read/write is output on the address bus. It is also output during memory refresh for synchronization.

Pin No.	Signal Name	In/Out	Function
20	$\overline{\text{IORQ}}$ (Input/Output Request)	Tri-state output: active low	During MI cycle Occurs when the CPU acknowledges a maskable interrupt, the external device to put the interrupt response vector on the data bus. Other than during MI cycle Indicates that the I/O device number required for this I/O read/write is output on the address bus.
21	$\overline{\text{RD}}$ (Read)	Tri-state output: active low	A signal which indicates that the data bus is in the input state. Memory or I/O device puts data on the data bus in synchronization with this signal.
22	$\overline{\text{WR}}$ (Write)	Tri-state: active low	This signal indicates that the data bus is in the output state. The data to the I/O device or memory is put on the data bus in synchronization with this signal.
28	$\overline{\text{RF}}$ (Refresh)	Output: active low	This signal indicates, during MI cycle, that the dynamic RAM refresh address is output onto the lower seven bit lines of the address bus. Dynamic RAM reads the refresh address using the $\overline{\text{MREQ}}$ signal which is output together with the $\overline{\text{RFSH}}$ signal.
18	$\overline{\text{HALT}}$ (Halt State)	Output: active low	This signal indicates that CPU has HALTed as the result of a HALT instruction execution. The $\overline{\text{INT}}$, $\overline{\text{NMI}}$, or $\overline{\text{RESET}}$ signal is required to leave the HALT state. CPU repeats dynamic RAM refresh by executing a NOP instruction, even while in the HALTed state.
24	$\overline{\text{WAIT}}$ (Wait)	Input: active low	CPU remains in the WAIT state while this signal is active. A low speed memory or I/O device can be directly connected to CPU by using this signal. No memory refresh is performed during the WAIT state.

Pin No.	Signal Name	In/Out	Function
16	$\overline{\text{INTR}}$ (Interrupt Request)	Input: active low	An interrupt request signal. When this signal becomes active, CPU enters the interrupt processing program after the current instruction has been executed.
17	$\overline{\text{NMI}}$ (Non Maskable Interrupt)	Input-negative: edge triggered	A non-maskable interrupt request signal. When this signal becomes active, CPU jumps to address $0066_{(16)}$ after the current instruction has been executed, regardless of whether interrupt is enabled or not. The $\overline{\text{NMI}}$ signal has a priority over the $\overline{\text{INT}}$ signal.
26	$\overline{\text{RS}}$ (Reset)	Input: active low	Resets CPU when active.
25	$\overline{\text{BURQ}}$ (Bus Request)	Input: active low	When active, this signal causes CPU to force the address bus ($A_{0\text{-}15}$), data bus ($D_{0\text{-}7}$), and tri-state system control terminals ($\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, and $\overline{\text{WD}}$) in the high impedance state, freeing the external buses for another device. The $\overline{\text{BUSRQ}}$ signal has priority over the $\overline{\text{NMI}}$ signal.
23	$\overline{\text{BUAK}}$ (Bus Acknowledge)	Output: active low	When active, this signal indicates that CPU has forced the address bus, data bus, and tri-state system control terminals in the high impedance state.
6	CLK (Clock)	Input	A 0/+5V single-phase clock signal

7.2 Slave CPU 6303

6303 is a 6800-series, 8-bit, C-MOS CPU. It incorporates a 4kB masked ROM which contains programs for controlling the microcassette tape drive, ROM capsule, V-RAM, LCD display unit, serial interface, and speaker. A mode six (Multiplexer Partial/Decode) is selected for the control operations. Stand-by and sleep modes, unique to 6303, are not used.

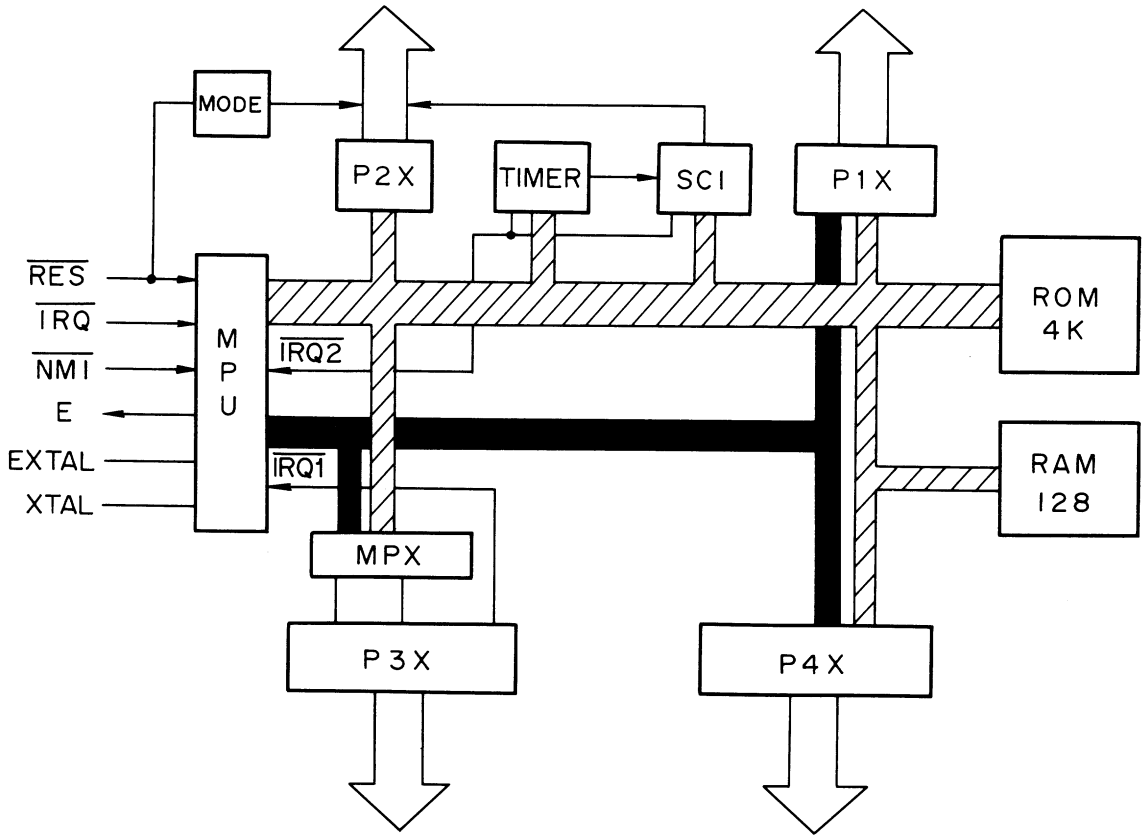


Fig. 7-2 6303 Slave CPU Functional Block Diagram

This computer uses a crystal oscillator for a 2.4576 MHz clock signal. The slave CPU operates with the 614.4 kHz system clock signal which is internally quartered from the primary frequency of 2.4576 MHz. The table opposite shows the port assignment.

Table 7-2

Port	Assignment
Port 1	Parallel I/O terminal
Port 2	Serial I/O terminal
Port 3	Address/data terminal
Port 4	Address terminal

Slave CPU 6303

1. Location: MAPLE Board, 130
2. Pin Assignment

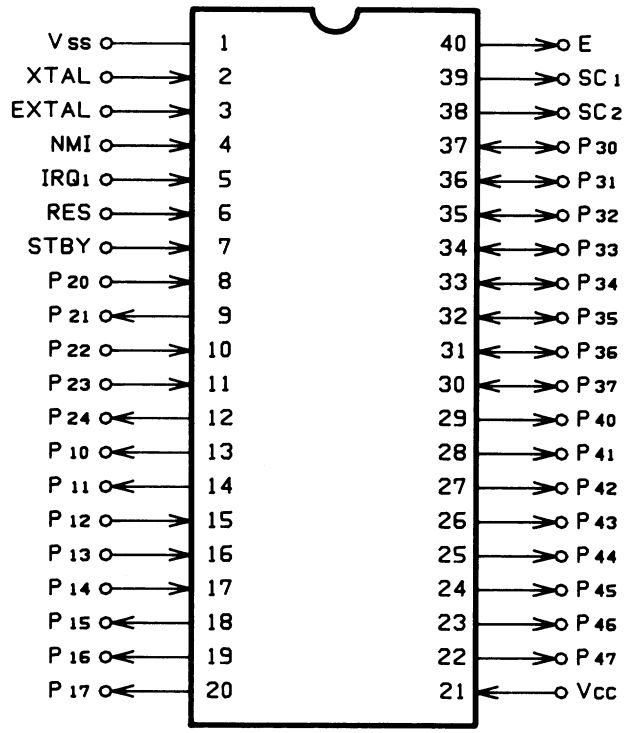


Table 7-3 6303 Slave CPU Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	G	–	GND
2	X TAL	In	Unused – reserved for external clock signal input.
3	EX TAL	In	External clock signal input 2.4576 MHz
4	$\overline{NMI}$	In	Unused – reserved for non-maskable interrupt input.
5	$\overline{INTR}$	In	Interrupt request
6	$\overline{RS}$	In	Reset signal
7	$\overline{STB}$	In	Unused – reserved for Stand-by signal input.
8	P20	In	Microcassette tape read data (RDMC)
9	P21	Out	Microcassette tape write data (WD)
10	P22	In	Unused – reserved for operation mode setting.
11	P23	In	Serial interface receive data
12	P24	Out	Serial interface transmit data
13	P10	Out	Microcassette head pinch motor ON/OFF (HMT)

Pin No.	Signal Name	In/Out	Function
14	P11	Out	Microcassette tape erase (ERAH)
15	P12	In	Microcassette tape write enable (WE)
16	P13	In	Microcassette tape head load/unload switch
17	P14	In	Serial interface PIN signal
18	P15	Out	Serial interface POUT signal
19	P16	Out	Speaker output
20	P16	Out	Speaker power on/off
21	VC	In	+5V (Circuit voltage)
22	A15	Out	Address bus
23	A14	Out	Address bus
24	A13	Out	Address bus
25	A12	Out	Address bus
26	A11	Out	Address bus
27	A10	Out	Address bus
28	A9	Out	Address bus
29	A8	Out	Address bus

Pin No.	Signal Name	In/Out	Function
30	DA7	In Out	Data address bus
31	DA6	In Out	Data address bus
32	DA5	In Out	Data address bus
33	DA4	In Out	Data address bus
34	DA3	In Out	Data address bus
35	DA2	In Out	Data address bus

Pin No.	Signal Name	In/Out	Function
36	DA1	In Out	Data address bus
37	DA0	In Out	Data address bus
38	R/$\overline{W}$	Out	Read/Write
39	AS	Out	Address strobe
40	E	Out	ENABLE

7.3 Sub-CPU 7508

This is a 4-bit, C-MOS CPU which incorporates a masked ROM, timer, and serial interface, etc. This CPU is always backed up by the battery, regardless whether power is on or off, it provides the following control functions:

1. Power on/off (POWER switch and an associated program)
2. Keyboard scanning and auto-repeat
3. RESET switch
4. Temperature and battery voltage sensing
5. D-RAM refresh
6. Clock (calendar and alarm services)

The sub-CPU exchanges data with the main CPU in a bit-serial fashion via the gate array GAH40M. Fig. 7-3 is a functional block diagram of the sub-CPU. Table 7-4 lists the terminal signals and summarizes their functions.

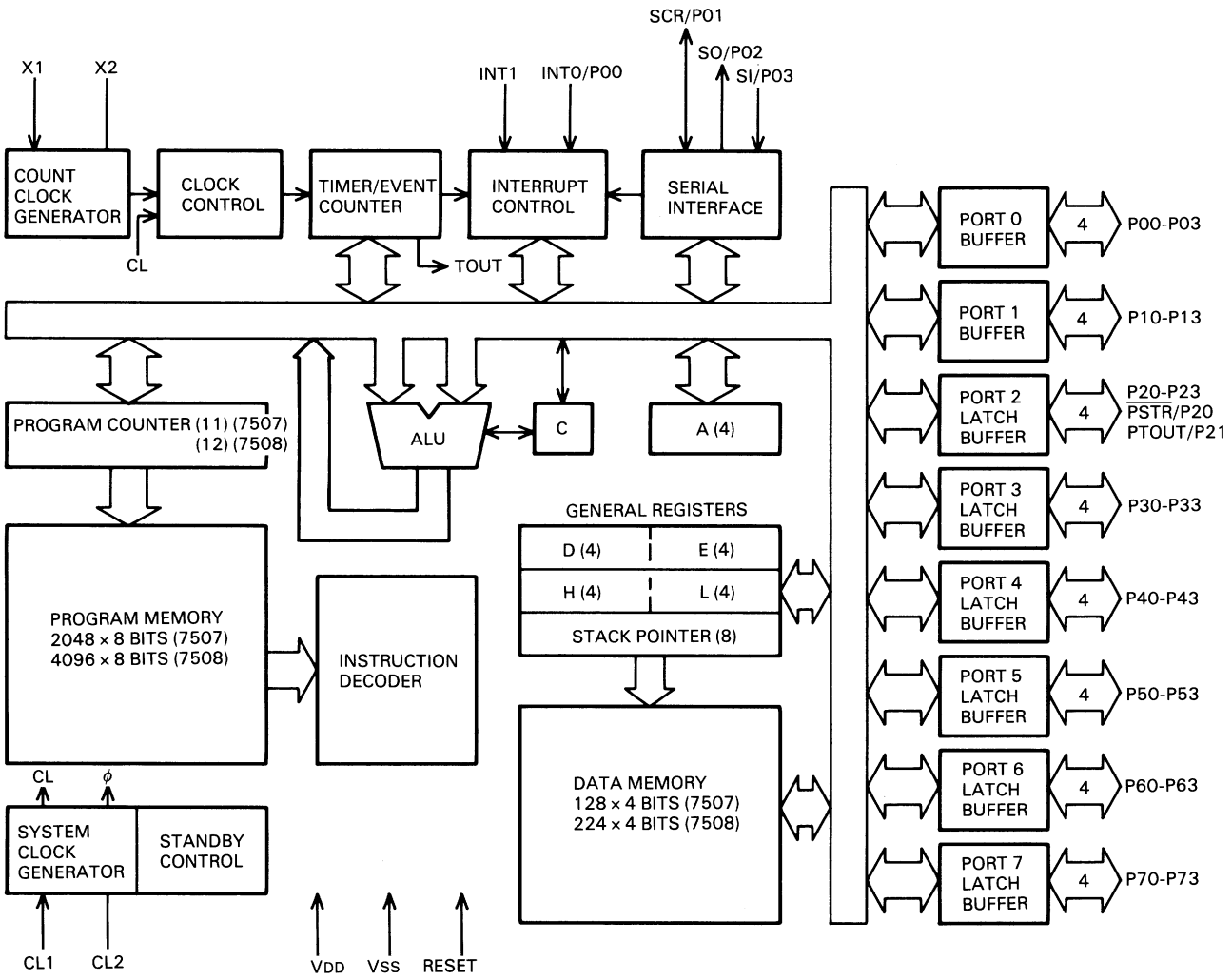


Fig. 7-3

7508 (Sub-CPU)

1. Location: MAPLE Board, 2E
2. Pin Assignments

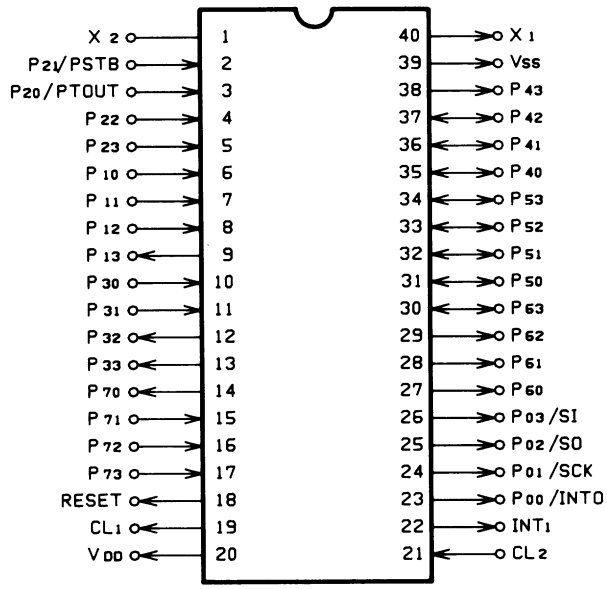


Table 7-4 7508 SUB-CPU Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	x 2	In	Unused.
2	P20	Out	GAH40M SIOR access control – H: 7508, L: Main CPU
3	P21	Out	A-D converter 7001 Chip Select - mode switching between address data and A-D conversion.
4	P22	Out	Ready signal
5	P23	Out	A-D converter 7001 power on/off
6	P10	In	Key return 0
7	P11	In	Key return 1
8	P12	In	Key return 2
9	P13	In	Key return 3
10	P30	Out	Key scan control
11	P31	Out	Key scan control
12	P32	Out	Key scan control
13	P33	Out	Key scan control
14	P70	Out	Power ON/OFF

Pin No.	Signal Name	In/Out	Function
15	P71	Out	Data write – prevents FF latches in gate array at power off.
16	P72	Out	Data write – D-RAM refresh control signal during power off.
17	P73	Out	Data CAS
18	RS	In	Reset signal input
19	CL1	In	Clock signal input
20	VC	In	+5V (Battery voltage: VB) terminal
22	CL2	In	Clock signal input
23	P00/INT0	In	POWER switch
24	$\overline{SCK}$	Out	Shift clock signal output – used for A-D conversion data/main CPU command read.
25	SO	Out	Serial data output
26	SI	In	Serial data output
27	P60	In	RESET switch
28	P61	In	Charge start detection
29	P62	In	Analog interface trigger input
30	P63	In	Test point
31	P50	In	Key return 4
32	P51	In	Key return 5
33	P52	In	Key return 6
34	P53	In	Key return 7
35	P40	Out	Reset signal – initializes main CPU and slave CPU, etc. via GAH40.
36	P41	Out	Charge mode control – normal/trickle charge.
37	P42	Out	Auxiliary battery backup enable/disable control.
38	P43	Out	Interrupt to main CPU
39	G	In	Ground terminal
40	X1	In	External clock signal input – 1 kHz

7.4 Gate Array GAH40D

GAH40D is the gate array for D-RAM control. It controls memory access and memory refresh. It also incorporates a clock frequency divisor which divides 9.8 MHz input to 4.9 MHz, 2.45 MHz, 32 KHz and 1 KHz of clock frequency. Fig. 7-4 shows an internal block of diagram of the GAH40D.

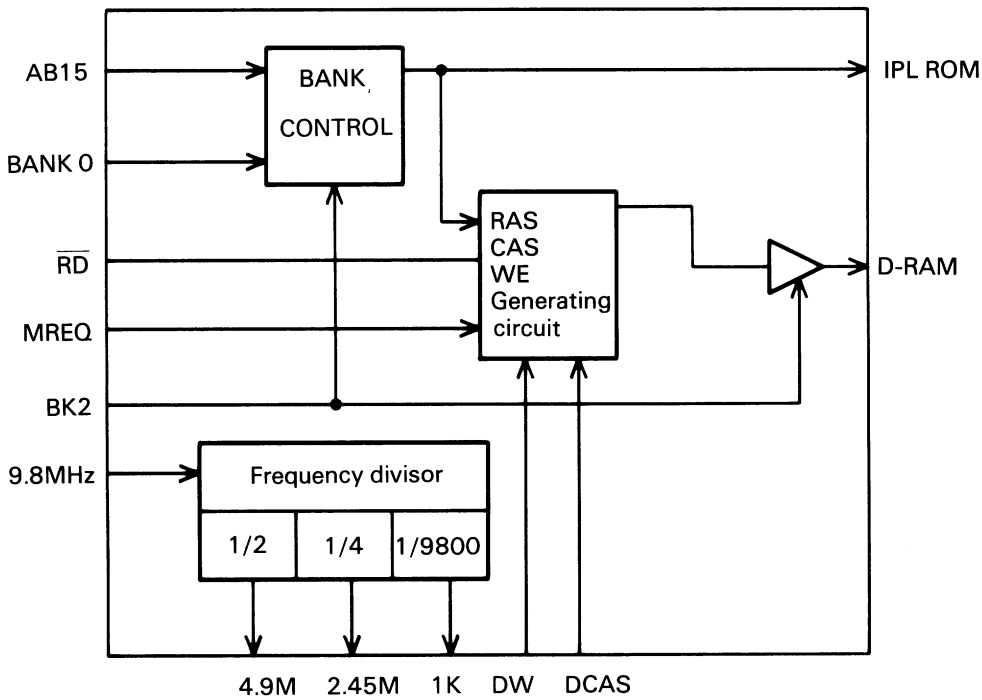


Fig. 7-4

The BANK 0/1 signal is provided from the gate array GAH40M. The main CPU sends this signal by writing bit 0 to I/O address 00. (0: bank 0, 1: bank 1)
BK2 signal is provided from the option unit.

GAH40D

1. Location: MAPLE Board, 6A
2. Pin Assignment

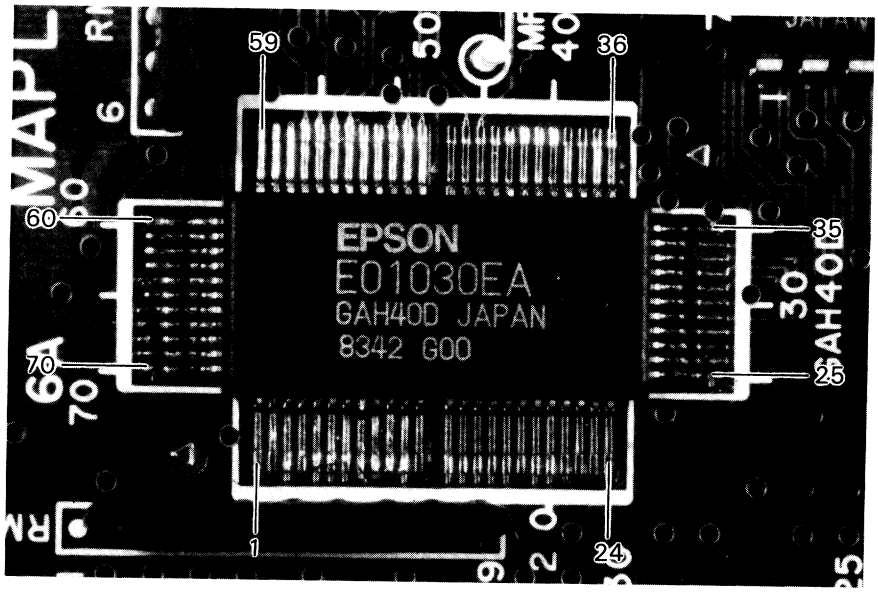


Table 7-5 GAH40D Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	N/C	–	Not used.
2	N/C	–	Not used.
3	AB12	In	Address bus 12
4	N/C	–	Not used.
5	AB 6	In	Address bus 6
6	AB 13	In	Address bus 13
7	AB 5	In	Address bus 5
8	$\overline{RST}$	In	Reset input from sub-CPU 7508. Whole reset signal $\overline{RSQ}$ is generated from this signal.
9	DRA 2	Out	DRAM address 2 (10)
10	DRA 1	Out	DRAM address 1 (9)
11	AB 14	In	Address bus 14
12	G	–	Ground

Pin No.	Signal Name	In/Out	Function
13	AB 4	In	Address bus 4
14	AB 15	In	Address bus 15
15	AB 3	In	Address bus 3
16	DRA 0	Out	DRAM address 0(8)
17	$\overline{\text{RAS1}}$	Out	Low address stroke: RAS signal to RAS.
18	W1	Out	Write enable: WE signal to DRAM.
19	AB 2	In	Address bus 2
20	AB 1	In	Address bus 1
21	AB 0	In	Address bus 0
22	N/C	–	Not used
23	N/C	–	Not used
24	N/C	–	Not used
25	$\overline{\text{RD}}$	In	Read signal
26	$\overline{\text{CSROM}}$	Out	IPL ROM chip select signal
27	$\overline{\text{MR}}$	Out	Memory read signal
28	$\overline{\text{Z-INT}}$	Out	Interrupt request signal to main CPU
29	$\overline{\text{Z-RF}}$	In	Refresh signal from main CPU
30	VC	–	Circuit voltage (+5V)
31	$\overline{\text{HLTA}}$	In	Halt signal
32	$\overline{\text{M1}}$	In	Indicates that main CPU is in machine cycle 1 (opcode fetch)
33	$\overline{\text{MRQ}}$	In	Memory request signal
34	$\overline{\text{RSO}}$	Out	System reset signal resets the whole machine.
35	DRA 3	Out	DRAM address 3 (11)
36	N/C	–	Not used
37	N/C	–	Not used
38	DRA 7	Out	DRAM address 7 (15)
39	N/C	–	Not used

Pin No.	Signal Name	In/Out	Function
40	$\overline{RF}$	Out	Refresh signal for DRAM
41	DRA 4	Out	DRAM address 4 (12)
42	DRA 5	Out	DRAM address 5 (13)
43	DRA 6	Out	DRAM address 6 (14)
44	$\overline{CAS1}$	Out	Column address strobe: CAS signal to DRAM
45	$\overline{S\text{-}INT}$	In	Interrupt signal from gate array GAH40M. Generates $\overline{Z\text{-}INT}$ signal and causes an interrupt to main CPU.
46	BANK 1/0	In	Bank 0: Bank select signal from gate array GAH40M. Bank 0 at low level and IPL ROM is selected at $\overline{AB15}$.
47	G	–	Ground
48	4.9 M	Out	Clock output gained by dividing 9.8 MHz clock. Supplied to SED1320.
49	9.8 M	In	Clock input of 9.8404 MHz
50	$\overline{2.45\ M}$	Out	Clock output by dividing 9.8 MHz clock into four. Clock for main CPU.
51	1KC	Out	Clock output by dividing 32 KHz clock to 32. Clock for sub-CPU 7508.
52	TEST	In	Test terminal. Normally kept low.
53	OFF	In	Initializes signal for the whole internal circuit. At high level, initializes all FFs. Hold 4.9 M, 2.45 M, $\overline{CS\ ROM}$, $\overline{RD}$ and $\overline{Z\text{-}INT}$ at high level and others inactive. Outputs $\overline{RSO}$.
54	32K	In	Basic clock input of 32.768 KHz. Generates 1 KC (Clock).
55	DW	In	Data write signal. W1 (write enable) control data supplied from sub-CPU 7508 when main CPU is on standby.
56	DCAS	In	Data CAS. CAS 1 control data supplied from sub-CPU 7508 when main CPU is standby.
57	N/C	–	Not used
58	N/C	–	Not used

Pin No.	Signal Name	In/Out	Function
59	N/C	–	Not used
60	N/C	–	Not used
61	N/C	–	Not used
62	N/C	–	Not used
63	N/C	–	Not used
64	$\overline{\text{BK2}}$	In	DRAM select signal from option unit.
65	VC	–	Circuit voltage (+5V)
66	AB 10	In	Address bus 10
67	AB 9	In	Address bus 9
68	AB 8	In	Address bus 8
69	AB 11	In	Address bus 11
70	AB 7	In	Address bus 7

7.5 Gate Array GAH40M (E01031AA)

This gate array incorporates the following functional blocks; the operation is controlled by the Z80 main CPU.

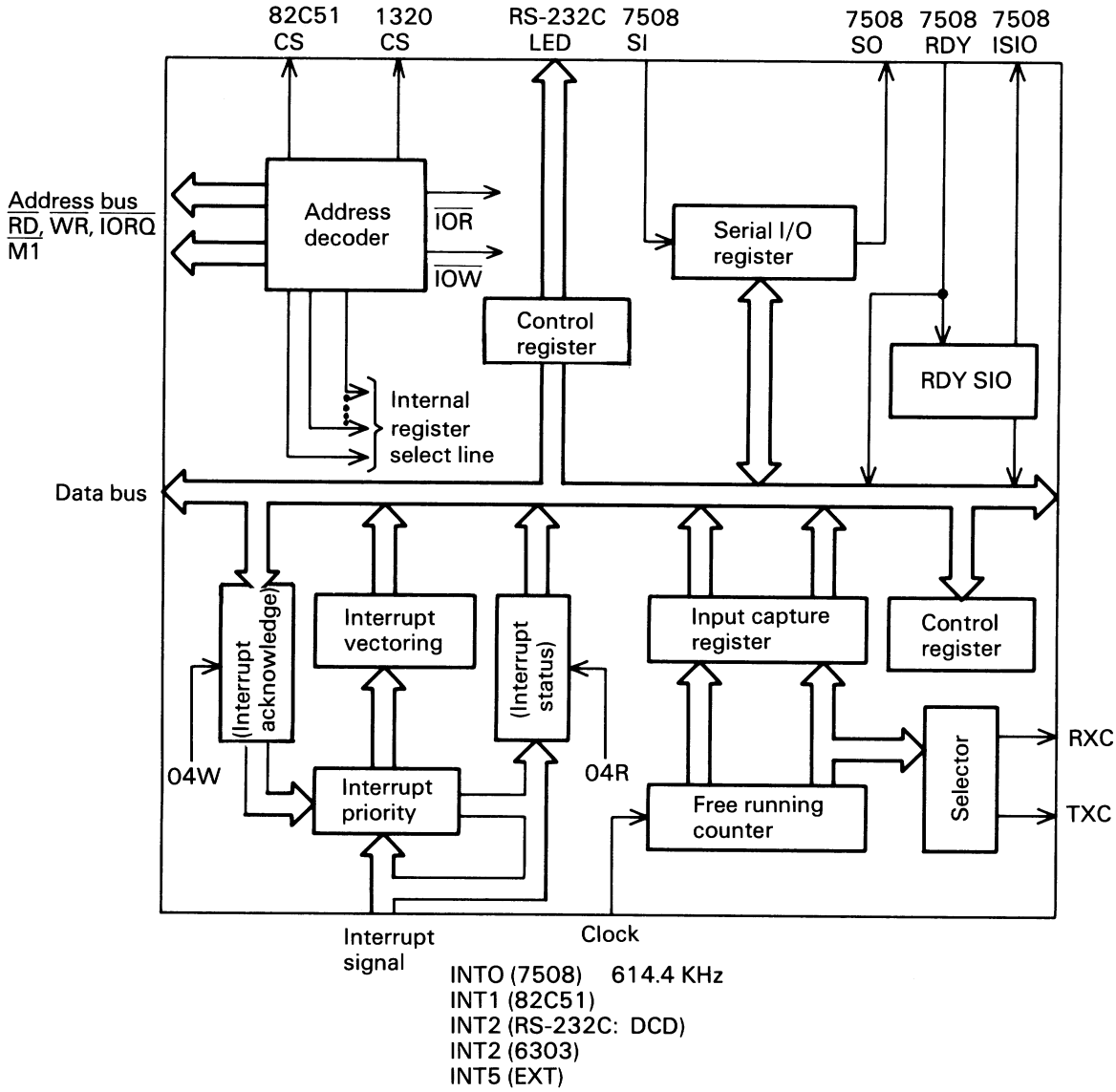


Fig. 7-5

As shown in Fig. 7-5, this gate array includes the address decoder, the 7508 interface, an interrupt controller, a timer and baud rate generator, and I/O ports for the RS-232C and the LED display.

Table 7-6

Write			Read	
00 CTLR1			00 ICLR · C	
7	BRG 3	Baud rate generator select 3 timer	7	ICR7
6	BRG 2	Baud rate generator select 2 timer	6	ICR6
5	BRG 1	Baud rate generator select 1 timer	5	ICR5
4	BRG 0	Baud rate generator select 0 timer	4	ICR4
③	SWBCD	Barcode reader switch timer	3	ICR3
2	BCD1 (μp)	Barcode mode select 1 timer	2	ICR2
1	BCK0 (down)	Barcode mode select 0 timer	1	ICR1
⓪	$\overline{\text{BANK0}}$	Bank switching	0	ICR0
01 CMDR			01 ICRH · C	
7			7	ICR15
6			6	ICR14
5			5	ICR13
4			4	ICR12
3			3	ICR11
2	1: reset OVF(Pulse)	timer	2	ICR10
1	1: reset RDYSIOFF(Pulse)	SIO	1	ICR9
0	1: set RDYSIOFF (Pulse)	SIO	0	ICR8
02 CTLR2			02 ICRL · B	
7			7	ICR7
6			6	ICR6
⑤	AUX	External auxiliary output	5	ICR5
④	INHRS Inhibit RS-232C	RS232	4	ICR4
③	SWRS RS-232C switch	RS232	3	ICR3
②	LED2	LED	2	ICR2
①	LED1	LED	1	ICR1
⓪	LED0	LED	0	ICR0
03			03 ICRH · B	
			7	ICR15
			6	ICR14
			5	ICR13
			4	ICR12
			3	ICR11
			2	ICR10
			1	ICR9
			0	ICR8

Write	
04 IER	
7	
6	
5	IER5 (INTEXT enable)
4	IER4 (INTOVF enable)
3	IER3 (INTICF enable)
2	IER2 (INT 6303 enable)
1	IER1 (INT 82C51 enable)
0	IER0 (INT 7508 enable)
05	
06 SIOR	
7	SIO 7
6	SIO 6
5	SIO 5
4	SIO 4
3	SIO 3
2	SIO 2
1	SIO 1
0	SIO 0
07	

Read			
04 ISR			
7	0		
6	0		
⑤	INT 5 (INTEXT)	External interrupt	
4	INT 4 (OVF)	Overflow flag timer	
3	INT 3 (ICF)	Input capture flag timer	
②	INT 2 (INT 6303)	6303 interrupt	
①	INT 1 (INT 82C51)	82C51 interrupt	
⓪	INT0 (INT7508)		7508 interrupt
05 STR			
7			
6			
5			
4			
3	RDYSIO	SIO ready	SIO
②	RDY	ready	SIO
①	BRDT	Barcode reader data timer	
0	$\overline{\text{BANK0}}$	$\overline{\text{BANK0}}$	
06 SIOR			
7	SIO 7		
6	SIO 6		
5	SIO 5		
4	SIO 4		
3	SIO 3		
2	SIO 2		
1	SIO 1		
0	SIO 0		

07	During interrupt
	1
	1
	1
	1
Interrupt vectoring	Vect 2
	Vect 1
	Vect

(1) Address Decoder

The address decoder performs each register specification, chip select signal output control of 82C51 (2C) and SED1320 (7C), decoding of I/O read/write signals, etc.

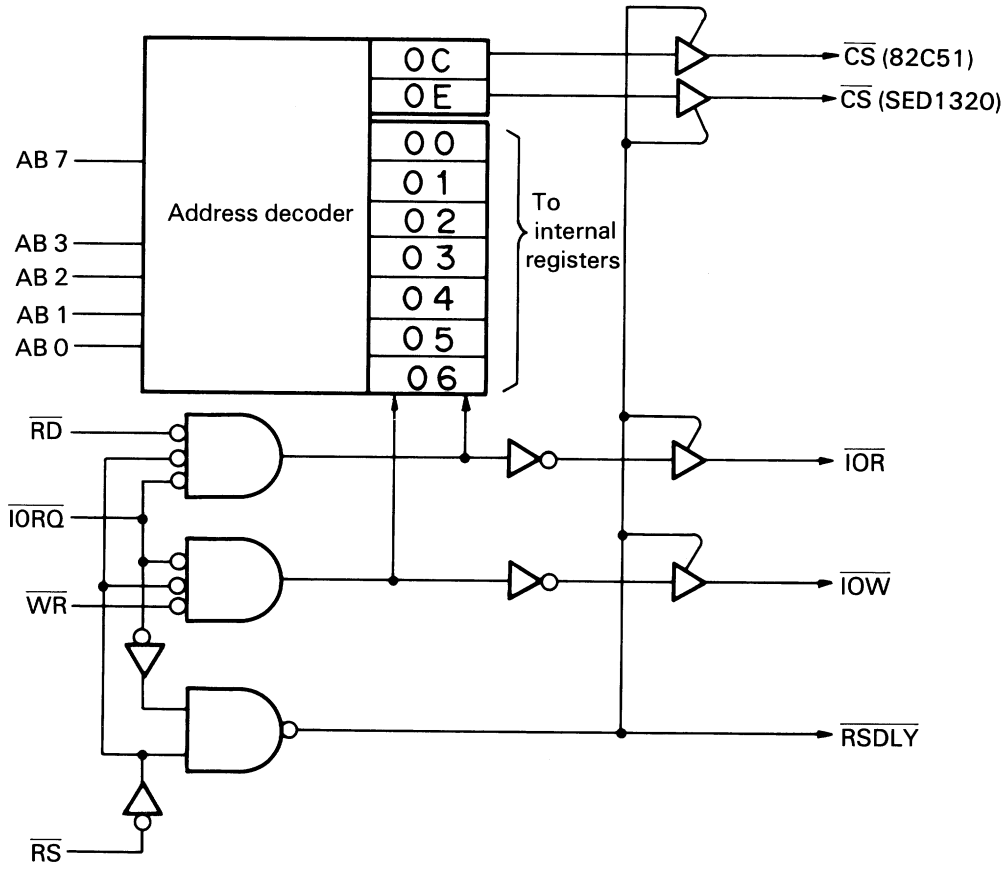


Fig. 7-6

As shown in Figure 7-6, the main CPU can directly select internal registers via four address lines. The CS signals of the 82C51 and SED1320 are also controlled by the I/O address decoder via this registers.

(2) Interrupt Controller

Fig. 7-7 shows six kinds of interrupt input, two of which are used for internal timer interrupt. Priority and vector addresses are assigned to each interrupt signal as shown in the table below.

Table 7-7 Priority and Vector Addresses

Priority	Signal Name	Description	Interrupt vector D7 6 5 4 3 2 1 0	Corresponding mask IER (04)	Corresponding status ISR (04)
Low	$\overline{\text{INT5}}$	($\overline{\text{INTEXT}}$) External pin: request from external expansion board	1 1 1 1 1 0 1 0	IER5	ISR5
	INT4	(OVF) Inside: FRC overflow	1 1 1 1 1 0 0 0	IER4	ISR4
	INT3	(ICF) Inside: ICR bar code trigger	1 1 1 1 0 1 1 0	IER3	ISR3
	$\overline{\text{INT2}}$	($\overline{\text{INT6303}}$) External pin: request from 6303	1 1 1 1 0 1 0 0	IER2	ISR2
	$\overline{\text{INT1}}$	($\overline{\text{INT82C51}}$) External pin: request from 82C51	1 1 1 1 0 0 1 0	IER1	ISR1
High	$\overline{\text{INT0}}$	($\overline{\text{INT7508}}$) External pin: request from 7508	1 1 1 1 0 0 0 0	IER0	ISR0

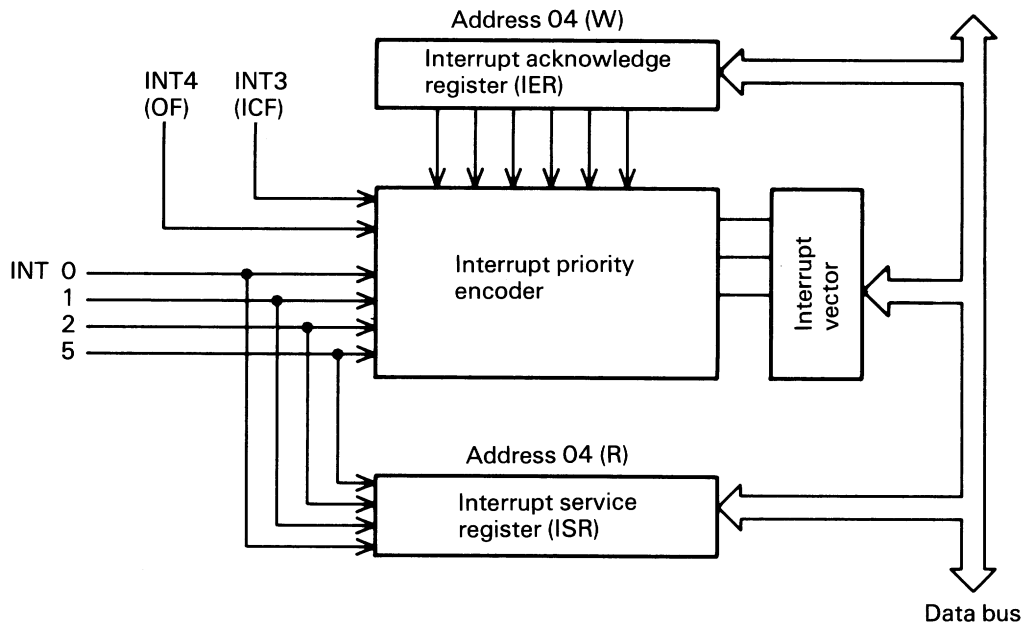


Fig. 7-7

This interrupt controller controls each interrupt acknowledge and mask operation at bit setting for IER. When an interrupt occurs, a vector address is output on the data bus.

(3) Timer and baud rate generator

An 2.4576 MHz clock supplied from the outside is divided into a basic clock of 614.4 KHz (1.6276 μsec) which operates the free running counter (FRC). FRC is a counter of 16 bits; the low-order, 8 bit output of the FRC Cover is also used for the RS-232C transmit/ receive clock.

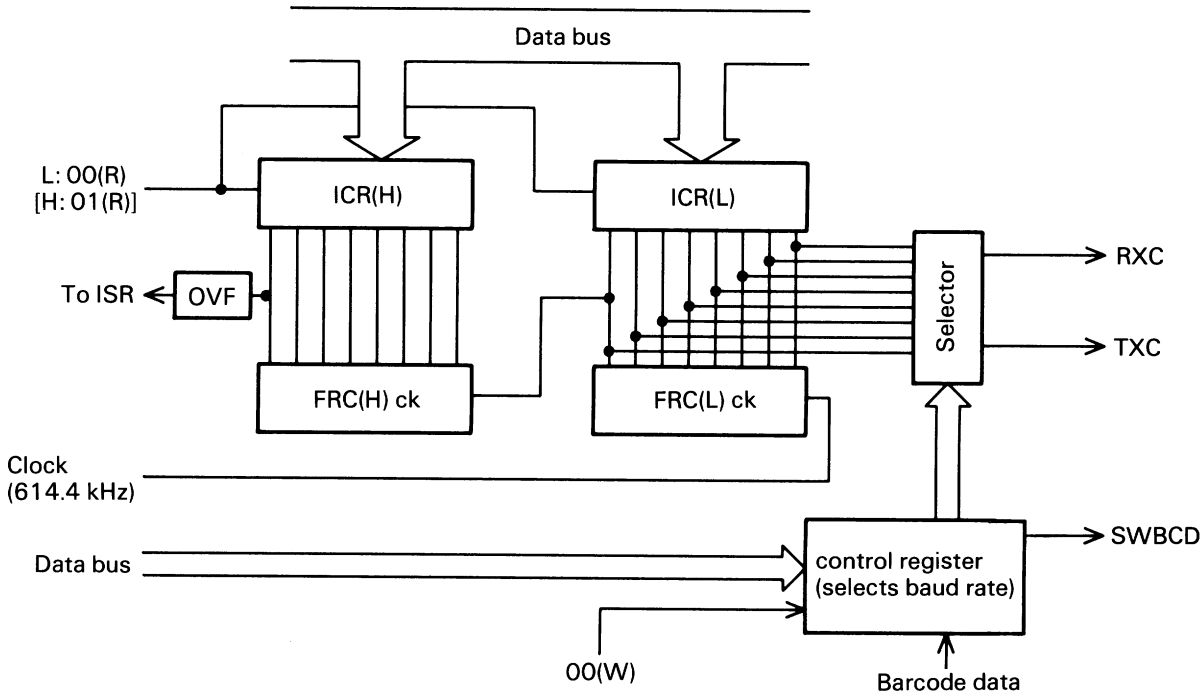


Fig. 7-8

When reading the content of FRC, it is necessary to latch the content to ICR (Input Capture Register) by reading address 00H. Because the counter consists of 16 bits, address 00H (low-order 8 bits) and 0IH (high-order 8 bits) must be read separately.

Bits 1 and 2, set to the control register, combined with input data cause a trigger signal from BRDT; this signal allows data going to ICR from FRC to be latched.

(4) 7508 interface

The 7508 interface contains the circuitry for handshaking between the parallel-serial converting register on the main CPU and 7508.

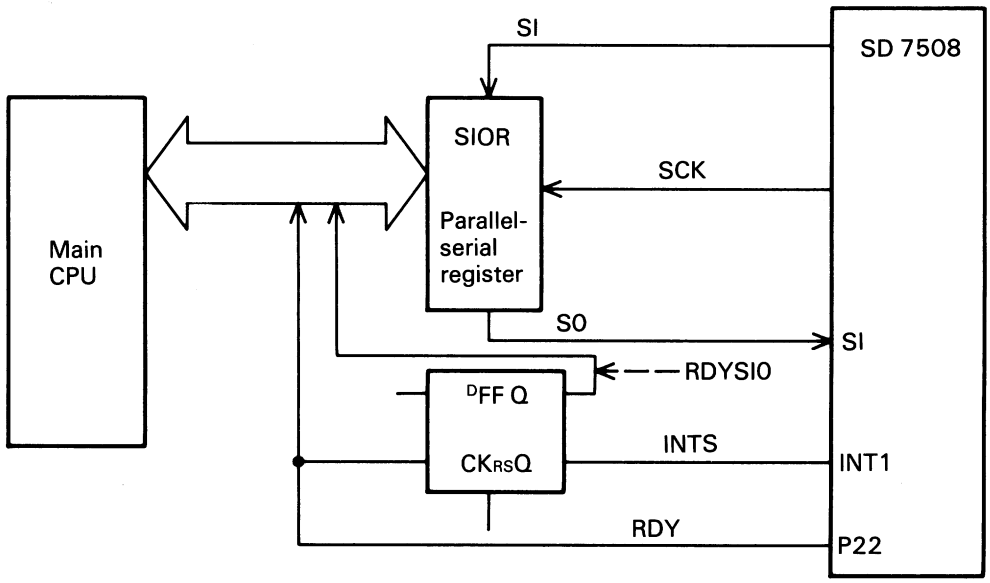


Fig. 7-9

Handshaking is performed in the internal flip-flop. When it is set, it means that the main CPU can access SIOR. When it is reset, it means that an interrupt signal is sent to the 7508 and the command set at SIOR is read by the 7508. The internal flip-flop is controlled by bits 0 and 1 of address 0IH.

After the R/W operation to/from SIOR is completed, the set status must be changed by writing to address 0IH.

Table 7-8

Address 0IH Bit 1	Reset RDYSI0	The main CPU sets a command to SIOR and requests processing to 7508.
Address 0IH Bit 0	Set RDYSI0	The power is turned on and access to 7508 is completed.

(5) I/O port

Power supply for the RS-232C, memory bank switching, and LED display on keyboard are controlled through the I/O port.

(RS-232C)

Fig. 7-10 controls power increases

The bits 3 and 4 of I/O address 02H.

±8V output is controled by the INHRS signal, and is performed in order to inhibit output voltage on the line during saturation time.

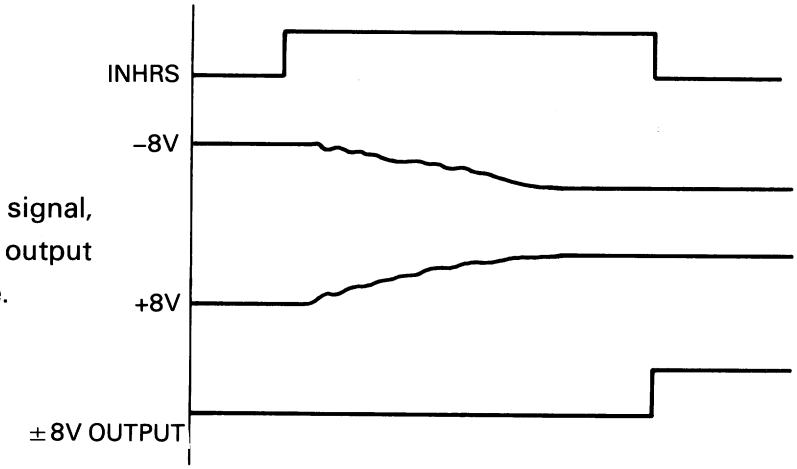


Fig. 7-10

(Bank switch)

The address space of the main CPU can be changed using bit 0 of I/O address 00H as shown below.

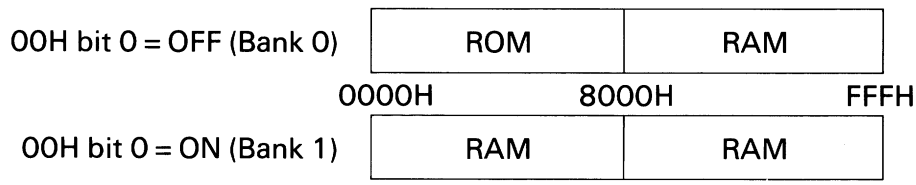


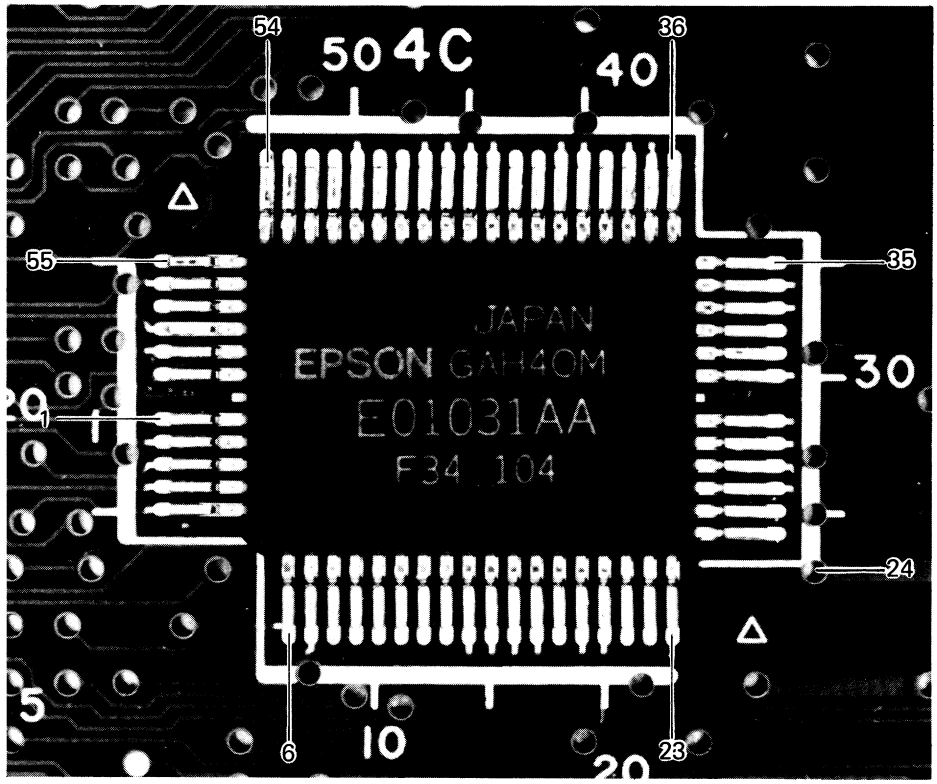
Fig. 7-11

(LED display)

ON/OFF operation of shift mode LED on the keyboard is controlled using bits 0 to 2 of address 02H. (Bit ON drives the corresponding LED.)

GAH40M

1. Location: MAPLE Board, 4C
2. Pin assignments



Note: Pins 25 and 59 are cut.

Table 7-9 GAH40M Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	DB6	In/Out	Data bus 6
2	DB1	In/Out	Data bus 1
3	$\overline{IR}$	Out	Indicates that data is being output according to main CPU instruction (RS-232C → main CPU).
4	DB 0	In/Out	Data bus 0
5	DB 2	In/Out	Data bus 2
6	$\overline{CSOE}$	Out	SED1320 chip select signal
7	$\overline{RS}$	In	Reset input: Supplied from GAH40D.
8	$\overline{IW}$	Out	Indicates that data is being input according to main CPU instruction (main CPU → RS-232C).
9	N/C	–	Not used.
10	TXC	Out	Baud rate control clock (for RS-232C).

Pin No.	Signal Name	In/Out	Function
11	$\overline{\text{INT0}}$	In	Sub-CPU 7508 interrupt signal
12	SWBCD	Out	Barcode power supply (+5V) switching signal
13	RXC	Out	Clock which controls receive character synchronization (RS-232C).
14	BCD	In	Bar code read data
15	CSIO	In	HIGH: Indicates that sub-CPU 7508 can access SIOR. LOW: Indicates that main CPU can read/write.
16	SI	In	Serial data input from sub-CPU 7508.
17	SO	Out	Serial data output to sub-CPU 7508.
18	$\overline{\text{S-INT}}$	Out	Interrupt signal to main CPU. Gives an interrupt via GAH40D ($\overline{\text{Z-INT}}$ signal).
19	DB 5	In/Out	Data bus 5
20	DB 3	In/Out	Data bus 3
21	N/C	–	Not used.
22	N/C	–	Not used.
23	N/C	–	Not used.
24	N/C	–	Not used.
25	N/C	–	Not used.
26	SWRS	Out	Switching signal for RS-232C power supply
27	INHRS	Out	Controls output voltage during power saturation time of RS-232C.
28	OFF	In	Power off. To prevent latch-up by isolating output in high impedance.
29	G	–	Ground
30	TEST	In	Test terminal. Normally kept low level.
31	N/C	–	Not used.
32	AUX	Out	RS-232C transmit/receive line control

Pin No.	Signal Name	In/Out	Function
33	$\overline{\text{INT 1}}$	In	Serial controller 82C51 interrupt signal
34	$\overline{\text{INT 5}}$	In	Interrupt signal from option unit
35	N/C	–	Not used.
36	SCK	In	Data transmit/receive shift clock against SIOR register. Provided from sub-CPU 7508.
37	$\overline{\text{INT 2}}$	In	RS-232C CD signal interrupt signal
38	$\overline{\text{RD}}$	In	Read signal: Synchronized to AND of IORQ. Outputs data on data bus.
39	AB 1	In	Address bus 1
40	$\overline{\text{WR}}$	In	Write signal: Synchronized to AND of IORQ. Outputs data on data bus.
41	INTS	Out	Interrupt signal to sub-CPU 7508
42	AB 0	In	Address bus 0
43	RDY	In	Ready signal of sub-CPU
44	LED 2	Out	Lamp control signal of LED on keyboard (lowest of the three)
45	AB 7	In	Address bus 7
46	LED 1	Out	Lamp control signal of LED on keyboard (highest of the three)
47	LED 0	Out	Lamp control signal of LED on keyboard (center of the three)
48	$\overline{\text{IORQ}}$	In	Main CPU in MI cycle: Request to output interrupt response vector on data bus.
49	AB 2	In	Address bus 2
50	$\overline{\text{CSOC}}$	Out	Serial controller 82C51 chip select signal.
51	$\overline{\text{BANK0/1}}$	Out	Bank select signal
52	$\overline{\text{M1}}$	In	Main CPU in machine cycle 1: Interrupt response vector is read to main CPU by AND operation with IORQ.
53	N/C	–	Not used.

Pin No.	Signal Name	In/Out	Function
54	N/C	–	Not used.
55	N/C	–	Not used.
56	DB 4	In/Out	Data bus 4
57	AB 7	In	Address bus 27
58	DB 7	In/Out	Data bus.
59	2.45	In	2.45 MHz clock on which timer and baud rate generator are based.
60	VC	–	Circuit voltage (+5V)

7.6 Gate Array GAH40S

Gate array GAH40S, which is controlled by the 6303 slave CPU, in turn controls the microcassette tape drive, LCD controller, and ROM capsule. It consists of three segments: an address decoder, a microcassette tape drive interface, and a P-ROM interface. Figs. 7-12 through 7-14 are functional block diagrams of these blocks.

(1) Address decoder block

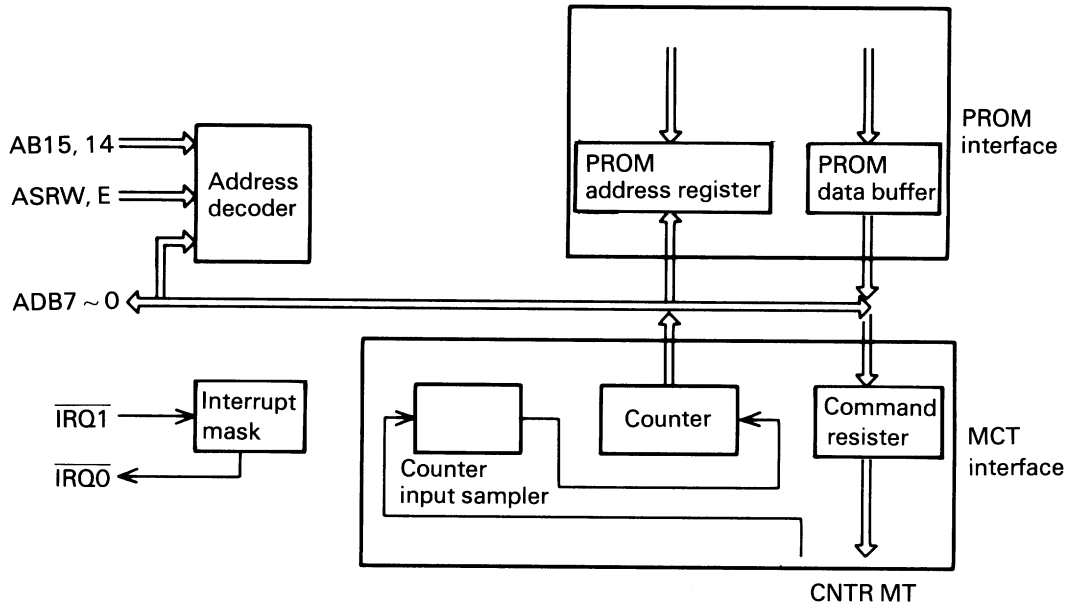


Fig. 7-12 Address decoder block diagram

(2) P-ROM interface block

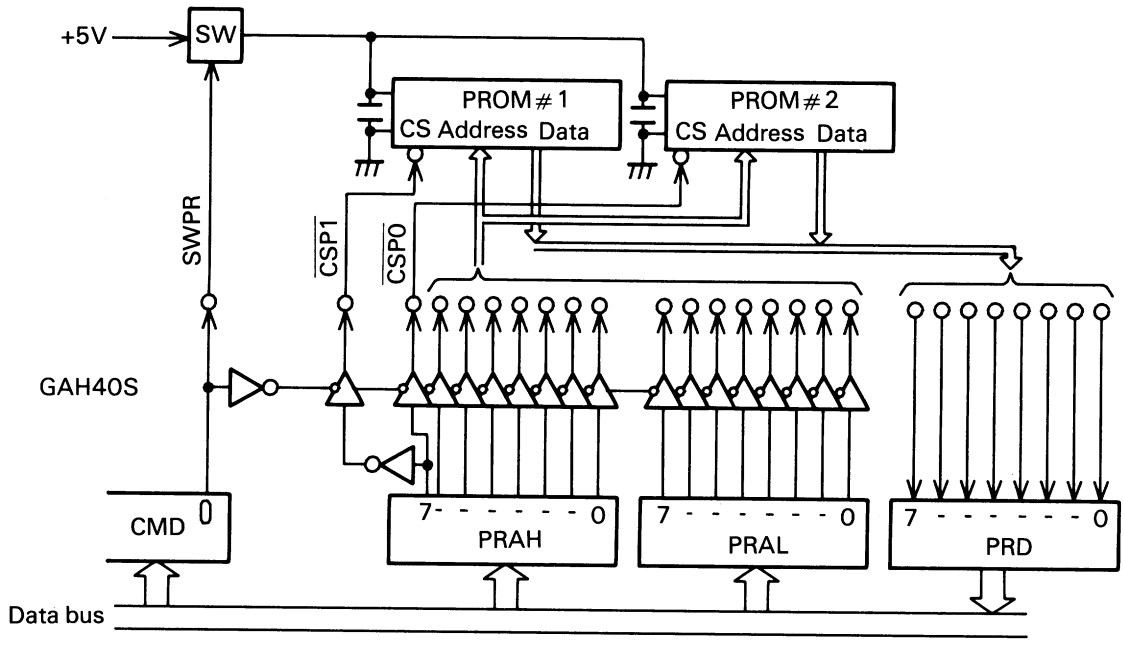


Fig. 7-13 P-ROM Interface Block Diagram

(3) Microcassette tape drive interface block

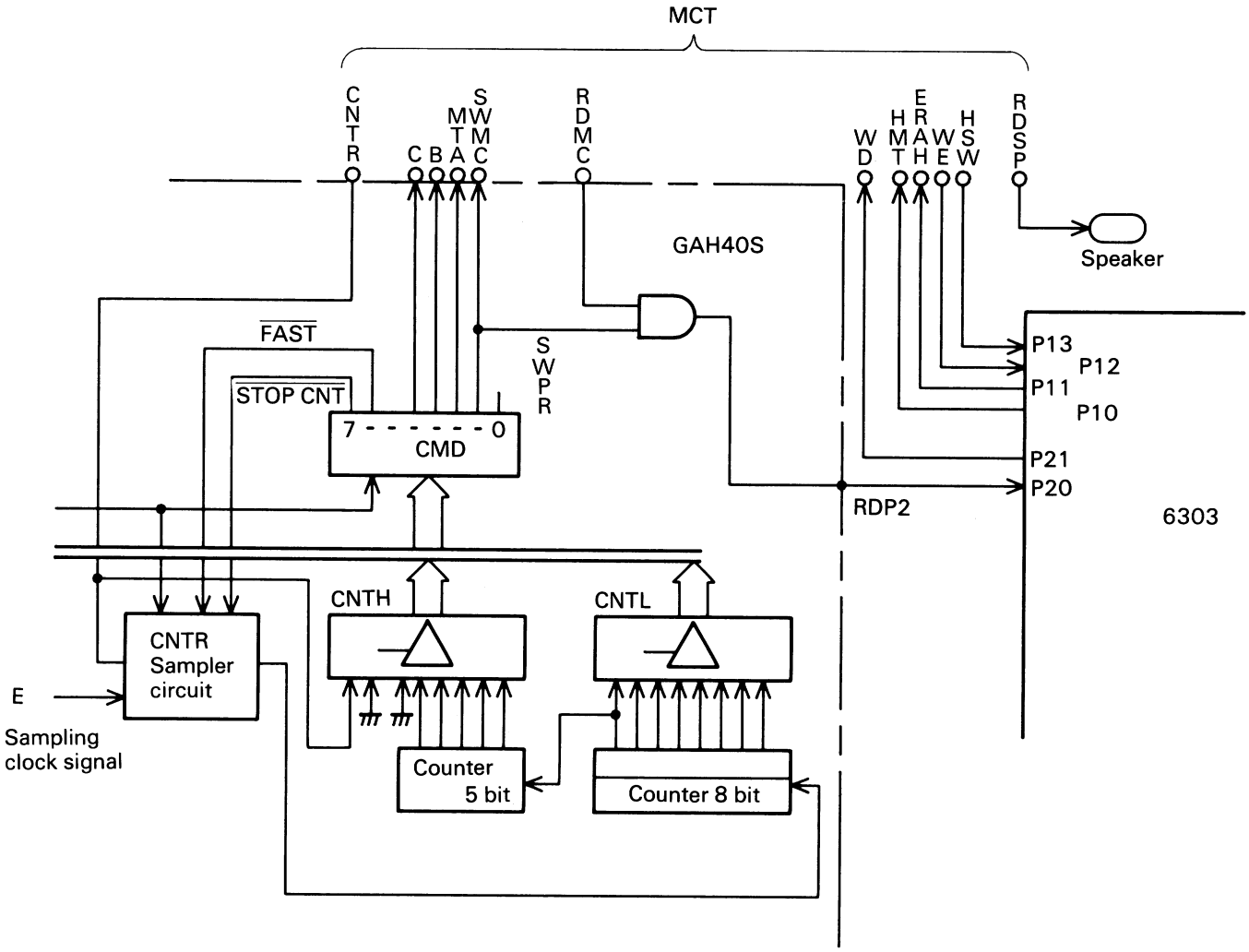
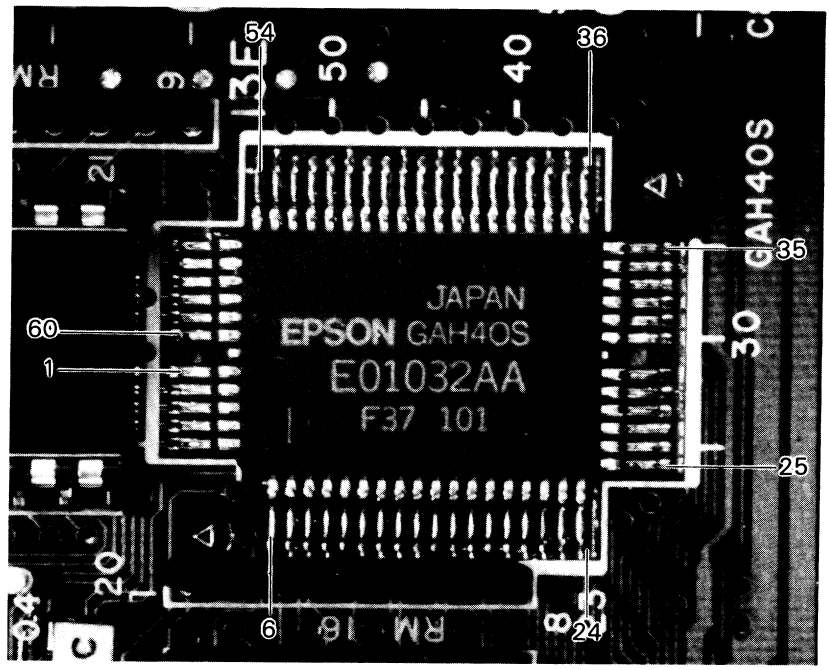


Fig. 7-14 Microcassette Tape Drive Interface Block Diagram

GAH40S

1. Location: MAPLE Board, 13E
2. Pin assignments



Note: Pins 25, 27 are cut.

Table 7-10 GAH40S Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	PRA 12	Out	PROM address 12
2	PRA 14	Out	PROM address 14
3	PRA 7	Out	PROM address 7
4	PRA 13	Out	PROM address 13
5	PRA 6	Out	PROM address 6
6	PRA 8	Out	PROM address 8
7	PRA 11	Out	PROM address 11
8	PRA 4	Out	PROM address 4
9	PRA 9	Out	PROM address 9
10	PRA 5	Out	PROM address 5
11	PRA 10	Out	PROM address 10
12	PRA 3	Out	PROM address 3
13	PRA 2	Out	PROM address 2

Pin No.	Signal Name	In/Out	Function
14	$\overline{\text{CSP 1}}$	Out	PROM chip select.
15	PRD 0	In	PROM data 0
16	$\overline{\text{CSP 0}}$	Out	Chip select
17	PRD 7	In	PROM data 7
18	PRA 1	Out	PROM address 1
19	PRA 0	Out	PROM address 0
20	PRD 6	In	PROM data 6
21	PRD 1	In	PROM data 1
22	PRD 4	In	PROM data 4
23	PRD 3	In	PROM data 3
24	PRD 2	In	PROM data 2
25	PRD 5	In	PRD data 5
26	MTDA	Out	Microcassette drive motor control signal A
27	MTDB	Out	Microcassette drive motor control signal B
28	MTDC	Out	Microcassette drive motor control signal C
29	G	–	Ground
30	N/C	–	Not used
31	SWMCT	Out	Microcassette power switch
32	CNTR	In	Counter signal from microcassette
33	RDMC	In	Microcassette read data
34	$\overline{\text{CSLV}}$	Out	SED1320 VRAM chip select signal. Low level when addresses 8000 to BFFF are specified.
35	N/C	–	Not used.
36	$\overline{\text{CSLC}}$	Out	SED1320 internal register select signal. Low level when addresses 0024 to 0027 are specified.
37	AB15	In	Slave CPU address 15
38	AB14	In	Slave CPU address 15
39	N/C	–	Not used.

Pin No.	Signal Name	In/Out	Function
40	N/C	–	Not used.
41	DA 0	In/Out	Slave CPU address data bus 0
42	DA 4	In/Out	Slave CPU address data bus 4
43	DA 5	In/Out	Slave CPU address data bus 5
44	DA 6	In/Out	Slave CPU address data bus 6
45	DA 1	In/Out	Slave CPU address data bus 1
46	DA 7	In/Out	Slave CPU address data bus 7
47	DA 3	In/Out	Slave CPU address data bus 3
48	DA 2	In/Out	Slave CPU address data bus 2
49	E	In	Enable signal from slave CPU 6303
50	N/C	–	Not used.
51	SWPR	Out	PROM power switch
52	TEST	–	Test terminal. Normally kept low.
53	R/$\overline{W}$	In	Read/write signal from slave CPU 6303
54	$\overline{SINT}$	In	Interrupt signal from SED 1320
55	AS	Out	Address strobe signal from slave CPU 6303
56	PRD	Out	AND output from RDMC input and SMMC. Outputs RDMC input to terminal when SWMC is high.
57	N/C	–	Not used.
58	RS	In	Reset signal
59	$\overline{IRQ0}$	Out	Interrupt request signal to slave CPU
60	VC	–	Circuit voltage (+5V)

7.7 A-D Converter μPD7001

The μPD7001 is an 8-bit, C-MOS serial output, analog-to-digital converter which incorporates a 4-channel analog input multiplexer. In this computer, the reference voltage is set to +2.0V, providing an effective resolution of the upper six bits. The LSB corresponds to approximately 0.03V. It employs a sequential comparison A-D conversion method, and requires a conversion time of 140μs.

The computer assigns the analog input channels for battery voltage sensing, temperature sensing, barcode data input, and external analog signal input. Fig. 7-15 is a functional block diagram and Fig. 7-16 outlines the timing relationships among the operating signals.

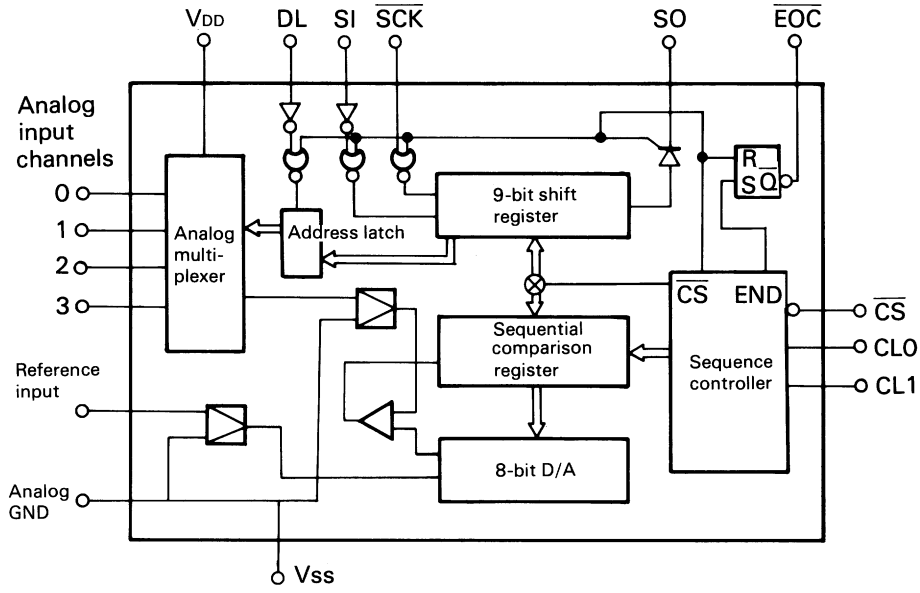


Fig. 7-15 A-D Converter μPD7001 Block Diagram

Timing chart

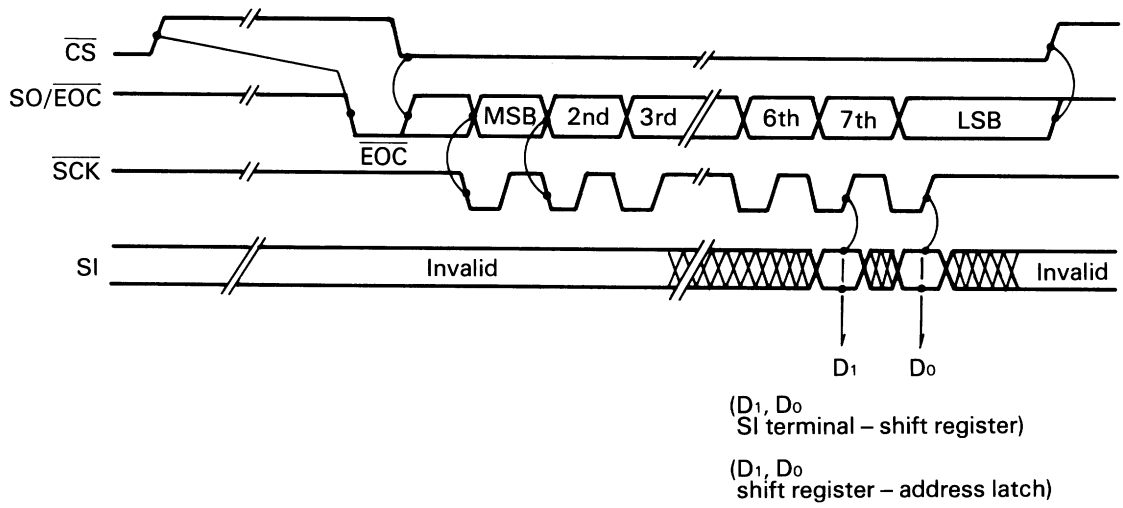


Fig. 7-16 A-D Converter Operation Timing Chart

μPD7001

1. Location: MAPLE Board, 1D
2. Pin Assignments

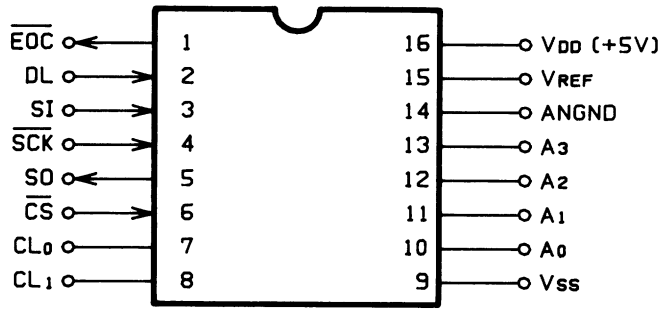


Table 7-11 μPD 7001 Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	End of Conversion ($\overline{EOC}$)	Open drain – output	High impedance while $\overline{CS}$ is low, returns low when A – D conversion ends.
2	Data Latch (DL)	In	Latches the multiplexer address in the shift register at its falling edge.
3	Serial Input (SI)	In	Terminal which provides multiplexer address to be read to the shift register. The serial input data is read at the rising edge of the $\overline{SCK}$ signal.
4	Serial Clock ($\overline{SCK}$)	In	Controls the shift operation of the 9-bit interface shift register.
6	Chip Select ($\overline{CS}$)	In	Controls μPD7001's internal modes. When $\overline{CS}$ is high: A-D conversion mode When $\overline{CS}$ is low : Interface mode – DL, SI, $\overline{SCK}$, and SO, etc. have been strobed with $\overline{CS}$. All the terminals are disabled while $\overline{CS}$ is high.
7	Clock (CL_0)	For connection of clock oscillation CR	
8	Clock (CL_1)	For connection of clock oscillation CR	
9	— (Vss)	Externally connect to the GND and analogue GND terminals	
10 ~ 13	Analogue input ($A_0 \sim A_3$)	Analogue input pin	
14	Analogue (GND)	Ground pin for analogue input and reference input	
15	Reference input (V_{REF})	Used for full scale voltage setting. Supply voltage of about +2.5V.	
16	Power supply (Vcc)	Power supply pin (+5V)	

7.8 Serial Controller 82C51

The 82C51 controls serial data transfers between the RS-232C interface and the option unit. Its operation modes vary speed of tronsfer, parity, and character length, etc., modes are controlled by a control word which is written in the 82C51 by the main CPU. Data are transferred one byte at a time. The transmit and receive clock signals are supplied from the gate array GAH40M. Figure 7-17 is a block diagram illustrating 82C51 signal flow to and from external connectors.

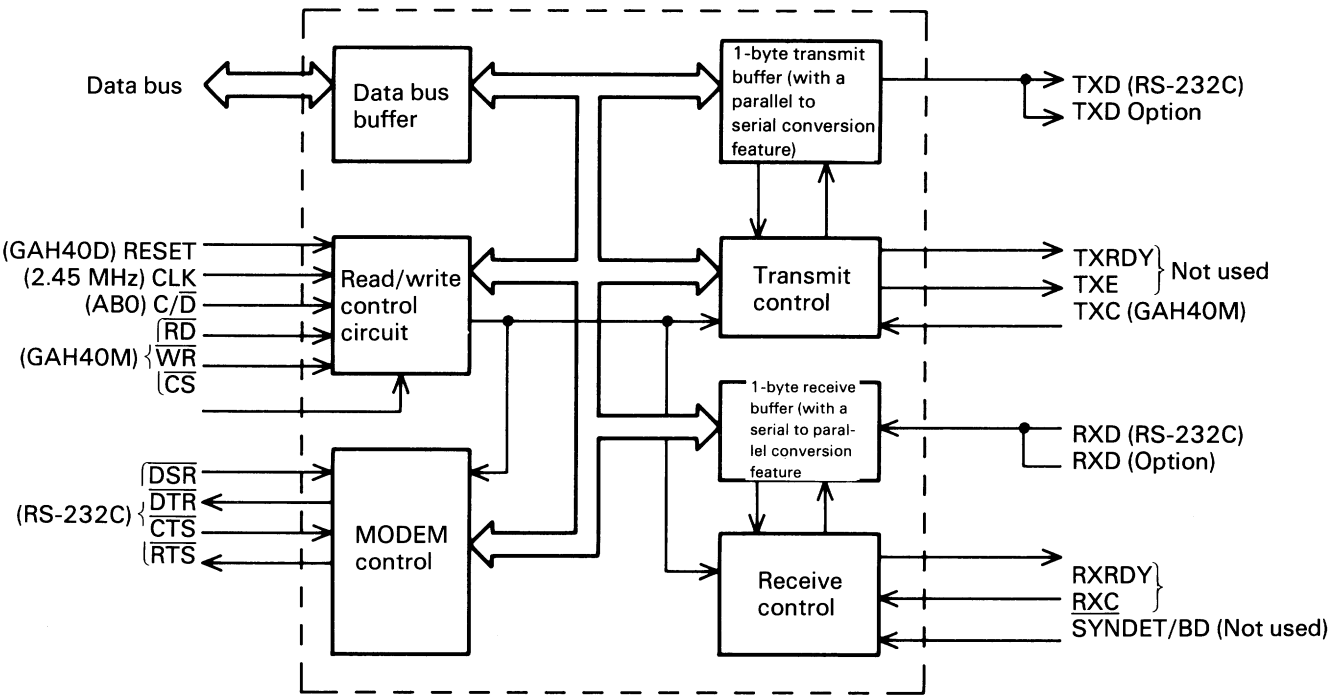


Fig. 7-17 82C51 Serial Controller Block Diagram

The signals to the RS-232C interface are converted to the ±8V (RS-232C) levels between 82C51 and the interface. The Carrier Detect (CD) signal, which is not included in the above block diagram, is connected to the interrupt port of GAH40M to interrupt the main CPU.

The 82C51 itself can support both synchronous mode (BI-SYNC) and asynchronous mode (Start-Stop system: includes start/stop bits); however, in this CPU, TXE and SYNDET/BD are not connected for SYNC character control signals.
When an asynchronous system is used, processing on the SYNC character, etc. needs to be supported by the application software.

The 82C51 cannot simultaneously process transmit/receive data to and from the RS-232C interface and option unit. Thus, the GAH40M AUX signal is provided to allow an external control for enabling and disabling the RS-232C transmit/receive lines.

82C51

1. Location: MAPLE Board, 13E

   This is a serial interface, CPU-programmable, USART chip which can provide full-duplex communications.

3. Pin Assignments

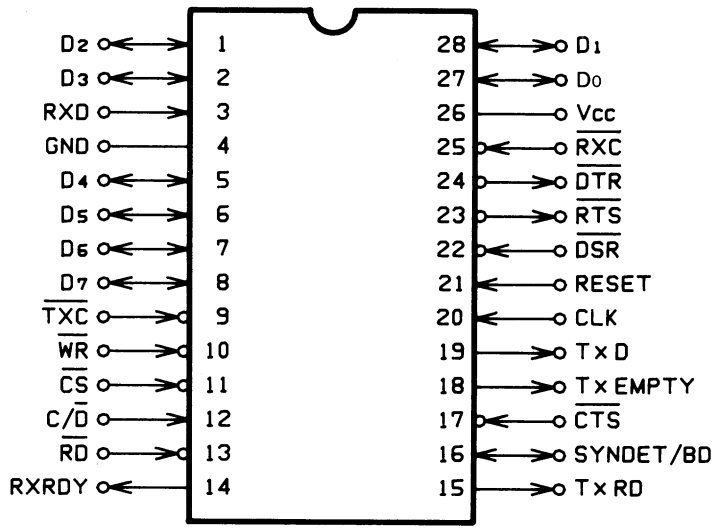


Table 7-12 82C51 Pin Assignments

Pin No.	Signal Name	Signal direction	Meaning
1	D2	In/Out	Data bus 2
2	D3	In/Out	Data bus 3
3	RXD	In	Receive data (from RS-232C interface or optionl unit)
4	GND	–	Circuit ground
5	D4	In/Out	Data bus 4
6	D5	In/Out	Data bus 5
7	D6	In/Out	Data bus 6
8	D7	In/Out	Data bus 7
9	$\overline{TXC}$	In/Out	Data bus 7
10	$\overline{WR}$	In	Transmitter clock
11	$\overline{CS}$	In	Chip select
12	$\overline{CD}$	In	Command/data
13	$\overline{RD}$	In	Read signal (from 82C51 to data bus)

Pin No.	Signal Name	Signal Direction	Meaning
14	RX RDY	Out	This is a CPU-programmable USART chip which is a serial interface, capable of providing full-duplex communications.
15	N/C	–	Not used.
16	N/C	–	Not used.
17	$\overline{CTS}$	In	Clear to send
18	N/C	–	Not used.
19	TXD	Out	Transmit data
20	CLK	In	2.45M Hz clock
21	RS	In	Reset
22	$\overline{DSR}$	In	Data set ready
23	$\overline{RTS}$	Out	Request to send
24	$\overline{DTR}$	Out	Data terminal ready
25	$\overline{RXC}$	In	Receiver clock
26	VC	In	Circuit voltage (+5V)
27	D0		Data 0
28	D1		Data 1

7.9 SED1120 (LCD Driver)

SED1120 is the X driver of the LCD. It converts serially transmitted data to parallel data in 4-bit units and outputs drive signals to 64 segments. The internal diagram is shown in Fig. 7-18. The drive level voltage may vary according to data received via DINs 0 to 3.

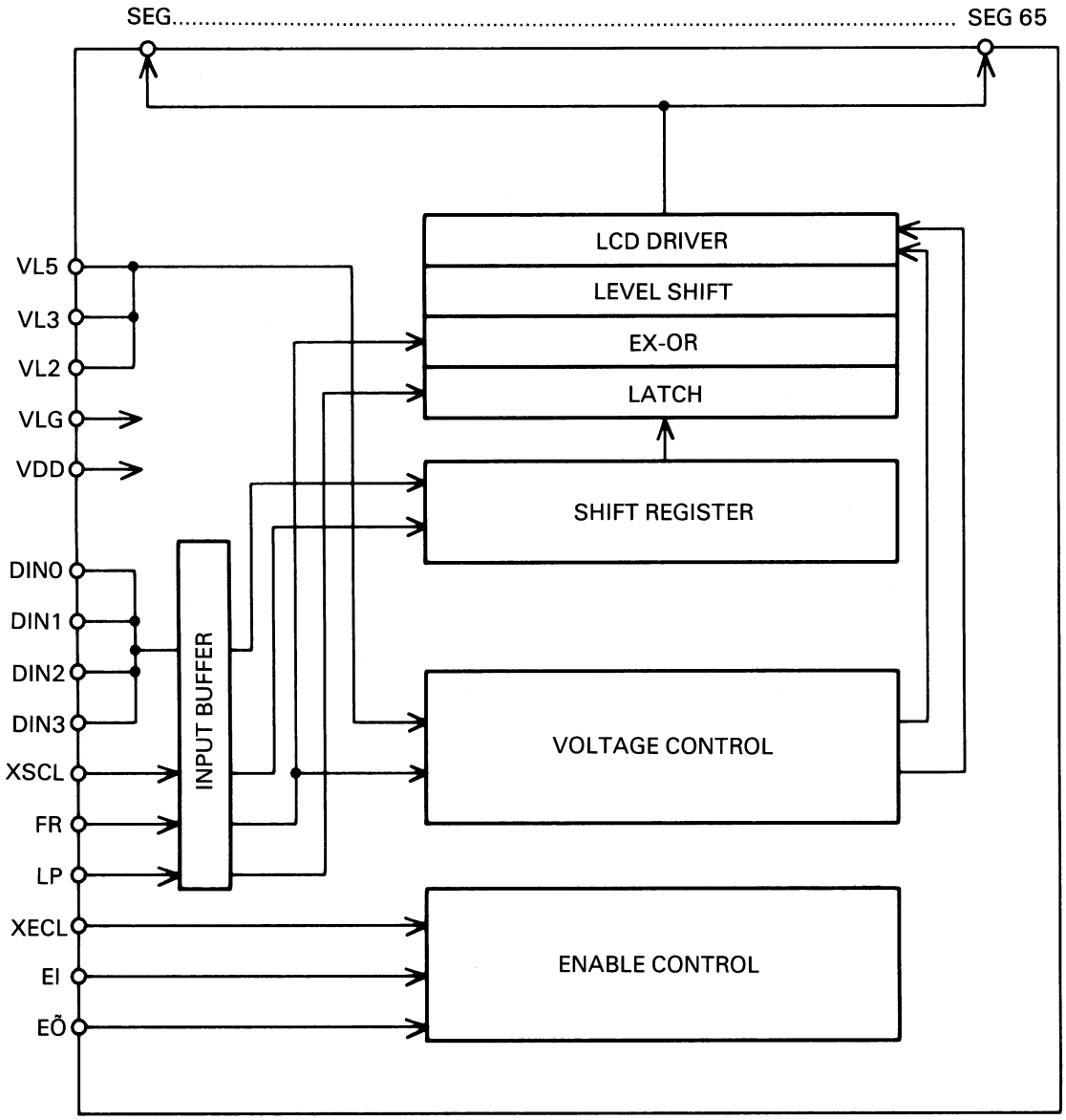


Fig. 7-18

SED1120

1. Location: LCD Board, X1 – X8
2. Pin Assignments
3. Pin Assignments

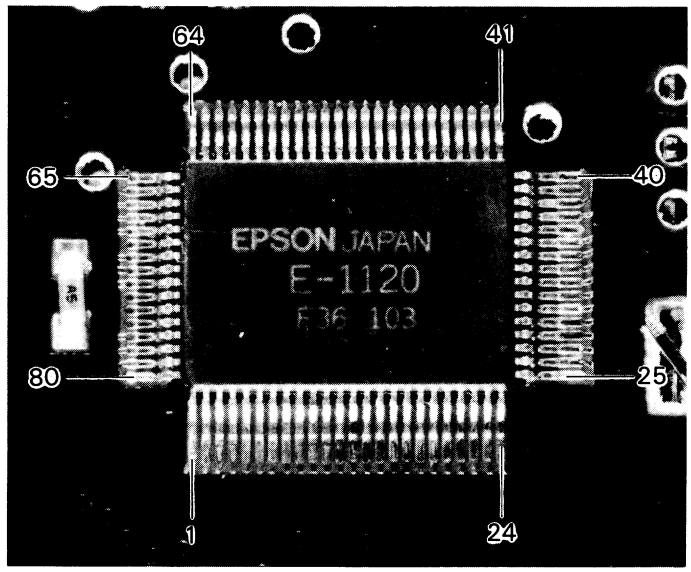


Table 7-13 SED1120 Assignments

Pin No.	Signal Name	In/Out	Function
1	S27	Out	LCD drive segment output 27
2	S26	Out	LCD drive segment output 26
3	S25	Out	LCD drive segment output 25
4	S24	Out	LCD drive segment output 24
5	S23	Out	LCD drive segment output 23
6	S22	Out	LCD drive segment output 22
7	S21	Out	LCD drive segment output 21
8	S20	Out	LCD drive segment output 20
9	S19	Out	LCD drive segment output 19
10	S18	Out	LCD drive segment output 18
11	S17	Out	LCD drive segment output 17
12	S16	Out	LCD drive segment output 16
13	S15	Out	LCD drive segment output 15

Pin No.	Signal Name	In/Out	Function
14	S14	Out	LCD drive segment output 14
15	S13	Out	LCD drive segment output 13
16	S12	Out	LCD drive segment output 12
17	S11	Out	LCD drive segment output 11
18	S10	Out	LCD drive segment output 10
19	S9	Out	LCD drive segment output 9
20	S8	Out	LCD drive segment output 8
21	S7	Out	LCD drive segment output 7
22	S6	Out	LCD drive segment output 6
23	S5	Out	LCD drive segment output 5
24	S4	Out	LCD drive segment output 4
25	S3	Out	LCD drive segment output 3
26	S2	Out	LCD drive segment output 2
27	S1	Out	LCD drive segment output 1
28	S0	Out	LCD drive segment output 0
29	E0	–	Not used.
30	D3	In	Serial data 3
31	D2	In	Serial data 2
32	D1	In	Serial data 1
33	D0	In	Serial data 0
34	XSCL	In	Transmission clock signal input terminal
35	LP	Latch pulse	
36	FR	Frame signal	
37	S32	Out	LCD drive segment output 32
38	S33	Out	LCD drive segment output 33
39	S34	Out	LCD drive segment output 34
40	S35	Out	LCD drive segment output 35
41	S36	Out	LCD drive segment output 36

Pin No.	Signal Name	In/Out	Function
42	S37	Out	LCD drive segment output 37
43	S38	Out	LCD drive segment output 38
44	S39	Out	LCD drive segment output 39
45	S40	Out	LCD drive segment output 40
46	S41	Out	LCD drive segment output 41
47	S42	Out	LCD drive segment output 42
48	S43	Out	LCD drive segment output 43
49	S44	Out	LCD drive segment output 44
50	S45	Out	LCD drive segment output 45
51	S46	Out	LCD drive segment output 46
52	S47	Out	LCD drive segment output 47
53	S48	Out	LCD drive segment output 48
54	S49	Out	LCD drive segment output 49
55	S50	Out	LCD drive segment output 50
56	S51	Out	LCD drive segment output 51
57	S52	Out	LCD drive segment output 52
58	S53	Out	LCD drive segment output 53
59	S54	Out	LCD drive segment output 54
60	S55	Out	LCD drive segment output 55
61	S56	Out	LCD drive segment output 56
62	S57	Out	LCD drive segment output 57
63	S58	Out	LCD drive segment output 58
64	S59	Out	LCD drive segment output 59
65	S60	Out	LCD drive segment output 60
66	S61	Out	LCD drive segment output 61
67	S62	Out	LCD drive segment output 62
68	S63	Out	LCD drive segment output 63
69	VL5	In	LCD drive voltage

Pin No.	Signal Name	In/Out	Function
70	VL2	IN	LCD drive voltage
71	VL3	In	LCD drive voltage
72	VLG	In	Ground
73	VDD	In	+5V (Logic circuit voltage supply)
74	TEST	–	Unused.
75	E 1	In	Enable input (corresponding to Chip Select)
76	XECL	In	Enable transfer clock signal
77	S31	In	LCD drive segment output 31
78	S30	In	LCD drive segment output 30
79	S29	In	LCD drive segment output 29
80	S28	In	LCD drive segment output 28

7.10 SED1130

SED1130 is a Y-driver of the LCD display. It converts transferred data from serial to parallel, and provides drive signals for the 64 horizontal lines.

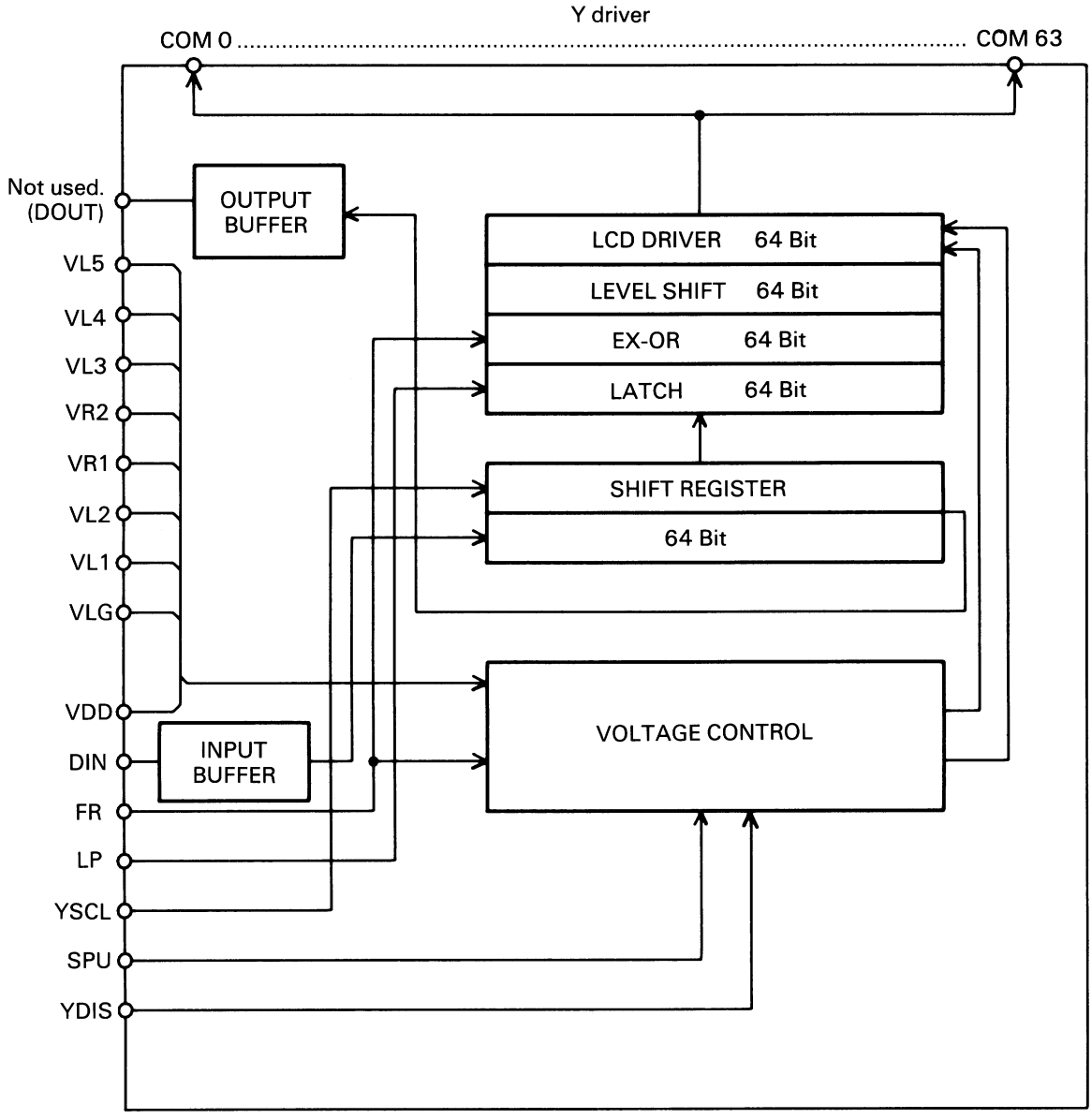


Fig. 7-19

On Y drive lines, data transferred in serial is included in the shift register bit by bit according to YSCL signals (shift clock). Then, Y drive signals corresponding to these data are output. Data transfer timing is shown in Fig. 7-20.

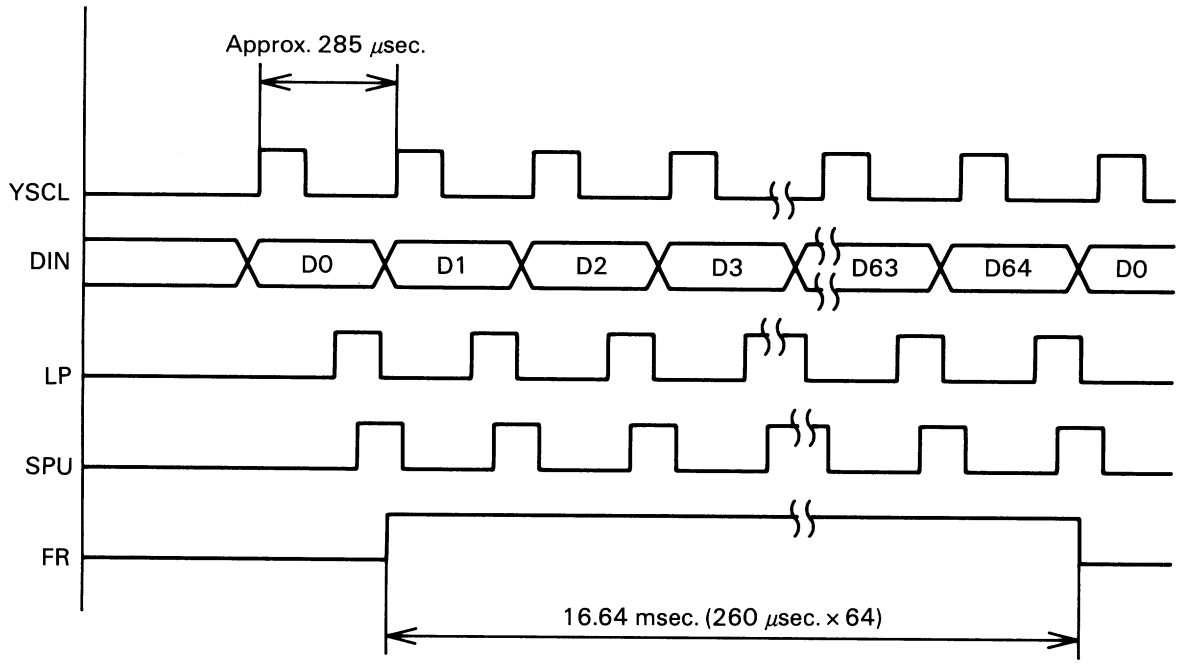


Fig. 7-20

When a YSCL signal is output, DIN is included in the internal shift register, an LP signal latches the content of the shift register, and the latched data is output on the Y drive line.

SED1130

1. Location: MAPLE Board, Y1
2. Pin Assignments

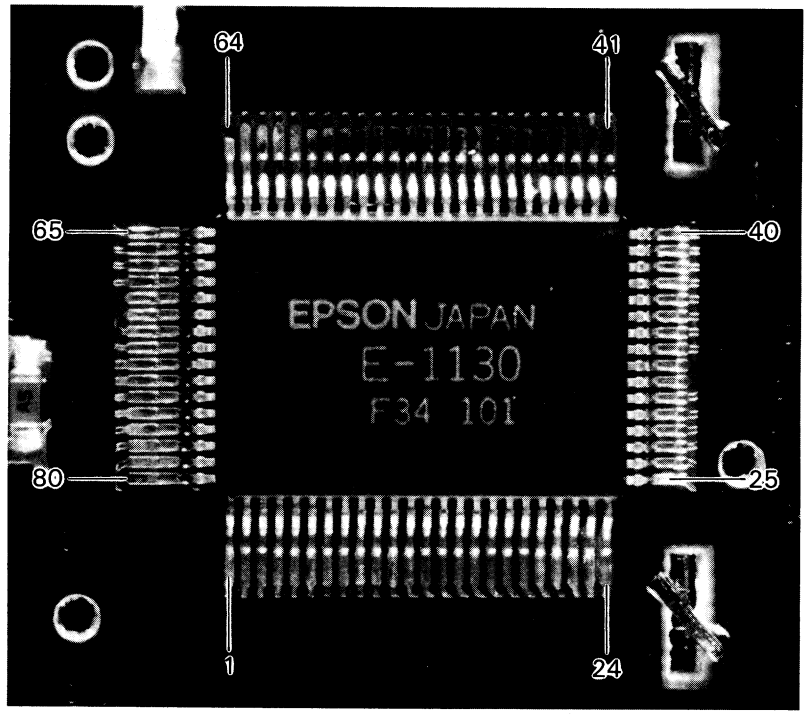


Table 7-14 SED1130 Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	COM 31	Out	LCD drive common output 31
2	COM 30	Out	LCD drive common output 30
3	COM 29	Out	LCD drive common output 29
4	COM 28	Out	LCD drive common output 28
5	COM 27	Out	LCD drive common output 27
6	COM 26	Out	LCD drive common output 26
7	COM 25	Out	LCD drive common output 25
8	COM 24	Out	LCD drive common output 24
9	COM 23	Out	LCD drive common output 23
10	COM 22	Out	LCD drive common output 22
11	COM 21	Out	LCD drive common output 21
12	COM 20	Out	LCD drive common output 20
13	COM 19	Out	LCD drive common output 19

Pin No.	Signal Name	In/Out	Function
14	COM 18	Out	LCD drive common output 18
15	COM 17	Out	LCD drive common output 17
16	COM 16	Out	LCD drive common output 16
17	COM 15	Out	LCD drive common output 15
18	COM 14	Out	LCD drive common output 14
19	COM 13	Out	LCD drive common output 13
20	COM 12	Out	LCD drive common output 12
21	COM 11	Out	LCD drive common output 11
22	COM 10	Out	LCD drive common output 10
23	COM 9	Out	LCD drive common output 9
24	COM 8	Out	LCD drive common output 8
25	COM 7	Out	LCD drive common output 7
26	COM 6	Out	LCD drive common output 6
27	COM 5	Out	LCD drive common output 5
28	COM 4	Out	LCD drive common output 4
29	COM 3	Out	LCD drive common output 3
30	COM 2	Out	LCD drive common output 2
31	COM 1	Out	LCD drive common output 1
32	COM 0	Out	LCD drive common output 0
33	COM 32	Out	LCD drive common output 32
34	COM 33	Out	LCD drive common output 33
35	COM 34	Out	LCD drive common output 34
36	COM 35	Out	LCD drive common output 35
37	COM 36	Out	LCD drive common output 36
38	COM 37	Out	LCD drive common output 37
39	COM 38	Out	LCD drive common output 38
40	COM 39	Out	LCD drive common output 39
41	COM 40	Out	LCD drive common output 40

Pin No.	Signal Name	In/Out	Function
42	COM 41	Out	LCD drive common output 41
43	COM 42	Out	LCD drive common output 42
44	COM 43	Out	LCD drive common output 43
45	COM 44	Out	LCD drive common output 44
46	COM 45	Out	LCD drive common output 45
47	COM 46	Out	LCD drive common output 46
48	COM 47	Out	LCD drive common output 47
49	COM 48	Out	LCD drive common output 48
50	COM 49	Out	LCD drive common output 49
51	COM 50	Out	LCD drive common output 50
52	COM 51	OUT	LCD drive common output 51
53	COM 52	OUT	LCD drive common output 52
54	COM 53	Out	LCD drive common output 53
55	COM 54	Out	LCD drive common output 54
56	COM 55	Out	LCD drive common output 55
57	COM 56	Out	LCD drive common output 56
58	COM 57	Out	LCD drive common output 57
59	COM 58	Out	LCD drive common output 58
60	COM 59	Out	LCD drive common output 59
61	COM 60	Out	LCD drive common output 60
62	COM 61	Out	LCD drive common output 61
63	COM 62	Out	LCD drive common output 62
64	COM 63	Out	LCD drive common output 63
65	D Out	–	Unused
66	VL5	In	LCD drive voltage
67	VL4	In	LCD drive voltage
68	VL3	In	LCD drive voltage
69	VR1	In	LCD drive voltage

Pin No.	Signal Name	In/Out	Function
70	VR2	In	LCD drive voltage
71	VL2	In	LCD drive voltage
72	VL1	In	LCD drive voltage
73	VLG	In	Ground
74	VDD	In	+5V (Logic circuit voltage supply)
75	YSPU	In	Low impedance drive input – Normally high. When low, the externally connected resistor parallels the internal impedance, lowering the total impedance through which the line can be driven at the divided LCD voltages (VL1 – 5).
76	YDIN	In	Serial data input
77	YSCL	In	Transmission clock input
78	YDIS	In	Display control input
79	FR	In	Frame signal
80	LP	In	Latch pulse

7.11 LCD/V-RAM Controller SED1320

The gate array is the LCD driver controller which displays the LCD panel using a 6kB external V-RAM. It also provides the interface between the main and slave CPUs and the character generation capability for LCD display. Fig. 7-21 is a functional block diagram of SED1320.

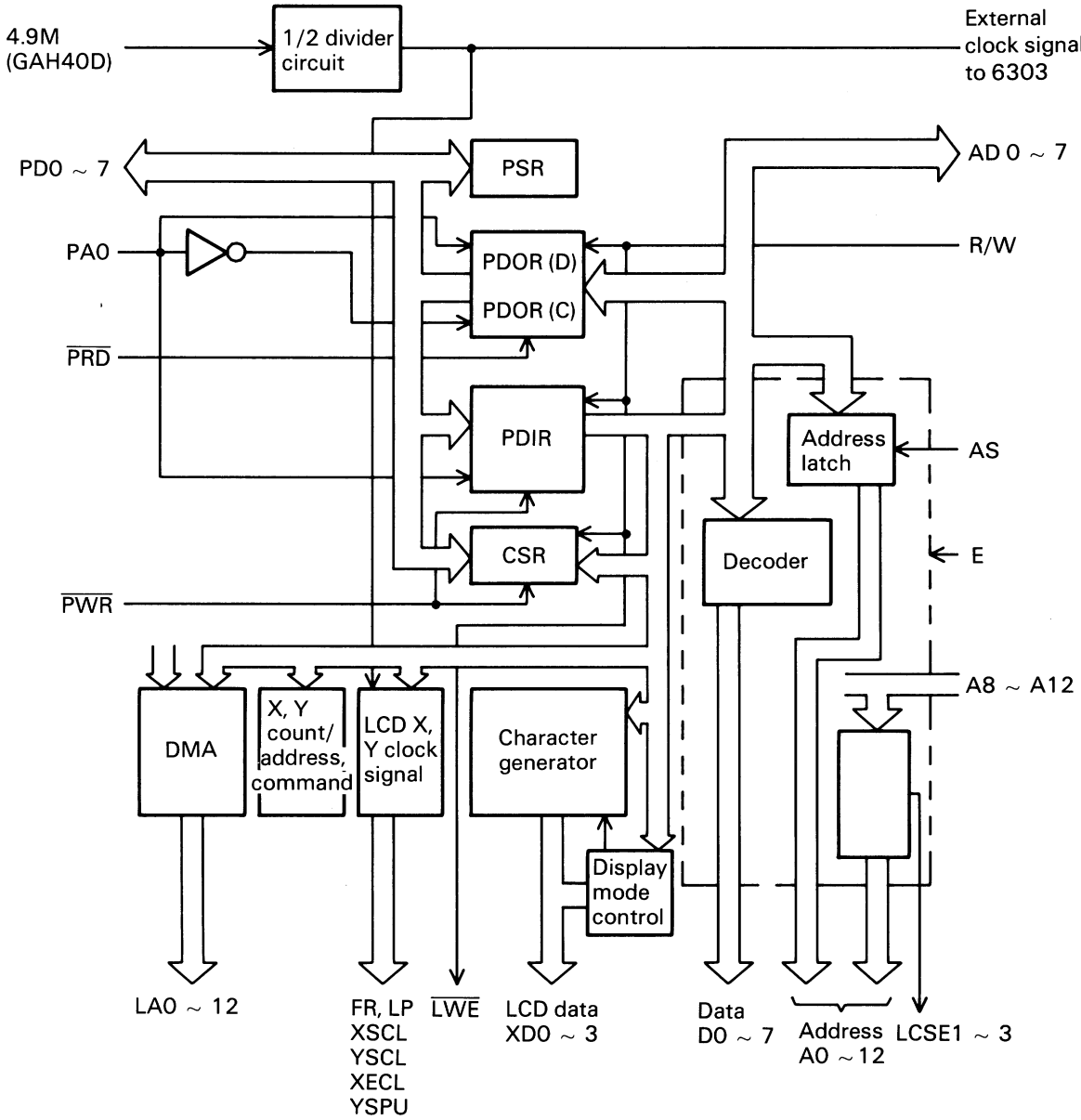


Fig. 7-21 SED1320 Gate Array Functional Block Diagram

7.11.1 LCD/V-RAM Control

This gate array incorporates registers for controlling the screen pointer, etc. as well as a 1/2 clock frequency divider which generates the LCD clock signal from the 4.9 MHz input clock signal. The screen control is accomplished by a procedure in which the slave CPU 6303 sends commands/ data to SED1320; the SED1320 responds with one-byte return codes.

V-RAM read/write is accomplished by the slave CPU. Data transfer to the LCD drivers is made via the DMA controller incorporated in the SED1320.

Displayed text character fonts are generated by the incorporated character generator. The used character set is determined by the DIP SW4 setting which any one of the international character sets. The switch is read at initialization.

7.11.2 Communications Between Main And Slave CPUs

When the main CPU sends a command or data to the PDIR register, the $\overline{\text{SINT}}$ signal interrupts the slave CPU via the gate array GAH40S ($\overline{\text{INTR}}$ signal). The slave CPU reads the command/data by setting the interrupt mask register in GAH40S. When data is transferred from the slave to the main CPU, the slave CPU deposits the data to the PDOR register which is read by an I/O read from the main CPU. In either direction of transfer, a handshake can be established between the two CPUs in which the CPUs can examine the state of the port data register PDIR/PDOR through a port status change or register (PSR) and control status register (CSR).

SED1320

1. Location: MAPLE Board, 7C
2. Pin Assignments

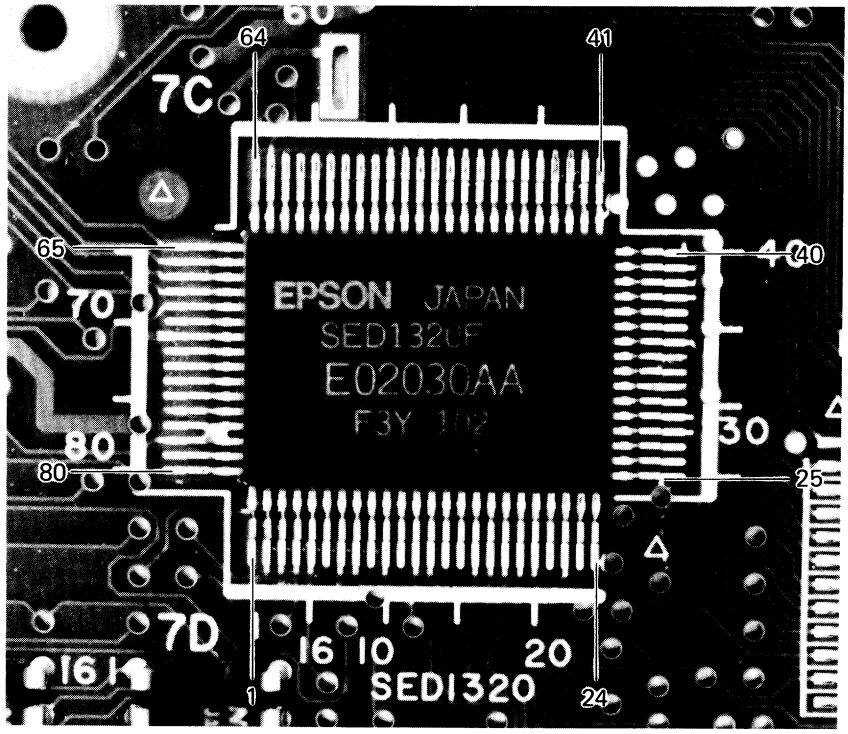


Table 7-15 SED1120 Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	RS	In	System reset signal: provided from GAH40D; initializes internal registers.
2	$\overline{\text{SINT}}$	Out	System interrupt request: causes an interrupt to slave CPU 6303 via GAH40S. $\overline{\text{SINT}}$ becomes low when command is set in PDIR register by main CPU. $\overline{\text{SINT}}$ becomes high when the slave CPU reads CSR register.
3	$\overline{\text{SCS}}$	In	System chip select and V-RAM select signal
4	$\overline{\text{SCS1}}$	In	System chip select: Register select signal in SED1320.
5	SE	In	System enable: Pulse at 1.63 μsec interval
6	SAS	In	System address strobe: Latches low-order address at power fall.
7	R/$\overline{\text{W}}$	In	System read/write signal

Pin No.	Signal Name	In/Out	Function
8	SAD 0	In/Out	System (slave CPU 6303) address data bus 0: Data is input/output synchronizing to SE signals.
9	SAD 1	In/Out	System (slave CPU 6303) address data bus 1: Data is input/output synchronizing to SE signals. Pins 10 – 14 missing
15	SAD 7	In/Out	System (slave CPU 6303) address data bus 7: Data is input/output synchronizing to SE signals.
16	SA 8	In	System (slave CPU 6303) address data bus 8: Data is input/output synchronizing to SE signals.
17	SA 9	In	System (slave CPU 6303) address data bus 9: Data is input/output synchronizing to SE signals.
18	SA 10	In	System (slave CPU 6303) address data bus 10: Data is input/output synchronizing to SE signals.
19	SA 11	In	System (slave CPU 6303) address data bus 11: Data is input/output synchronizing to SE signals.
20	SA 12	In	System (slave CPU 6303) address data bus 12: Data is input/output synchronizing to SE signals.
21	N/C	–	Not used.
22	$\overline{\text{PCS}}$	In	Port chip select: Provided from GAH40H
23	$\overline{\text{PWR}}$	In	Port write (write port data 0 to 7): Provided from GAH40M.
24	PR D	In	Port read (read port data 0 to 7): Provided from GAH40M.
25	PA 0	In	Port address 0 (address 0 of main CPU): Selects port register.
26	PD 0	In/Out	Port data (data bus of main CPU) 0
27	PD 1	In/Out	Port data (data bus of main CPU) 1
28	PD 2	In/Out	Port data (data bus of main CPU) 2

Pin No.	Signal Name	In/Out	Function
29	PD 3	In/Out	Port data (data bus of main CPU) 3
30	PD 4	In/Out	Port data (data bus of main CPU) 4
31	PD 5	In/Out	Port data (data bus of main CPU) 5
32	PD 6	In/Out	Port data (data bus of main CPU) 6
33	PD 7	In/Out	Port data (data bus of main CPU) 7
34	LD 0	In/Out	Local data (for V-RAM) 0
35	LD 1	In/Out	Local data (for V-RAM) 1
36	LD 2	In/Out	Local data (for V-RAM) 2
37	LD 3	In/Out	Local data (for V-RAM) 3
38	LD 4	In/Out	Local data (for V-RAM) 4
39	LD 5	In/Out	Local data (for V-RAM) 5
40	LD 6	In/Out	Local data (for V-RAM) 6
41	LD 7	In/Out	Local data (for V-RAM) 7
42	LA 0	Out	Local address (for V-RAM) 0
43	LA 1	Out	Local address (for V-RAM) 1
44	LA 2	Out	Local address (for V-RAM) 2
45	LA 3	Out	Local address (for V-RAM) 3
46	LA 4	Out	Local address (for V-RAM) 4
47	LA 5	Out	Local address (for V-RAM) 5
48	LA 6	Out	Local address (for V-RAM) 6
49	LA 7	Out	Local address (for V-RAM) 7
50	LA 8	Out	Local address (for V-RAM) 8
51	LA 9	Out	Local address (for V-RAM) 9
52	LA 10	Out	Local address (for V-RAM) 10
53	LCSE 1	Out	Local chip select 1 (V-RAM 11C)
54	LCSE 2	Out	Local chip select 2 (V-RAM 10C)
55	LCSE 3	Out	Local chip select 3 (V-RAM 9C)
56	N/C	–	Not used.

Pin No.	Signal Name	In/Out	Function
57	N/C	–	Not used.
58	LWE	Out	Local read/write signal: Read/write signals for V-RAM. Low level gives write signal.
59	YSPU	Out	Y speed up signal: LP signal with timing shifted by a half cycle. Output at an interval of approx. 280 μsec. Has an on-time of approx. 10μ.
60	YDO 0	Out	Y data: Y line data for LCD display
61	YSCL	Out	Y shift clock: Shifts Y data to falling edge of clock to be shifted. Output at an interval of approx. 280 μsec.
62	YDIS	Out	Y display: Displayed on LCD when HIGH.
63	FR	Out	Frame signal: Connected to XY driver.
64	LP	Out	Latch pulse signal: Connected to XY driver. Latches data at falling edge. Output at an interval of approx. 280 μsec.
65	XSCL	Out	X shift clock: Shifts X data
66	XD 0	Out	X data 0: X line data for LCD display.
67	XD 1	Out	X data 1: X line data for LCD display.
68	XD 2	Out	X data 2: X line data for LCD display.
69	XD 3	Out	X data 3: X line data for LCD display.
70	XECL	Out	X enable clock. Output 8 pulses at an interval of approx. 280 μsec.
71	VC	–	Circuit voltage (+5V)
72	N/C	–	Not used.
73	LOSC	In	Local clock (4.8 MHz)
74	N/C	–	Not used.
75	G	–	Circuit ground

Pin No.	Signal Name	In/Out	Function
76	LCK 0	Out	Local clock 0: External clock for slave CPU 6303. 2.45 MHz obtained by dividing LOSC into two frequencies.
77	G	–	Circuit ground
78	G	–	Circuit ground
79	N/C	–	Not used.
80	N/C	–	Not used.

7.12 DRAM μPD4265

This DRAM is a 64K x 1 bit quasi-CMOS chip, which reduces power consumption. It is used only at the output section. It can be refreshed in two modes: an automatic, self refresh, which uses the $\overline{RF}$ signal at pin 1; and a hidden refresh, which uses the $\overline{CAS}$ signal at pin 15. While power is off, the sub-CPU 7508 provides three modes for saving reducing power consumption. Those modes are automatically selected depending on sensed ambient temperature.

Figs. 7-22 and 7-23 respectively show the Timing relationships among major control signals in the read and write cycles.

(Read cycle)

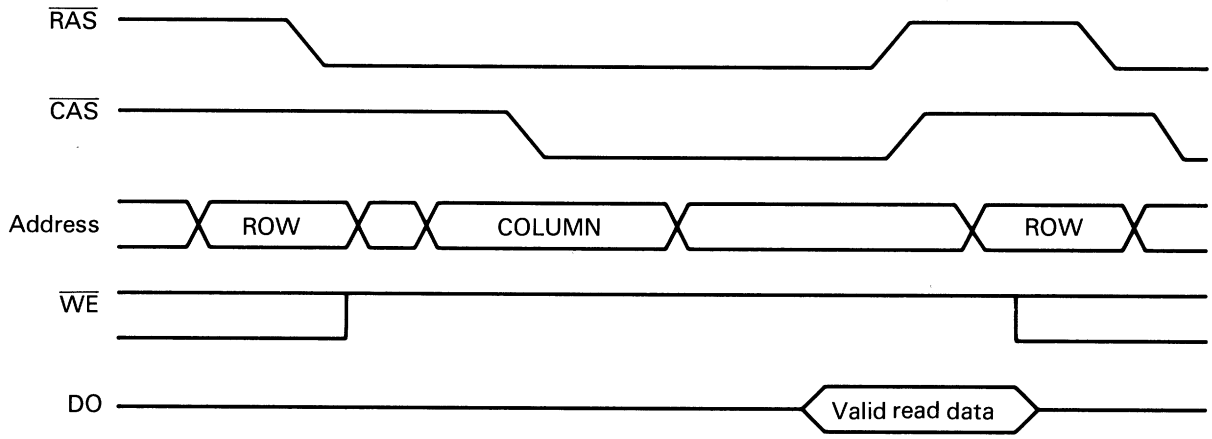


Fig. 7-22 DRAM Read Cycle Operation Timing

(Write cycle)

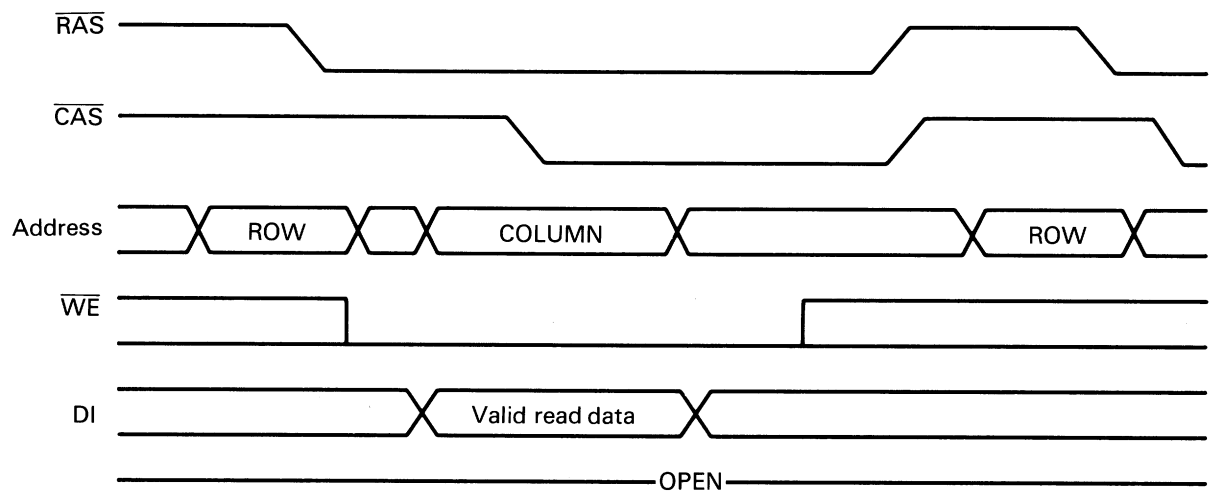
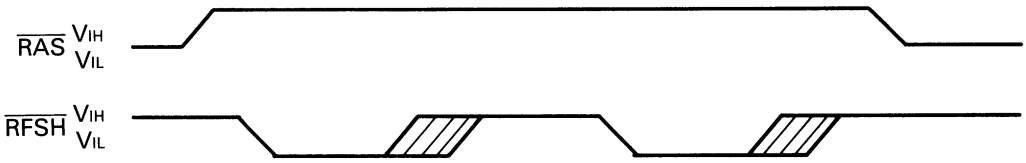
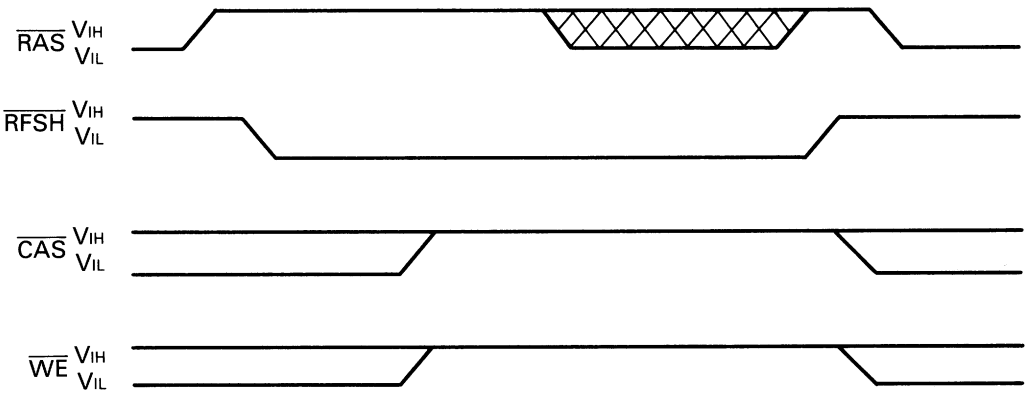


Fig. 7-23 DRAM Write Cycle Operation Timing

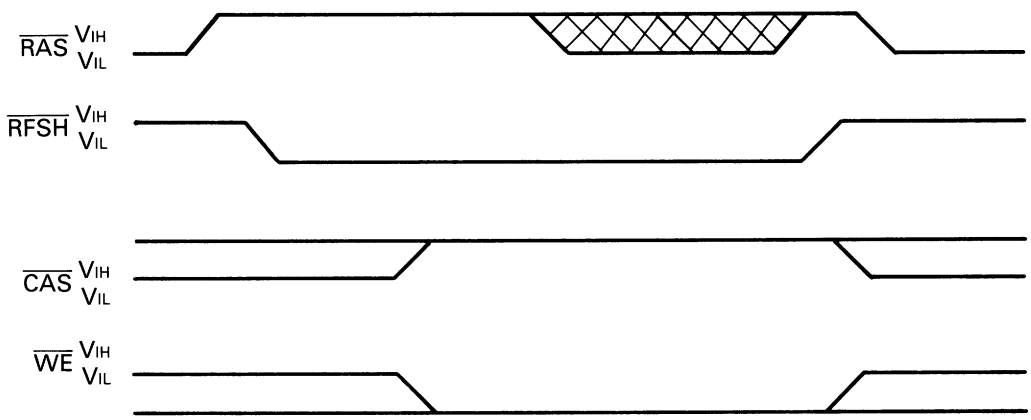
AUTOMATIC PULSE REFRESH CYCLE



SELF REFRESH CYCLE (0°C TO 70°C)



SELF REFRESH CYCLE (0°C TO 45°C)



SELF REFRESH CYCLE (0°C TO 25°C)

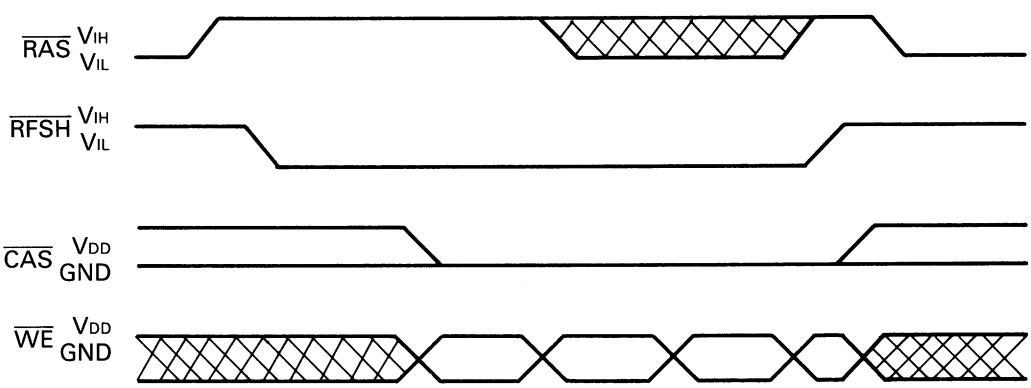


Fig. 7-27

HIDDEN AUTOMATIC PULSE REFRESH CYCLE

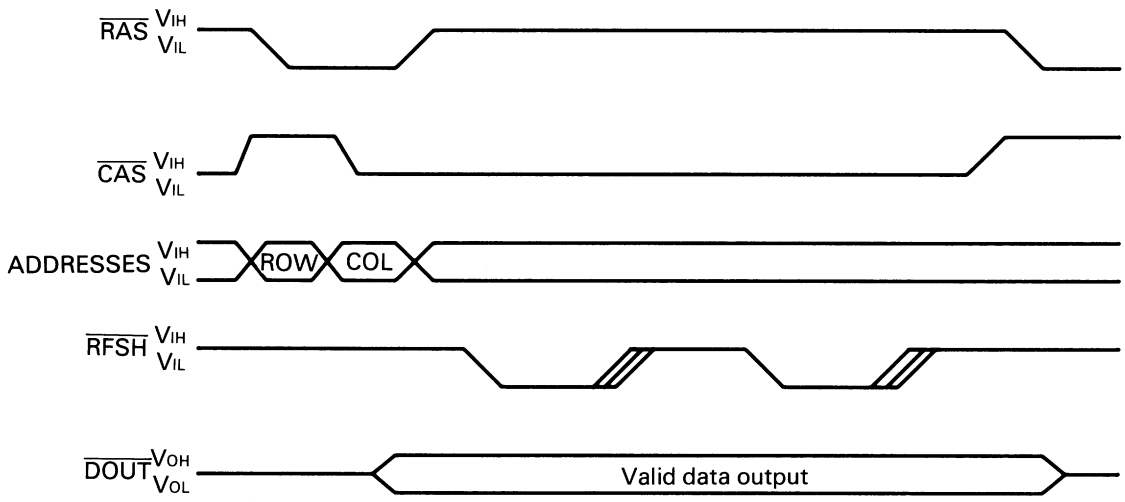


Fig. 7-28

HIDDEN REFRESH

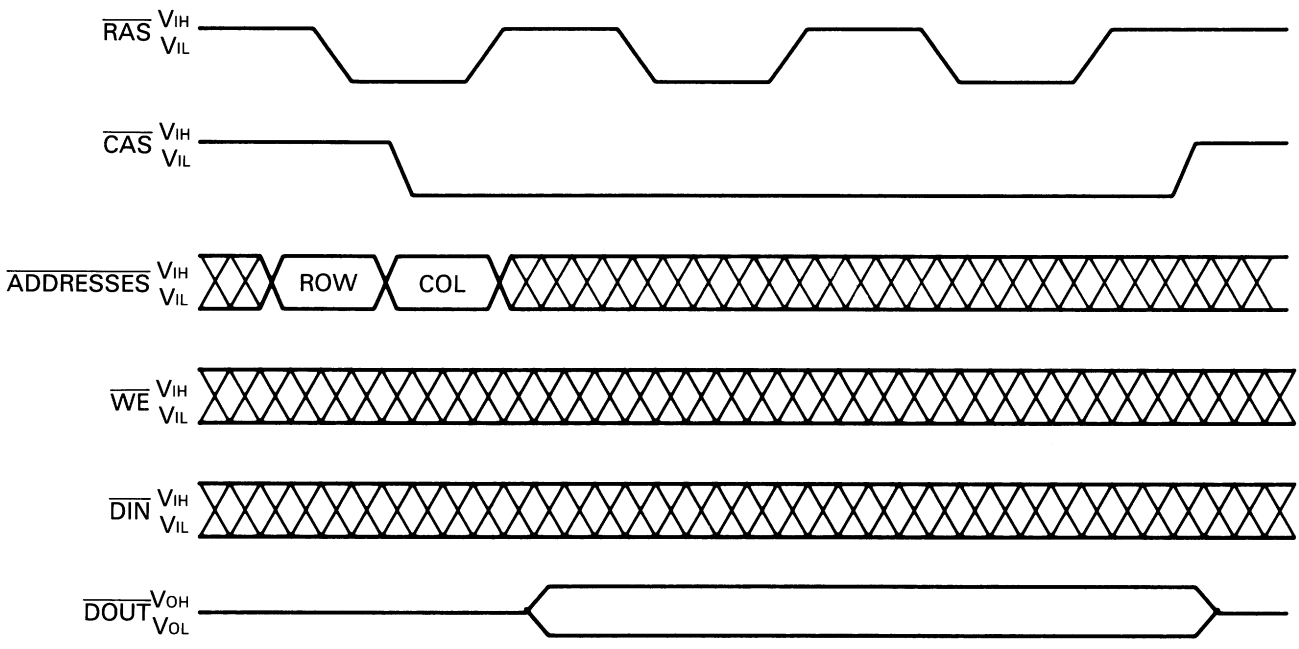


Fig. 7-29

μPD4265

1. Location: MAPLE Board, 4D – 7D And 4E – 7E
   MAP-RF, 10A – 17A And 10B – 17B
2. Pin Assignments

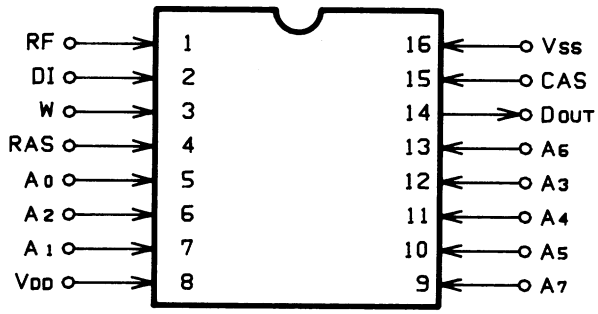


Table 7-16 μPD4265 Pin Assignments

Pin No.	Signal Name	In/Out	Function
1	$\overline{RF}$	In	Refresh
2	DI	In	Data IN
3	$\overline{W}$	In	Write enable
4	$\overline{RAS}$	In	ROW address strobe
5,6,7	A 0 ~ A 2	In	Address
8	VDD	In	+5V (circuit voltage)
9 ~ 13	A 3 ~ A 7	In	Address
14	D 0	Out	Data out
15	$\overline{CAS}$	In	Column Address strobe
16	VSS	In	Ground

7.13 V-RAM 6117

The 6117 is a 2048 x 8 bit C-MOS static RAM. This computer has three 6117 RAMs, totalling a 6KB capacity, which are used mainly as LCD memory. All the V-RAMs are backed up by the battery and can hold stored data if power is turned off. The RAMs are accessed via the slave CPU 6303. A functional block diagram of V-RAM circuitry is illustrated in Fig. 7-30.

Fig. 7-30 is a functional block diagram of 6117.

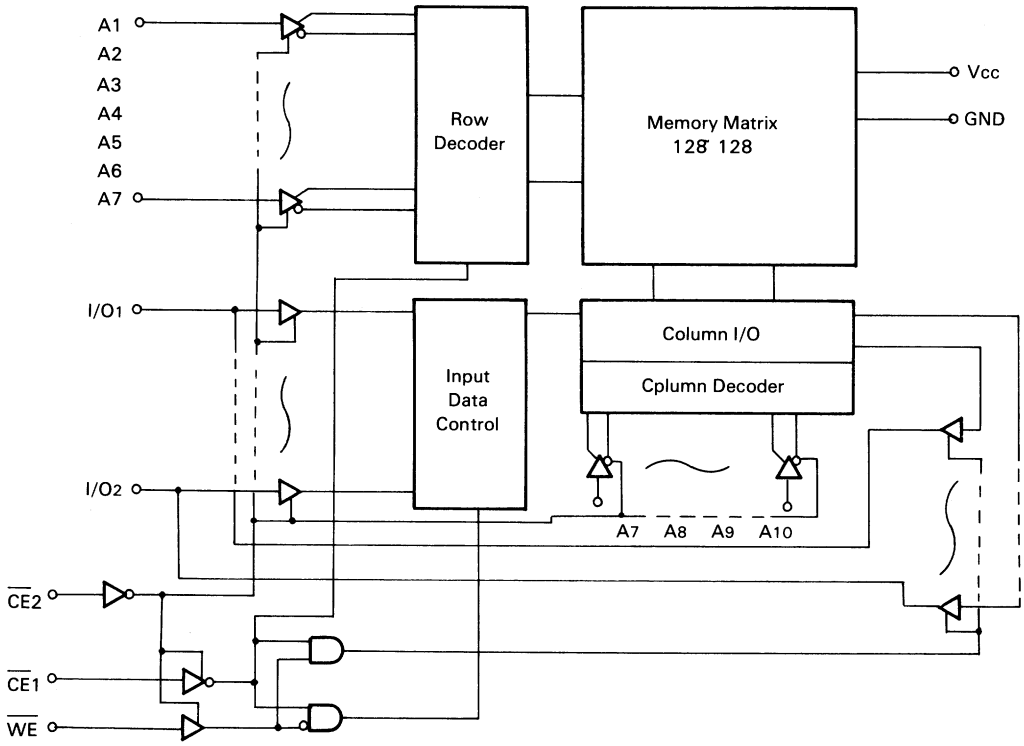


Fig. 7-30 6117 V-RAM Block Diagram

6117PE

1. Location: MAPLE Board, 9C, 10C, 11C
2. Pin Assignments

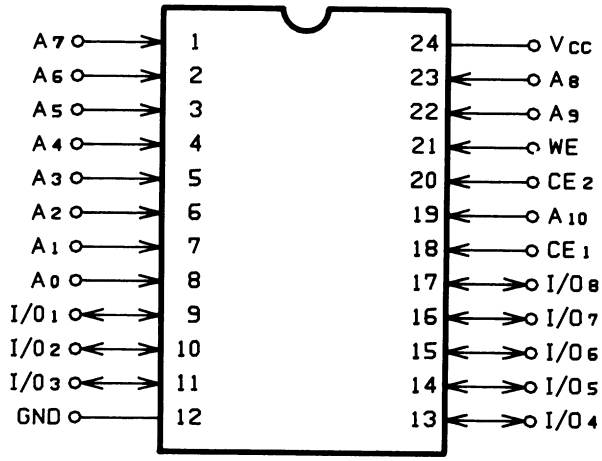


Table 7-17 6117PE Pin Assignments

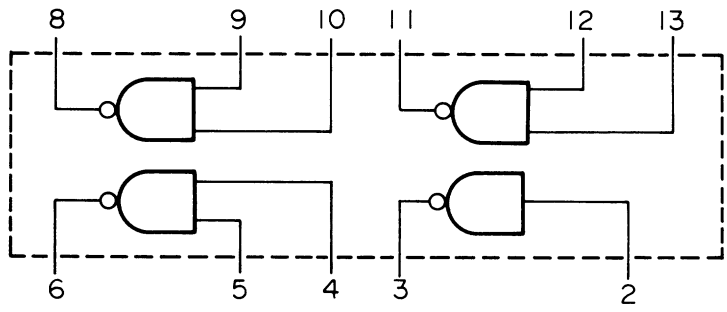
Pin No.	Signal Name	In/Out	Function
1	AB 7	In	Address 7
2	AB 6	In	Address 6
3	AB 5	In	Address 5
4	AB 4	In	Address 4
5	AB 3	In	Address 3
6	AB 2	In	Address 2
7	AB 1	In	Address 1
8	AB 0	In	Address 0
9	D 0	In/Out	Data 0
10	D 1	In/Out	Data 1
11	D 2	In/Out	Data 2
12	N/C	–	Not used.
13	D 3	In/Out	Data 3

Pin No.	Signal Name	In/Out	Function
14	D 4	In/Out	Data 4
15	D 5	In/Out	Data 5
16	D 6	In/Out	Data 6
17	D 7	In/Out	Data 7
18	CE 1	In	Chip enable 1
19	AB 10	In	Address 10
20	CE 2	In	Chip enable 2
21	WE	In	Low level: Write High level: Read
22	AB 9	In	Address 9
23	AB 8	In	Address 8
24	Vcc	–	Circuit voltage (+5V)

7.14 Other ICs

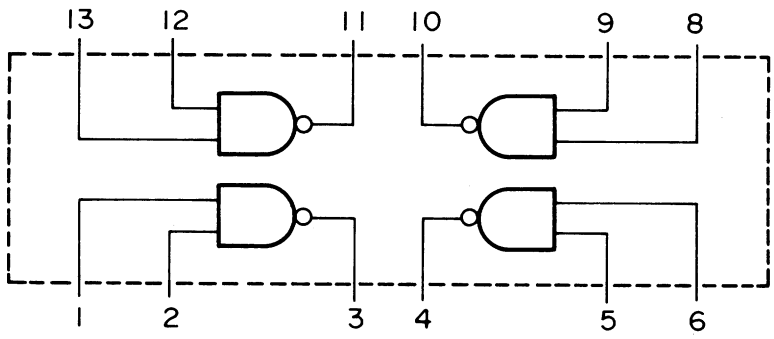
The circuit diagrams of the other ICs used in this computer are shown in the following:

75188

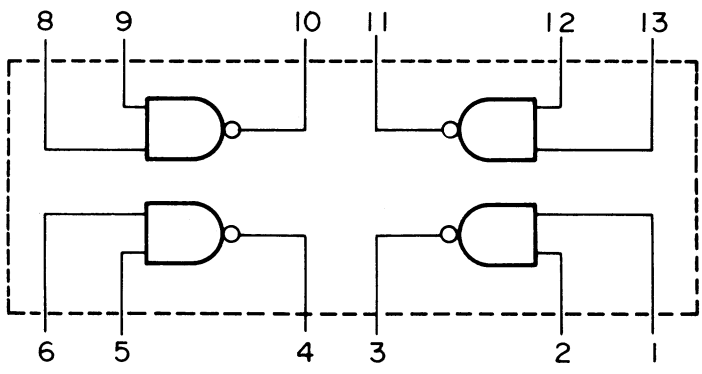


(Pin 1: Vcc, 7 : GND)

4093BP

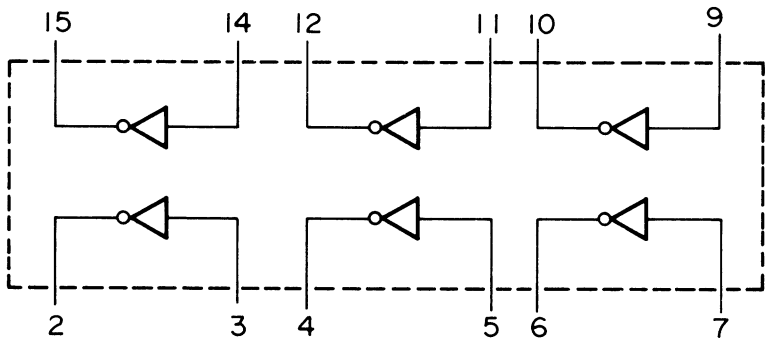


4011UBP



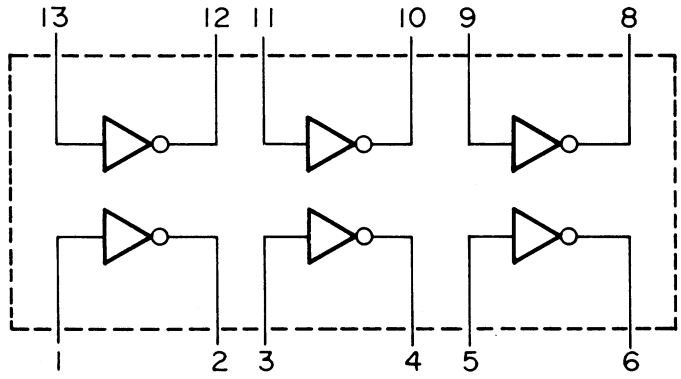
(Pin 7: Vss, 14: V_{DD})

4093BP



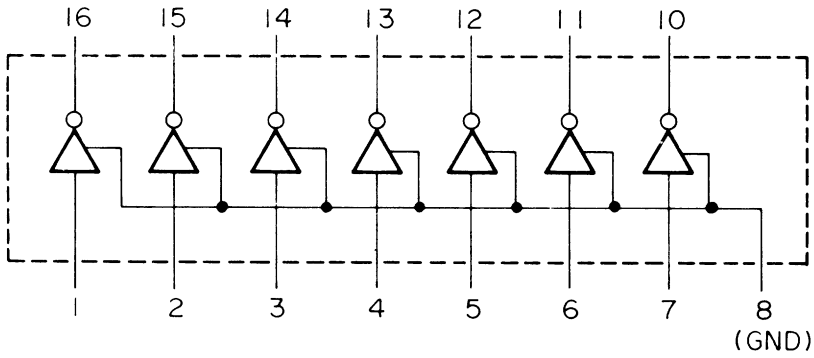
(Pin 8: GND, 1 : Vcc, 13/16 Unused)

40H004



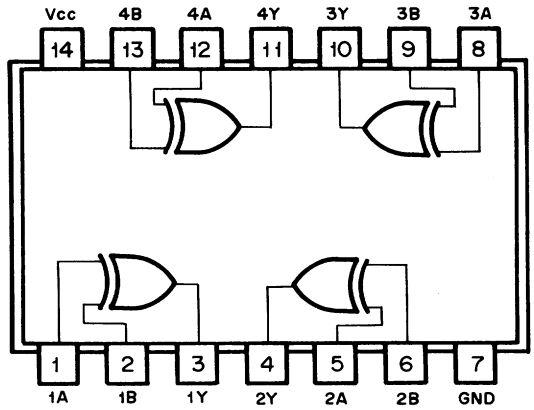
(Pin 7: GND, 14: V_{DD})

TD62504

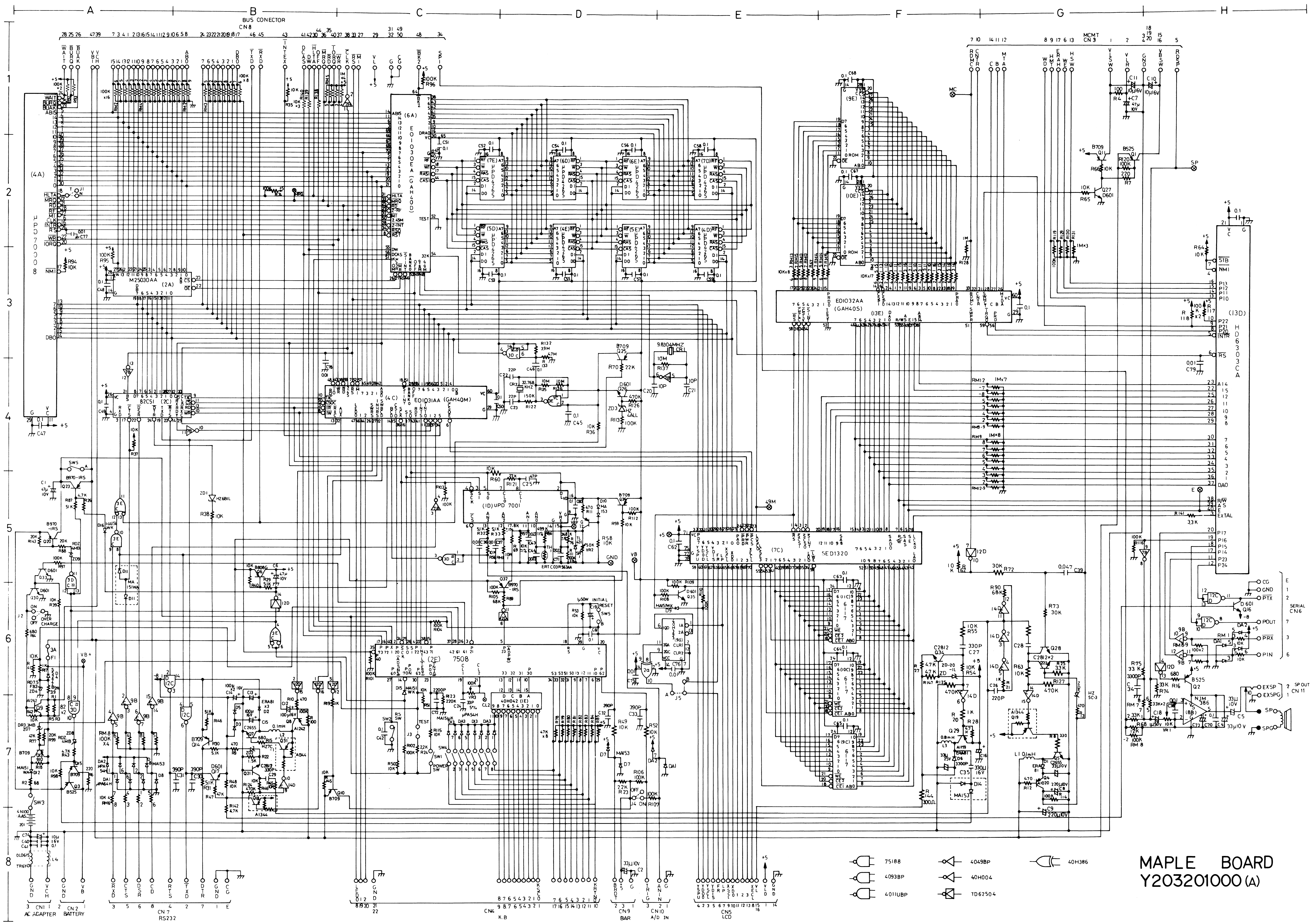


(Pin 9: Not used)

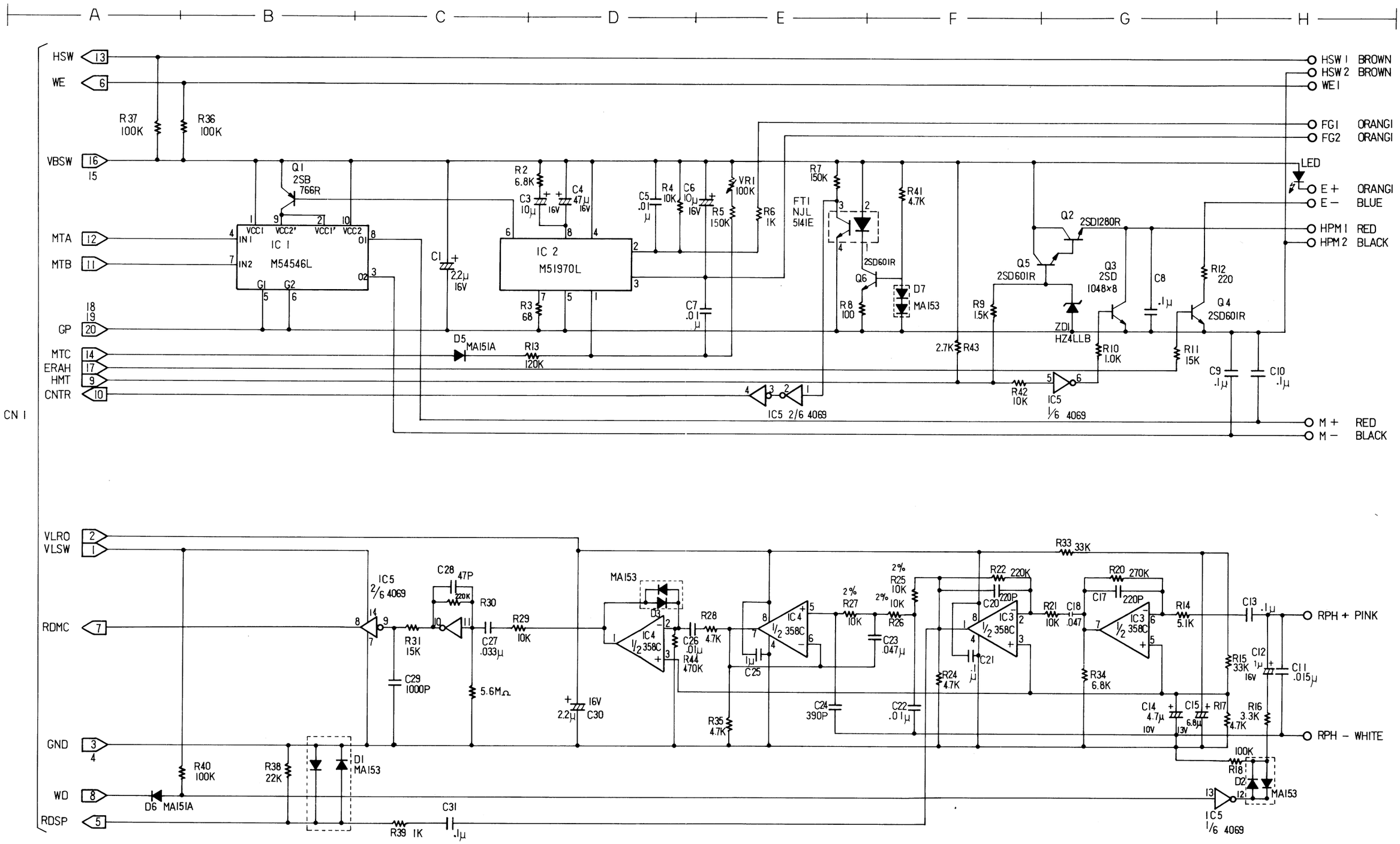
40H386



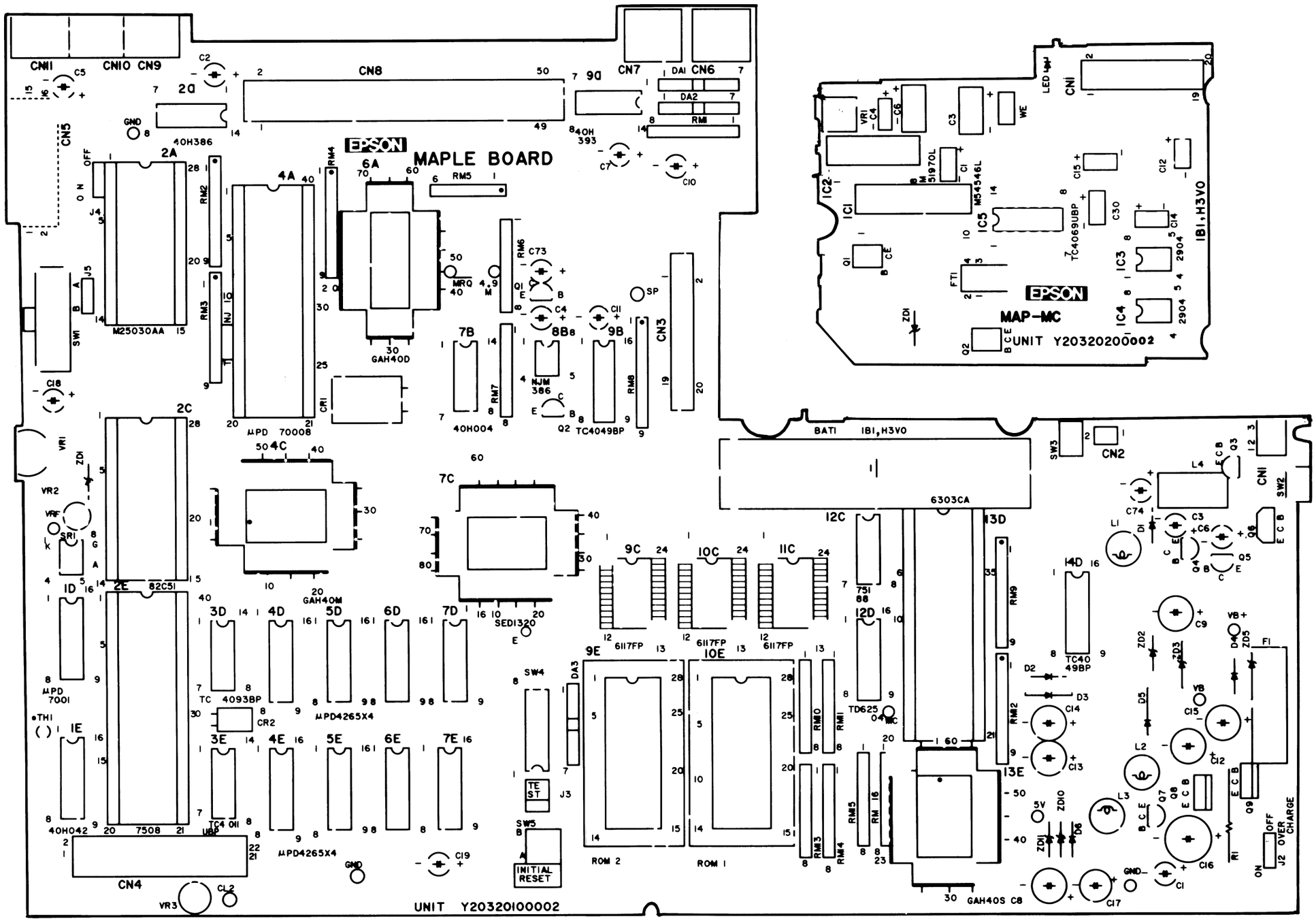
$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

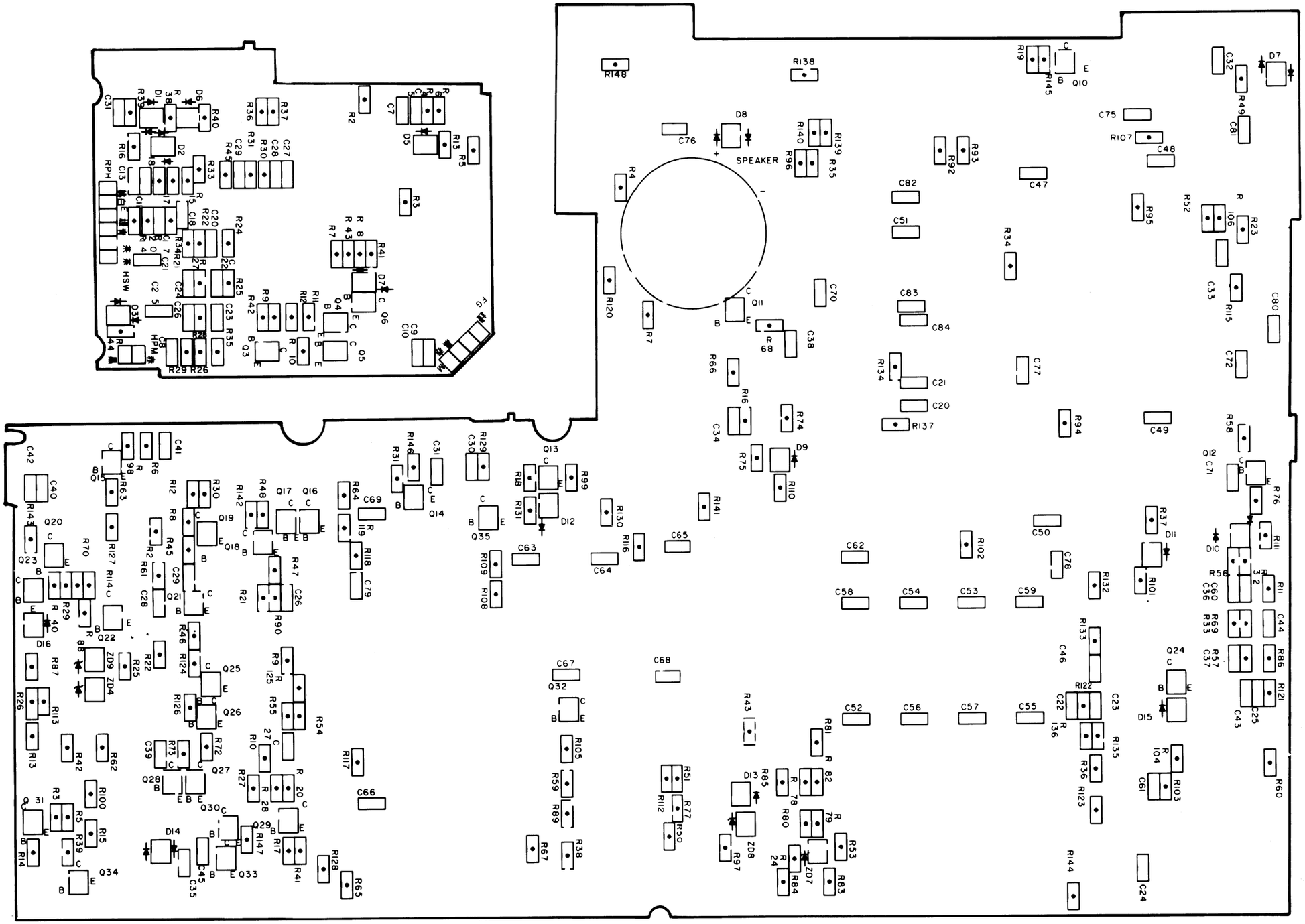


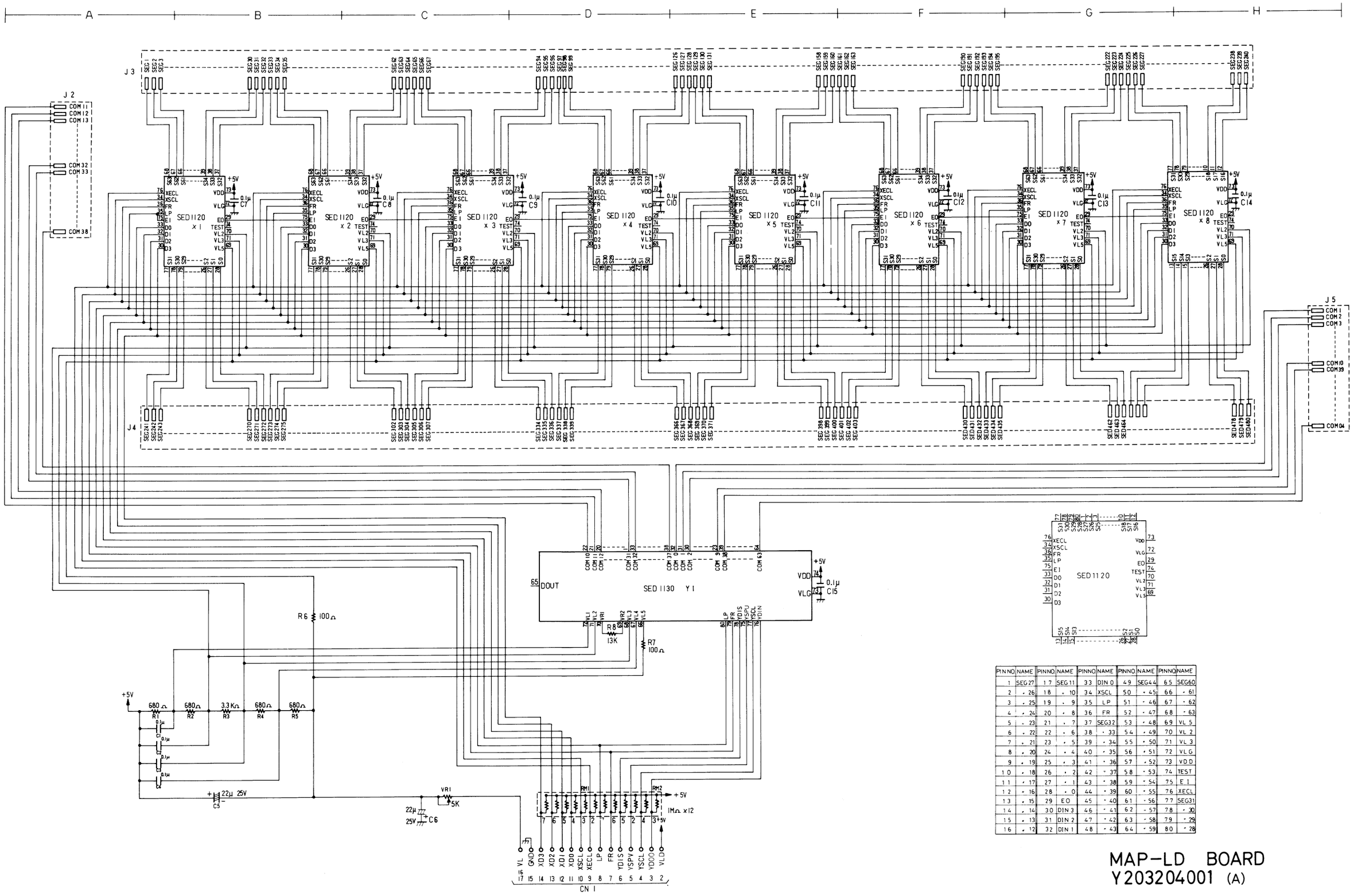
BUS CONECTOR
CN8
μPD70008
M25020AA (2A)
82C51 (2C)
E01030EAA (GAH40D) (6A)
E01031AA (GAH40M) (4C)
E01032AA (GAH40S) (3E)
(1D) UPD 7001
7508 (2E)
40H042 (1E)
SED1320 (7C)
HD6303CA (13D)
9.8304MHZ
32.768 KHZ
ERT C03R563AA
INITIAL RESET
OVER CHARGE
CN1 AC ADAPTER
CN2 BATTERY
CN7 RS232
CN4 K.B
CN9 BAR
CN10 A/D IN
CN5 LCD
SERIAL CN6
SP OUT CN11
75188
4093BP
4011UBP
4049BP
40H004
1D62504
40H386
MAPLE BOARD
Y203201000 (A)



MAP−MC BOARD
Y203202001 (A)

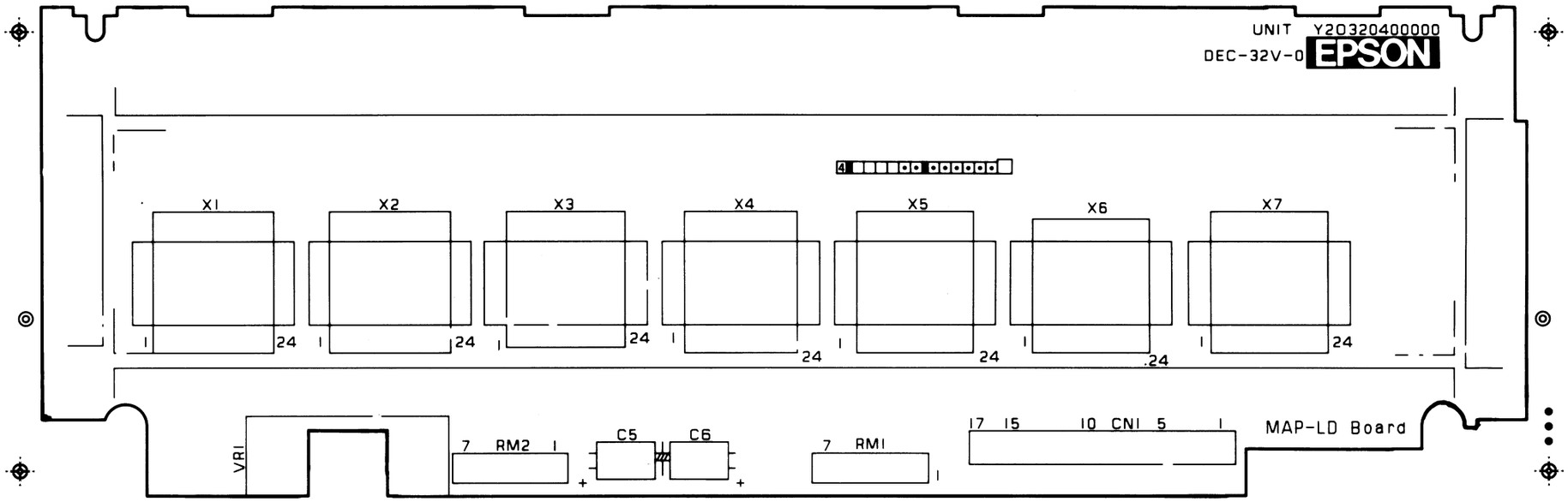

EPSON
MAPLE BOARD
CN11
CN10
CN9
CN8
CN7
CN6
CN5
CN4
CN3
CN2
CN1
M25030AA
μPD 70008
μPD4265X4
TC4049BP
TC4093BP
TC4011BP
TC4069UBP
TC4040BP
M5346L
M51970L
6117FP
SED1320
6303CA
82C51
μPD 7001
7508
ROM 2
ROM 1
INITIAL RESET
UNIT Y20320200002
MAP-MC
UNIT Y20320100002
IBI,H3V0
BATI
GND
VB
5V
EPSON MAPLE-BOARD-X SILK(COMP)

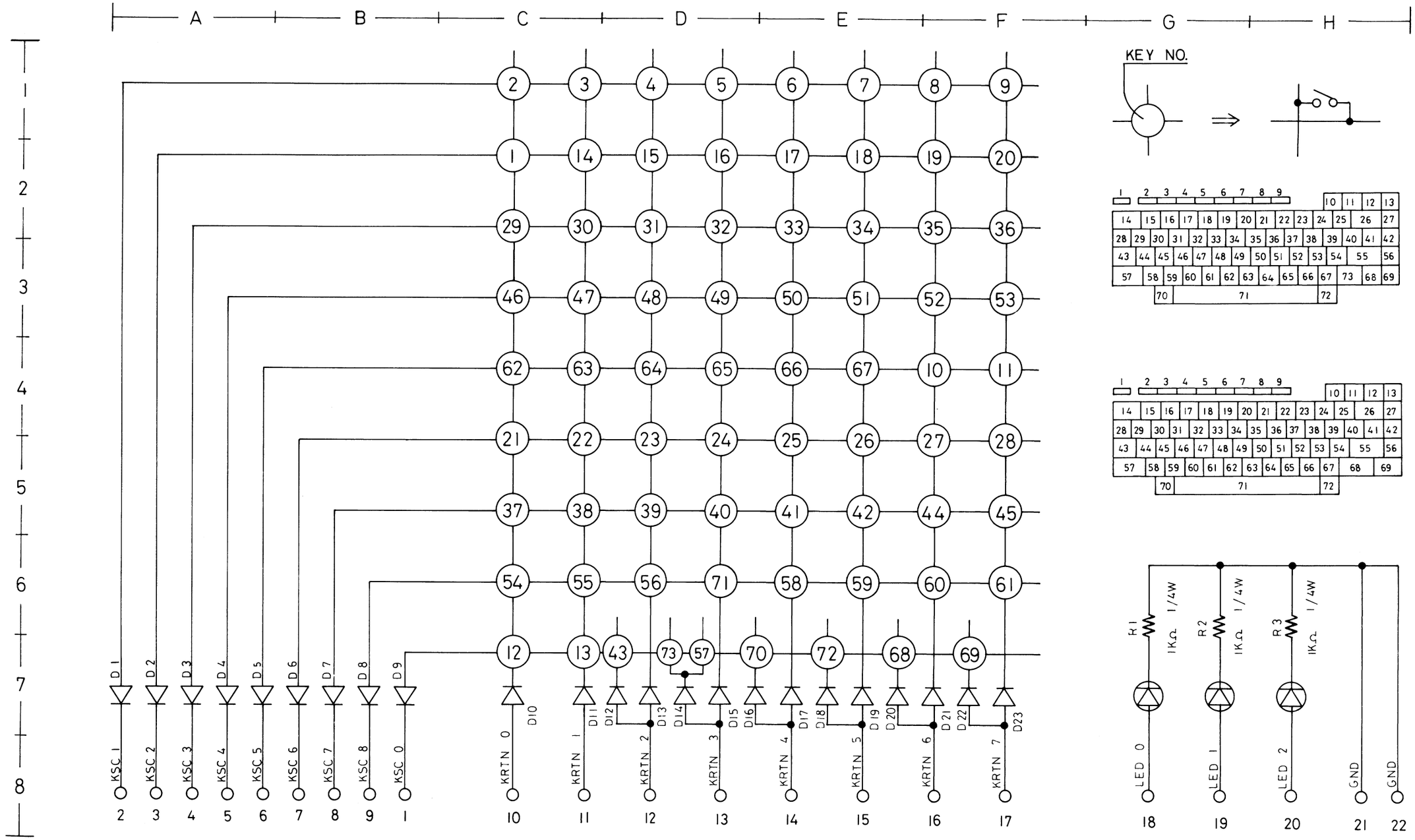

EPSON MAPLE-BOARD-X SILK(SOLD)
SPEAKER



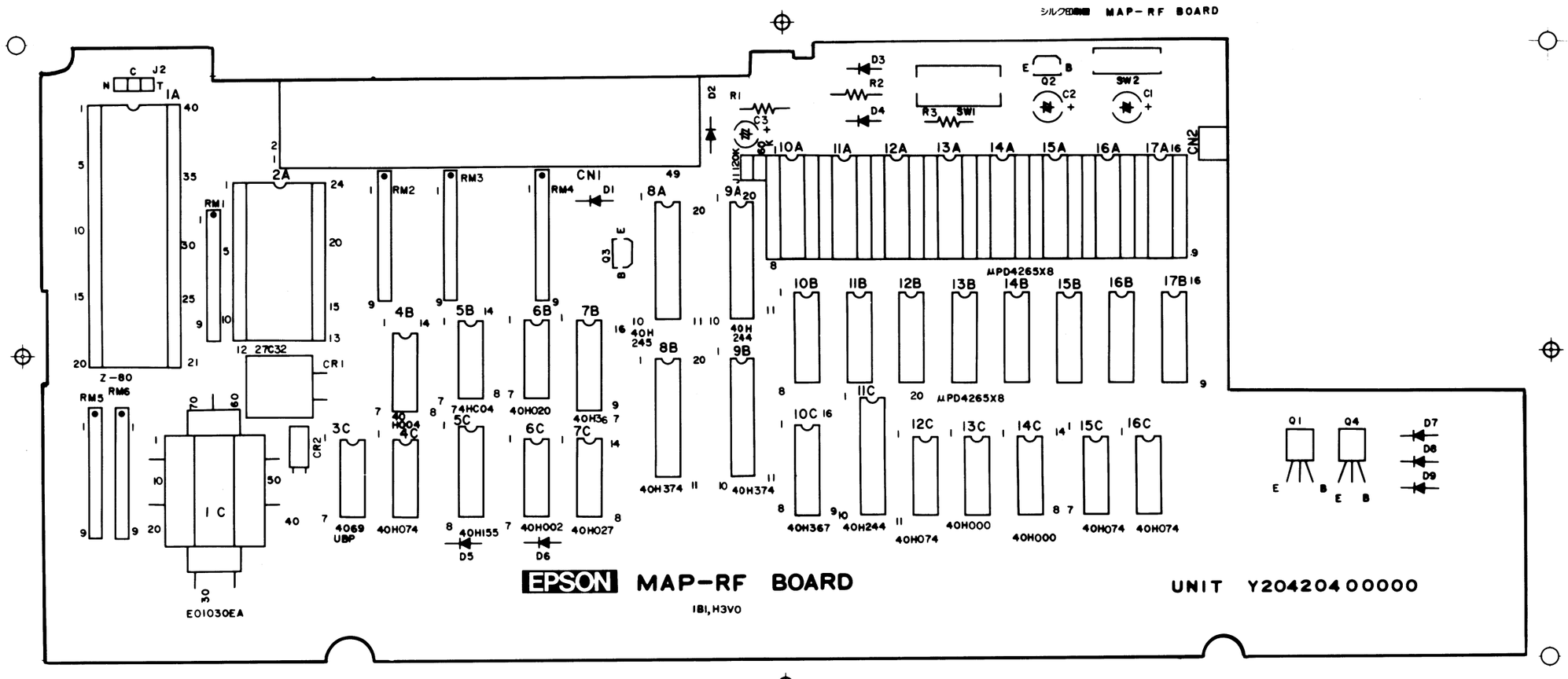
PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	SEG 27	17	SEG 11	33	DIN 0	49	SEG 44	65	SEG 60
2	" 26	18	" 10	34	XSCL	50	" 45	66	" 61
3	" 25	19	" 9	35	LP	51	" 46	67	" 62
4	" 24	20	" 8	36	FR	52	" 47	68	" 63
5	" 23	21	" 7	37	SEG 32	53	" 48	69	VL 5
6	" 22	22	" 6	38	" 33	54	" 49	70	VL 2
7	" 21	23	" 5	39	" 34	55	" 50	71	VL 3
8	" 20	24	" 4	40	" 35	56	" 51	72	VL G
9	" 19	25	" 3	41	" 36	57	" 52	73	VDD
10	" 18	26	" 2	42	" 37	58	" 53	74	TEST
11	" 17	27	" 1	43	" 38	59	" 54	75	E 1
12	" 16	28	" 0	44	" 39	60	" 55	76	XECL
13	" 15	29	EO	45	" 40	61	" 56	77	SEG 31
14	" 14	30	DIN 3	46	" 41	62	" 57	78	" 30
15	" 13	31	DIN 2	47	" 42	63	" 58	79	" 29
16	" 12	32	DIN 1	48	" 43	64	" 59	80	" 28

MAP-LD BOARD
Y203204001 (A)


UNIT Y20320400000
DEC-32V-0
EPSON
X1
X2
X3
X4
X5
X6
X7
24
VR1
7 RM2 1
C5
C6
7 RM1 1
17 15 10 CN1 5 1
MAP-LD Board


A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
KEY NO.
2 3 4 5 6 7 8 9
10 11 12 13
14 15 16 17 18 19 20 21 22 23 24 25 26 27
28 29 30 31 32 33 34 35 36 37 38 39 40 41 42
43 44 45 46 47 48 49 50 51 52 53 54 55 56
57 58 59 60 61 62 63 64 65 66 67 73 68 69
70 71 72
1 14 15 16 17 18 19 20
29 30 31 32 33 34 35 36
46 47 48 49 50 51 52 53
62 63 64 65 66 67 10 11
21 22 23 24 25 26 27 28
37 38 39 40 41 42 44 45
54 55 56 71 58 59 60 61
12 13 43 73 57 70 72 68 69
D 1
D 2
D 3
D 4
D 5
D 6
D 7
D 8
D 9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
KSC 1
KSC 2
KSC 3
KSC 4
KSC 5
KSC 6
KSC 7
KSC 8
KSC 0
KRTN 0
KRTN 1
KRTN 2
KRTN 3
KRTN 4
KRTN 5
KRTN 6
KRTN 7
R1
R2
R3
1KΩ 1/4W
LED 0
LED 1
LED 2
GND
GND
2 3 4 5 6 7 8 9 1
10 11 12 13 14 15 16 17
18 19 20 21 22

MAP-RF BOARD
Y204204001 (A)


MAP-RF BOARD
EPSON MAP-RF BOARD
181, H3V0
UNIT Y204204 00000
E01030EA
Z-80
μPD4265X8
μPD4265X8
1C
4069 UBP
40H074
40HI55
40H002
40H027
74HC04
40H020
40H374
40H374
40H367
40H244
40H074
40H000
40H000
40H074
40H074
CN1
CN2
CR1
CR2
SW1
SW2
Q1
Q2
Q3
Q4
D1
D2
D3
D4
D5
D6
D7
D8
D9
R1
R2
R3
C1
C2
C3
27C32

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