3.2.3 Points to Remember When Using the 7508

The following points should be noted when transferring commands or data directly to and from the 7508 CPU:

(1) Remember to disable 7508 interrupts when transferring commands or data to or from the 7508 CPU.
Interrupts can be disabled by:
- DI instruction.
- Rewriting the IER (P04H).
- BIOS MASKI function.

The 7508 must be disabled for interrupts while the procedures shown in figures 3.2.1 and 3.2.2. are being executed.

(2) Complete the send or receive sequence for a command before proceeding with the next command. Normal processing cannot be guaranteed unless the application program sends or receives the required number of data bytes.

3.3 7508 Commands

This section gives a detailed description of 7508 commands. See Section 3.2 for the procedure for transferring data or commands to and from the 7508.

The table below lists the commands that the 7508 CPU accepts from the main CPU.

No.	Command function	Code	No.	Command function	Code
1	Power OFF	01H	14	Power Switch Read	08H
2	Read Status	02H	15	Alarm Read	09H
3	KB Reset	03H	16	Alarm Set	19H
4	KB Repeat Timer 1 Set	04H	17	Alarm OFF	29H
5	KB Repeat Timer 2 Set	14H	18	Alarm ON	39H
6	KB Repeat Timer 1 Read	24H	19	DIP Switch Read	0AH
7	KB Repeat Timer 2 Read	34H	20	Stop Key Interrupt disable	0BH
8	KB Repeat OFF	05H	21	Stop Key Interrupt enable	1BH
9	KB Repeat ON	15H	22	7 chr. Buffer	0CH
10	KB Interrupt OFF	06H	23	1 chr. Buffer	1CH
11	KB Interrupt ON	16H	24	1 sec. Interrupu OFF	0DH
12	Clock Read	07H	25	1 sec. Interrupt ON	1DH
13	Clock Write	17H	26	KB Clear	0EH
			27	System Reset	0FH

Commands are identified by a 1 in it bit position 7 of the command code and data by a 0 in bit position 7.

(1) Power off

Function: Turns off power to the main CPU (Z-80).

Sequence:

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	1	(Write)

Explanation:
This command is used to turn off power to the main CPU (Z-80).

Note: This command is not available to application programs. Use the BIOS POWEROFF function in application programs.

(2) Read status

Function: Reads the 7508 status or key code.

Sequence:

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1	0	(write)
								(read)

Bits 7-0 : Status or key code

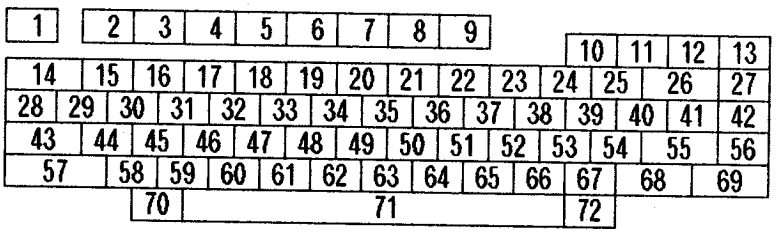
Explanation:
1) This command is used to read the 7508 status to identify the interrupt source when an interrupt occurs or after the reset state is released.
2) The status byte is classified into two types, the key code and status. The meanings of key code and status are described below.

1. Key code
Status bytes 0BEH and below indicate key code.
The correspondence between the keys and key codes is shown in figures 3.3.1 and 3.3.2.

There are two types of keys, ordinary and switch keys. When an ordinary key is pressed, the 7508 returns only a make code corresponding to the key. For a switch key, however, the 7508 returns a make code (0B2H - 0B7H) when the key is pressed and a break code (0A2H - 0A7H) when it is released.

(i) Hard code table (standard keyboard)

The figure and table below show the correspondence between the keys on the standard keyboard and the key codes. Break and Make in the table indicate that the code is returned at the time the SHIFT key is pressed and released, respectively.

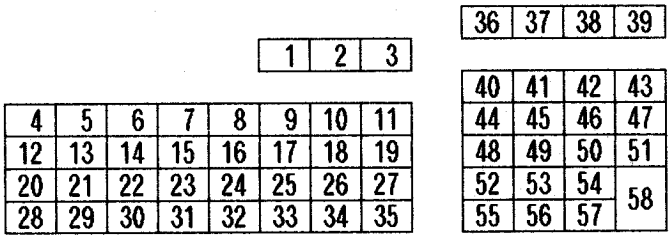


Higher / Lower	0	1	2	3	4	5	6	7	8	9	A	B
0	2	1	29	46	62	21	37	54	12			
1	3	14	30	47	63	22	38	55	13			
2	4	15	31	48	64	23	39	56			43 Break	43 Make
3	5	16	32	49	65	24	40	71			57 Break	57 Make
4	6	17	33	50	66	25	41	58			70 Break	70 Make
5	7	18	34	51	67	26	42	59			72 Break	72 Make
6	8	19	35	52	10	27	44	60			68 Break	68 Make
7	9	20	36	53	11	28	45	61			69 Break	69 Make

Figure 3.3.1 Correspondence between Key Numbers and Key Codes (Standard Keyboard)

(ii) Hard code table (item keyboard)

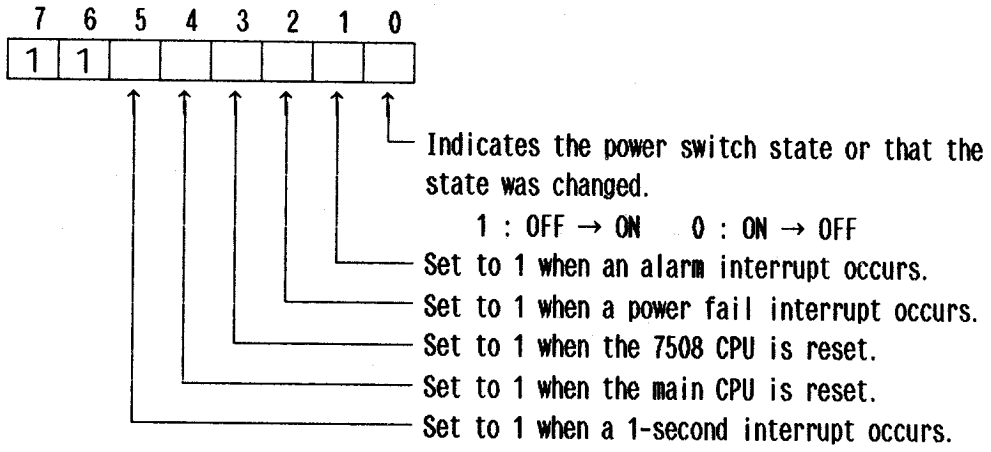
The figure and table below show the correspondence between keys on the item keyboard and key codes. Break and Make in the table indicate that the code is returned at the time the SHIFT key is pressed and released, respectively.



Higher / Lower	0	1	2	3	4	5	6	7	8	9	A	B
0			43	51	4	20	12	28				
1		36	44	52	5	21	13	29				
2		37	45	53	6	22	14	30			1 Break	1 Make
3		38	46	54	7	23	15	31				
4		39	47	55	8	24	16	32				
5		40	48	56	9	25	17	33			2 Break	2 Make
6		41	49	57	10	26	18	34			3 Break	3 Make
7		42	50	58	11	27	19				35 Break	35 Make

Figure 3.3.2 Correspondence between Key Numbers and Key Codes (Item Keyboard)

2. Status
Status bytes ØC0H and above indicate that an interrupt occurred or that the reset state was released. Otherwise, the status byte ØBFH is returned. Each bit of the status byte has the meaning listed below. When two or more interrupts or resets occur simultaneously, the corresponding bits are set to 1.

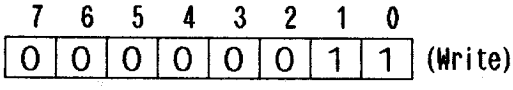


PINE OS reads this 75Ø8 status information during interrupt processing following an interrupt, or in address Ø start processing (system initialize, reset, power-on, and alarm/wake processing) when the 75Ø8 or main CPU is reset. PINE OS determines what to do next on the basis of this information.

(3) KB reset

Function: Initializes the keyboard.

Sequence:



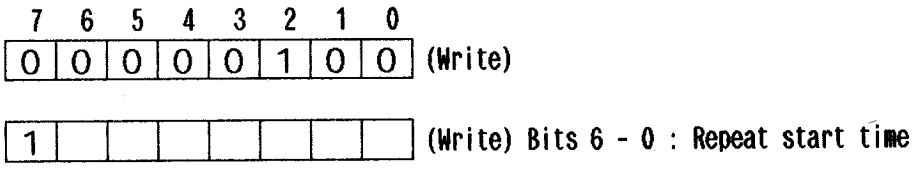
Explanation:
1) Initializes the keyboard as follows:
   - Sets the keyboard repeat start time to 656 ms.
   - Sets the keyboard repeat interval to 7Ø ms.
   - Clears the key buffer.
   - Enables interrupts from the keyboard.
2) Scans the keyboard and loads information concerning the currently pressed key into the buffer.

Note: PINE OS uses this command to initialize and reset the system.

(4) KB repeat timer 1 set

Function: Sets the keyboard repeat start time.

Sequence:



Explanation:

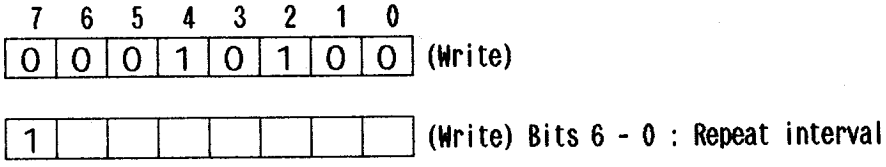
1) The corresponding key code is read repeatedly as long as an ordinary key (i.e. a key other than the switch and special keys) is held down. This command defines the interval between the time when a key is first pressed and the time when the auto repeat function starts.
2) The send data specifies the repeat start time in 1/64 second (approximately 15 ms) increments. The maximum repeat start time is approximately 2 seconds. The MSB of the data must be always set to 1.
3) The initial value is 656 ms.

Note: In PINE OS, BIOS CONOUT (ESC + ØF1H) is used to set the repeat start time.

(5) KB repeat timer 2 set

Function: Defines the keyboard repeat interval.

Sequence:



Explanation:

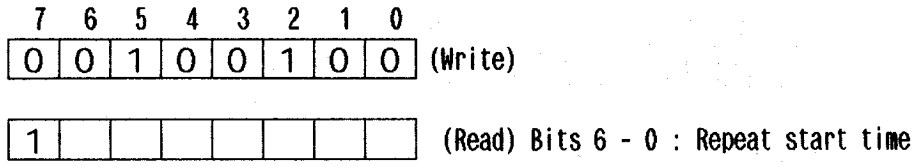
1) Defines the interval at which the key code of a key being held down is to be repeatedly entered.
2) The send data specifies the keyboard repeat interval in 1/256 second (approximately 3.9 ms) increments. The maximum period is Ø.5 second. The MSB of the data must be always set to 1.
3) The initial value is approximately 7Ø ms.

Note: In PINE OS, BIOS CONOUT (ESC + ØF2H) is used to set the repeat interval.

(6) KB repeat timer 1 read

Function: Reads the keyboard repeat start time.

Sequence:



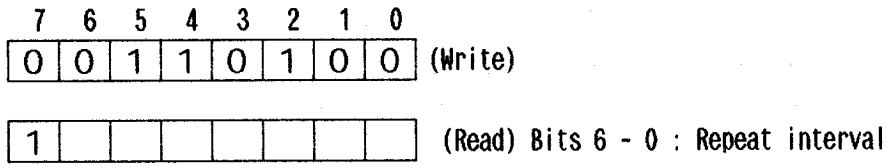
Explanation:

1) Returns the keyboard repeat start time which is currently set.
2) The receive data specifies the keyboard repeat start time in 1/64 second (approximately 15 ms) increments. The MSB of the data is always set to 1, but the repeat start time is treated as if the MSB were 0.

(7) KB repeat timer 2 read

Function: Reads the keyboard repeat interval.

Sequence:



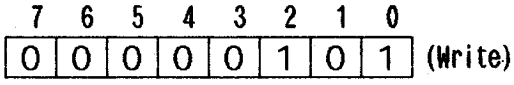
Explanation:

1) Returns the keyboard repeat interval which is currently set.
2) The receive data specifies the keyboard repeat interval in 1/256 second (approximately 3.9 ms) increments. The MSB of the data is always set to 1, but the repeat interval is treated as if the MSB were 0.

(8) KB repeat off

Function: Disables the keyboard auto repeat function.

Sequence:



Explanation:

This command is used to disable the keyboard auto repeat function. After this command is executed, the key code is returned only once, even if the key is held down.

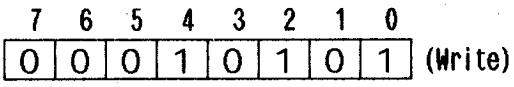
Notes:

1. In PINE OS, the KB repeat function is enabled by default when an item keyboard is installed.
2. In PINE OS, BIOS CONOUT (ESC + ØFØH) is used to switch on or off the keyboard repeat function.

(9) KB repeat on

Function: Enables the keyboard auto repeat function.

Sequence:



Explanation:

1) This command is used to enable the keyboard auto repeat function. After this command is executed, the key code is returned at every repeat interval time if a key is held down for longer than the repeat start time. The auto repeat function is invalid for switch and special keys.
2) The KB repeat function is enabled by default.

Note: In PINE OS, BIOS CONOUT (ESC + ØFØH) is used to switch the keyboard auto repeat function ON/OFF.

(10) KB interrupt off

Function: Disables the Z-80 CPU for all keyboard interrupts.

Sequence:

7	6	5	4	3	2	1	0	
0	0	0	0	0	1	1	0	(Write)

Explanation:

1) This command is used to disable the Z-80 CPU for keyboard interrupts. When a key is pressed after this command is executed, the key code is placed in the 7508 buffer but no interrupt request is sent to the Z-80 CPU. If command (11) is subsequently executed, any keyboard interrupt code stored in the buffer is sent to the Z-80.
2) Extra key codes are ignored when the key buffer is full. However, the STOP key code can be added to the end of the buffer.

Note: In PINE OS, this function is supported by BIOS MASKI.

(11) KB interrupt on

Function: Enables the Z-80 CPU for keyboard interrupts.

Sequence:

7	6	5	4	3	2	1	0	
0	0	0	1	0	1	1	0	(Write)

Explanation:

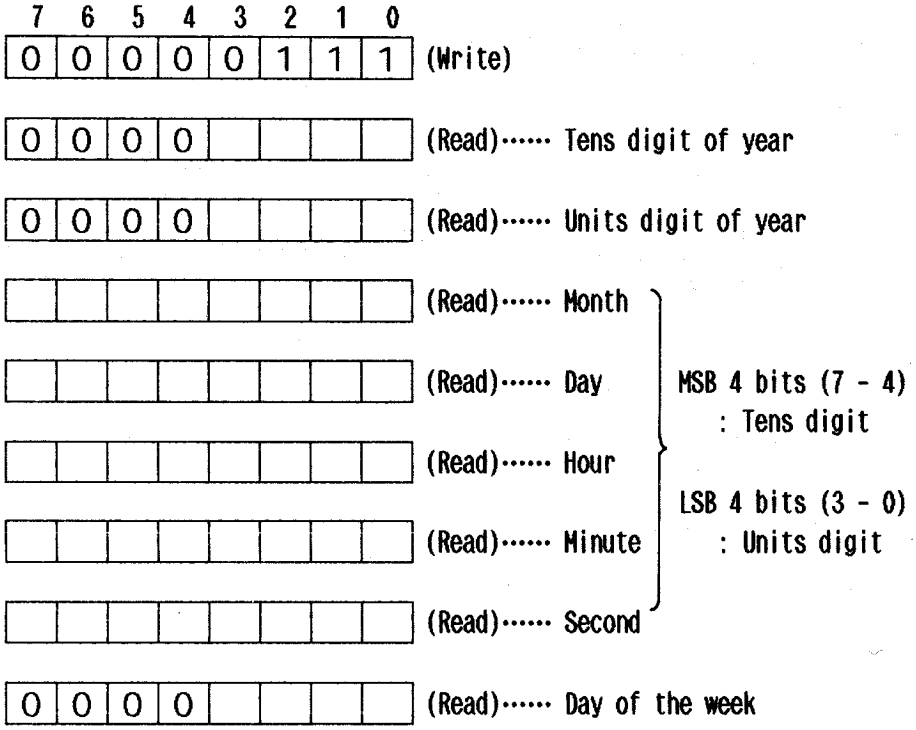
1) This command is used to enable the Z-80 CPU for keyboard interrupts.
2) KB interrupts are enabled by default.

Note: In PINE OS, this function is supported by BIOS MASKI.

(12) Clock read

Function: Reads the current time of the 7508 calendar/clock.

Sequence:



Explanation:

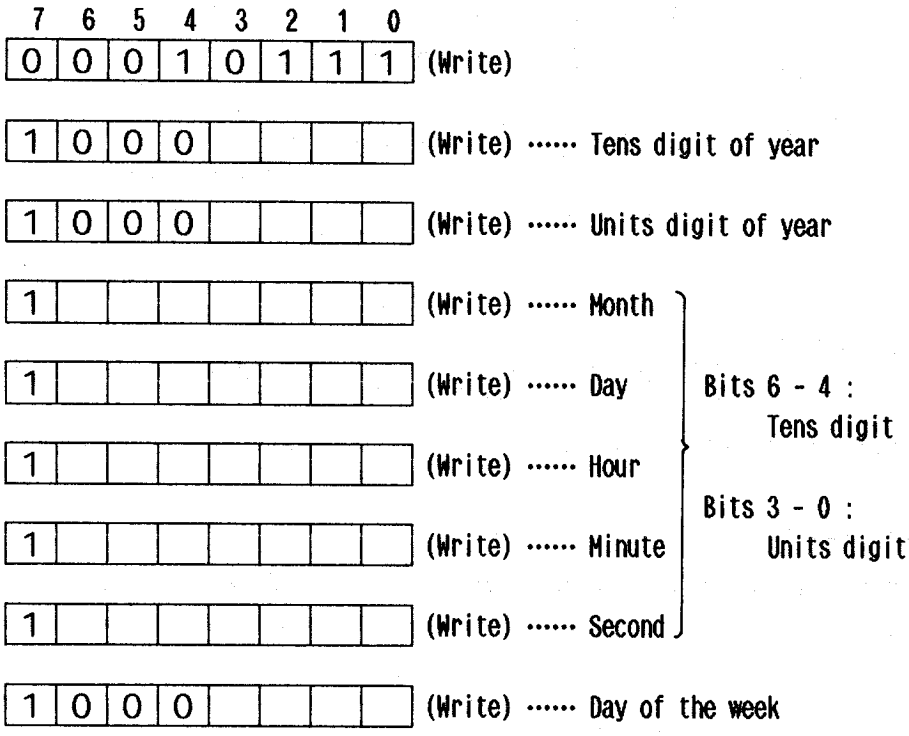
1) This command is used to read the contents of the 7508 calendar/clock.
2) The read data includes the year, month, day, hour, minute, second and day of the week. All these items are specified in BCD notation.
3) The time is expressed in the 24-hour system, and for the day of the week 0 through 6 correspond to Sunday through Saturday. Since the 7508 CPU does not check the read data, the contents of the calendar/clock cannot be guaranteed if logically invalid data was entered at the time of the last clock write.

Note: In PINE OS, this function is supported by BIOS TIMDAT.

(13) Clock write

Function: Sets the 7508 calendar/clock.

Sequence:



Explanation:

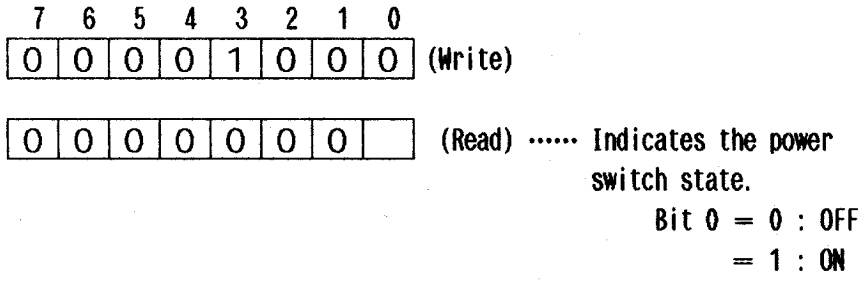
1) This command is used to specify the year, month, day, hour, minute, second and day of the week for the 7508 calendar/clock. All these items are defined in BCD notation. The MSB of send data bytes must always be set to 1.
2) The time is expressed in the 24-hour system. The day of the week is automatically updated within the range 0 through 6. Since the 7508 CPU does not check the set data, the contents of the calendar/clock cannot be guaranteed if logically invalid data is entered.
3) When partially updating the calendar/clock, set every bit of the data bytes not to be updated to 1 and send all data bytes. Items coded as 11111111 will be ignored.

Note: In PINE OS, this function is supported by BIOS TIMDAT.

(14) Power switch read

Function: Reads the current state of the power switch.

Sequence:



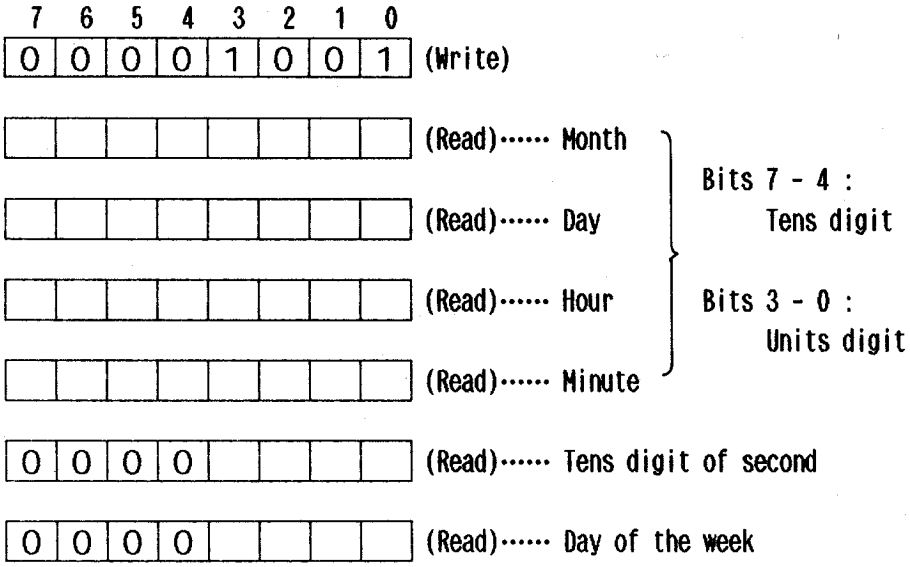
Explanation:
This command is used to read the ON/OFF state of the power switch on the side panel of the main unit.

Note: In PINE OS, this function is supported by BIOS READSW.

(15) Alarm read

Function: Reads the alarm time which is currently set.

Sequence:



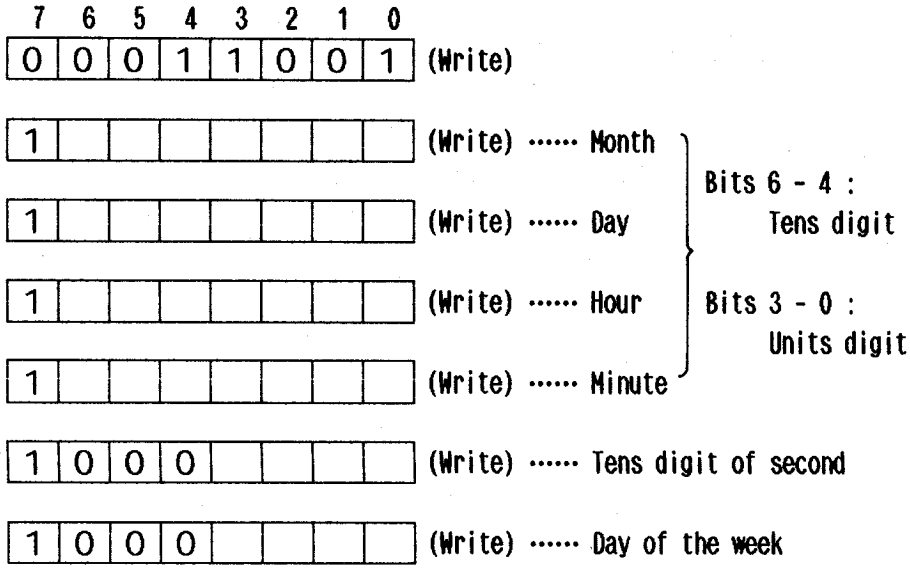
Explanation:
This command is used to read the month, day, hour, minute, second, and day of the week of the alarm time which is currently set. All these items are specified in BCD notation.

Note: In PINE OS, this function is supported by BIOS TIMDAT.

(16) Alarm set

Function: Sets the alarm time.

Sequence:



Explanation:

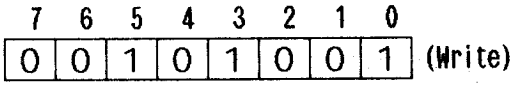
1) This command is used to specify the month, day, hour, minute, second, and day of the week for the alarm time. All these items are defined in BCD notation. The MSB of data bytes must always be set to 1.
2) It is permissible to specify an item as eight 1 bits. (For example, setting the minute field to all 1's causes alarm interrupts to be generated every minute.)
3) The year and the units digit of the second cannot be specified.
4) To enable the alarm function, command (18) must be executed after this command.

Note: In PINE OS, this function is supported by BIOS TIMDAT.

(17) Alarm off

Function: Disables alarm interrupts.

Sequence:



Explanation:

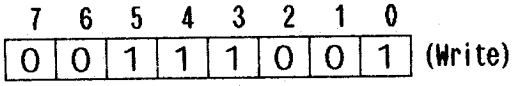
1) This command is used to disable alarm interrupts to the Z-80 CPU. Any alarm interrupts generated in alarm off state are ignored. Subsequently, these interrupts are suppressed even if the alarm state is switched to ON.
2) Alarm interrupts are disabled by default.

Note: In PINE OS, this function is supported by BIOS TIMDAT and MASKI.

(18) Alarm on

Function: Enables alarm interrupts.

Sequence:



Explanation:

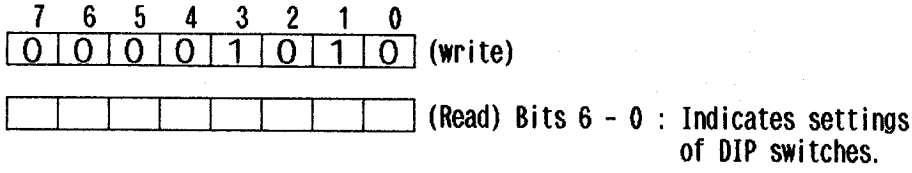
1) This command is used to enable the Z-80 CPU for alarm interrupts.
2) Alarm interrupts are generated at the alarm time specified by command (16).

Note: In PINE OS, this function is supported by BIOS TIMDAT and MASKI.

(19) DIP switch read

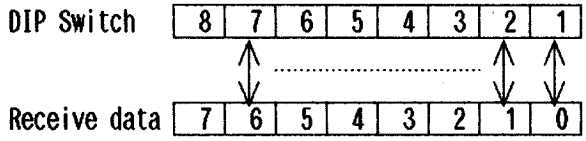
Function: Reads the settings of the DIP switches on the rear panel of the main unit.

Sequence:



Explanation:

1) The figure below shows the correspondence between the DIP switches and receive data bits.



2) In the receive data, a 1 bit indicates that the DIP switch is set to ON, and a Ø bit indicates OFF. The MSB (bit 7) indicates the keyboard type regardless of individual DIP switch settings.

MSB = 1 : Item keyboard
= Ø : Standard keyboard

Note: In PINE OS, the DIP switch bits are used to specify the following items:

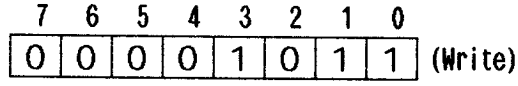
DIP switch bit 8 : Keyboard type
bits 7, 6 : LST: device
bits 4-1 : Character set setting

This function is supported by BIOS READSW.

(2Ø) STOP key interrupt disable

Function: Enables the Z-8Ø CPU for keyboard interrupts.

Sequence:



Explanation:

1) This command is used to enable the Z-8Ø CPU for keyboard interrupts.
2) This command performs the same function as command (11).

(21) STOP key interrupt enable

Function: Enables the Z-80 CPU only for STOP key interrupts and disables all other keyboard interrupts.

Sequence:

7	6	5	4	3	2	1	0	
0	0	0	1	1	0	1	1	(Write)

Explanation:

1) This command is used to enable the Z-80 CPU only for the STOP key interrupt. After this command is executed, no keyboard interrupts other than the STOP key interrupts can be generated. The key code of a pressed key is placed in the key buffer.
2) If an item keyboard is installed, sending this command leads to the same result as executing command (10). Remember that the item keyboard has a different key code system than the standard keyboard.

Note: In PINE OS, this function is used in BIOS BEEP processing and supported by BIOS MASKI.

(22) 7 chraracter buffer

Function: Sets the keyboard buffer length to 7 characters.

Sequence:

7	6	5	4	3	2	1	0	
0	0	0	0	1	1	0	0	(Write)

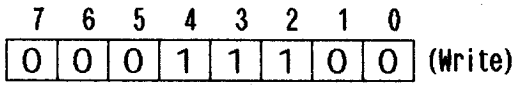
Explanation:

1) This command is used to set the 7508 keyboard buffer length to 7 characters. Unsent key data is temporarily stored in the buffer.
2) Extra key or switch codes are ignored when the buffer is full. However, the STOP key code can be added to the end of the buffer.
3) The keyboard buffer length is set to 7 characters by default.

(23) 1 chraracter buffer

Function: Sets the keyboard buffer length to 1 character.

Sequence:



Explanation:

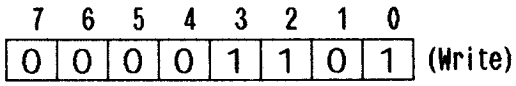
1) This command is used to set the 7508 keyboard buffer length to 1 character.
2) The 1 character buffer performs the same function as the 7 character buffer mentioned by command (22).

Note: PINE OS provides a keyboard buffer which can store up to 32 characters.

(24) 1 sec. interrupt off

Function: Disables one second interrupts.

Sequence:



Explanation:

This command is used to disable one second interrupts from the 7508. After this command is executed, the Z-80 CPU is disabled for 1-second interrupts.

Notes:

1) In PINE OS, this function is supported by BIOS MASKI.
2) In PINE OS, 1-second interrupts are used to control the clock under the following conditions:
   (1) When checking auto power-off time
   (2) When the alarm screen is displayed
   (3) When ROM cartridge power is off

   After this command is executed, the clock cannot be controlled under the conditions listed above.

(25) 1-second interrupt on

Function: Enables 1-second interrupts from the 7508.

Sequence:

7	6	5	4	3	2	1	0	
0	0	0	1	1	1	0	1	(Write)

Explanation:

This command is used to enable 1-second interrupts from the 7508. After this command is executed, the Z-80 CPU is enabled for 1-second interrupts.

Notes:

1) In PINE OS, this function is supported by BIOS MASKI.
2) In PINE OS, this command is issued during reset processing or system initialize processing.

(26) KB clear

Function: Resets keyboard buffer data.

Sequence:

7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	0	(Write)

Explanation:

1) This command is used to clear the 7508 keyboard buffer, scan the keyboard and load information concerning the currently pressed key into the buffer.
2) This command differs from command (3). It does not initialize the keyboard status (e.g. the repeat start time).

Note: In PINE OS, this command is used to scan the key codes which were stored in the buffer before the STOP key was pressed.

(27) System reset

Function: Resets the 7508 CPU.

Sequence:

7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	1	(Write)

Explanation:
This command is used to reset (initialize) the 7508 CPU.

Note: This command cannot be used in application programs. The PINE starts system initialize processing when it receives a System Reset command.

CHAPTER 4 PINE INTERFACES

CHAPTER 4 PINE INTERFACES

This chapter discusses the interfaces for the following PINE facilities:

1. Cartridge
2. Serial communication facilities
3. System bus
4. Others

4.1 Cartridge Interface

4.1.1 General

The PINE is provided with a cartridge interface which interfaces to optional equipment such as the microcassette, ROM cartridge, RAM cartridge, cartridge printer, and universal cartridge. The cartridge interface operates in different modes depending on the optional unit connected. There are four cartridge interface modes: HS, IO, DB, and OT modes.

For cartridge devices, see Section 5.1, "Cartridges" in Part II "Software."

4.1.2 Cartridge Interface Modes

(1) HS mode (Hand Shake mode)
The HS mode is available for optional devices which has a processor. In this mode, data transfer is done between the input and output buffers. Handshaking is controlled by flags IBF and OBF.
(2) IO mode (Input/Output port mode)
In this mode, the cartridge interface controls transfer between a 4-bit input port and a 4-bit output port.
(3) DB mode (Data Bus mode)
This mode permits the PINE to treat the optional device as an ordinary IC device. The cartridge interface connects the main unit data bus directly to the cartridge data bus.
(4) OT mode (Output port mode)
In this mode, the cartridge interface serves as an 8-bit output port.

4.1.3 Selecting the Mode

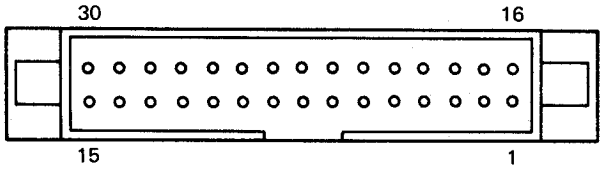
The operating mode of the cartridge interface can be selected by setting cartridge switches CSW1 and CSW0 (bits 1 and 0) of SWR (at P18H). CSW1 and CSW0 are initialized to 0 (HS mode) by an initialize routine implemented in a gate array.

CSW1	CSW0	Mode
0	0	HS mode
0	1	IO mode
1	0	DB mode
1	1	OT mode

4.1.4 Cartridge Connector Pin Assignments

The table below shows the cartridge connector pine assignments.

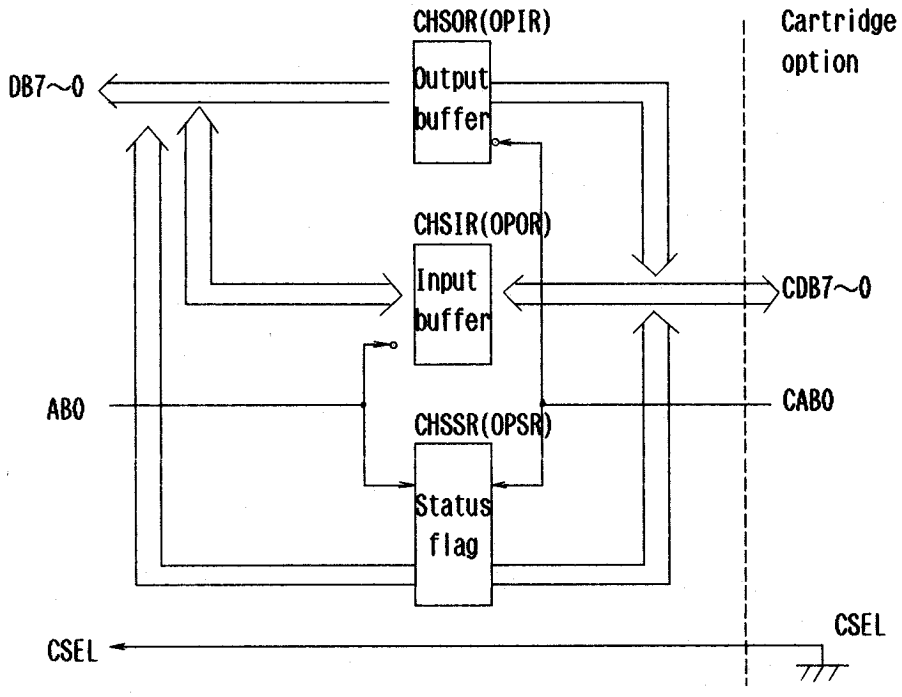
Pin No.	Name	Pin No.	Name
1	GND (ground for ±5V)	2	CAUD (audio input)
3	CDB4 (data bus)	4	$\overline{\text{CRD}}$ (read signal)
5	CDB0 (data bus)	6	$\overline{\text{CITO}}$ (interrupt)
7	$\overline{\text{CCS}}$ (chip select)	8	$\overline{\text{CRS}}$ (cartridge set)
9	CAB0 (address bus)	10	CSEL (mode select input)
11	GND (ground for VB1)	12	CDB2 (data bus)
13	VB1	14	CRXD (serial input)
15	−5V	16	+5V
17	CG (case ground)	18	CDB1 (data bus)
19	CG (case ground)	20	CAB1 (address bus)
21	FPOF	22	CDB7 (data bus)
23	CDB3 (data bus)	24	CEN
25	$\overline{\text{CWR}}$ (write signal)	26	CTXD (serial output)
27	CDB6 (data bus)	28	$\overline{\text{RS}}$ (reset)
29	CDB5 (data bus)	30	VB2



Name	H S	D B	I O	O T
CCS	(Input) Chip select input	(Output) Chip select output	Not used	Not used
CAB1	(Input) General-purpose input line	(Output) Address output	Not used	Not used
CABO	(Input) Address input	(Output) Address output	Not used	Not used
$\overline{\text{CRD}}$ $\overline{\text{CWR}}$	(Input) Read/Write pulse	(Output) Read/Write pulse	Not used	Not used
CDB 7~0	(I/O) Data bus input/output	(I/O) Data bus input/output	(Output) Port output (CDB - 7 CDB - 4) (Input) Port input (CDB - 3 CDB - 0)	(Output) 8 - bit port output
CSEL	(Input) Selects the optional device. CSEL = 0 : HS mode cartridge = 1 : Non HS mode cartridge			
$\overline{\text{CITO}}$	(Output) Interrupt signal	Not used	Not used	Not used
CAUD	(Input) Digital audio signal to SP (loud speaker)			
CTXD	(Output) Serial transmit data line			
CRXD	(Input) Serial receive data line			
$\overline{\text{CRS}}$	(Output) Reset signal to the cartridge option, Set to 0 by an initial reset.			

(Input) = Cartridge → PINE
(Output)= PINE → Cartridge

4.1.5 HS Mode



(1) Explanation
In the HS mode, the PINE interfaces to the optional cartridge unit through an input and output buffers. When the PINE writes a byte into the output buffer, the optional unit can read it. When the optional unit writes a data byte into the input buffer, the PINE can read it. Handshaking is controlled by OBF (Output Buffer Full) and IBF (Input Buffer Full). CDB7-CDB0, CAB0, $\overline{CRD}$, $\overline{CWR}$, and $\overline{CCS}$ are sent from the optional unit.

The cartridge interface identifies a byte sent from the PINE with ASB0 set to 1 as a command and a byte sent with ASB0 set to 0 as a data byte. The value of AB0 is latched into status flag register bit F0. The optional unit can read this flag with a Status Read.

When a byte is written into the output buffer, whether it is a command or data byte, OBF is set to 1 and $\overline{CIT0}$ to 0, generating an interrupt request to the optional unit. The state of OBF can be read by both the PINE and optional unit with a Status Read (the role of OBF and IBF is reversed between the PINE and optional unit; OBF viewed from the PINE is interpreted as IBF by the optional unit).

The optional unit identifies the occurrence of a data write from the PINE through an interrupt or status read and takes in the write data with the state of command/data flag F0. OBF is reset to 0 and $\overline{CIT0}$ to 1 when the output buffer is read by the optional unit. The optional unit reads the output buffer with CAB0 set to 0 and reads status with CAB0 set to 1.

When the optional unit writes a byte into the input buffer (the type of data written by the optional unit is irrelevant, so the CAB0 state is a don't care. However, CAB0 is set to 0 by convention), IBF is set to 1. The PINE can tests this state with a Status Read and reads the data from the input buffer. IBF is reset to 0 by reading the input buffer. The PINE reads the input buffer with AB0 reset to 0 and reads status with AB0 set to 1.

In the HS mode, CAB1 is used as not an address line but as a general-purpose input from the optional unit. The state of CAB1 can be read by the PINE as part of status data.
When the cartridge unit is used in the HS mode, CSEL must be pulled down to the 0 level.

(2) I/O address space
The I/O address space in the HS mode is shown in the table below.

HS mode I/O address space

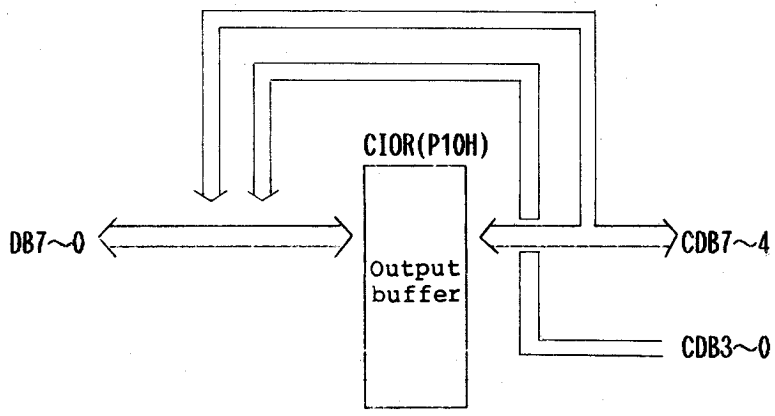
R/W	I/O address	Register Name	7	6	5	4	3	2	1	0	Flag
READ	10H	CHSIR	8 bits data								IBF reset
	11H	CHSSR						CAB1	IBF	OBF	
	12H	Not used (access inhibited)									
	13H										
Write	10H	CHSOR	8 bits data								OBF set, F0=0
	11H	CHSOR	8 bits command								OBF set, F0=1
	12H	Not used (access inhibited)									
	13H										

I/O address space as viewed from the cartridge option

R/W	CAB0	Register Name	7	6	5	4	3	2	1	0	Flag
READ	0	OPIR	8 bits data								OPIBF reset
	1	OPSR					F0		OPIBF	OPOBF	
WRITE	0	OPOR	8 bits data								OPOBF reset
	1		Not used (access inhibited)								

Note the following relationships:
OPIR = CHSOR OPOR = SHSIR
OPIBF = OBF OPOBF = IBF

4.1.6 IO Mode



(1) Explanation
In the IO mode, the cartridge interface consists of a 4-bit output port (CDB7-CDB4) and a 4-bit input port (CDB3-CDBØ). Output data is latched into an 8-bit latch (CIOR). Input data is read directly (without latching) into the CPU over CDB3 through CDBØ. The address of the input/output port it 1ØH.

When the PINE CPU writes output data into the port at P1ØH, the contents of the 8-bit data bus are latched into the CIOR. THe higher order 4 bits of the CIOR output are connected to CDB7 through CDB4. The lower order 4 bits of the CIOR output are not connected.

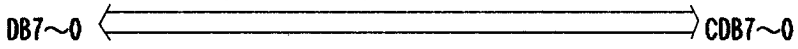
When port P1ØH is read, data from CDB3 through CDBØ are directed directly to the lower four bits of the PINE data bus. The higher order 4 bits of the data bus are loaded with the higher order 4 bits of the output buffer.

In the IO mode, CSEL must be held at the 1 level. $\overline{CCS}$, CAB1, CABØ, $\overline{CWR}$, and $\overline{CRD}$ must be held in the high impedance state, so they must be pulled up or down into the inactive state. The $\overline{CIT0}$ output is set to 1.

(2) IO address space
The IO address space in the IO mode is shown in the table below.

R/W	IO address	Register Name	7 6 5 4	3 2 1 0
READ	10H	CIOR	(Output port contents)	CDB3~0
	11H	Not used (access inhibited)		
	12H			
	13H			
WRITE	10H	CIOR	4 bits data	Don't care
	11H	Not used (access inhibited)		
	12H			
	13H			

4.1.7 DB Mode



(1) Explanation
In the DB mode, the PINE CPU handles the cartridge option as an ordinary I/O device. To the CPU, the cartridge option looks like an I/O device having four I/O addresses.

CDB7 through CDBØ are connected directly to system data bus bits DB7 through DBØ. $\overline{CCS}$, $\overline{CRD}$, $\overline{CWR}$, CAB1, and CABØ are controlled by the CPU; that is, these lines are all output lines.

$\overline{CCS}$ is set to Ø when one of I/O addresses 1ØH through 13H is selected. CAB1 and CABØ serve as the lowest 2 address bits. $\overline{CRD}$ and $\overline{CWR}$ are I/O read and write pulses generated by the CPU.

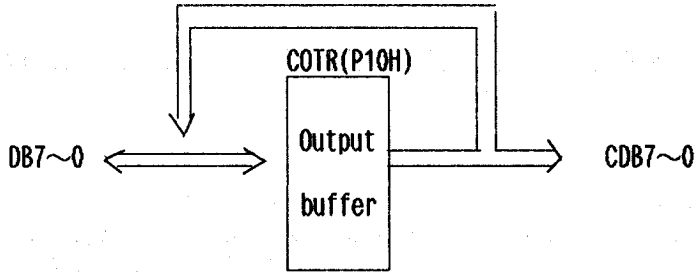
In the DB mode, CSEL must be set to 1 and the $\overline{CIT0}$ output to 1.

(2) I/O address space
The I/O address space in the DB mode is shown in the table below.

R/W	IO address	Register Name	7	6	5	4	3	2	1	0
READ	10H	Defined by the cartridge option.								
	11H									
	12H									
	13H									
WRITE	10H									
	11H									
	12H									
	13H									

Note: The higher 4 bits (bits 7-4) of P13H are used to identify the optional unit.

4.1.8 OT Mode



(1) Explanation
In the OT mode, the cartridge interface consists of an 8-bit output port (latch). The address of the output buffer (COTR) is 10H. When the CPU writes a data byte into port address 10H, the contents of the data bus (DB7-DB0) are latched into the COTR and, simultaneously, placed on the output port pins CDB7 through CDB0. When port 10H is read, the contents of the COTR are read into the CPU.

In the OT mode, CSEL must be held at the 1 level. $\overline{CCS}$, CAB1, CAB0, $\overline{CWR}$, and $\overline{CRD}$ must be held in the high impedance state, so they must be pulled up or down into the inactive state. The CIT0 output is set to 1.

(2) IO address space
The IO address space in the OT mode is shown in the table below.

R/W	IO address	Register Name	7 6 5 4 3 2 1 0
READ	10H	COTR	(Output port contents)
	11H	Not used (access inhibited)	
	12H		
	13H		
WRITE	10H	COTR	8 bits data
	11H	Not used (access inhibited)	
	12H		
	13H		

Note: Physically, CHSOR, CIOR, and COTR refer to the same register.

4.1.9 Identifying the Cartridge Mode

The cartridge interface is initialized to the HS mode and CSW1 and CSWØ are set to Ø when an initial reset is performed. Simultaneously, flags (IBF and OBF) are reset to Ø. In other words, when the PINE is powered on or reset, CDB7-CDBØ, $\overline{CRD}$, $\overline{CWR}$, $\overline{CCS}$, CAB1, and CABØ are placed into the input (high impedance) state, preventing the occurrence of data conflicts even when an optional unit is connected to the cartridge interface in any mode.

The PINE OS establishes the cartridge mode, on an initial reset or when the cartridge option is replaced, all in the HS mode. To do this, the system examines CSEL. If CSEL is Ø, identifying an HS mode option, the system transfers control immediately to the corresponding option handling routine. If CSEL is 1, indicating an option other than HS mode options, the system puts the interface into the DB mode to further identify the cartridge option. In the DB mode, $\overline{CCS}$, $\overline{CRD}$, $\overline{CWR}$, CAB1, and CABØ are all designated as outputs. In the other modes, these signals are not used at all, so no output data conflict can occur. The system then reads P13H and examines the higher order 4 bits. The optional device must supply its device address on CDB7 through CDB4 so that the system can identify the type of the option.

When the system identifies a DB mode option, it transfers control immediately to the corresponding option handling routine. If the option is an IO or OT mode option, however, the system must initialize the output ports before setting up the mode. To do this, the system returns once to the HS mode, writes the initialization data into the higher order 4 bits of the CIOR or 8 bits of the COTR, then sets up the IO or OT mode.

Figure 4.1.1 shows the flowchart for setting up the cartridge mode.

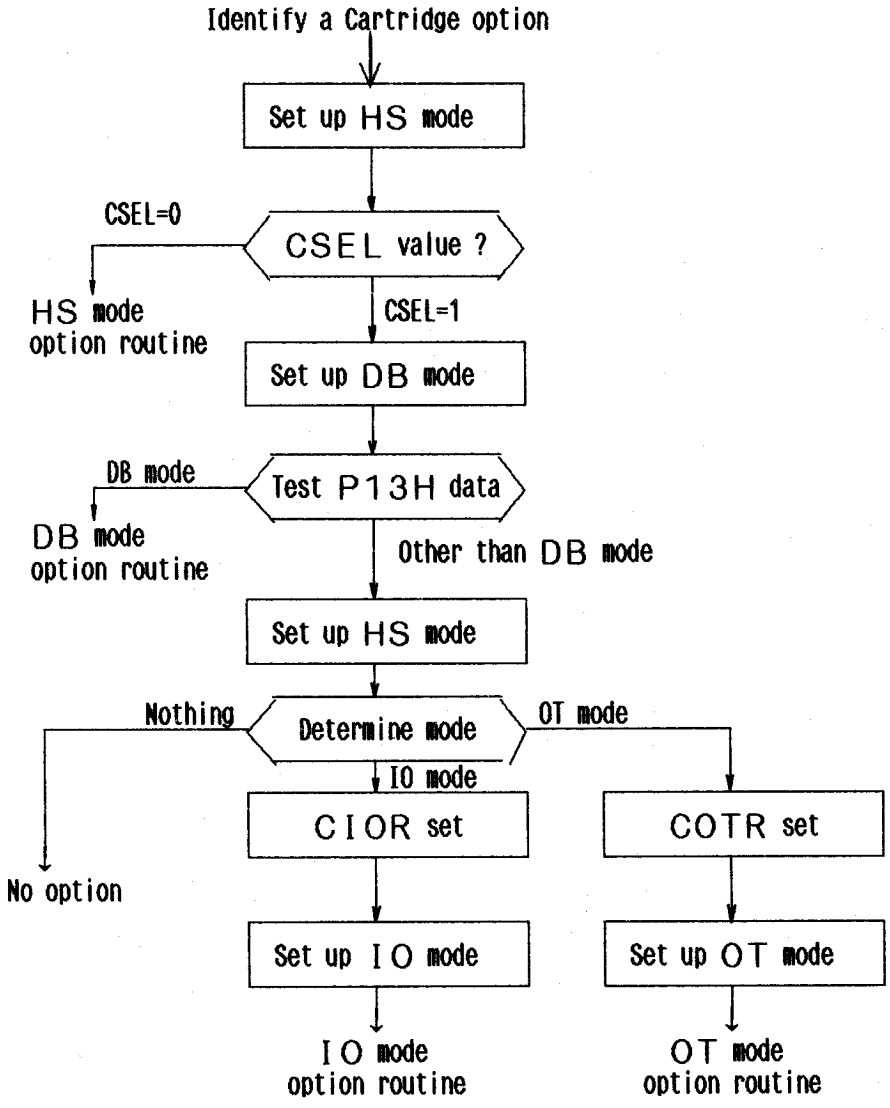


Fig. 4.1.1 Identifying a Cartridge Option

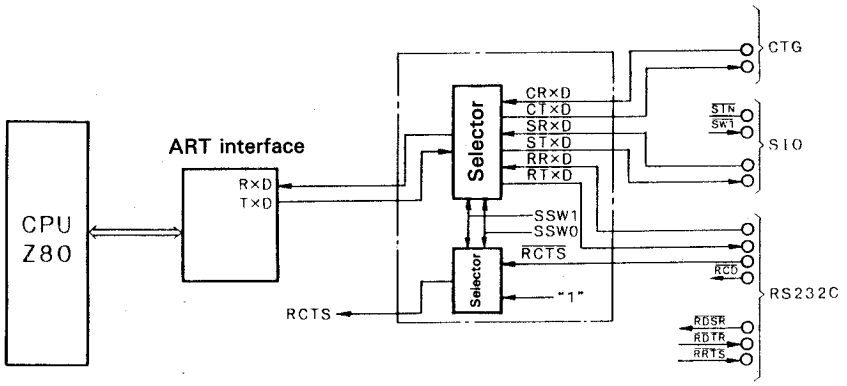
4.2 Serial Interfaces

4.2.1 General

The PINE is provided with three types of serial interfaces (RS-232C, SIO, and CTG SIO). During system operation, one of these interfaces is selected by a serial switch circuit and connected to the (8251-compatible) ART interface.

4.2.2 Serial Switch

The serial interface is selected out of the RS-232C, SIO, and cartridge SIO by select bits SSW1 and SSW0 of SWR (bits 3 and 2). The serial interface block diagram is shown below, followed by a table showing the relationship between the serial interfaces and the values of SSW1 and SSW0.



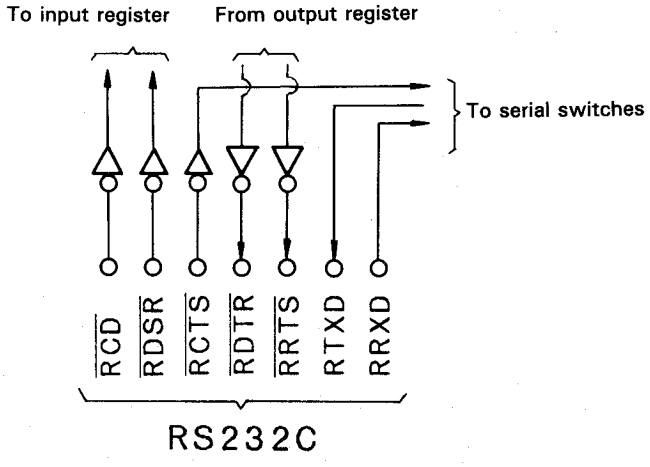
Serial mode	SSW1	SSW0	RXD	TXD	RCTS
0	0	0	(CTG) CRXD	(CTG) CTXD	1
1	0	1	(SIO) SRXD	(SIO) STXD	1
2	1	0	(RS-232C)RTXD	(RS-232C)RTXD	Inverted signal of $\overline{\text{RCTS}}$
3	1	1	(RS-232C)RRXD	(SIO) STXD	Inverted signal of $\overline{\text{RCTS}}$

Serial mode 3 is a special mode in which data is received from the RS-232C interface and sent to the SIO interface. CTXD, STXD, and RTXD are held high (mark level) when not selected.

4.2.3 RS-232C Interface

The RS-232C interface has two data lines (RRXD and RTXD) and three control inputs ($\overline{RCD}$, $\overline{RCTS}$, and $\overline{RDSR}$) and two control output ($\overline{RRTS}$ and $\overline{RDTR}$). RRXD and RTXD are connected to the ART through serial switches. The state of $\overline{RCD}$, $\overline{RCTS}$, and $\overline{RDSR}$ can be read by reading IOSTR bits 4, 5, and ARTSR bit 7, respectively. These signals use negative logic and their state is inverted before being input to the main CPU which uses positive logic. This means that when the signal at a RS-232C terminal is Ø, the corresponding register bit is set to 1.

$\overline{RCTS}$ behaves in different ways depending on the value of serial switches SSW1 and SSWØ. $\overline{RDTR}$ and $\overline{RCTS}$ are the inverted outputs of ARTCR bits 1 and 5. When these bits are set to 1, the corresponding bits at the RS-232C interface are set to Ø.



The RS-232C signals as read by the main CPU from the registers, those at the GAPNIO gate array pins, and those at the RS-232C connector differ in polarity. The polarity of these signals is summarized in the table below.

Signal name	Register	GAPNIO	Connector	Initial value (register bit, GAPNIO pin)
RRXD Receive Data	Note 1	RRXD +	$\overline{\text{RRXD}}$ −	
RTXD Transmit Data		RTXD +	$\overline{\text{RTXD}}$ −	
RRTS Request To Second	ARTCR 5 +	$\overline{\text{RRTS}}$ −	RRTS +	0. 1
RDTR Data Terminal Ready	ARTCR 1 +	$\overline{\text{RDTR}}$ −	RDTR +	0. 1
RCTS Clear To Send	IOSTR 5 +	$\overline{\text{RCTS}}$ −	RCTS +	
RDSR Data Set Ready	ARTSR 7 +	$\overline{\text{RDSR}}$ −	RDSR +	
RCD Carrier Detect	IOSTR 4 +	$\overline{\text{RCD}}$ −	RCD +	

\+ : positive
− : negative

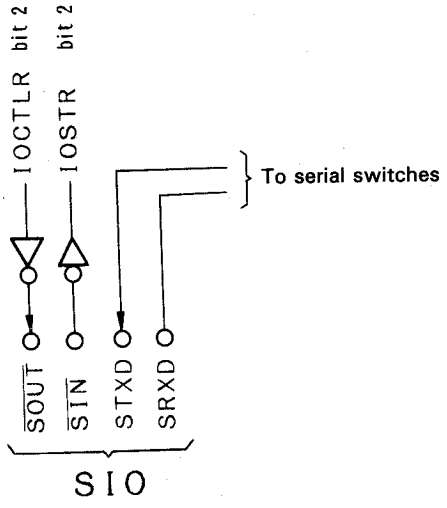
Note 1: The state of RRXD can be obtained by reading IOSTR bit 3 when SSW1 is set to 1.

4.2.4 SIO Interface

The SIO interface is a simplified version of the RS-232C interface. It has two data lines (SRXD and STXD) and two control lines ($\overline{SIN}$ and $\overline{SOUT}$).

SRXD and STXD are connected to the ART through serial switches. $\overline{SIN}$ is an inverted signal of IOSTR bit 2. For example, IOSTR bit 2 is 1 when $\overline{SIN}$ pin is set to Ø. $\overline{SOUT}$ corresponds to IOCTLR bit 2. It is set to Ø when IOCTLR bit 2 is set to 1.

The state of SRXD can be obtained by reading IOSTR bit 3 in serial mode 1.



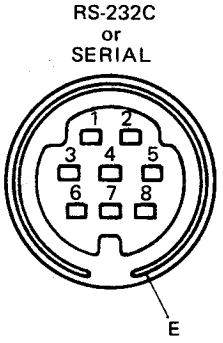
4.2.5 Connectors

(1) RS-232C

Pin No.	Description
1	GND (Ground)
2	$\overline{RTX}$ (Transmit Data)
3	$\overline{RRX}$ (Receive Data)
4	RTS (Request to Send)
5	CTS (Clear to Send)
6	DSR (Data Set Ready)
7	DTR (Data Terminal Ready)
8	CD (Carrier Detect)
E	CG (Frame Ground)

(2) SIO

Pin No.	Description
1	GND (Ground)
2	$\overline{STX}$ (Transmit Data)
3	$\overline{SRX}$ (Receive Data)
4	
5	
6	SIN (Status Input)
7	SOUT (Control Output)
8	
E	CG (Frame Ground)



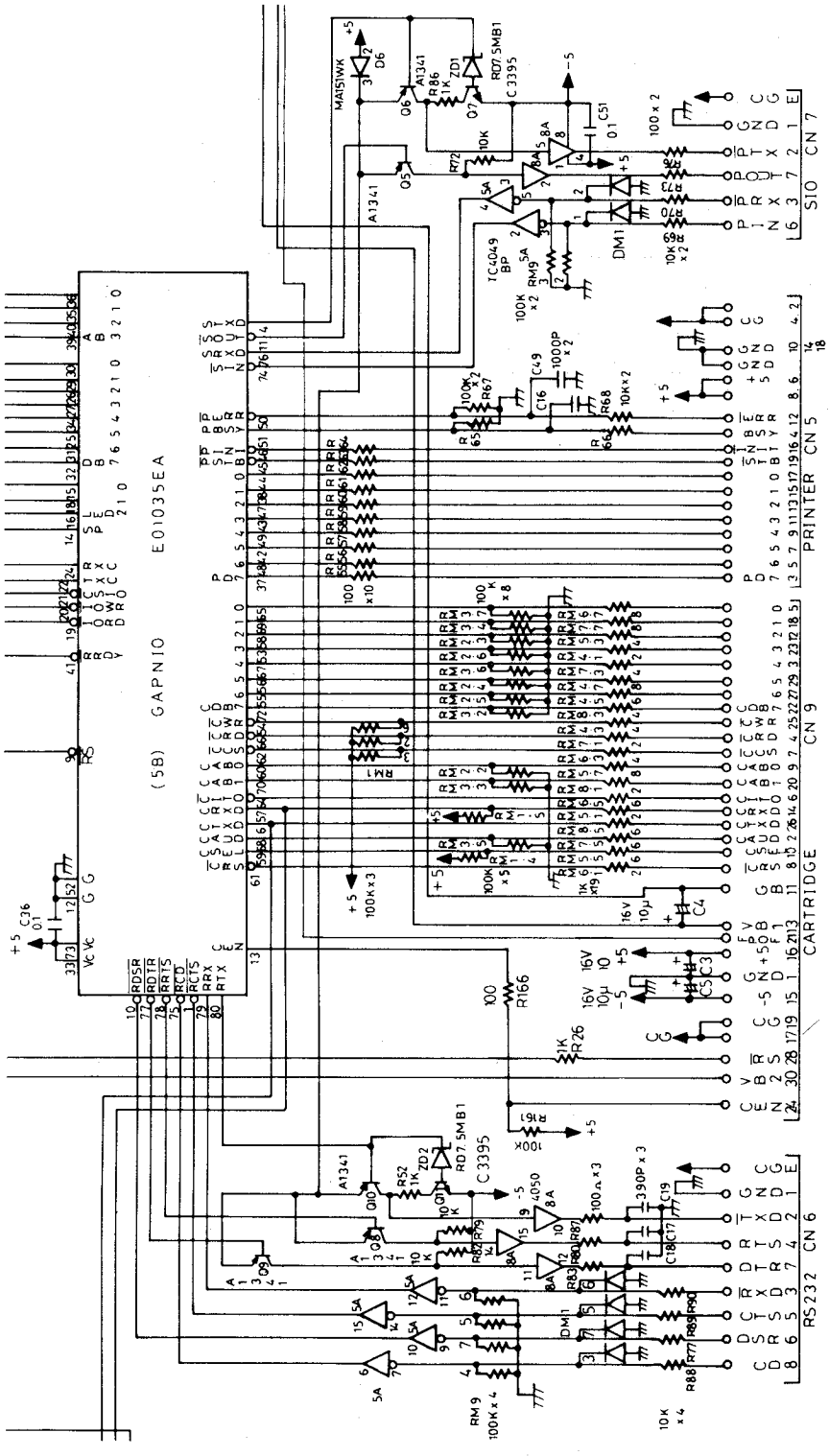


Fig. 4.2.1 Cartridge Interface Circuit Diagram

4.3 System Bus

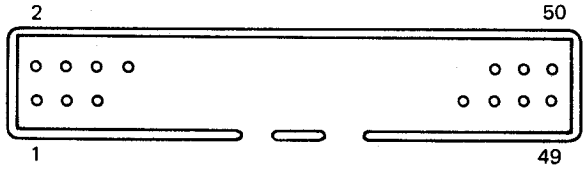
4.3.1 General

The PINE system bus connects to the external RAM disk option. The PINE OS uses I/O port 94H to identify the presence of the external RAM disk unit. This port address must not be used by the user when an external unit other than RAM disk units is connected.

4.3.2 Connector Pin Assignments

Pin	Description	Pin	Description
1	VCH (charge power, 7.8~ 8.8V)	2	VB1 (4.8~ 6.5V, 300mA)
3	VB2 (PW.ON : 5V, 15mA) (PW.OFF: 4.8-6.5V, 0.5mA)	4	VBK (internal battery, 4.8V)
5	GND (VL)	6	VL (5V, 70mA)
7	DB7 (Data bus)	8	DB6 (Data bus)
9	DB5 (Data bus)	10	DB4 (Data bus)
11	DB3 (Data bus)	12	DB2 (Data bus)
13	DB1 (Data bus)	14	DB0 (Data bus)
15	$\overline{MEN}$ (External memory select)	16	$\overline{INTE}$ (Interrupt input)
17	$\overline{WAIT}$ (Wait)	18	$\overline{PON}$ (Power On signal)
19	$\overline{CLK}$ (System clock)	20	CTXD/BUSAK
21	$\overline{RD}$ (Read)	22	$\overline{IORQ}$ (I/O request)
23	$\overline{WR}$ (Write)	24	$\overline{MRQ}$ (Memory Request)
25	$\overline{HLTA}$ (Halt acknowledge)	26	CRXD/BUSRQ
27	CG (Frame ground)	28	CG (Frame ground)
29	$\overline{RS}$ (Reset)	30	$\overline{M1}$ (Machine cycle 1)
31	AB0 (Address bus)	32	AB1 (Address bus)
33	AB2 (Address bus)	34	AB3 (Address bus)
35	AB4 (Address bus)	36	AB5 (Address bus)
37	AB6 (Address bus)	38	AB7 (Address bus)
39	AB8 (Address bus)	40	AB9 (Address bus)

41	AB10 (Address bus)	42	AB11 (Address bus)
43	AB12 (Address bus)	44	AB13 (Address bus)
45	AB14 (Address bus)	46	AB15 (Address bus)
47	OFF (Off signal)	48	DW (Refresh control)
49	DCAS (Refresh control)	50	$\overline{RSI}$ (Reset input)



PON: Generated by the slave CPU to activate the DC-to-DC converter. This line is battery backed up.
OFF: Held at the high level when power is off and used to switch the PINE from the memory backup state to the power-on state. This line is controlled by the slave CPU and battery backed up.
$\overline{CLK}$: Is the 3.6864 MHz system clock.
$\overline{RS}$: System reset signal. This line is battery backed up.
$\overline{RSI}$: Setting this line low generates a reset signal to the PINE CPU.
DCAS: Used by the system bus side to set the PINE into the self-refresh mode. This line is battery backed up.
DW: Same as above.
$\overline{MEN}$: When this line is held low, the main CPU can access the ROM or RAM in the main unit. When this line is set high by the system side, the main CPU can access the ROM or RAM on the system bus side. In this case, the RAM in the main unit is undergo memory refreshing and the main CPU can access the I/O registers with no problem.
$\overline{WAIT}$: WAIT input from the system bus.
$\overline{INTE}$: Interrupt enable signal from the system bus.

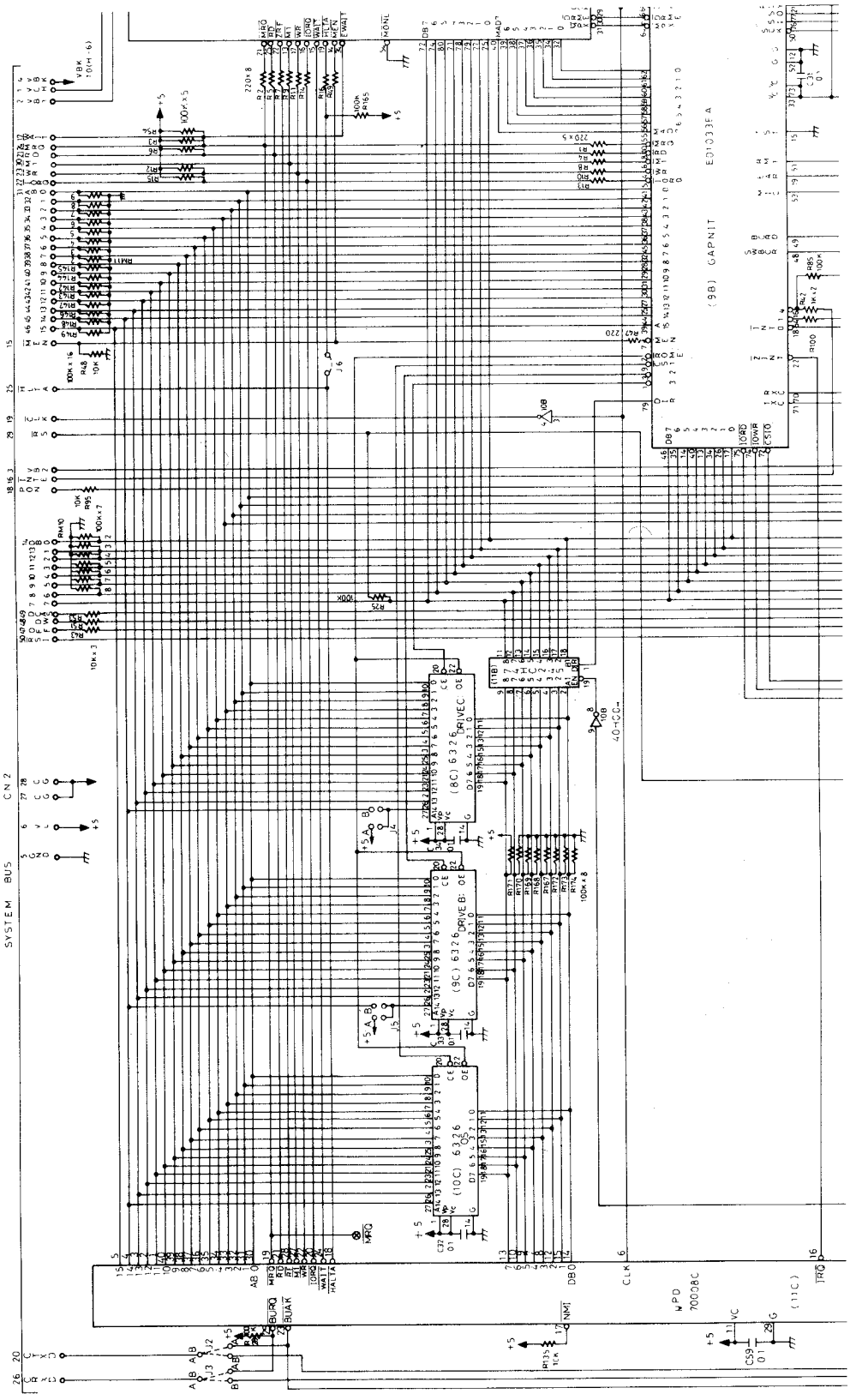


Fig. 4.3.1 System Bus Circuit Diagram

4.4 Other Interfaces

4.4.1 General

This section describes the Printer, loudspeaker, external cassette, and barcode interfaces.

4.4.2 Printer Interface

The Centronics interface is an 8-bit parallel interface which interfaces the PINE to one of the EPSON standard printers. It uses $\overline{\text{PSTB}}$ strobe output and PBSY busy input for handshaking. It has also $\overline{\text{PERR}}$ which indicates printer error status and $\overline{\text{PINI}}$ which initializes the printer. Including data lines, the Centronics interface has a total of 12 signal lines.

(1) Block diagram
Figure 4.4.1 shows the Centronics interface block diagram.

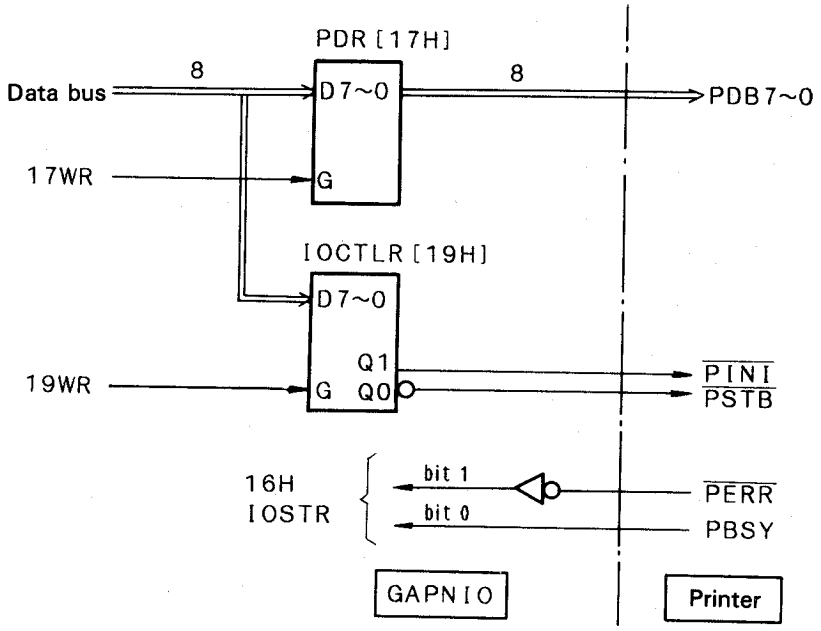
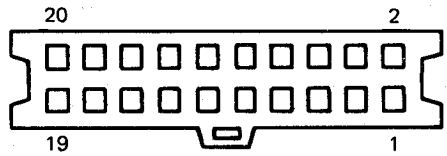


Fig. 4.4.1 Printer Interface Block Diagram

(2) Connector

Pin	Description	Pin	Description
1	CG (Frame ground)	2	CG (Frame ground)
3	PDB7 (Print data)	4	PBSY (Busy signal)
5	PDB6 (Print data)	6	+5V
7	PDB5 (Print data)	8	+5V
9	PDB4 (Print data)	10	GND (Ground)
11	PDB3 (Print data)	12	$\overline{\text{PERR}}$ (Error signal)
13	PDB2 (Print data)	14	GND (Ground)
15	PDB1 (Print data)	16	$\overline{\text{PINIT}}$ (Reset signal)
17	PDB0 (Print data)	18	GND (Ground)
19	$\overline{\text{PSTB}}$ (Strobe signal)	20	NC

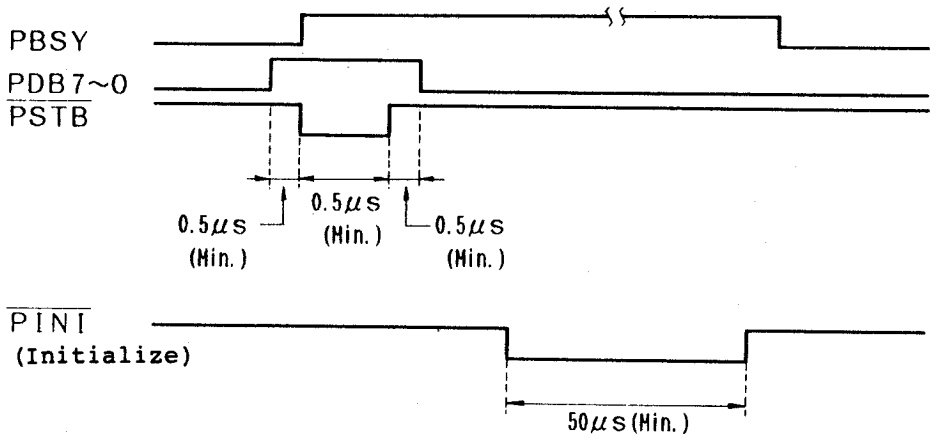
PRINTER



(3) Relationship between register bits and interface pins

pin name	Main unit to printer	Logic	Description	Register bit	Explanation
PDB7~0	→	Positive	8-bit parallel data	[17H] PDR	Writing is into register bits sets the corresponding. PDB pins to 1. PDR can not be initialized.
$\overline{\text{PSTB}}$	→	Negative	Data strove signal with a pulse width of 0.5us minimum. This signal is low active and normally held high.	[19H] IOCTLR bit0 • PSTB	Writing a 1 into IOCTLR bit 0 (PSTB) sets the PSTB pin to 0. Initially, the PSTB bit is reset and the $\overline{\text{PSTB}}$ pin is set to 1.
$\overline{\text{PINI}}$	→	Negative	Initializes the printer controller. This signal has minimum pulse width of 50us. It is active low and normally held high.	[19H] IOCTLR bit1 • $\overline{\text{PINI}}$	Writing a 1 into IOCTLR bit 1 (PINI) sets the $\overline{\text{PINI}}$ pin to 0. The PINI pinis set to 0 by an initial reset.
PBSY	←	Positive	A high in this bit indicates that the printer is busy and cannot receive print data.	[16H] IOSTR bit0 • PBSY	The PBSY register bit is set to 1 when the PSSY pin is set to 1.
$\overline{\text{PERR}}$	←	Negative	A low in this bit indicates that the printer is in an error state.	[16H] IOSTR bit1 • PERR	The $\overline{\text{PERR}}$ register bit is set to 1 when the PSSY pin is set to 0.

(4) Timing chart



4.4.3 Loudspeaker Interface

The loudspeaker interface controls the output signal to the loudspeaker. It inputs the audio signal (CAUD) from the cartridge interface and the SP signal (IOCTLR bit 7) that is set by the CPU and outputs the loudspeaker output.

A switch named AUSW (SWR bit 4) is provided which turns on and off the CAUD signal to the loudspeaker. When this switch is 1, the CAUD signal is passed to the loudspeaker.

(1) Block diagram
Figure 4.4.2 shows the loudspeaker block diagram.

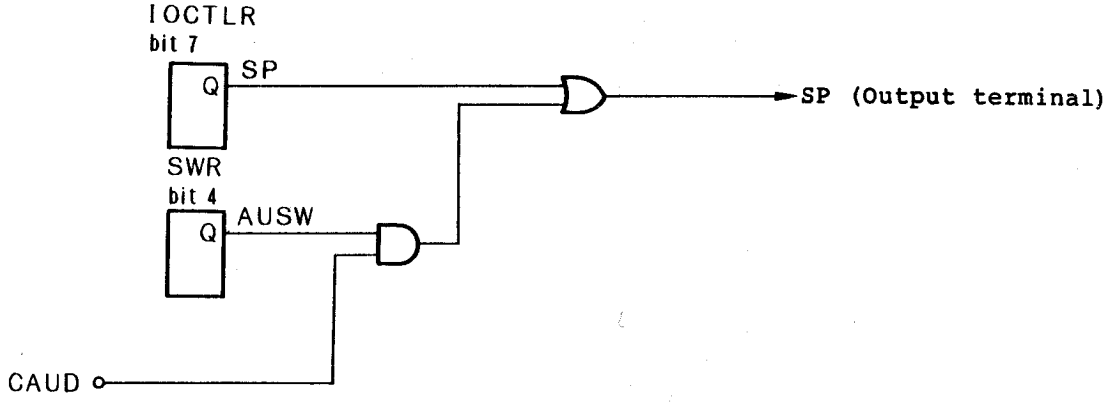


Fig. 4.4.2 Loudspeaker Block Diagram

(2) Loudspeaker signal states
The table below shows the relationship between the SP, AUSW, and CAUD signals.

SP (IOCTLR bit 7)	AUSW (SWR bit 4)	CAUD	Speaker output terminal
0	1	(CAUD)	CAUD
(SP)	0	*	SP
0	0	*	0
(SP)	1	(CAUD)	CAUD+SP

The following four types of signals can be output to the loudspeaker:

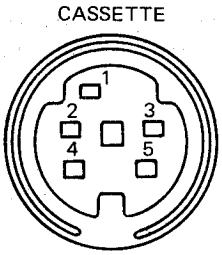
1. CAUD
2. SP
3. Ø
4. Superimposition of CAUD and SP

PINE OS generates beep sounds by turning on and off SP; it does not control the AUSW bit.

4.4.4 Miscellaneous Interface Signals

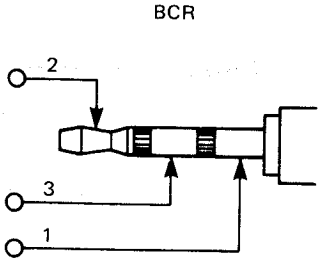
(1) External cassette

Pin No.	Name	
1	GND	(Ground)
2	RMT	(Remote output)
3	RMT	(Remote output)
4	MIC	(Microphone output)
5	EAR	(Earphone input)
E		



(2) Barcode reader

Pin No.	Name	
1	GND	(Ground)
2	BRD	(Barcode data)
3	+5V	(Power source)



(3) External buzzer

Pin No.	Name
1	GND (Ground)
2 , 3	EX
10	SP