Chapter 3

Base Unit

Chapter 3 - Base Unit

3.1 Base unit overview

3.1.1 Base unit configuration

The PX-16 base unit consists of a mother board equipped with many of the functions of the EPSON PCe, a power supply, various interface connectors and a case. This is the core of the PX-16 computer system, and it is supplied with space for three options, namely cartridge 1, cartridge 2 and the external interface. Each may be connected to optional devices as required to provide a variety of system configurations.

3.1.2 Mother board configuration

The PX-16 mother board, the heart of the unit, is composed of the following:
Items marked with (*) are compatible with the EPSON PCe and the IBM PC/XT.

(1) CPU: µPD70108 (V20)

Intel 8088 compatible CMOS CPU
Clock is switchable to 4.77MHz or 10MHz

(2) Slave CPU: µPD75106

4-bit CMOS CPU
Clock is 2.0MHz

This CPU handles keyboard control, real time control (RTC), power supply on/off and power failure detection.

(3) ROM

4M bit mask ROM is supplied as the system ROM (ROM0) in this machine as standard equipment, and application ROMs (ROM1~ROM3) may be CMOS EPROM or CMOS mask ROM devices from 256K bit through 4M bit. The ROMs that may be used are as follow:

ROM0: Mask ROM - 4Mbit, 2Mbit
EPROM - 1Mbit

ROM1~3: Mask ROM - 4Mbit, 2Mbit, 512Kbit, 256Kbit
EPROM - 1Mbit, 512Kbit, 256Kbit

However, the 4Mbit and 2Mbit mask ROMs are 32-pin ROM chip, the 256Kbit and 512Kbit mask ROMs must be pin-compatible with the 27C256/27C512, and the 1Mbit EPROM must be pin- compatible with the 27C1001.

ROM1~3 require switch settings which locate on the mother board as indicated below depending on the size of the ROM used.

ROM size	bit 1	bit 2
256kbit EPROM, mask ROM	ON	OFF
512kbit EPROM, mask ROM	ON	ON
1Mbit EPROM	-	ON
2Mbit mask ROM	OFF	ON
4Mbit mask ROM	OFF	ON

Table 3-1-1 ROM switch setting

For details refer to Section "3.2.3. ROM"

(4) RAM

THe PX-16 uses CMOS 128KB pseudo-static RAM chips, and comes with a standard configuration of 256KB. Installation of the 384KB SRAM board option can be performed to raise the main RAM capacity to the maximum of 640KB, and the RAM disk to a maximum of 768KB.

All of this RAM memory is read/write controlled by the memory control gate array. Refresh is handled automatically and the memory is backed up to prevent data loss even when power is turned off.

(5) T4750 (DMA controller, timer, interrupt controller)*

8237 equivalent: Programmable DMA controller
8253 equivalent: Programmable general-purpose timer
8259 equivalent: Programmable interrupt controller

(6) UART chip (asynchronous communications controller)*

UART (Universal Asynchronous Receiver Transmitter)
Data input from peripheral devices or modems is converted from serial to parallel, and data output by the CPU is converted from parallel to serial.

(7) GAPCAB (address bus buffer)*

Address bus buffer
DMA address upper 4 bits page register

(8) GAPCCK (clock generator)*

Clock generator
Bus controller
Reset controller

(9) GAHIDB (Data bus controller)

Data bus lower 8 bits
Address bus lower 8 bits
DIP switch input port

(10) GAHIMC (memory controller)

Memory (ROM, RAM) control (8255 simulation)
Expansion RAM disk support (Intel Above-Board compatible)
Bank ROM function
8255 equivalent PIO control function

(11) GAHIIO (I/O controller)

I/O address set
Printer interface control
Cartridge 1 interface control (PX-4/HX-40 compatible)
Barcode reader interface control
UART (Universal Asynchronous Receiver Transmitter)
Expansion interrupt controller
System clock control

(12) Cartridge 1 interface

Connector: 30-pin
Control mode: HS, DB, IO and OT
Other: Serial line (1200/75, 75/1200, 110, 150, 200, 300, 600, 1200, 2400, 4800, 9600, 19200, 38400bps)
Interrupt: P-RDY, IBF
HX-40/PX-4 cartridge interface compatible

(13) Cartridge 2 interface

Connector: 80 pin
Other: Additional PX-16 signal for EPSON PCe compatibility. For connection of display units.

(14) Expansion interface

Connector: 80 pin
Other: Additional PX-16 signal for EPSON PCe compatibility.
For connection of communication boards.

(15) System bus

Connector: 80 pin
Other: Additional PX-16 signal for EPSON PCe compatibility.
For connection of disk units.

(16) Printer interface

Connector: 20-pin Mini-Centronics
Other: Centronics compatible

(17) Serial interface

Connector: 9-pin mini-DIN
Baud rate: 110, 150, 300, 600, 1200, 2400, 4800, 9600, 19200, 38400bps)
Output voltage: ±7V
Other: RING detection provided

(18) Barcode reader interface

Connector: 6-pin mini-DIN
Power supply: +5V (software controllable)
Other: HC-10/EHT-10 compatible.
Barcode video input and post-decoding code input selectable.

3.2 Memory

3.2.1 Memory overview

The PX-16 memory consists of the following:

(1) Main RAM - HM658128FP 128KB CMOS pseudo-SRAM

Capacity: 256KB (standard) 640KB (expansion)
Battery back-up
(Write protect and self-refresh functions supported, up to 512KB usable as internal RAM disk)

(2) System RAM HM6116FP 2KB CMOS SRAM

Capacity: 2KB
Battery back-up
(Used for system variable storage)

(3) RAM disk HM658128FP 128KB CMOS pseudo-SRAM

Capacity: 384KB or 768KB by connecting the 384KB RAM board. Adding to the internal RAM disk, RAM disk is expanded up to 1280KB.

(4) Video RAM MB8464A 64KB CMOS SRAM

Capacity: 8KB~16KB. Mounted in display device.

(5) ROM0 32-pin IC socket 1 unit

4Mbit mask ROM (ROMBIOS, MS-DOS Version 3.20, GW-BASIC, utilities)
Usable ROMs: CMOS (1Mbit EPROM, 2Mbit mask ROM, 4Mbit mask ROM)
No-wait, 3-wait control supported.

(6) ROM1~3 32-pin ZIF (Zero Insertion Force) socket 3 units

Usable ROMs: CMOS (256Kbit, 512Kbit EPROM or mask ROM, 1Mbit EPROM, 2Mbit or 4Mbit mask ROM)
3-wait in 10Hz operation
Application ROM sockets

The PX-16 main CPU is capable of directly addressing 1MB, for which reason the RAM disk and ROMs 0~3 are accessed through bank switching.

The PX-16 address map is as indicated below.

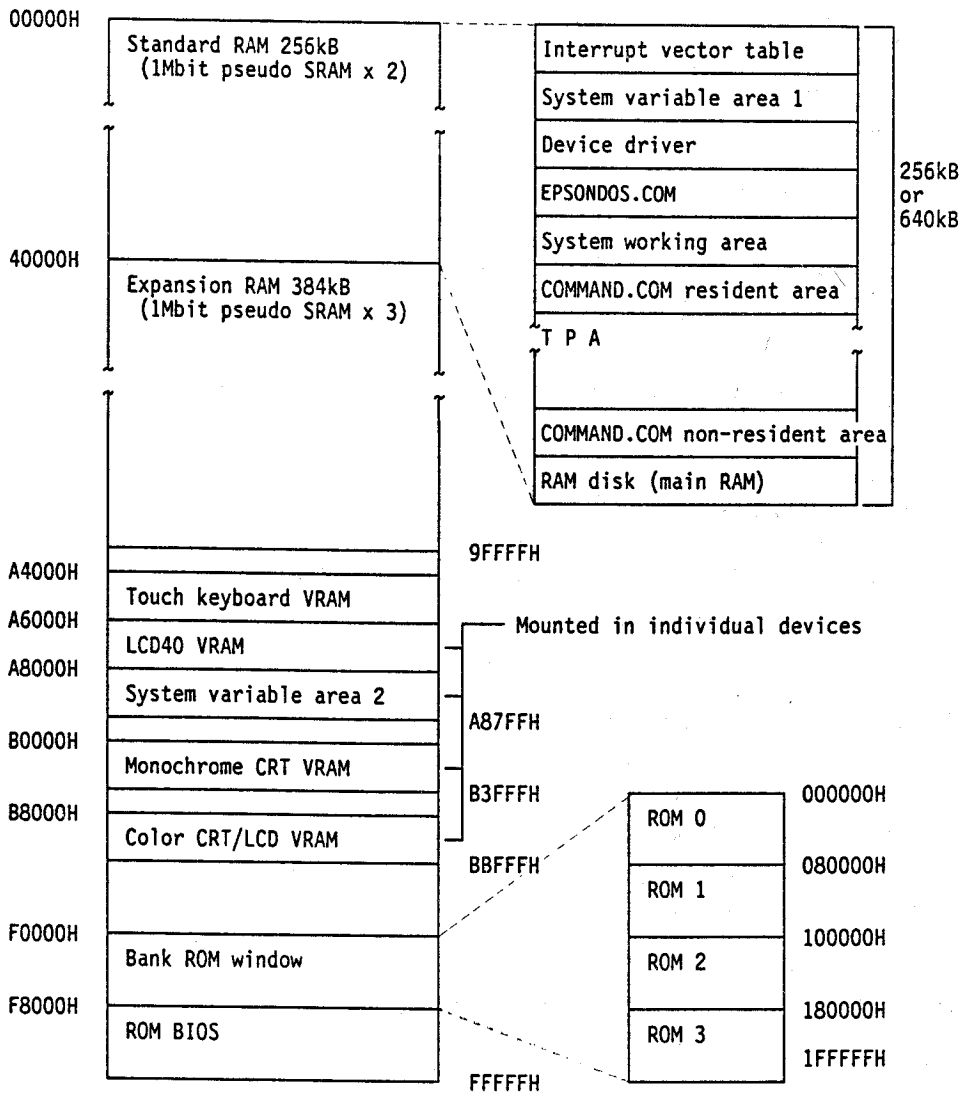


Fig. 3-2-1 Memory map

Note 1: Expansion RAM disk is accessed in free addresses between C4000H~EFFFFH.

Note 2: ROM0~ROM3 are accessed through the ROM access window.

Note 3: ROM BIOS corresponds to the last 32KB of ROM0.

Note 4: All RAM is battery backed-up, but when a cartridge is removed, its internal VRAM will be cleared.

Note 5: System variable area 2 is allocated only in the HC boot mode.

3.2.2 Memory access wait

PX-16 memory access will have varying waits depending on CPU clock speed (4.77 or 10MHz). The memory access waits are as indicated below.

Memory	Wait count	
	4.77 MHz	10 MHz
Main RAM	0	0
System RAM	0	3
RAM disk	0	3
ROM BIOS	0	0 or 3
ROM disk	0	3

Table 3-2-1 Wait count

When ROM BIOS is accessed at 10MHz, if the access speed of the accessed ROM is 150ns or faster 3-wait and no-wait can be selectable. The wait count can be set in bit 6 of I/O register P11E6H. For details, refer to Section 3.6. "I/O register description".

VRAM access is subject to 3-wait operation only when there is conflict between controller VRAM access and CPU VRAM access.

3.2.3 ROM

(1) ROM sockets

The PX-16 has one IC socket (ROM0) for the system ROM, and three ZIF sockets (ROM1~3) for application ROM installation. In other words, a total of four ROM chips can be mounted. These ROM sockets can mount a maximum of 4Mbit (512KB) ROMs, for a total maximum capacity of 2Mbytes. The ROMs that can be used in each socket are given below.

	EPROM			MASK ROM				
	256kb	512kb	1Mb	256kb	512kb	1Mb	2Mb	4Mb
ROM 0	x	x	(3)	x	x	x	(4)	(4)
ROM 1	(1)	(2)	(3)	(1)	(2)	x	(4)	(4)
ROM 2	(1)	(2)	(3)	(1)	(2)	x	(4)	(4)
ROM 3	(1)	(2)	(3)	(1)	(2)	x	(4)	(4)

(1) Pin-compatible with Intel 27C256
(2) Pin-compatible with Intel 27C512
(3) Pin compatible with Intel 27C1001. When ROM0 is a 1Mbit EPROM, jumpers must be set as J3=b, J4=ON and J5=ON (for details, refer to "2.1.2 Switches").
(4) 32-pin ROM

Table 3-2-2 Usable ROM

Depending on the specific ROM size used for ROM1~3, DIP switch setting is also required. When installing a ROM chip, always turn off system power first, set the DIP switches as required, and then install the ROM. ROM1 corresponds to SW8, ROM2 to SW7, and ROM3 to SW6. The appropriate DIP switch setting is given below.

ROM size	bit 1	bit 2
256Kbit EPROM, mask ROM	ON	OFF
512Kbit EPROM, mask ROM	ON	ON
1Mbit EPROM	-	ON
2Mbit mask ROM	OFF	ON
4Mbit mask ROM	OFF	ON

"-" means do not care.

Table 3-2-3 ROM switch setting

ROM 0~3 are all supported by the OS as disk drives, but drive names of ROM disk will vary depending on whether system is in RAM preference or FDD preference. The drive names will be:

	ROM 0	ROM 1	ROM 2	ROM 3
RAM preference	B	C	D	E
FDD preference	E (D)	F (E)	G (F)	H (G)

Table 3-2-4 ROM drive name

Note 1: For FDD preference, if there is no HDD connected to the PX-16, the drive names will be moved up one notch.

(2) ROM format

The PX-16 ROM0~ROM3 chips are all supported by the OS as ROM disks.

ROM0 is the standard system ROM, where the OS is stored. This system ROM stores ROM BIOS, MS-DOS, GW-BASIC, and utilities, and is a 4Mbit ROM as indicated below.

System ROM memory map

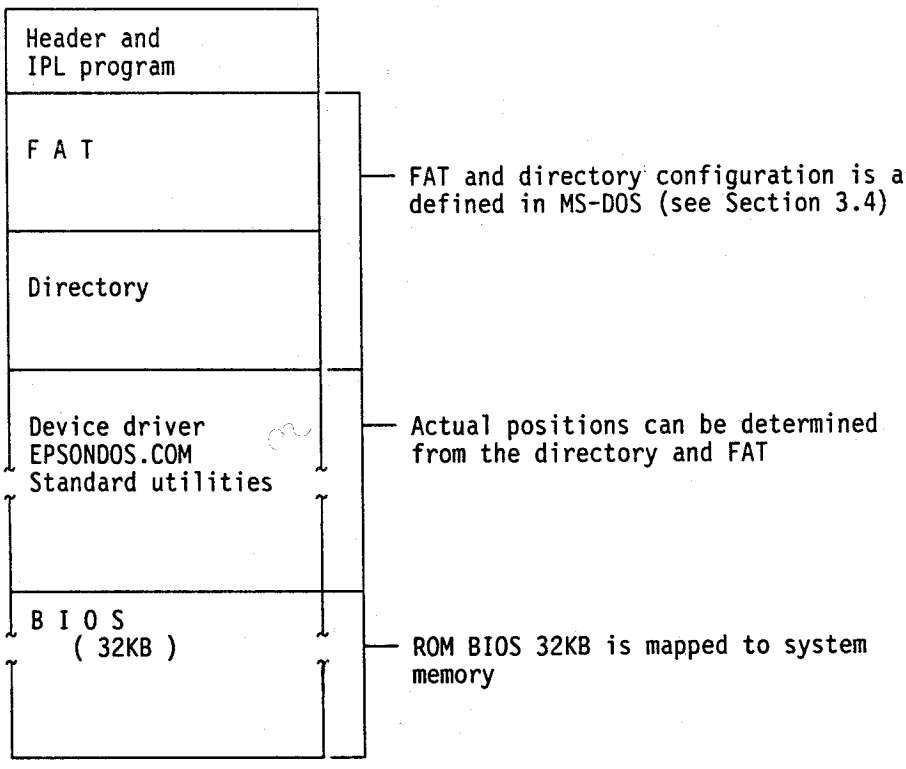


Fig. 3-2-2 System ROM memory map

ROM1~3 can also be mounted with a maximum of 4Mbit (512KB) ROM chips. Each is accessed as a different drive, but it is also possible to define two or three as a single drive. Data essential for disk access for the PX- 16 ROM must be stored in the first 32 bytes. The ROM disk format is as follows:

ROM disk format
Sides/drive: 1
Tracks/side: Dependent on ROM capacity
Sectors/track: 16
Bytes/sector: 512
Sectors/cluster: 1
Directory area: Stored file number/16 sectors (rounded up)

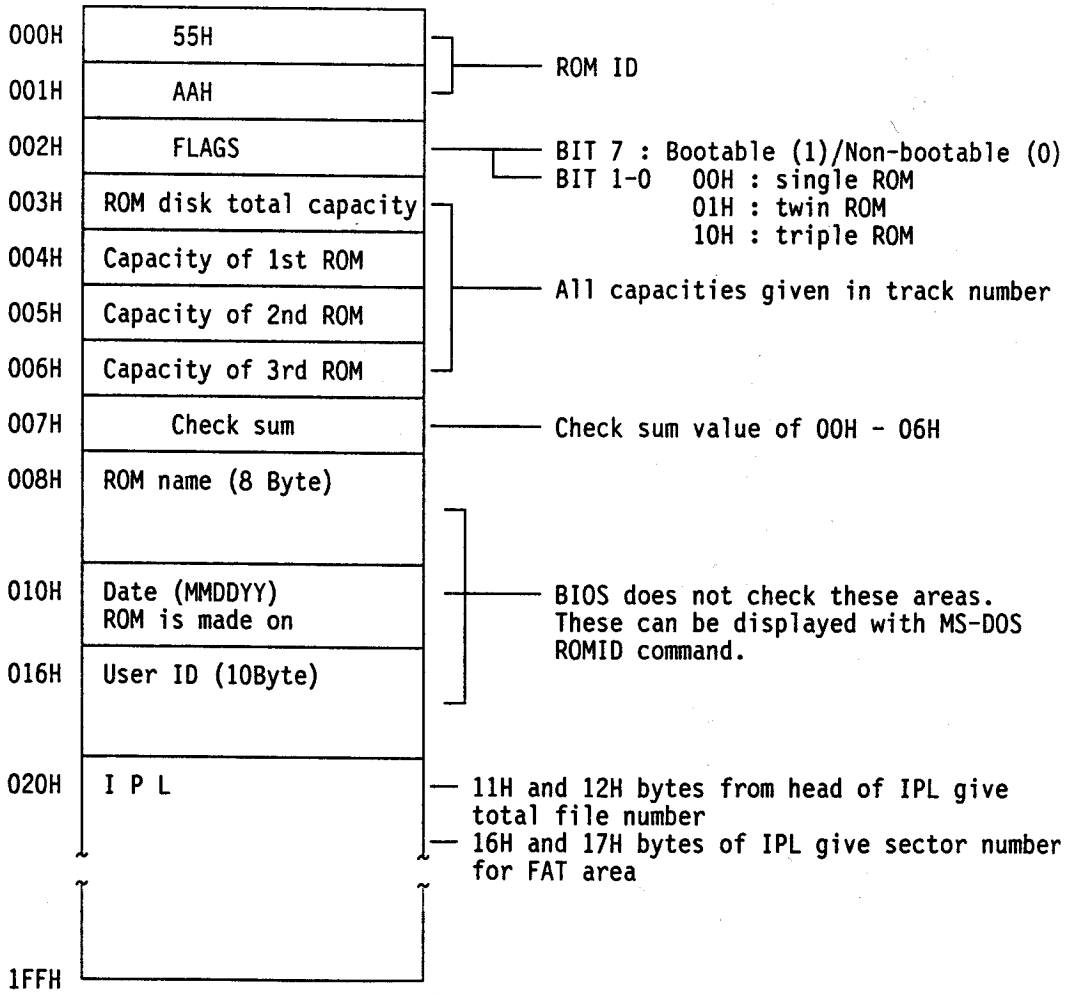


Fig. 3-2-3 Header and IPL format

The ROMFORM utility automatically adds the header shown above to each ordinary file. This makes it possible to write the files into ROM without further modification. For details, see "5.6 ROMFORM".

(3) ROM access

ROM BIOS is stored in the upper 32Kbytes of the ROM0 address, and is mapped to F8000H~FFFFFH of memory (address map). Other ROM memory is accessed through bank switching, with memory addresses F0000H~F7FFFH defined as the ROM access window. ROM addresses that can be accessed through bank switching are from 000000H~200000H (2Mbytes), in order of ROM0, ROM1, ROM2, and ROM3, with each ROM assigned 512Kbytes (4Mbits).

The ROM access I/O ports (registers) are in address P11E7H, and are write only.

I/O address	Name	R/W	Bit							
			7	6	5	4	3	2	1	0
P11E7H	ROM bank register	W	ROM EN	RAM EN	A20	A19	A18	A17	A16	A15

A20~A15 written to the ROM bank register are synthesized with A14~A0 output from the CPU to generate a 21-bit address and access ROM.

High-speed access

ROM BIOS

When the system clock is set to high-speed operation (10MHz) and ROM BIOS is to be accessed (F8000H~FFFFFH), the wait count can be set to 0 or 3 waits. This setting is handled by bit 6 of I/O address P11E6H. Refer to Section 3.6 for details.

Bank ROM

When the system clock is in high-speed mode (10MHz) and the bank ROM (F0000H~F7FFFH) is accessed, three waits are automatically inserted.

3.2.4 RAM disk

(1) Overview

The PX-16 RAM disk is composed of part of the main RAM (internal RAM disk) and the expansion RAM disk. When the main RAM is the standard 256Kbytes, a maximum of 128Kbytes can be allocated as RAM disk, or a maximum of 512Kbytes when the RAM has been expanded to 640Kbytes. The internal RAM disk specification within main RAM can be defined in 32Kbyte units for cold-starting.

The expansion RAM disk is either 384Kbytes or 768Kbytes, depending on the mounting of the 384Kbyte RAM board. The expansion RAM disk can be used as an extension of the internal RAM disk. The expansion RAM disk is compatible with the Intel Above-Board specification.

RAM disk sumcheck is performed at read/write to check that the data has not been corrupted.

The PX-16 can mount a maximum of 1280Kbytes of RAM disk (Sum of the internal RAM disk and expansion RAM disk), which can be supported by the OS for use as a high-speed, large-capacity disk drive.

(2) RAM disk format

The PX-16 RAM disk format is as follows:

Disk size	32kB	64kB	128kB	384kB	512kB	786kB	896kB	1280kB
Bytes/sector	512 Bytes							
Sectors/track	16 sectors							
Tracks/side	4	8	16	48	64	96	112	160
Sides/drive	1							
Directories	112							
Number of FAT	1							
FAT ID	0FBH							

Table 3-2-5 RAM disk format

(3) RAM disk access

The PX-16 RAM disk is equipped with four 8-bit bank registers. This enables the system to access up to 2Mbytes of memory space.

Name	R/W	Bit							
RAM disk bank register		7	6	5	4	3	2	1	0
	W	ENABLE	A20	A19	A18	A17	A16	A15	A14

1 : Access enabled

0 : Access disabled

I/O address	Selected register
0258H	Register selected when A15=0 and A14=0
4258H	Register selected when A15=0 and A14=1
8258H	Register selected when A15=1 and A14=0
C258H	Register selected when A15=1 and A14=1

Table 3-2-6 Selection of Bank register

For RAM disk bank access, a bank access window is taken at the free area between C4000H ~ EFFFFH. The bank access window is allocated in 16K bytes units, whose sum is 64K bytes. The start address for this window is determined by the values of bit 7 for I/O addresses P0259H, P4259H and P8259H, as indicated below.

Start address	Bit 7 of 8259H	Bit 7 of 4259H	Bit 7 of 0259H
C4000H	0	0	0
C8000H	0	0	1
CC000H	0	1	0
D0000H	0	1	1
D4000H	1	0	0
D8000H	1	0	1
DC000H	1	1	0
E0000H	1	1	1

Table 3-2-7 Start address for Bank Access window

At this time, if data is written to P0259H, P4259H, P8259H and PC259H, a value other than bit 7 is written to P0258H, P4258H, P8258H and PC258H.

For access within the range of the bank access window, the values for A15 and A14 output by the CPU define one of the above bank registers (P0258H, P4258H, P8258H, PC258H). The addresses A20~A14 from the selected bank register are synthesized with addresses A13~A0 output from the CPU, enabling access of the 2Mbyte memory from the address from A20~A0 (RAM disk address).

Access example

The RAM disk access procedure is outlined below.

① 0 is written to I/O register P8259H and 80H to I/O register P4259H.

1) RAM disk can be accessed through D0000H~DFFFFH.

② 88H is written to I/O register P8258H (enabling access) and access D8100H.

2) Address output from the CPU is A15=1, A14=0, so that I/O register P8258H is selected (the content of P8258H becomes the RAM address A20~A14).

3) The content of I/O register P8258H (A20~A14) is synthesized with the output of the CPU (addresses A13~A0), and RAM disk address 20100H is accessed.

Default values

0258H, 4258H, 8258H, C258H bit 7 : 0
0258H, 4258H, 8258H, C258H bits 0~6 : Not fixed
0259H, 4259H, 8259H, C259H bit 7 : 0

Note : If a "1" is written to bit 7 of C259H, $\overline{\text{IOCHCK}}$ will be low when the RAM disk is read causing NMI, and so care is required. To return $\overline{\text{IOCHCK}}$ to high write "0" to C259H and then read the RAM disk again. $\overline{\text{IOCHCK}}$ is latched by the RS latch so that after $\overline{\text{IOCHCK}}$ is returned to high it is necessary to set PB5 of 8255 to high or the value read from 8255 PC6 will not be returned.

(4) Other

① RAM disk access requires bank switching as described above, but this processing is handled by the OS and so the user is not required to control it.

② When the RAM disk is to be initialized, run at least eight dummy cycles for each chip (128KB).

3.3 System Control

3.3.1 System start

(1) Overview

PX-16 IPL is carried out in either HC boot mode (can use all functions unique to PX-16) or PC boot mode (PC compatible mode). The procedure for starting the PX-16 system differs depending on whether HC boot or PC boot mode IPL was executed. Further, there is a system reset switch and a reset switch, and the start will differ depending on whether either has been pushed.

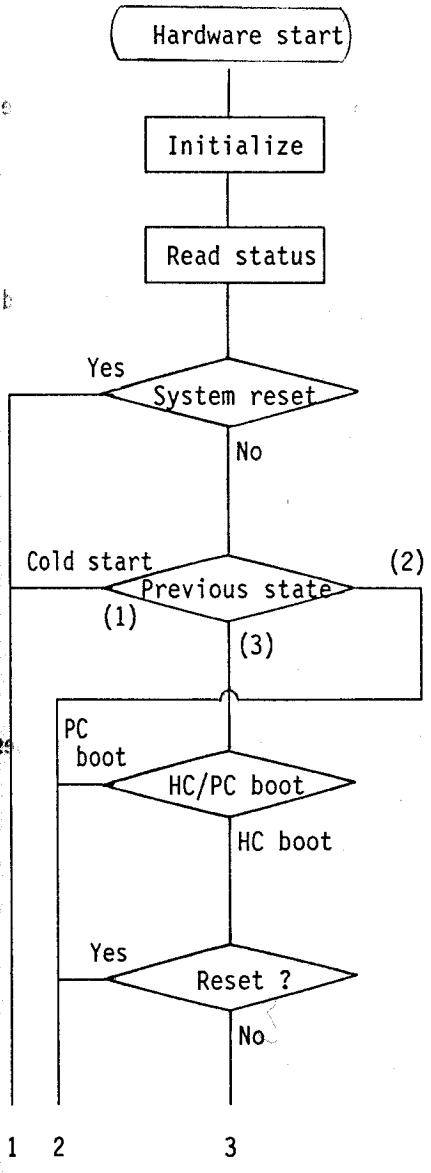
The PX-16 system is started in three modes:

(a) Cold start
(b) Warm start
(c) Resume start

Details on these three start modes follow.

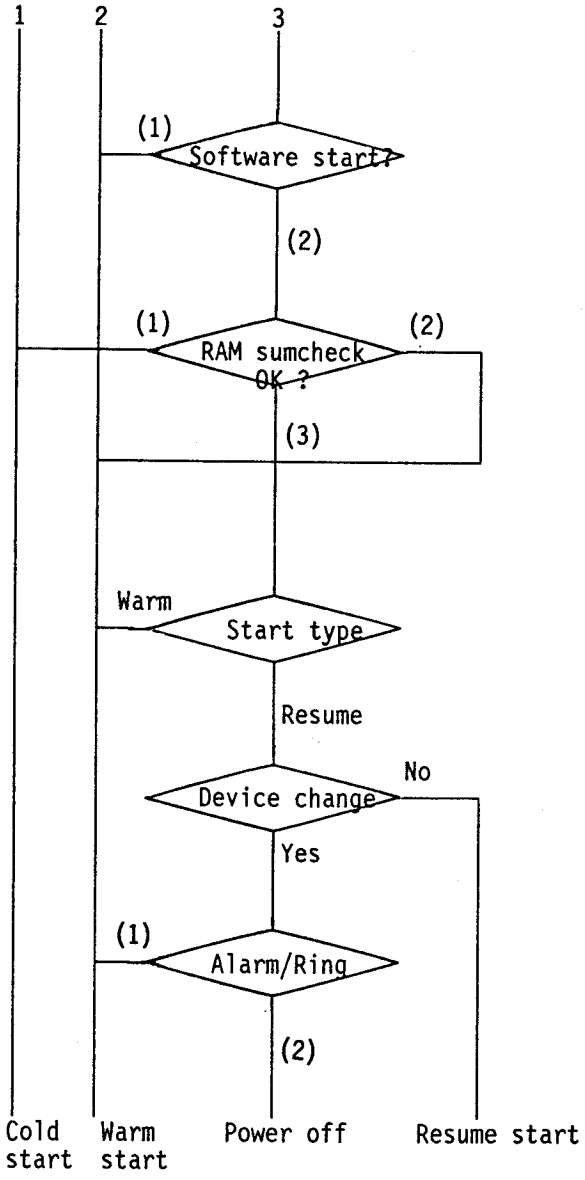
(2) Starting types

System startup types depending on start conditions are given in the following diagram.



IPL processing	step	Description
Hardware start	1	Power on
Initialize	2	Disables interrupts, opens system RAM disk, turns off display, etc.
Read status	3	Reads interrupt and power-on status from slave CPU
System reset	4	Determines if system turned off by system reset switch
Previous state	5	Examine previous processing environment when power is turned off; (1) During cold start is executing (2) During processing other than cold start is executing (3) Other
HC/PC boot	6	Checks DIP switch setting.
Reset ?	7	Examine reset switch is pressed;

Fig. 3-3-1 IPL Process (1)



IPL processing	step	Description
	8	Determine if start is software start (1) CTRL + ALT + DEL (2) Power switch
	9	Execute sumcheck for installed RAM (1) system RAM error (2) Main RAM, expansion RAM error (3) Normal (no errors)
	10	Determine if warm start or resume start
	11	Check if any change is statuses of devices installed to base unit
	12	Check cause of power ON (1) Power switch (2) Alarm/Ring
Cold start Warm start Power off Resume start		To system start processing

Note: Steps 5 to 8 are all provided to see if step 9 (RAM sumcheck) is required or not

Fig. 3-3-2 IPL Process (2)

(3) Cold start

The cold start sequence initializes all PX-16 system, and is initiated by the following codi-tions;

① System reset switch is pressed
When the system reset switch is pressed whether the PX-16 is power OFF or ON, the PX-16 is forced into the power-off state. When the PX-16 is power OFF and the system reset switch is pressed, the fact that the system reset switch is pressed is stored by the slave CPU as status, and causes a system reset (cold start) when power is turned on subsequently.

② A starter is restarted during cold start processing.
This condition occurs when a power-on sequence is executed after a power-off during cold start processing or when a reset occurs during cold start processing (Note 1).

③ One of the following errors is found during warm or resume start processing:
(i) The RAM size (main or expansion RAM) or the RAM disk size has been changed.
(ii) A corruption in system RAM has been found during HC boot.

Note 1: The "cold start processing" is from turning on the PX-16 to when control is trans-ferred to BIOS (with INT 18H or INT 19H).

The following actions are taken during cold start processing (See fig. 3-3-2):

① Power-on self-test
The available devices are checked. See subsection "(6) Power-on Self-test" for details.

② Memory check and display
The entire main RAM area is checked and the available size is displayed. When the PX-16 is started in HC boot, the expansion RAM disk is checked and its available size is displayed.

③ RAM disk creation (only HC boot)
The message "00 x 32KB RAM disk assign" will be displayed, and numeric input is enabled. If the RAM disks specified by the input cannot be secured, a beep will result and the system will request new input.

④ Hardware reset
The available devices are initialized. See subsection "(6) Power-on Self-test" for details.

⑤ Interrupt vector setup
An extended vector table is created in the HC boot mode and a PC compatible inter-rupt table is created in the PC boot mode.

⑥ System variable setup
The system variables are initialized. See Section "3.3.6 System variables" for details.

⑦ IPL
INT 18H is issued in the HC boot mode and INT 19H in the PC boot mode.

<Cold start processing>

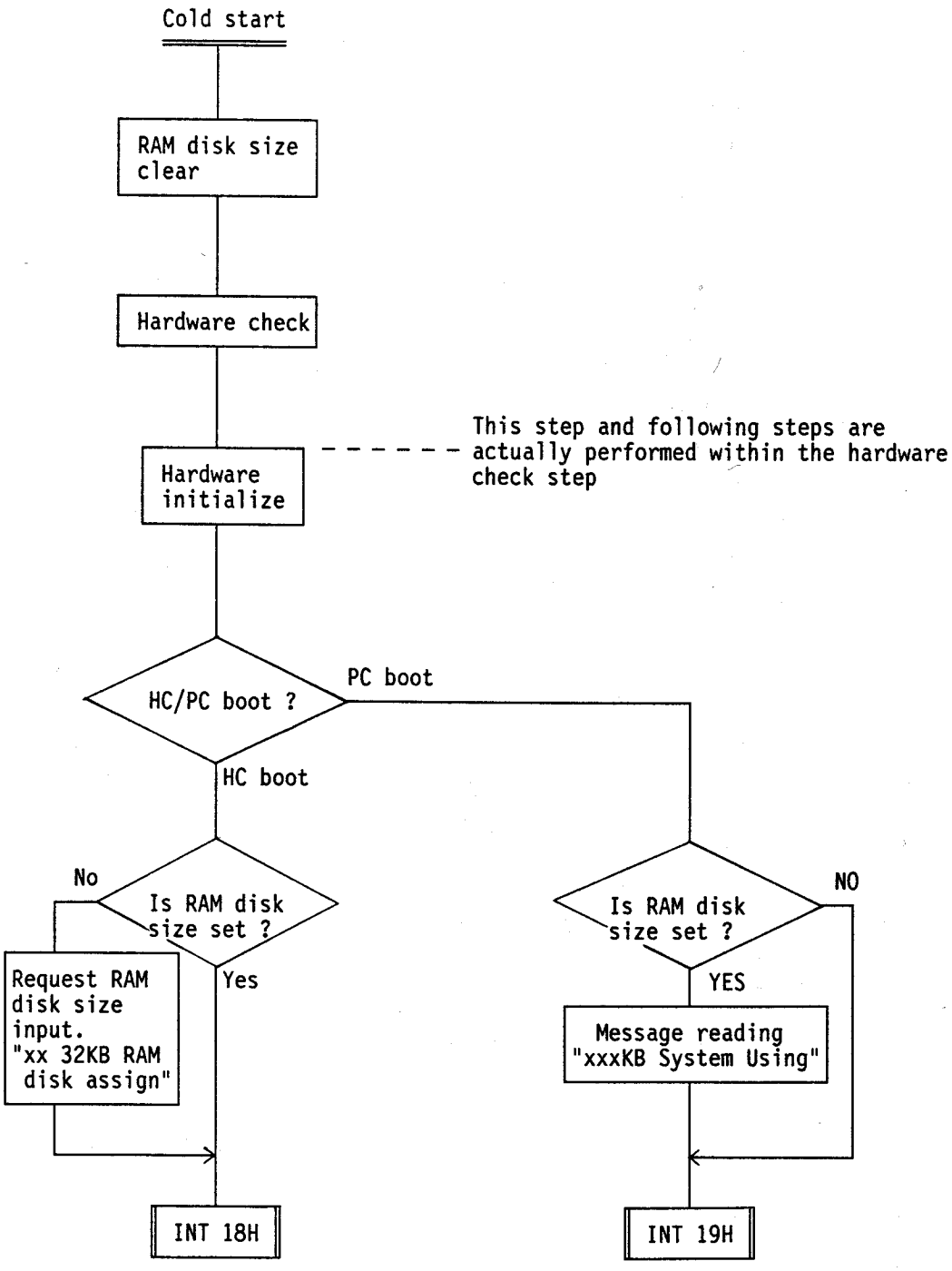
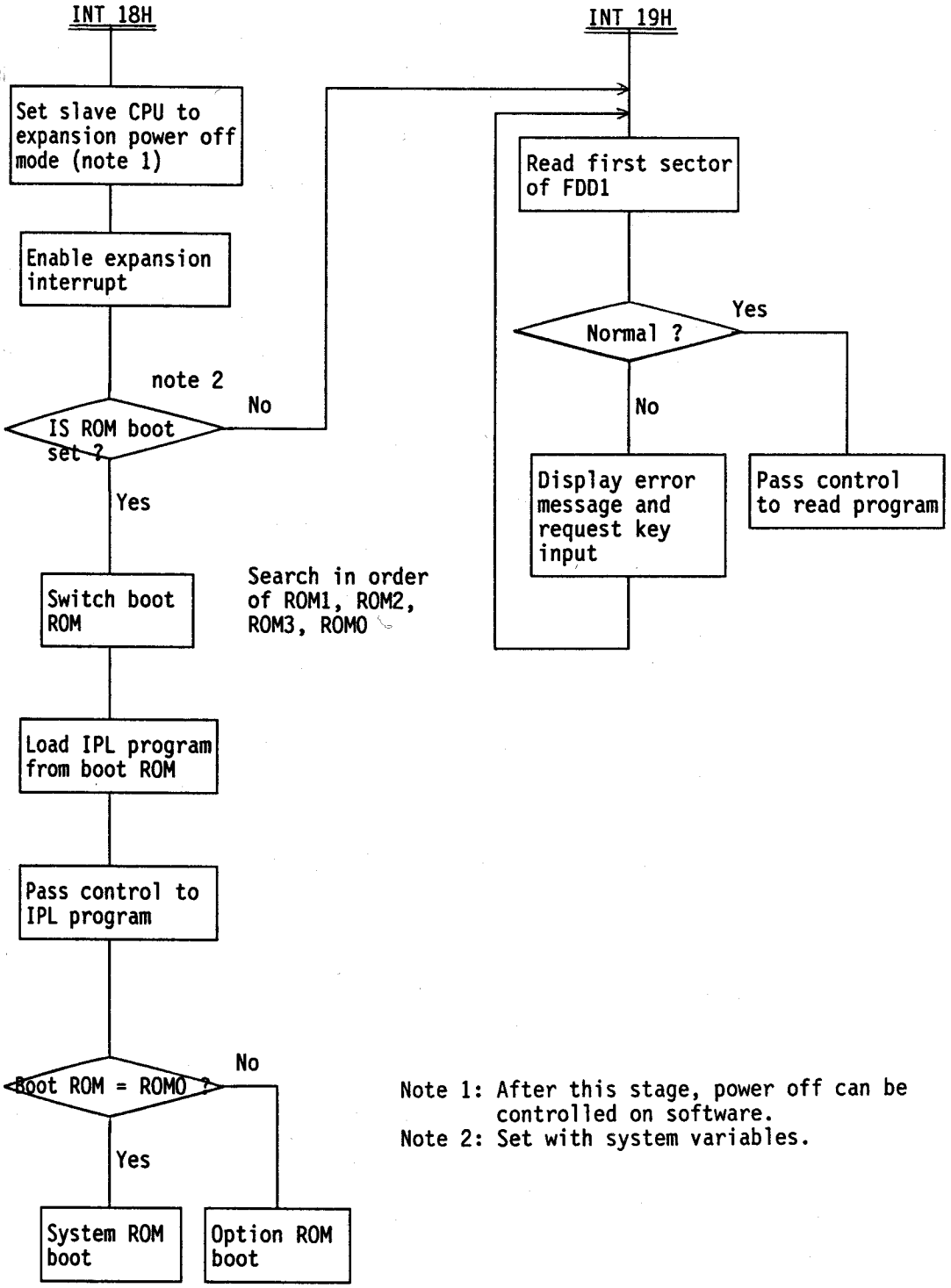


Fig. 3-3-3 Cold start processing

<INT 18H/INT 19H proccessing>



Note 1: After this stage, power off can be controlled on software.
Note 2: Set with system variables.

Fig. 3-3-4 INT 18H/INT 19H processing

(4) Warm start

The warm start is the normal PX-16 start sequence, and preserves RAM disk in both HC and PC boot. A warm start sequence is initiated by the following conditions:

① Reset switch is pressed
When the reset switch is pressed, warm start will be executed. When the reset switch is pressed in the power-off status, warm start will be executed in the next power on sequence.

② Software start
The Ctrl, Alt, and Del keys are pressed simultaneously while the PX-16 is on.

③ Start type set to warm
If the power-on start type has been set to "Warm" when the PX-16 is on, the start type will be warm. The power-on start type ("Warm" or "Resume") can be specified with the MS-DOS XMODE command. For PC boot the start type is not checked, and warm start will be executed.

④ One of the following errors is found during resume start processing:
(i) The main or expansion RAM is corrupted.
(ii) The availability status of an I/O device is changed.

The following actions are taken during warm start processing (See fig. 3-3-2):

① Power-on self-test (PC boot mode only)
The available devices are checked. See subsection "(6) Power-on Self-test" for details.

② Memory display (PC boot mode only)
The size of the main RAM area that is being used by the system is displayed using the message "xxxKB used by system", and the size of the main RAM area available for application programs is also displayed.

③ Hardware reset
The available devices are initialized. See subsection "(6) Poser-on Self-test" for details.

④ Interrupt vector setup
(Same as the interrupt vector setup procedure for cold start.)

An extended vector table is created in the HC boot mode and a PC compatible interrupt table is created in the PC boot mode.

⑤ System variable setup
The system variables are initialized. See subsection "(6) Power-on Self-test" for details.

⑥ IPL
(Same as the IPL procedure for cold start.)
INT 18H is issued in the HC boot mode and INT 19H in the PC boot mode.

<Warm start processing>

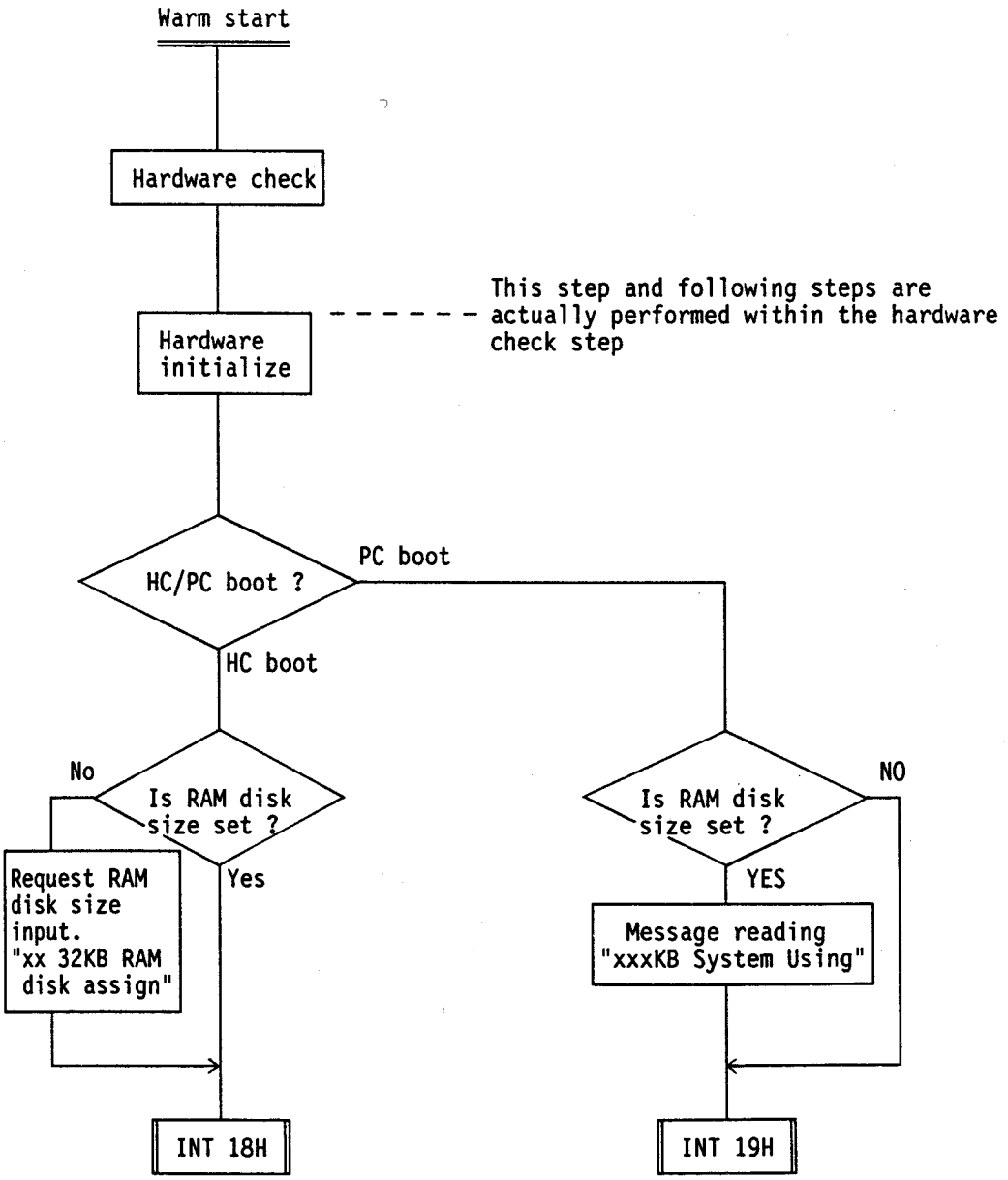


Fig. 3-3-5 Warm start processing

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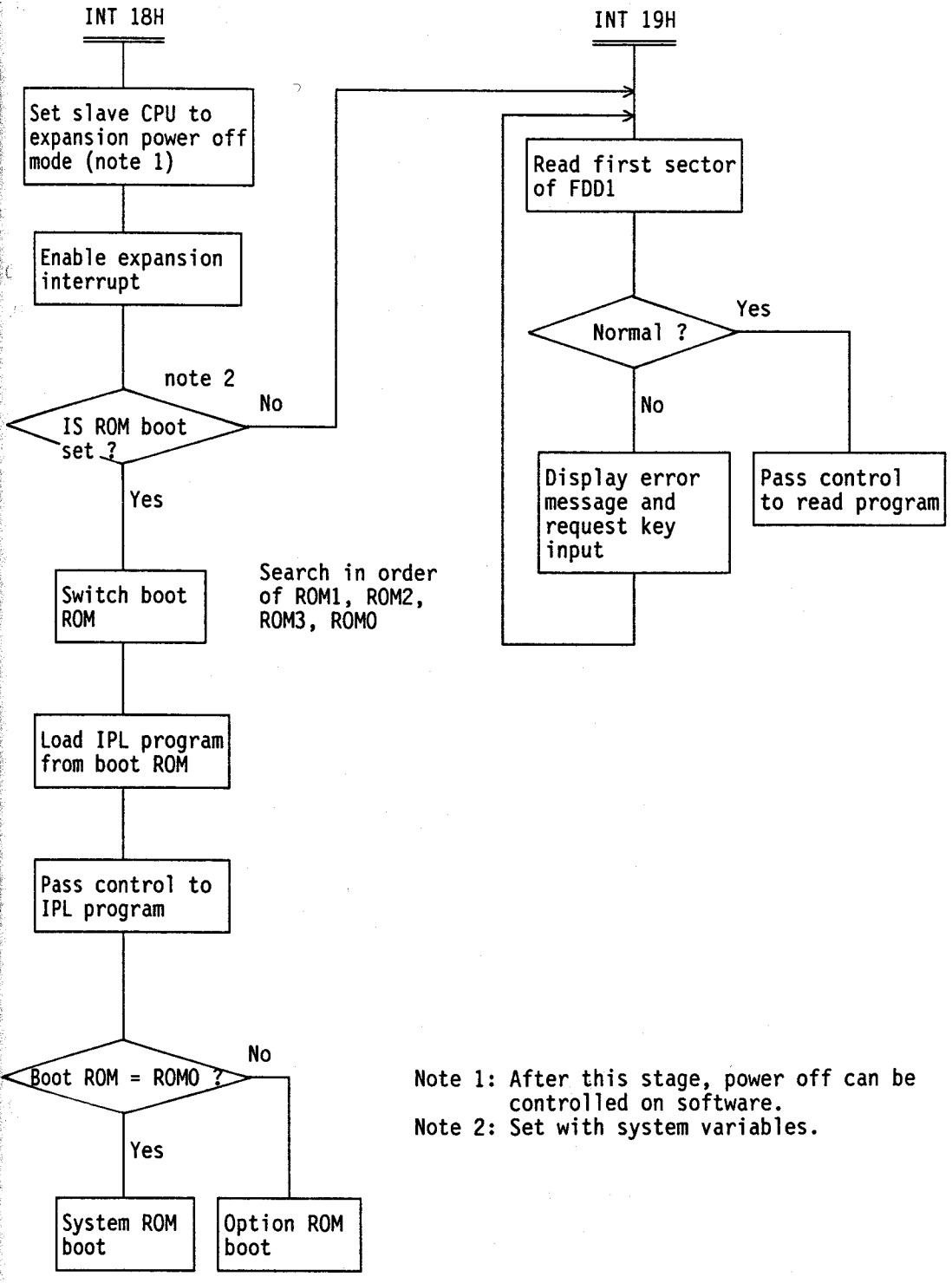
<INT 18H/INT 19H processing>



Note 1: After this stage, power off can be controlled on software.
Note 2: Set with system variables.

Fig. 3-3-6 INT 18H/INT 19H processing

(5) Resume strat (HC boot only)

When a resume start is performed, the system is restored into the original state immediately before the last power-off occurred and continues processing. Resume start processing is effective only when accesses to I/O devices were done all through BIOS. Normal resume start processing is not guaranteed if I/O device accesses were made directly.

Since the warm start mode is selected by default, it is necessary to select the resume start mode using one of the following sequences:

(a) INT 18H with function 01
(b) XMODE command

A resume start sequence is initiated by the following conditions:

① If the power-on start type has been set to "Resume" when the PX-16 power is turned on. Start type can be set by the above 2ways.

② A power-on sequence is performed after the system was turned off by a power failure. This includes automatic power off by the system and POWER switch manipulation.

③ A power-on sequence is performed after the system was turned off by the automatic power off.

The following actions are taken during resume start processing:

① Check for device change

A check is made on the device availability status to determine whether there is any status change compared with that at power-off time.
Device checked are as follows.

(a) Display devices
- LCD type changes (LCC80, LCD40, CRT/LCD cartridge, etc.)
- Display type changes (color, monochrome, etc.)

(b) Input devices
- Keyboard type changes (standard keyboard, touch keyboard)
- National character set changes

(c) Drive
- RAM: Main RAM/RAM disk size change
- ROM: Presence/absence of option ROM (ROM1-ROM3)
- FDD/HDD: Drive changes
- Cartridge 1: Presence or absence of cartridge 1 option

(d) External devices
- RS-232C: Number of RS-232C devices
- Printer: Number of printer devices

(e) Others
- Switch: Clock switch changes

When a change in the status of an available device is detected, the following processing is performed:

Resume start through power on:
Two short beeps generated, and then warm start processing.

Resume start after alarm or ring:
Three long beeps generated, and then power off.

RAM alteration detected:
Two long beeps generated, and then cold start processing.

② I/O device restoration

The I/O devices are restored into the state when the power-off occurred based on the information that was saved at the power-off time.

Devices are restored by resume start as shown below.

(a) Display devices
- LCD80/CRT: The controller is restored into the state when power was turned off.
- LCD40/touch keyboard: Restored.

(b) Input devices
- Keyboard: Restored
- LED: Restored. The EL backlight is forced on.

(c) Drive
- RAM/ROM: Restored according to whether they are installed or not.
- FDD/HDD: The controller is initialized.
- Cartridge 1: Restored according to whether cartridge 1 option is installed or not.

(d) External devices
- RS-232C: Restored.
- Printer: The printer is reset.
- Barcode reader: Restored

(e) Others
Since other controllers are used by the system, the restore information about them is not guaranteed.

③ Main CPU register restoration

The contents of the main CPU registers are restored based on the information that was saved at the power-off time. Consequently, control is returned to the program that was running when power was turned off.

However, when a corruption in RAM in the power-off state is found:
System RAM corruption -- Cold start
Main or extended RAM corruption -- Warm start

<Resume start processing>

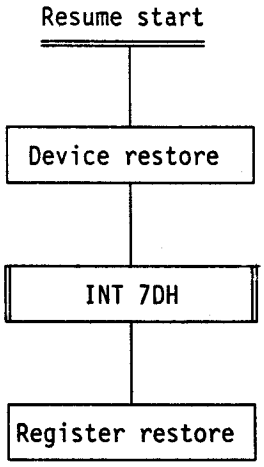


Fig. 3-3-7 Resume start processing

(6) Power-on Self-tests

The PX-16 performs the following power-on self-tests to improve its system reliability:

(a) Power-on check

A power-on check is performed when the PX-16 is booted in the HC boot mode and started in the warm or resume start mode. It searches for any RAM corruptions in the power- off mode.

(b) Hardware test

A hardware check is performed when the PX-16 is booted in the PC boot mode or when it is booted in the HC boot mode and started in the cold start mode. All hardware resources are inspected.

(c) System variable initialization

When the PX-16 is booted in the HC boot mode, all system variables are initialized.

Table 3-3-1 lists the check items that are examined at power-on time.
Table 3-3-2 lists the hardware test items.
Table 3-3-3 lists the initial values of the system variables.

	Error check	Error processing	Identified by	Remarks
Cold start	Hardware test			
Warm start (HC boot mode)	System RAM sumcheck	Cold start	Two long beeps	
	Main RAM sumcheck	Warm start	One short beep and one long beep	
	Extended RAM sumcheck	Warm start	One long beep and one short beep	
Resume start (HC boot mode)	System RAM sumcheck	Cold start	Two long beeps	
	Main RAM sumcheck	Warm start	One short beep and one long beep	
	Expansion RAM disk sumcheck	Warm start	One long beep and one short beep	
	Attached device check	Warm start	Two short beeps	When power switch is ON
		Power off	Three long beeps	When alarm or ring detected

Table 3-3-1 Power-on Check Items

Note 1: If a read/write error occurs in the 96-byte area (stack area used during start processing) at the end of the system RAM, all LEDs are lit and the PX-16 is forced to halt.

Note 2 : After start processing is complete, a short beep is generated in the cold or warm start mode and a long beep in the resume start mode.

Note 3 : When a change in RAM disk size is recognized at start processing, two long beeps are generated and cold start processing is executed.

x : Cannot continue
o : Can continue
F1: F1 key to resume

Test item	Error processing	Continue	Remarks
Slave CPU	Loop indefinitely	x	
Timer 1 (8253)	IOPORT_A = 2 Operation is not guaranteed	x	
DMA controller (8237)	IOPORT_A = 3 Operation is not guaranteed	x	
RAM (64kB)	IOPORT_A = 4 Operation is not guaranteed	x	
System RAM	IOPORT_A = 5 Operation is not guaranteed	x	
CRT I/F Option CRT ROM	One long beep and two short beeps	o	
Interrupt controller (8259)	101-System board error (6)	x	
Timer 0	101-System board error (7)	x	
RAM	xxxxx 201-Memory error	F1	xxxxx indicates the address in error
Keyboard	301-Keyboard error	F1	
	xx 301-Keyboard	o	xx denotes a scan code
DMA refresh request	101-System board error (8)	x	
Option ROM	xxxxx ROM error	F1	xxxxx indicates the address in error
Diskette	601-Diskette error	F1	
Clock	163-Time & Date not set	F1	

Table 3-3-2 Hardware Test Items

Note 1 : The code enclosed in parentheses is made appear when a 101 error occurs by resetting a DIP switch (SW5).

Note 2 : Press '1' key instead of 'F1' key for the touch keyboard.

——— : No change
DIP switch : Determines by the DIP switch (SW5) setting

		Cold start	Warm start	Resume start	Remark
	Clock (Date, Time)	Reset	———	———	
	Alarm interrupt	Disable	———	———	
	1 second interrupt	Enable	Enable	———	
Power control	Expanded power off	note 1	note 1	———	note 1 HC boot: On PC boot: Off
	Power on type	Warm	———	———	
	Auto power off	Disable	———	———	
	Auto backlight off	Reset 1 minutes	———	———	
	Printer power off	Disable	———	———	
Input	Repeat (standard keyboard)	On	On	———	
	Repeat (touch keyboard)	Off	Off	———	
	Key buffer	Clear	Clear	Clear	
	Country (Scan code)	DIP switch	DIP switch	———	
	LED	Off	Off	———	
Display	Country (CG)	DIP switch	DIP switch	———	
Others	RAM disk	Format	———	———	
	Backlight (Touch keyboard)	On	On	On	NOTE 2 Value set up by XMODEM
	RS-232C	9600 bps 8 bit none	note 2	———	

Table 3-3-3 Initial System Variable Values

3.3.2 System Termination

(1) Overview

Causes of power off in the PX-16 may be normal power switch off operation, power failure due to low batteries, or software-controlled. However, all of these types only occur in HC boot systems. In PC boot systems, software- controlled power off is not supported.

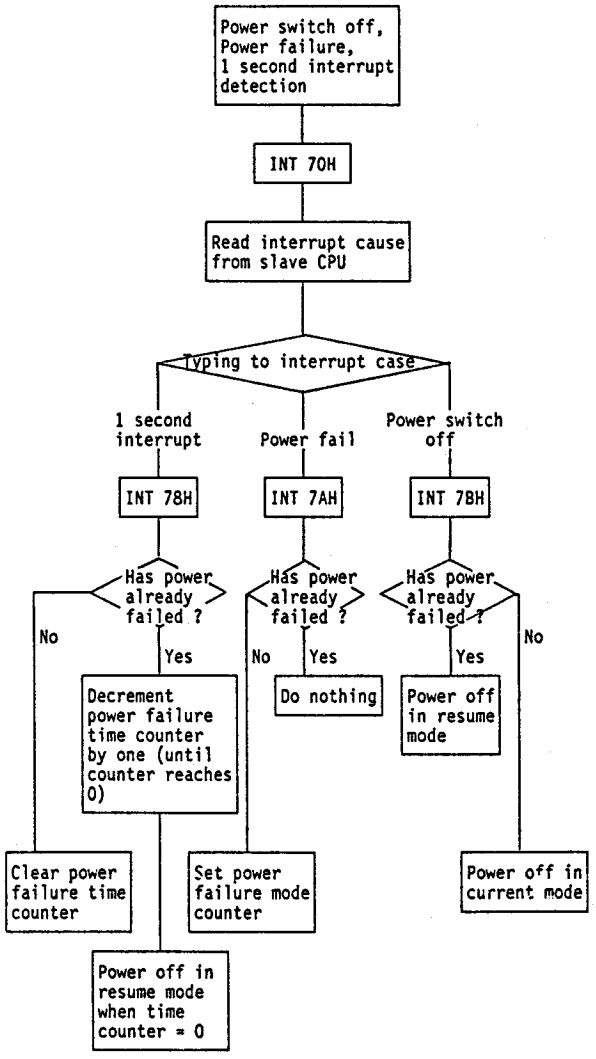
The PX-16 system is terminated by the following four events:

(a) The power switch is set to OFF.
(b) A power failure occurs (battery low).
(c) An auto power-off occurs.
(d) A BIOS call to power off is made.

These events are explained in the subsequent subsections.

(2) System termination flow (HC boot only)

System termination processing flows as indicated below occur for differing termination causes.



Processing content	step	Description
	1	Detects the salve CPU interrupt and calls INT 70H
	2	Interrupt cause status read in from slave CPU with INT 70H
	3	Check in order for power failure, 1 second interrupt power switch off, and call corresponding BIOS
	4	Check if power has already failed in each BIOS processing sequence
	5	Perform specific processing

Fig. 3-3-8 System Termination Process

(3) Setting the POWER Switch to OFF

Setting the POWER switch to OFF switches off PX-16 power.
In PC boot, turning off the POWER switch causes the slave CPU to forcibly power-off the main power supply, and terminates all operations at that point.

In HC boot the system terminates after the following operations during the power-off sequence:

(a) Sum check on main and extended RAM
(b) Sum check on system RAM
(c) Saving I/O device information for resume processing
(d) Saving register information for resume processing

<Power switch off interrupts>

INT 7BH

Check the value of system variable SEC_TIMER0.

1) If the system is not in a battery failure state (SEC_TIMER0 = 0000H), a power off request is issued in accordance with current power off mode (POWER_ON_STATUS).

2) If the system is in a battery failure state (SEC_TIMER0 ≠ 0000H), a power off request in the resume mode is issued.

This interrupt is issued only one time when the power switch off is detected.

(4) Power failure

The Power indicator LED flashes when the system detects a battery low condition when the NiCd battery are being used to drive the system. The LED will continue to flash until an AC adapter is connected. If a power failure occurs, the user must connect the AC adapter.

The system takes the following actions when a power failure occurs in HC boot:

① Sets up the power-off time in which power is to be turned off after the occurrence of the power failure (the default value is 2 minutes; INT 7AH).

② Checks for the persistence of the power failure once per second, and resets the power failure if the AC adapter is connected. If power is still off, it decrements the power-off time by one (INT78H).

③ If power is not turned off by the user, the system automatically turns off the PX-16 when the power-off time has elapsed.

If the power switch is set to OFF when the power failure occurs, or the system automatically turns off the main unit, the system enters the resume mode and can continue the processing that had been executed when the system powered off (when the system had been booted in the HC boot mode).

<Power failure interrupt>

INT 7AH

Check the value of system variable SEC_TIMER0.

1) If it is the first power failure state (SEC_TIMER0 = 0000H), LOW_BATTERY_OFF_TIME x 60 is calculated and that value set to the SEC_TIMER0.

2) If the system is already in a battery failure state (SEC_TIMER0 ≠ 0000H), the interrupt terminates with doing nothing.

This interrupt is issued when the power failure is detected the first time, and when the slave CPU generates an interrupt during a power failure.

<1-second interrupt>

INT 7AH

Check the status information for the interrupt from the slave CPU.

1) If the system is currently in a power failure state, decrement SEC_TIMER0 by one. If the result is 0000H, issue a resume mode power off request.

2) If the system is not in a power failure state, SEC_TIMER0 is set to 0.

<Alterations in power failure time>

Changing the value of LOW_BATTERY_OFF_TIME (A800:04) will alter the power off time. The value may be from 01H~FFH, and in BIOS a maximum of 255. The initial (default) value is 02H, or 2 minutes.

However, the maximum monitor time for the slave CPU (time from power failure generation to power off in PC boot) is four minutes (initial value 4 minutes), and the actual valid monitor time is 03H (3 minutes).

Note: Setting the value to 04H is the same as the slave CPU monitor time, and therefore power failure processing may not terminate normally.

(5) Auto Power-off (HC Boot Mode only)

The PX-16 is automatically turned off, if no key- related interrupt (INT 09H or INT 77H) occurs for a certain period of time (Note 1). When this type of power-off occurs, the system performs the power-off sequence that is explained in subsection (3) above.

The next power-on condition initiates a resume mode so that the system can continue processing that was interrupted at the power-off time.

The auto power-off feature can be enabled by setting the period in which the auto power-off feature is activated using one of the following steps:

(a) INT 18H with function 01H
(b) XMODE command

However, the auto power-off counter is reset when one of the following software interrupts occurs:

INT 10H (LCD_I/O interrupt)
INT 13H (Disk_I/O interrupt)
INT 14H (Communication_I/O interrupt)
INT 17H (Printer_I/O interrupt)
INT 18H (Extend_I/O interrupt)

This feature is valid only when the PX-16 has been booted in the HC boot mode and is not available when the PX-16 has been booted in the PC boot mode. By default, the auto power-off feature is disabled.

(6) BIOS Call (HC boot only)

Terminating the PX-16 through a BIOS call is valid only when the PX-16 has been booted in the HC boot mode. Software power off is handled through the following BIOS call:

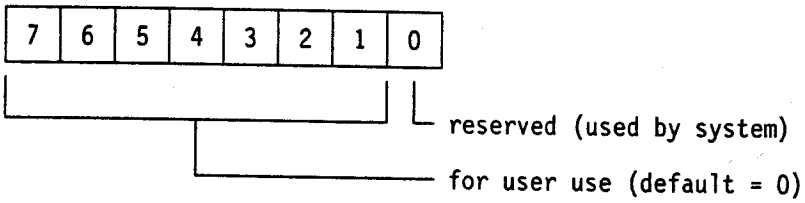
INT 18H with a function code of 06

(AL) = 0 is power off in current mode.
= 1 is power off in resume mode.

(7) Power off disable

Power off can be disabled by rewriting the value of DISABLE_POWER_OFF (A800:53).

DISABLE_POWER_OFF



When power off is temporarily disabled by an application, set bit n (n=1~7) of DISABLE_POWER_OFF to 1.

To clear the disable perform the following processing:

1) Reset the bit previously set to 1 back to 0.
2) Check if other bits of the DISABLE_POWER_OFF byte have been set to 1, but do not change them.
3) If all other bits are 0, check the MSB of the POWER_OFF_FLAG. If it is 0, do nothing.
4) If there is a 1, it indicates there was a power off request during disable. Execute the power off in accordance with the LSB of the POWER_OFF_FLAG.
5) Power off calls INT18H function 6
   in the resume mode when POWER_OFF_FLAG LSB=0, and
   In the current mode when POWER_OFF_FLAG LSB=1.

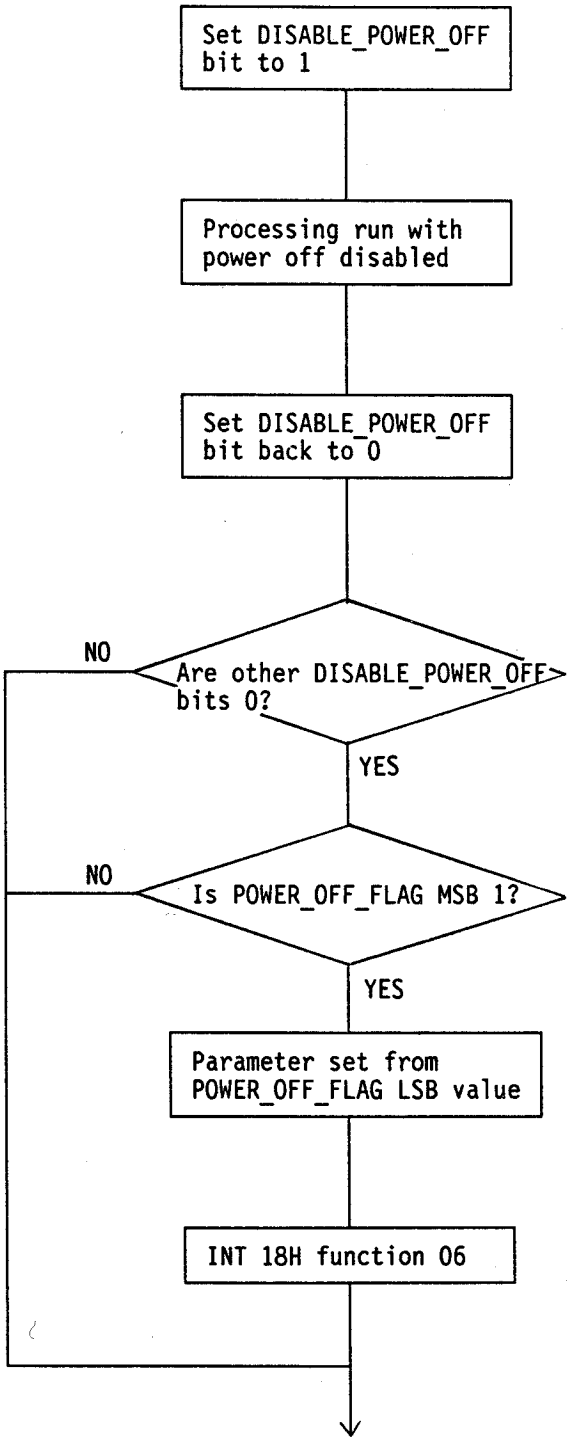


Fig. 3-3-9 Power-off Disable Process

3.3.3 Other Control Functions

(1) Alarm (HC boot mode only)

The alarm feature generates an interrupt at a given time. It functions in two modes:

- If the alarm time is reached when the PX-16 is off, it automatically puts the PX-16 into the power-on state.
- If the alarm time is reached when the PX-16 is on, it generates an interrupt.

When an alarm condition occurs, the system takes actions given below.

① If the alarm occurred when the PX-16 is off

(a) The system enters the power-on state and executes a power-on sequence.

(b) During power-on sequence, the system initiates a warm or resume start processing according to the power-on start type specification. See Section 3.3.1 for details.

(c) Disables the alarm feature.

② If the alarm occurred when the PX-16 is on

(a) Issues an INT 79H BIOS call.

The alarm time can be set using one of the following steps:

(a) INT 1AH (BIOS) Function 06H, 43H (set)
Function 07H (clear)

(b) XMODE command

(2) Ring (HC boot mode only)

The ring feature generates a RING signal to raise an interrupt from the external interface. It functions in two modes:

- If a ring condition occurs when the PX-16 is off, it automatically puts the PX-16 into the power-on state.
- If a ring condition occurs when the PX-16 is on, it generates an interrupt.

When a ring condition occurs, the system takes actions given below.

① If the ring occurred when the PX-16 is off

(a) The system enters the power-on state and executes a power-on sequence.

(b) During power-on sequence, the system initiates a warm or resume start processing according to the power-on start type specification. See Section 3.3.1 for details.

(c) Disables the ring feature.

② If the ring occurred when the PX-16 is on

(a) Issues an INT 76H BIOS call.

Power-on control using the ring interrupt is enabled using the following step:

(a) BIOS INT 18H with function code 08H

(3) Auto Backlight Off (HC boot mode only)

The system automatically turns off the EL backlight display for a connected touch keyboard if there is no key interrupt (INT 49H) or touch-key interrupt (INT 77H) generated to the touch LCD for a specific interval (1 minute by default). The backlight display is turned on again when a key is pressed or when a power-on sequence is performed.

The auto backlight off time can be changed using one of the following steps:

(a) INT 18H function 01H

(b) XMODE command

(4) Printer Power-off (HC boot mode only)

The system puts the cartridge printer H into the power save mode if there is no printer output (INT 17H) is sent to the cartridge printer H. The power save mode is reset by the system when a request for printer output occurs.

The system automatically turns off the cartridge printer H within several seconds after the PX-16 is turned on. By default, the printer power-off feature is disabled.

In the power save mode when a printer output request is encountered, the system automatically clears the printer power off and executes output.

Printer power off time may be set by:

(a) INT 18H function code 01H

(b) XMODE command

(5) Disk Power Save Feature (HC boot mode only)

① FDC stand-by mode

The system puts the FDC into the stand-by mode if there is no access to the FDC (Floppy Disk Controller) via BIOS for 60 seconds when the PX-16 has been booted in the HC boot mode. The stand-by mode is reset by the system when an access is made to the FDC through BIOS. This function is valid only on TF-16.

② Cartridge 1

The system shuts off power to cartridge 1 if there is no access to cartridge 1 via BIOS for 60 seconds when a ROM cartridge is installed in the cartridge 1 interface. Power to cartridge 1 is turned on by the system when an access is made to cartridge 1 through BIOS.

For RAM cartridges set/reset is accomplished through the same method.

3.3.4 Interrupts

(1) Overview

The PX-16 is equipped with the same eight levels of interrupts supported by the EPSON PCe and the IBM PC/XT, and also has an additional eight levels of interrupts for exclusive functions. The initial (default) status is the same as the EPSON PCe. Note should be taken of the following:

- There are three causes of an NMI with the EPSON PCe: parity errors, I/O channel checks, and the 8087. However, only I/O channel checks cause NMI with the PX-16.
- Eight levels of extended interrupts are cascaded to PX-16 interrupt level 2.
- The interrupt controller 8259A is backed up while power is off.

In addtion to standard 8-level interrupts, the PX-16 allows expanded interrupts to be used by command.

PX-16 interrupts are as indicated below.

	Level	Cause
Standard	NMI	IOCHCK INT
	0	Timer
	1	Keyboard
	2	Reserved
	3	RS-232C (secondary)
	4	RS-232C (primary)
	5	Hard disk
	6	Floppy disk
	7	Printer
Extended	8	Slave CPU
	9	UART RX ready
	10	Cartridge1 IBF
	11	Cartridge1 PRDY
	12	ICF (barcode reader)
	13	OVF (13.3ms interval timer)
	14	RING
	15	INTTP (Touch pannel)

Table 3-3-4 Interrupt List

(2) Extension method

PX-16 interrupt level 2 is reserved. Level 2 interrupts cause the cascade connection of the extended interrupt controller which controls the extended eight interrupt levels, making extension interrupt possible. For this reason, the interrupt controller (master controller, 8259A equivalent) must be redefined. With the PX-16, the OS automatically extendes interrupts when start-up is by HC boot, but only standard interrupts are valid when start-up is by PC boot.

When the extended interrupts are valid, the vectors corresponding to levels 8~15 are output by the extended interrupt controller.

To enable the extended interrupt function, set I/O register P11DFH bit 7 to "1".

The PX-16 OS supports interrupts as follows.

Standard	INT 08H - INT 0FH
extended	INT 70H - INT 77H

The block diagram of the extended interrupt is indicated below.

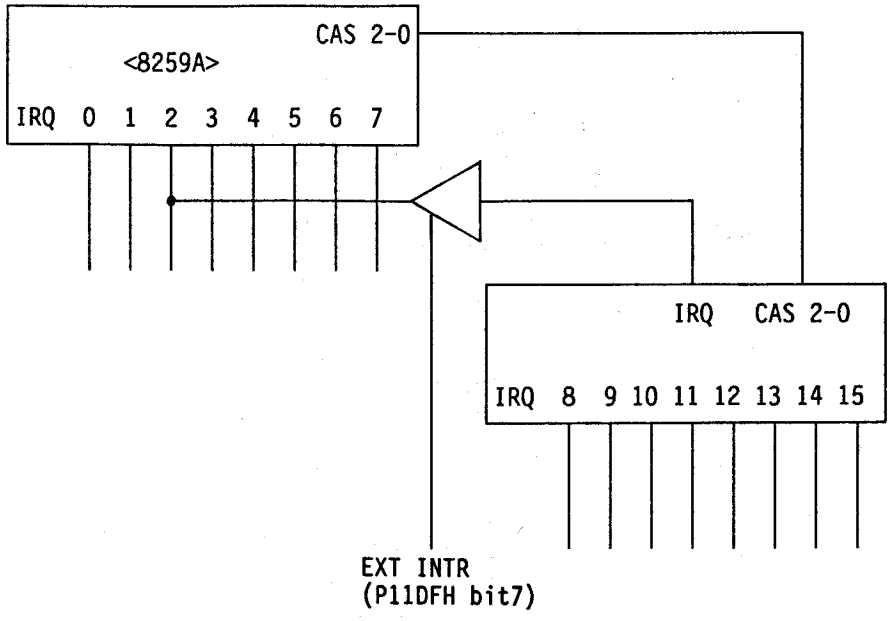


Fig.3-3-10 Extended Interrupt System Block Diagram

(3) Extended Interrupts

① Slave CPU Interrupts (INTSL)

These interrupts are raised by the slave CPU (μPD75106). When one of these interrupts occurs, it remains active until the slave CPU receives a response. The OS calls INT 78H to INT 7BH, according to the cause of slave CPU interrupts.

② UART RX RDY

This interrupt is raised by the RxRDY signal from the UART. It enables to receive data from either cartridge 1 or barcode reader serial communication, and is reset when received data is read. The OS supports receive interrupts.

③ Cartridge1 IBF

This interrupt is raised by the IBF signal occurring in the HS mode of communication with cartridge 1. IBF is set when a cartridge option writes data to the base unit, and reset when the base unit reads it. The OS does nothing when it receives a cartridgae 1 PRDY interrupt request.

④ Cartridge1 PRDY

The cartridge 1 interface CAB1 is connected to the interrupt controller, is active for 0 and inactive for 1. Cartridge printer H $\overline{\text{RDT}}$ is connected to CAB1. The OS does nothing when it receives a cartridgae 1 PRDY interrupt request.

⑤ ICF

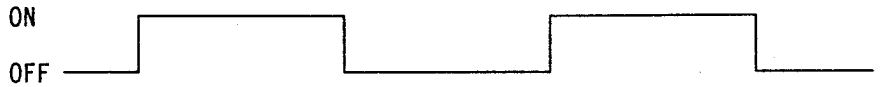
Setting bits 1 and 2 of I/O register P11D0H can latch an internal counter value when there is a transition in the state of the barcode input signal. When there is a change in barcode reader input, the internal counter value is latched and ICF is set at the same time. The ICF is the interrupt cause. ICF is reset by reading P11D2H. OS usually does notheing when it recieves an ICF interupt request, but if the barcode driver is installed, it extendeds barcode decode processing.

⑥ OVF

An OVF interrupt occurs at intervals of approximately 13.3 ms. OVF is reset by the RES_OVF command. (Write "1" to P11DFH bit 5.) The OS uses it for various timer counters.

⑦ RING

Ring Interrupt occurs at any change of Ring signals, from the interfaces of Cartridge 2, expansion I/F, and system bus.
When the RING is connected to a telephone ring, the interrupt request generated is as indicated below.



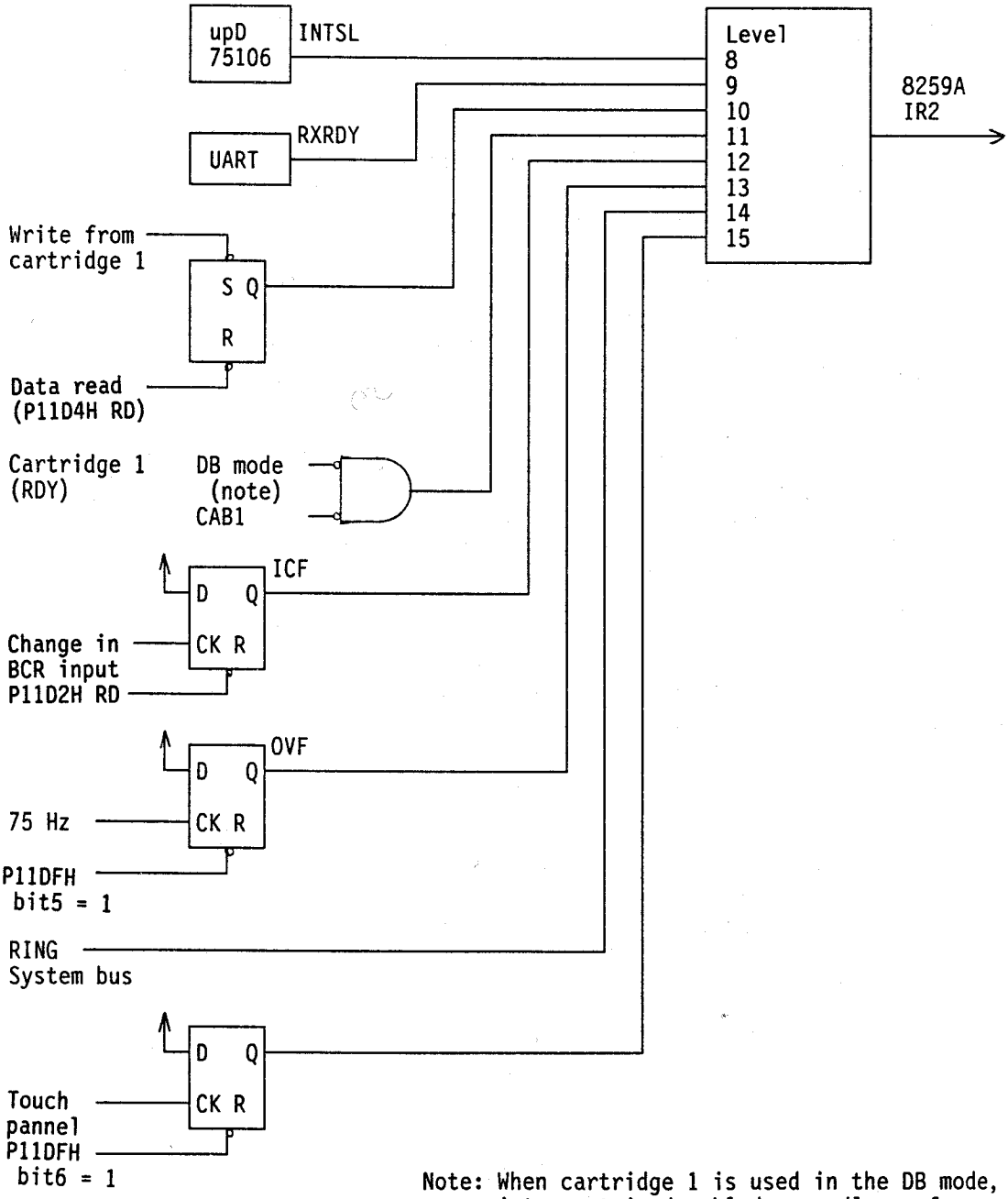
Interrupt request

The interrupt request is generally on for one second, which means that if the request is not responded to within about one second, the interrupt cause will vanish, and the output response vector cannot be guaranteed. The OS does nothing when it receives a RING interrupt request.

⑧ INTTP

Touch key interrupts are generated by pressing touch panel keys on the touch keyboard. Q of the flipflop is the interrupt cause. INTTP is reset by RES_TP command. (Write "1" to P11DFH bit 6.) OS supports touch panel scanning.

The block diagram for the extended interrupts is given below.



Note: When cartridge 1 is used in the DB mode, interrupt is desabled regardless of masking.

Fig. 3-3-11 Extended Interrupt

(4) Extended Interrupt EOI

In conventional PC BIOS, the interrupt controller that becomes the master through cascade connection is programmed for edge trigger. In this case, assuming that multiple interrupts were pending at the slave CPU, the IR2 input to the extended interrupt controller will remain active, and thereby prevent the master controller from noticing the pending extended interrupts. In the PX-16, hardware and the EOI command are used to generate edges.

The circuit used is indicated below.

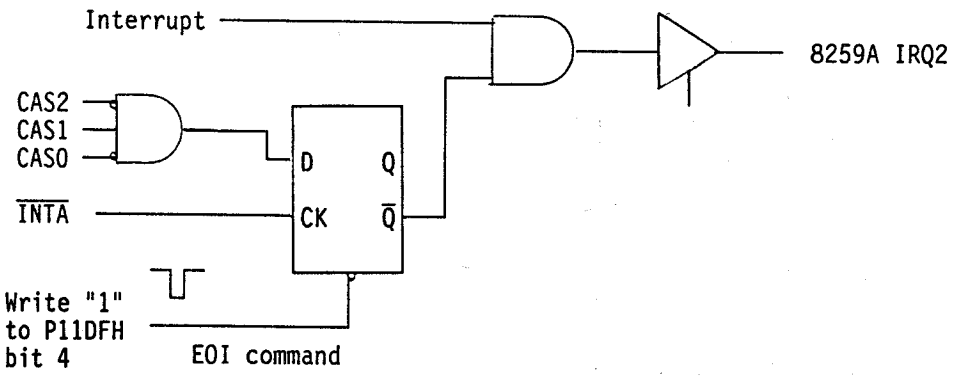
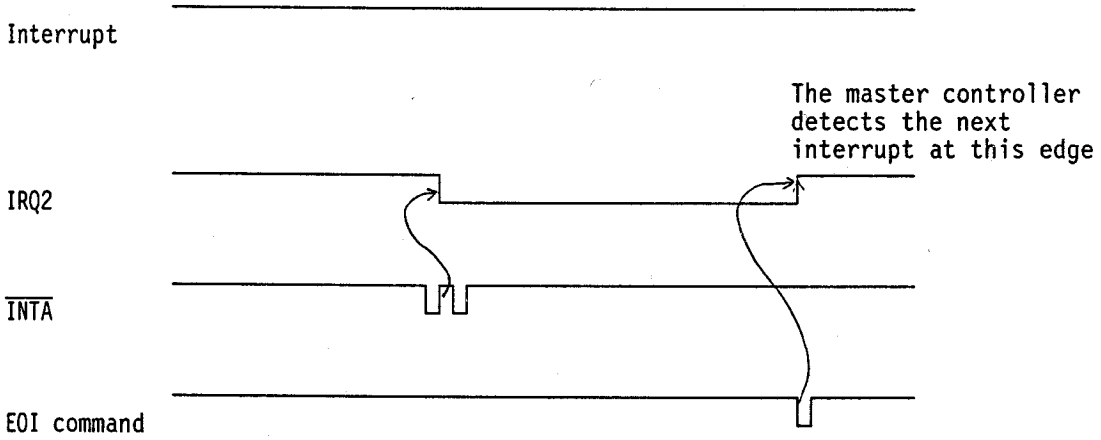


Fig. 3-3-12 EOI Block Diagram

EOI issue timing requires:

① Issue the EOI to the master, and
② Once the master is ready to receive the interrupt,
③ Issue the EOI to the extended interrupt controller.

The timing chart is indicated below.



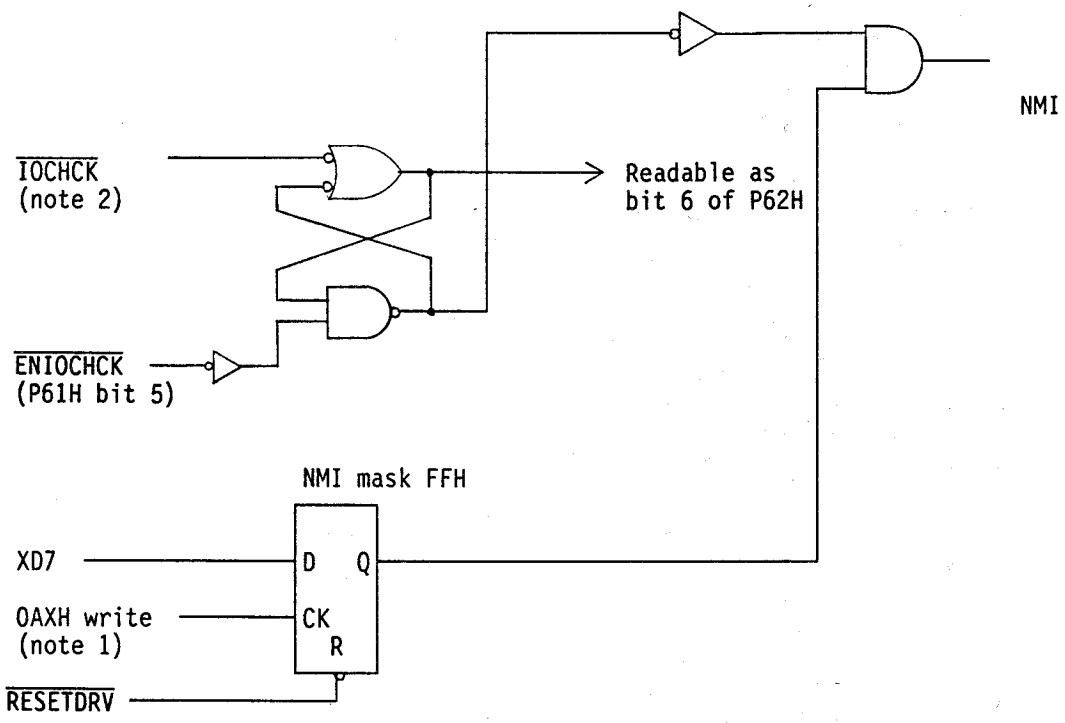
With the PX-16, the OS automatically performs EOI processing when any of interrupts INT 70H to INT 77H occurs, so user processing is not required.

(5) NMI

The nonmaskable interrupt NMI is raised by the $\overline{\text{IOCHCK}}$ signal.

In the EPSON PCe and IBM PC/XT, parity errors and interrupts from the coprocessor are also NMI, but this function is not provided in the PX-16.

The NMI block diagram is indicated below.



Note 1: Writing "1" to bit 7 of OAXH enables NMI
Note 2: IOCHCK is used to determine option installation
(LCD40, LCD80 ,etc.)

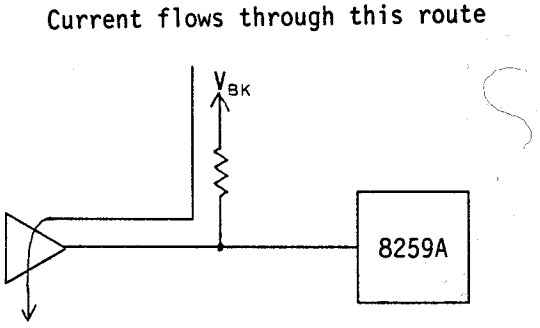
Fig. 3-3-13 NMI Block Diagram

The PX-16 halts after displaying an error message if an NMI (BIOS call 02H) occurs.

(6) Cautions when using the 8259A interrupt controller

The 8259-equivalent interrupt controller has an internal pull-up resistance on interrupt input.

The 8259 is backed-up, so if an interrupt is low level during power off, current will flow out through this pull-up resistance (see diagram below).



To prevent this in the PX-16, a tristate buffer is placed in interrupt input, and switched to high impedance in power off.

For this reason interrupt input during power off becomes high level, and simulates high-level interrupt generation.

In the resume mode this point must be given consideration after power on and the following processing used. The OS performs a dummy reset for interrupts to avoid invalid interrupts.