NOTES

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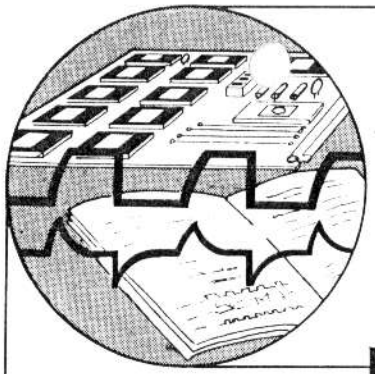

APPLICATION NOTE

APRIL 1983

NA-035A

Using 64K bit dynamic RAMS with EF9365, EF9366, EF9367 graphic display processors

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Integrated Circuits

INTRODUCTION

The recent appearance of 64 K x 1 and 16 K x 4 dynamic RAM chips has significantly simplified the task of system design using these low-cost but yet highly efficient memory chips around EF9365, EF9366 and EF9367 Graphic Display Processor circuits.

The objective of the present document is to assist the users in finding an appropriate solution to their design requirements, while an attempt has been made to familiarize them with the outstanding features of these memory chips.

For an efficient and easier comprehension of the subjects covered within the present document, it is preferred that the reader be already familiar with the subjects discussed in Application Note NA-002R2A, "General Application Pinciples for EF9365 - EF9366".

APPLICATIONS OF 64 K x 1 DYNAMIC RAM CHIPS (MCM 6665 or 4164 type)

BASIC APPLICATION : 512 x 512 RESOLUTION

In using 16 K x 1 RAMs, it was necessary to arrange the memory chips in a 2 rows of 8 column fashion. The row select function was then performed by MSL 3 signal as indicated in Figure 1.

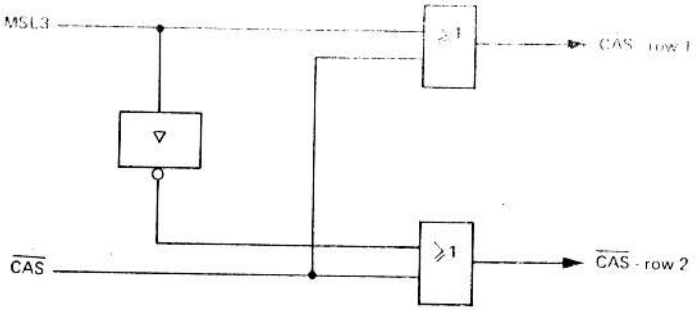


FIGURE 1 – ROW SELECTION SIGNAL

Using 8 chips of 64 K x 1 dynamic RAMs arranged in 1 row of 8 columns will result in a total memory size of 64 K words. Addressing the row so-arranged is readily accomplished by connecting the MSL 3 signal to the address line A7 of the memory, ie :

MSL 3 ——→ A7

The foregoing arrangement results in a considerable reduction in size since, the number of memory chips required in applications similar to those described in NA 002R2A application note, are reduced by a factor of 2. In addition, $\overline{CAS}$ signal is delivered directly to the memory chips, and does not need to be strobed with MSL 3 signal as previously.

However, there is a major disadvantage associated with the solution just outlined. That is the fact that half of the 64 K words offerred by the memory, remain unused.

In order to overcome this problem and to use the remaining half, the following solution may be adopted.

Since two pages of 512 x 512 pixels are accessible, the user may select, through program, the displayed page and the page to be modified.

The displayed page and the page to be modified could be the same, as is the case in text edition or could be different as in animation applications.

Figure 2 illustrates how this task may be accomplished.

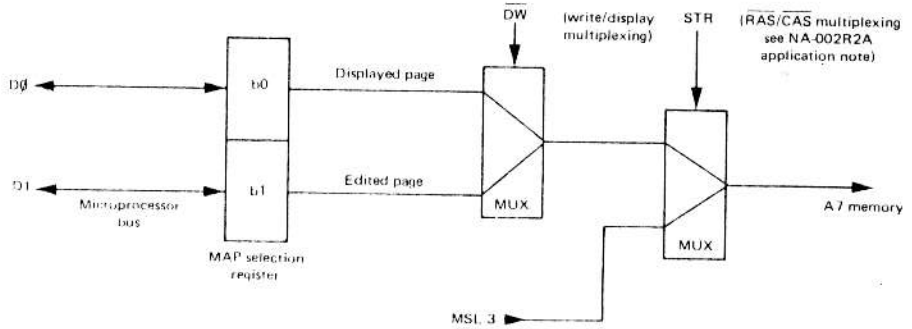


FIGURE 2 – PAGE SELECTION HARDWARE

$\overline{DW}$	STR	A7
0	0	b1
0	1	MSL 3
1	0	b0
1	1	MSL 3

TABLE 1 – MULTIPLEXER SELECT TRUTH TABLE

This principle is very advantageous in applications where a moving element is to be displayed. It is therefore possible to trace the position "n+ 1" of an object while displaying the position "n".

Remark :
The MCM 6665 and 4164 type memories are refreshed in 128 accesses. The refresh is performed directly by GDP (Graphic Display Processor) in 2 lines of 64 accesses per line during display or vertical blanking periods.

VERTICAL SCROLLING

Using the GDP (Graphic Display Processor) as display controller in graphic or alphanumeric display applications, requires very often an additional function which is not implemented on the chip. This function is "scrolling" and may be provided through the two pages available within 64K dynamic RAMs.

For example, the stored zone occupies an area of 1024 x 512 pixels, using EF9365 or EF9367 with FMAT = V_{CC}, and the displayed zone occupies an area of 512 x 512. The objective is to move the displayed zone into the memorized zone as outlined in Figure 3.

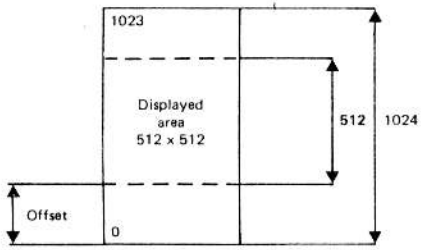


FIGURE 3 – DISPLAYED WINDOW VERSUS MEMORY AREA

Note :
The application presented here outlines the scrolling of the displayed zone. It is obvious that, the fundamentals discussed, apply to the edited zone too. It is therefore possible, in doubling the number of the components, to differentiate between the scrolling of the displayed zone and that of the edited zone ($\overline{ALL}$ signal will perform this function).

The theory of this application is to add an offset component whose value lies between 0 and 1023, to the vertical addresses generated by the GDP. The proposed diagram outlines the solution for a situation where the offset component is encoded in 8 bits, and that as a result, a scrolling of 4 lines per step is obtained.

In order to develop this application, all that is necessary is to modify the vertical addresses in both write and display modes. The horizontal addresses (h_i , X_i) must be transferred without any modification and exactly in the same form that the GDP has supplied them.

Therefore, multiplexers are used so as to allow either, the transfer of horizontal addresses generated by the GDP as well as the two least significant bits of the vertical address or, the transfer of the vertical addresses provided by the adder circuits, with the exception of the least significant bit which is supplied together with the horizontal addresses.

The addition is performed on the following words :

$$\begin{pmatrix} 0 \\ V_7/Y_8 \\ V_6/Y_7 \\ V_5/Y_6 \\ V_4/Y_5 \\ V_3/Y_4 \\ V_2/Y_3 \\ V_1/Y_2 \end{pmatrix} + \begin{pmatrix} O_9 \\ O_8 \\ O_7 \\ O_6 \\ O_5 \\ O_4 \\ O_3 \\ O_2 \end{pmatrix} = \begin{pmatrix} R_9 \\ R_8 \\ R_7 \\ R_6 \\ R_5 \\ R_4 \\ R_3 \\ R_2 \end{pmatrix}$$

Vertical addresses generated by the GDP + Offset = Result

		MSL				DAD						
$\overline{ALL}$	CK	0	1	2	3	0	1	2	3	4	5	6
0	0	X_0	X_1	X_2	V_1	h_5	h_4	h_3	h_2	h_1	h_0	V_0
0	1					V_7	V_6	V_5	V_4	V_3	V_2	t
1	0	X_0	X_1	X_2	Y_2	X_8	X_7	X_6	X_5	X_4	X_3	Y_1
1	1					Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_0

TABLE 2 – SIGNALS GENERATED BY THE GDP (FMAT = V_{CC})

Referring to Table 2, it may be noted that the valid vertical addresses (V_1,....., V_7 and Y_2,....., Y_8) are generated during the second portion of the cycle. It is therefore during this period that the outputs of the adders must be considered as valid memory addresses.

	$\overline{ALL}$	CK	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
A	0	0	R_2	DAD0	DAD1	DAD2	DAD3	DAD4	DAD5	DAD6	Display & refresh
B	0	1	R_9	R_8	R_7	R_6	R_5	R_4	R_3	DAD6	
A	1	0	R_2	DAD0	DAD1	DAD2	DAD3	DAD4	DAD5	DAD6	Write
B	1	1	R_9	R_8	R_7	R_6	R_5	R_4	R_3	DAD6	

TABLE 3 – SIGNALS GENERATED BY THE MULTIPLEXERS (DAD6 does not require multiplexing)

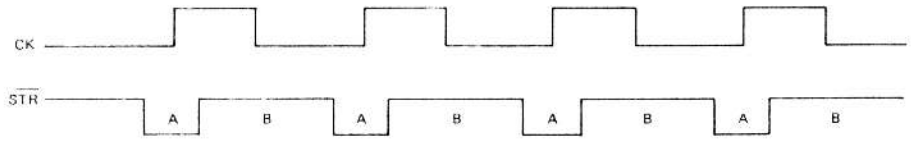
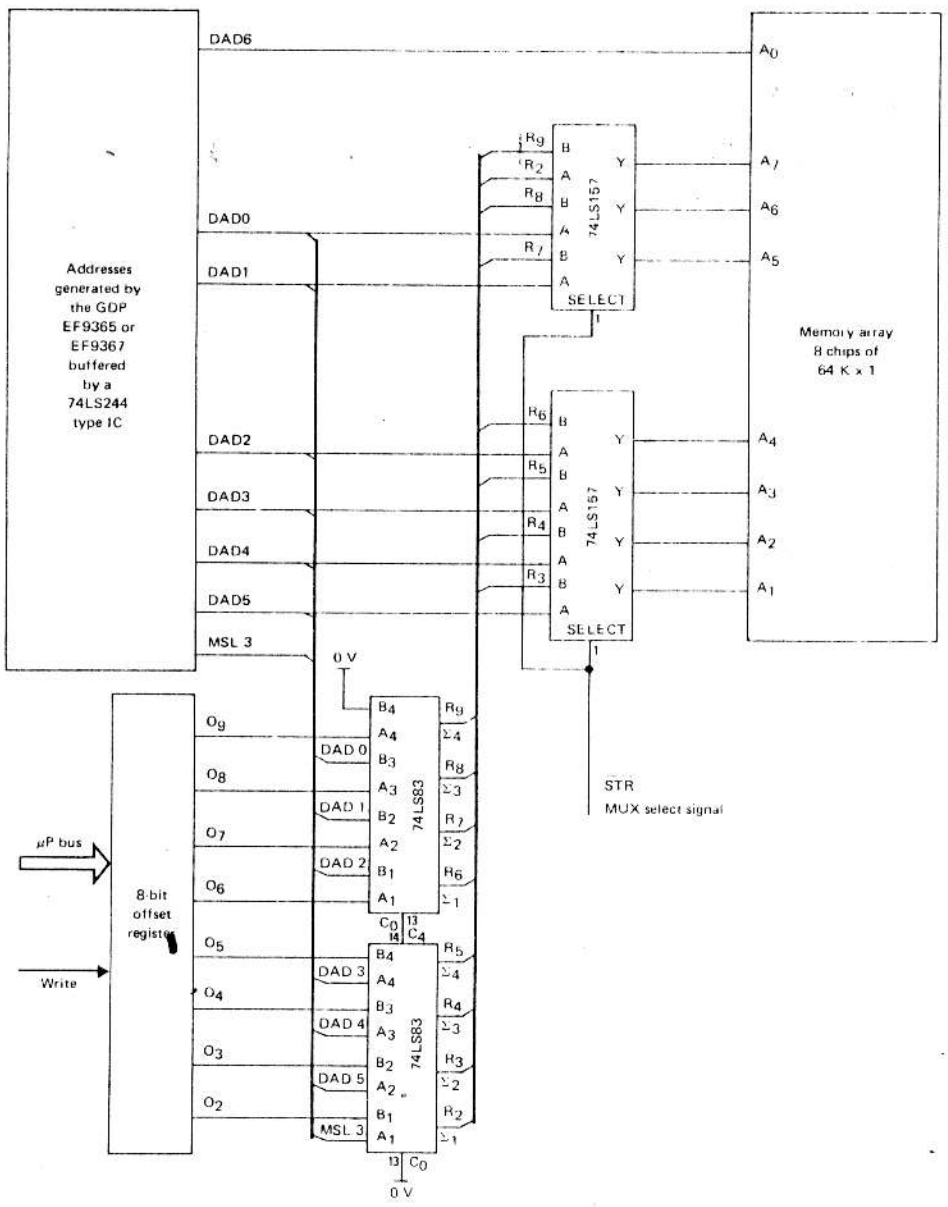


FIGURE 4 – TIMING WAVEFORM FOR MULTIPLEXERS CONTROL SIGNAL "$\overline{STR}$"

See also the details given in Application Note NA 002R2A.

FIGURE 5 – VERTICAL SCROLLING WITH EF9365 OR EF9367 CIRCUITS (FMAT = V_{CC})



Note : This application requires only 5 TTL-LS Integrated Circuits for its basic configuration.

OTHER SCROLLING APPLICATIONS

Vertical scrolling is also easily accomplished using EF9365 and EF9367 GDP circuits in non-interlaced mode of scanning. The following example demonstrates how an application giving access to 4 pages of 256 x 512 in steps of 4 line scrolling, is implemented using EF9366 Graphic Display Processor.

The addition is performed on the following words :

$$\begin{pmatrix} 0 \\ 0 \\ V_7/Y_7 \\ V_6/Y_6 \\ V_5/Y_5 \\ V_4/Y_4 \\ V_3/Y_3 \\ V_2/Y_2 \end{pmatrix} + \begin{pmatrix} O_9 \\ O_8 \\ O_7 \\ O_6 \\ O_5 \\ O_4 \\ O_3 \\ O_2 \end{pmatrix} = \begin{pmatrix} O_9/R_9 \\ R_8 \\ R_7 \\ R_6 \\ R_5 \\ R_4 \\ R_3 \\ R_2 \end{pmatrix}$$

Vertical addresses generated by EF9366 + Offset = Result

As in the previous example, multiplexers are employed here to transfer in succession, to the memory, the horizontal addresses generated by the GDP and the vertical addresses supplied by the adders.

		MSL				DAD						
$\overline{ALL}$	CK	0	1	2	3	0	1	2	3	4	5	6
0	0	X_0	X_1	X_2	1	h_5	h_4	h_3	h_2	h_1	h_0	V_0
0	1				1	V_7	V_6	V_5	V_4	V_3	V_2	V_1
1	0				1	X_8	X_7	X_6	X_5	X_4	X_3	Y_0
1	1				1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

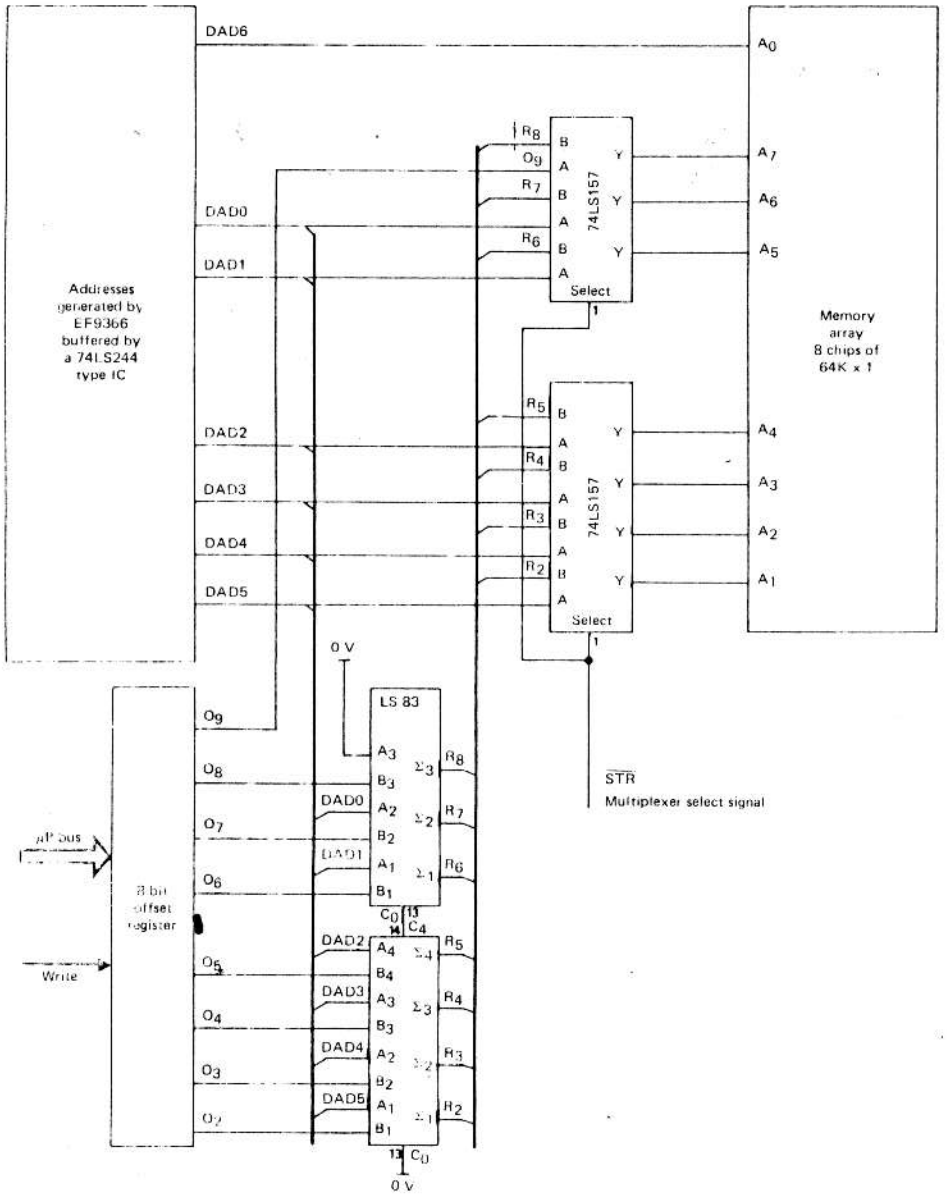
TABLE 4 – CONTROL SIGNALS GENERATED BY EF9366

	ALL	CK	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
A	0	0	O_9	DAD0	DAD1	DAD2	DAD3	DAD4	DAD5	DAD6	Display & refresh
B	0	1	R_8	R_7	R_6	R_5	R_4	R_3	R_2	DAD6	
A	1	0	O_9	DAD0	DAD1	DAD2	DAD3	DAD4	DAD5	DAD6	Write
B	1	1	R_8	R_7	R_6	R_5	R_4	R_3	R_2	DAD6	

TABLE 5 – SIGNALS GENERATED BY THE MULTIPLEXERS (DAD6 does not require multiplexing)

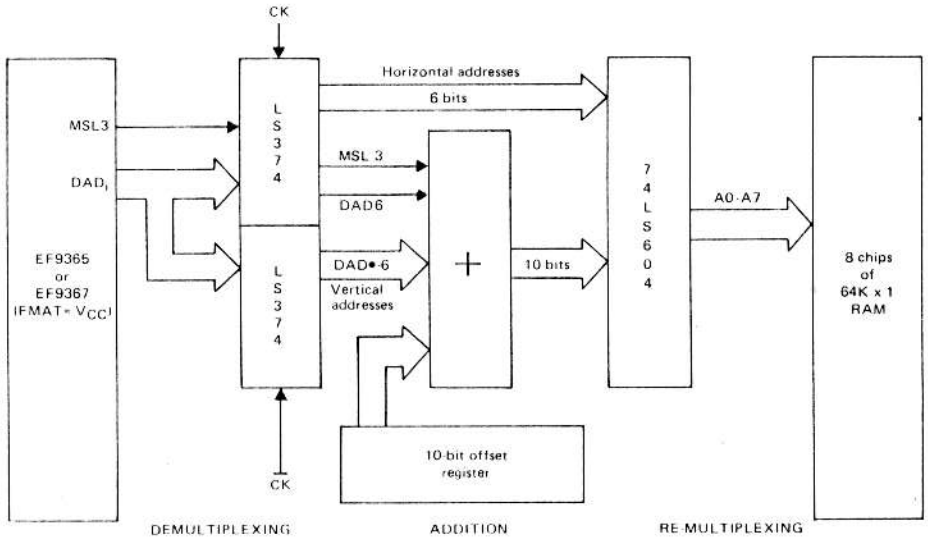
The control signal "STR" is identical to that of the preceding example.

FIGURE 6 – VERTICAL SCROLLING WITH EF9366



• The application examples discussed in the preceding sections, all perform the scrolling function in steps of 4 lines. Should a line by line scrolling be desired, it is then necessary to perform the addition on all of the vertical address bits (Y_0, ..., Y_8). These bits are multiplexed and supplied by the EF9366 circuit. It is therefore essential to demultiplex them before adding them to the contents of the offset register.

FIGURE 7 – BLOCK DIAGRAM FOR A 2 PAGE APPLICATION WITH EF9365 OR EF9367



In figure 7, it is assumed that all control and data signals supplied to the image memory and to the corresponding shift registers, are shifted (delayed) by the same amount that are the address signals after demultiplexing and re-multiplexing process.

• The fundamentals of the vertical scrolling just described, may be readily applied to horizontal scrolling. All that is necessary is to perform a similar sequence of addition on horizontal addresses.

The scrolling will then be easily accomplished in steps of 8 dots, through an adder circuit which performs the addition on h_0, ..., h_5 and X_3, ..., X_8 bits. Implementation of a dot by dot scrolling is more complicated since it involves the manipulation of 3 least significant bits X_0, X_1 and X_2, which are not present during the display cycles of the scanning process.

The implementation of such a scrolling necessitates a modification to the addressing structure of EF9365, EF9366, EF9367 and an external hardware for display counters.

APPLICATIONS OF 16K x 4 DYNAMIC RAMs (4416 type)

This new type of word-organized memory chips, offer a number of outstanding features well suited to graphic applications. In certain applications, a considerable reduction in chip count is also achieved, in using these circuits.

Nevertheless, there are a certain number of inherent particularities associated with this type of RAM chips, which prevent them from being employed in an exactly similar manner as conventional 16K x 1 or 64K x 1 RAMs.

The first particularity is the organization of the input and output lines of these memories. Data signals (4 lines) are bidirectional in contrast with conventional memory chips, which provide separate input/output pins.

Data inputs are supplied by the GDP or through a color selection logic circuitry, while the data out signals are used to load an external shift register. Consequently, in order to isolate the data in and the data out signals from each other, a three-state logic arrangement must be provided.

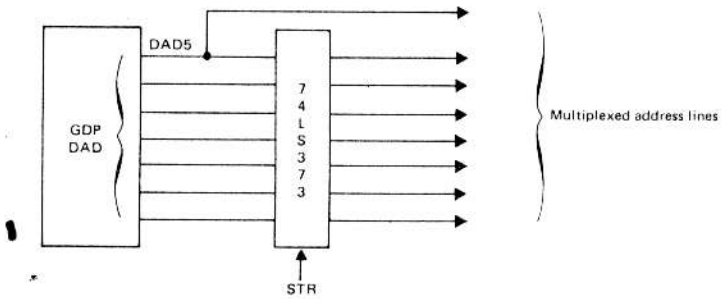
In addition, the chip select function which was, in conventional circuits, performed by $\overline{RAS}$, $\overline{CAS}$ and $\overline{WR}$ signals, is carried out differently in these memories. In fact, use is made of available control signals $\overline{OE}$ and $\overline{WE}$, which enable read and write operations while performing also, the chip select function.

The second particularity associated with these circuits is the multiplexing mode of the 14 address lines.

8 address bits must be supplied in order to be sampled by row sampling signal $\overline{RAS}$. Other remaining 6 address bits (2^{14} = 16K) are sampled by $\overline{CAS}$ signal.

The GDP supplies the address signals in a form compatible with 16K x 1 memories, that is, in two portions of 7 address bits. Interfacing is accomplished as follows : The first 7 address bits output by the GDP are stored within an external register. When following 7 address bits arrive, one of them (DAD5) is sampled with the outputs of the register by the $\overline{RAS}$ signal. Other six bits are stored and subsequently supplied to the memory chips when signal $\overline{CAS}$ becomes valid.

FIGURE 8 – INTERFACING GDP TO 16K x 4 MEMORY ADDRESS LINES



Whatever the type of the GDP (EF9365, EF9366, EF9367 - interlaced or non-interlaced mode), the 8 multiplexed address lines illustrated in Figure 8, are denoted, in display mode, by following bits : $h_5\ h_4\ h_3\ h_2\ h_1\ h_0\ V_0\ V_2$.

The entire memory is refreshed once all of the 256 possible row addresses have been scanned. In display mode, all possible combinations will be provided with an interval of 8 lines (value of V_2 is changed every 4 lines).

Therefore, in every instant of the time, the next arriving 6 lines, will refresh the entire memory.

		V_2	V_0	
line	i	1	1	
	i + 1	1	0	
	i + 2	1	1	All possible combinations
	i + 3	1	0	of V_2 and V_0 were encountered
	i + 4	0	1	in 6 lines.
	i + 5	0	0	
	i + 6	0	1	
	i + 7	0	0	
	i + 8	1	1	Interval : 8 lines

Successive bits V_2 and V_0 during display

Therefore, the interval between 2 memory accesses with identical addresses is 6 lines which corresponds to 384 μs during the display operation.

Between the last access to the display memory of a frame ($V_2 = V_0 = 0$) and the next access to the same location within the following frame, the times given below are elapsed :

- In 625 line, 50 Hz, interlaced mode : 56.5 x 64 μs + 6 x 64 μs = 4 ms.
- In 525 line, 60 Hz, interlaced mode : 54.5 x 64 μs + 6 x 64 μs = 3.87 ms.

Therefore, without even taking into consideration the refresh signals which are delivered automatically by the GDP, the requirement of refresh signals with 4 ms of duration imposed by these memories, is fulfilled.

Remarks :
For EF9365 and EF9367 circuits in non-interlaced mode or for EF9366 Graphic Display Processor, it is more appropriate to use DAD6 signal for multiplexing purposes rather than using the DAD5 signal. In fact, during the display period, bits V_0 and V_1 are supplied by DAD6 signal. Consequently, the memory is refreshed once every 4 display lines, while signals delivered by $\overline{RAS}$ are : $h_5\ h_4\ h_3\ h_2\ h_1\ h_0\ V_0\ V_1$.

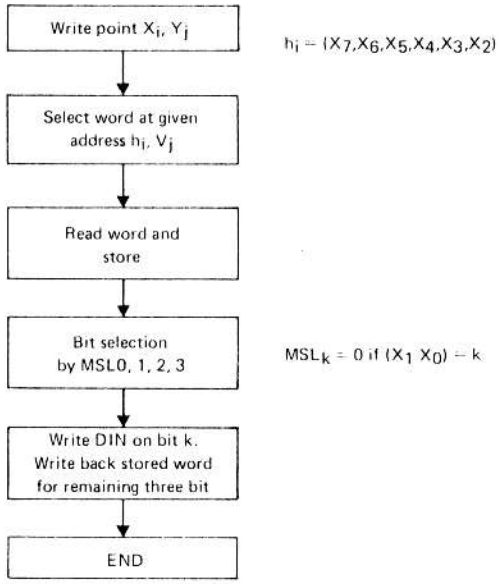
IMPLEMENTATION OF A 256 x 256 RESOLUTION USING 1 MEMORY CHIP WITH EF9365 GRAPHIC DISPLAY PROCESSOR OPERATING IN NON-INTERLACED SCANNING MODE

The EF9365 circuit allows a resolution of 256 x 256 in non-interlaced mode (FMAT – V_{SS}). In monochrome display applications, the 65536 bits (64K) representing 256 x 256 pixels, are stored within 16K x 4 bits of memory chip.

During the display cycles, memory chip provides and outputs simultaneously 4 bits which are then applied to a shift register for parallel to serial conversion in order to constitute the video signal.

During write cycles, the GDP supplies an address word (DAD signals) as well as the abscissa of the dot to be written (MSL signals) and the data (dot lit or switched off).

Since this is a word-organized memory, it is therefore not possible to execute a single bit write operation. The following discussion outlines the procedure for write cycle execution.



All these operations may be performed during one cycle, since the memory circuits discussed here authorize the execution of read-modify-write cycles.

To write a byte (clearing the screen, positioning the background), the 4 bits of the write byte are equal to DIN.

5 circuits are required in order to perform the above sequence of operation. This fact reduces the interest of employing 16K x 4 memory chips in similar applications.

SEQUENCE OF OPERATION DURING ONE MEMORY CYCLE

Signal names apply to the application diagram Figure 11.

STR 1	:	"STROBE" Control Signal for DIN, MSL, $\overline{DW}$ and BLK signals.
STR 2	:	"STROBE" Control Signal for DAD signals.
STR 3	:	"STROBE" Control Signal for DATA out signals.
$\overline{OE}$	:	Memory "READ" Enable Signal.
$\overline{WE}$	:	Memory "WRITE" Enable Signal.
$\overline{CMDOB}$	:	Enable Signal for Three State DATA buffers.
$\overline{LOAD}$	:	"LOAD" Shift Register.
SCK	:	Shift Register Clock (Dot frequency = 7 MHz).
HCK	:	System Clock (14 MHz).
CK	:	GDP Clock.
$\overline{RAS}$ & $\overline{CAS}$	:	Sampling Signals for memory row & column addresses.

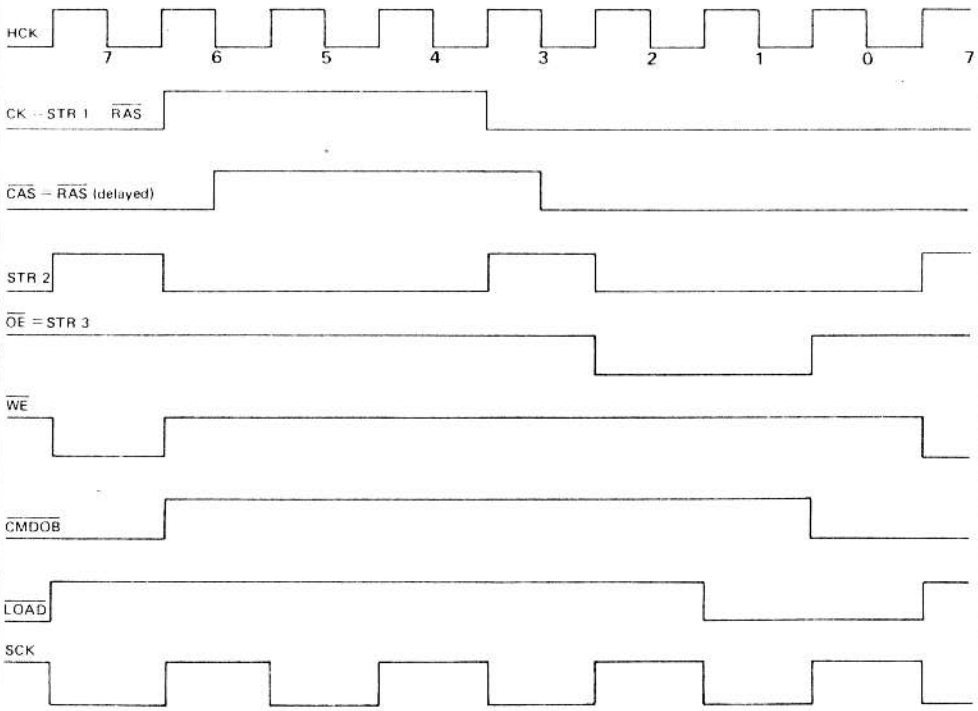
$\overline{CAS}$ signal is obtained by delaying $\overline{RAS}$ signal for approximately 30 ns.

These signals are all generated by a bipolar PROM which is addressed by a 3-bit counter whose clock is HCK. During every cycle, this PROM determines the states of output signals.

CK, $\overline{RAS}$ and STR 1 signals are the same.

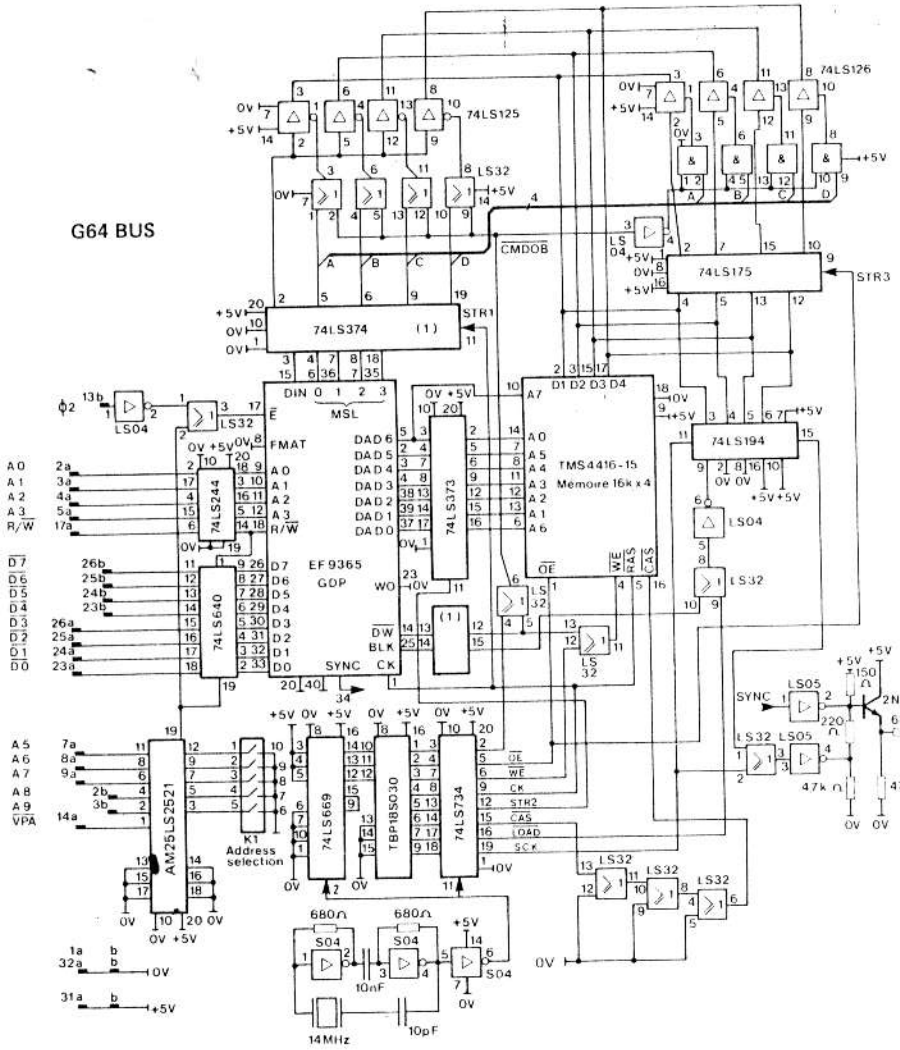
$\overline{OE}$ and STR 3 signals are also the same.

FIGURE 10 – TIMING WAVEFORMS



256 x 256 RESOLUTION USING EF9365 GRAPHIC DISPLAY PRO[illegible]SSOR

FIGURE 11 – EUROCARD MODULE BLOCK DIAGRAM (G64 BUS)



	Address / Signal	0	1	2	3	4	5	6	7
D_7	SCK	1	0	1	0	1	0	1	0
D_6	$\overline{LOAD}$	0	0	1	1	1	1	1	1
D_5	$\overline{CAS}$	0	0	0	0	1	1	1	0
D_4	STR 2	0	0	0	1	0	0	0	1
D_3	CK	0	0	0	0	1	1	1	0
D_2	$\overline{WE}$	1	1	1	1	1	1	1	0
D_1	$\overline{OE}$	1	0	0	1	1	1	1	1
D_0	$\overline{CMDOB}$	0	1	1	1	1	1	1	0
	Hexa data	86	05	C5	57	EF	6F	EF	52

A TBP 18S030 (32 x 8) type PROM is employed.
Only the first 8 bytes are used.

TABLE 6 – TIMING PROM CONTENTS

APPLICATION OF 16K x 4 (TYPE 4416) MEMORIES FOR 16 COLORS , 256 x 512 RESOLUTION , IN CONJUNCTION WITH EF9366 OR EF9367 CIRCUITS IN NON-INTERLACED SCANNING MODE.

One of the most suitable applications for these type of the word-organized memories is the application where, a pixel is represented by an entire memory word. This is the case for polychrome applications or where various levels of grey are required.

The available memory word of 4 bits will define either 16 different colors or 16 levels of grey.

The read-modify write operation is no longer required in order to execute a write instruction. This is due to the fact that, 4 new bits supplied by the color selection register, are all written simultaneously, without taking into consideration the previous state of the pixel in question.

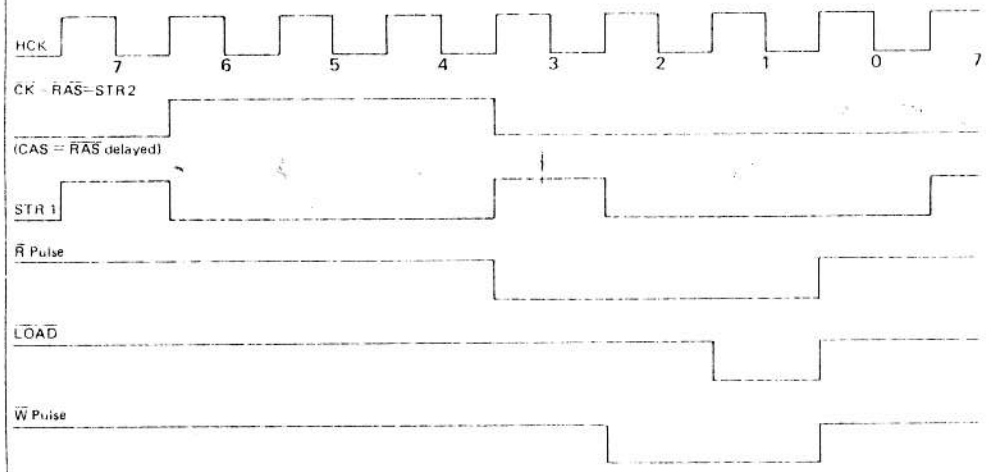
This application is quite compact, since the required hardware consists of only 8 chips for 16 colors or grey levels with a resolution of 256 x 512.

During display or refresh cycles, all for the 8 circuits are read enabled simultaneously by $\overline{OE}$ signal. The data input signals must therefore be in high impedance state.

32 bits are then output by memory chips and are subsequently supplied to four shift registers for parallel to serial conversion. In order to write a pixel ; loading of shift registers is inhibited - input data signals are enabled - and one chip out of 8 is write enabled by $\overline{WE}$ signal. The selected pixel will then accept the value corresponding to the bits supplied by color selection register. To write a byte (screen clearing, positioning the background), the 8 chips are selected simultaneously. At the end of the instruction (04, 06, 07, 0C hexadecimal), the screen will be entirely of the color defined by the color selection register.

The foregoing example does not require the DIN control signals provided by the GDP. Erase and write modes have no longer any significance. The user wishing to erase an object will remain in pen mode, will chose the background color and will then retrace the same object. This feature could have been conserved by implementing 2 color selection registers ; one for the object and the other for the background. Then, the DIN signals could have selected one of these two register (DIN = 0 ⟶ pen ⟹ foreground, DIN = 1 ⟹ eraser ⟹ background).

FIGURE 13 – TIMING WAVEFORMS



	Address / Signal	0	1	2	3	4	5	6	7
D_4	W Pulse	1	0	0	1	1	1	1	1
D_3	LOAD	1	0	1	1	1	1	1	1
D_2	R Pulse	1	0	0	0	1	1	1	1
D_1	STR 1	0	0	0	1	0	0	0	1
D_0	CK	0	0	0	0	1	1	1	0
	Hexa Data	1C	00	08	1A	1D	ID	ID	IE

A TBP 18S030 (32 x 8) type PROM is employed. Only the first 8 address bytes are used.

TABLE 8 – TIMING PROM CONTENTS

POSSIBLE EXTENSIONS OF 64K RAM MEMORY APPLICATIONS

It was seen that with a limited number of 64K memory chips, it was possible to improve performances in resolution and number of colors, in contrast with those obtained by 16K RAMs.

These characteristics may be further improved by increasing the number of memory chips. For example, a 256 colors, 512 x 512 resolution application, requires 32 memory chips of 16K x 4 (512 x 512 x 8).

One method to increase the number of colors without increasing the chip count is to employ a color palette.

The example of Figure 17 illustrates how an image containing 16 different colors selected out of possible 4096, is displayed. The color selection is achieved by 4 bits supplied by memory chips. These 4 bits are then applied, as address bits, to 3 fast memory chips (bipolar), which contain 16 words of 4 bits. The outputs of these memories (12 bits all together) are converted to R, G and B signals by 3 D/A 4-bit converters. During frame flyback, the memories are loaded with desired colors, by the microprocessors.

FIGURE 14 – APPLICATION DIAGRAM FOR 16 COLORS, 256 x 512 RESOLUTION WITH 16K x 4 MEMORIES

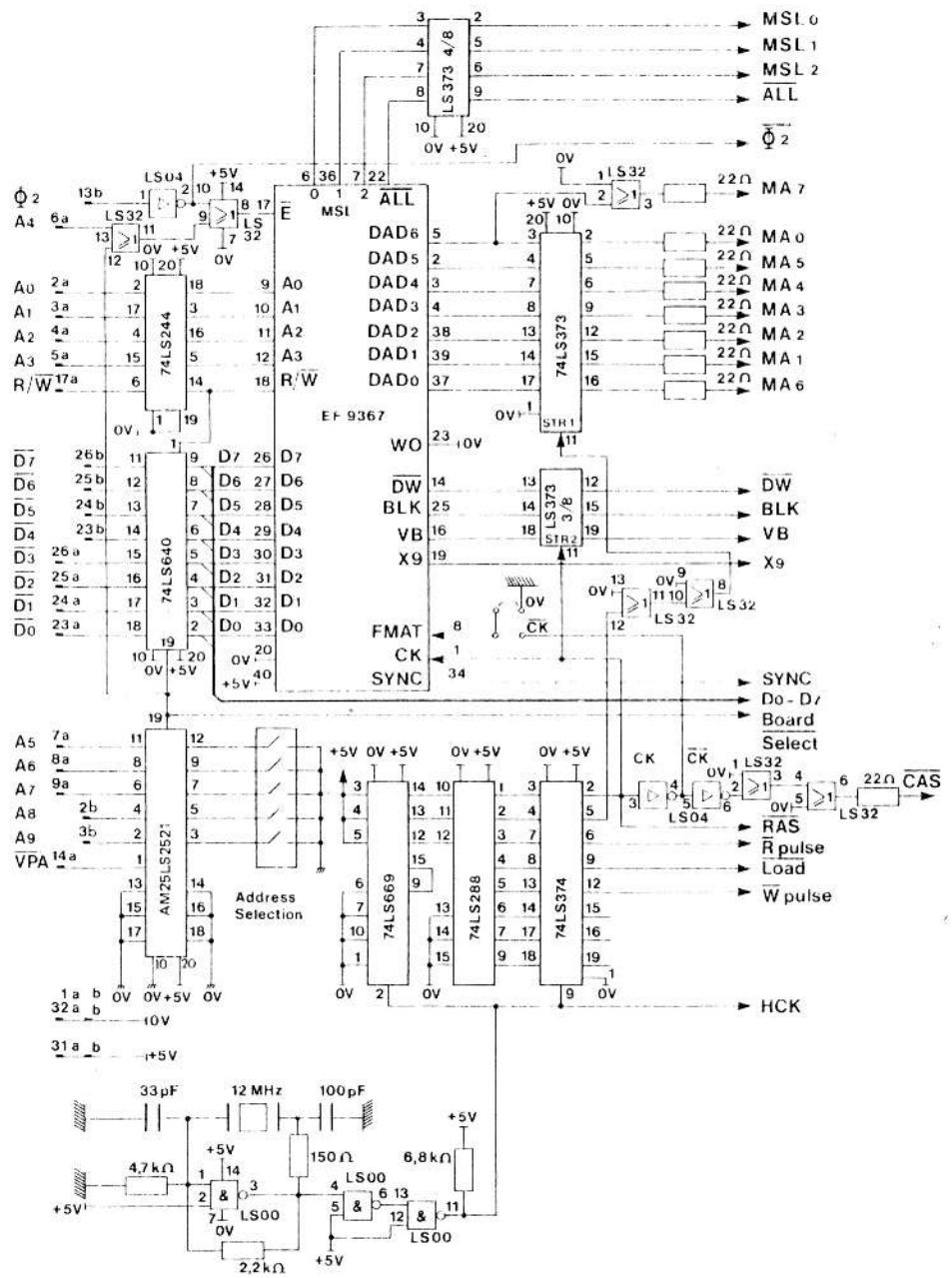
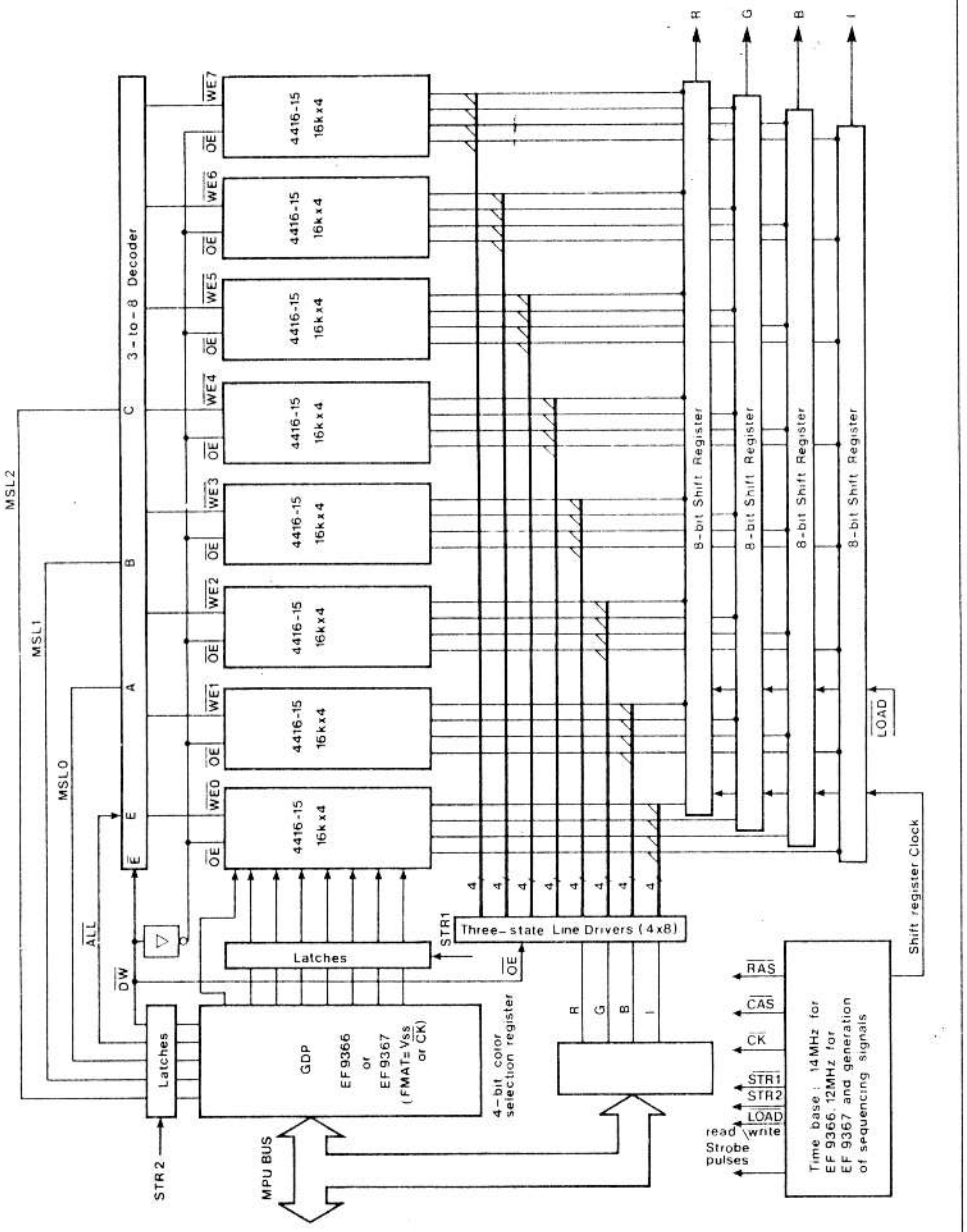


FIGURE 12 – FUNCTIONAL BLOCK DIAGRAM



CHOICE OF COLORS

Referring to Figures 15 and 16, bit I determines the level of half-intensity (darker). P_1, P_2 and P_3 potentiometers allow the adjustment of bit I influence. P_4, P_5 and P_6 potentiometers adjust the saturated levels of the colors. P_7 potentiometer adjusts the level of the synchro.

Table 7 indicates the 16 colors (including 2 blacks) selected by color selection register.

Hexa	D_3 I	D_2 B	D_1 V	D_0 R	COLOR
0	0	0	0	0	WHITE
1	0	0	0	1	CYAN
2	0	0	1	0	MAGENTA
3	0	0	1	1	BLUE
4	0	1	0	0	YELLOW
5	0	1	0	1	GREEN
6	0	1	1	0	RED
7	0	1	1	1	BLACK (1)
8	1	0	0	0	GREY
9	1	0	0	1	DARK CYAN
A	1	0	1	0	DARK MAGENTA
B	1	0	1	1	DARK BLUE
C	1	1	0	0	DARK YELLOW
D	1	1	0	1	DARK GREEN
E	1	1	1	0	DARK RED
F	1	1	1	1	BLACK (2)

TABLE 7 – COLOR SELECTION CODES

SEQUENCE OF OPERATION DURING ONE MEMORY CYCLE

Signal names apply to the application diagram Figure 14.

STR 1	: "STROBE" Control Signal for DAD signals.
STR 2	: "STROBE" Control Signal for MSL, ALL, $\overline{DW}$ and BLK signals.
CK	: GDP Clock.
HCK	: System Clock.
$\overline{LOAD}$	: "LOAD" Shift Register.
$\overline{RAS}$ & $\overline{CAS}$	: Sampling Signals for Memory Row & Column Addresses.
$\overline{W}$ Pulse	: Memory "WRITE" Enable Signal.
$\overline{R}$ Pulse	: Memory "READ" Enable Signal.

$\overline{CAS}$ signal is obtained by retarding $\overline{RAS}$ signal for approximately 30 ns.

CK and $\overline{RAS}$ signals are identical

FIGURE 15 – APPLICATION DIAGRAM CONTINUED

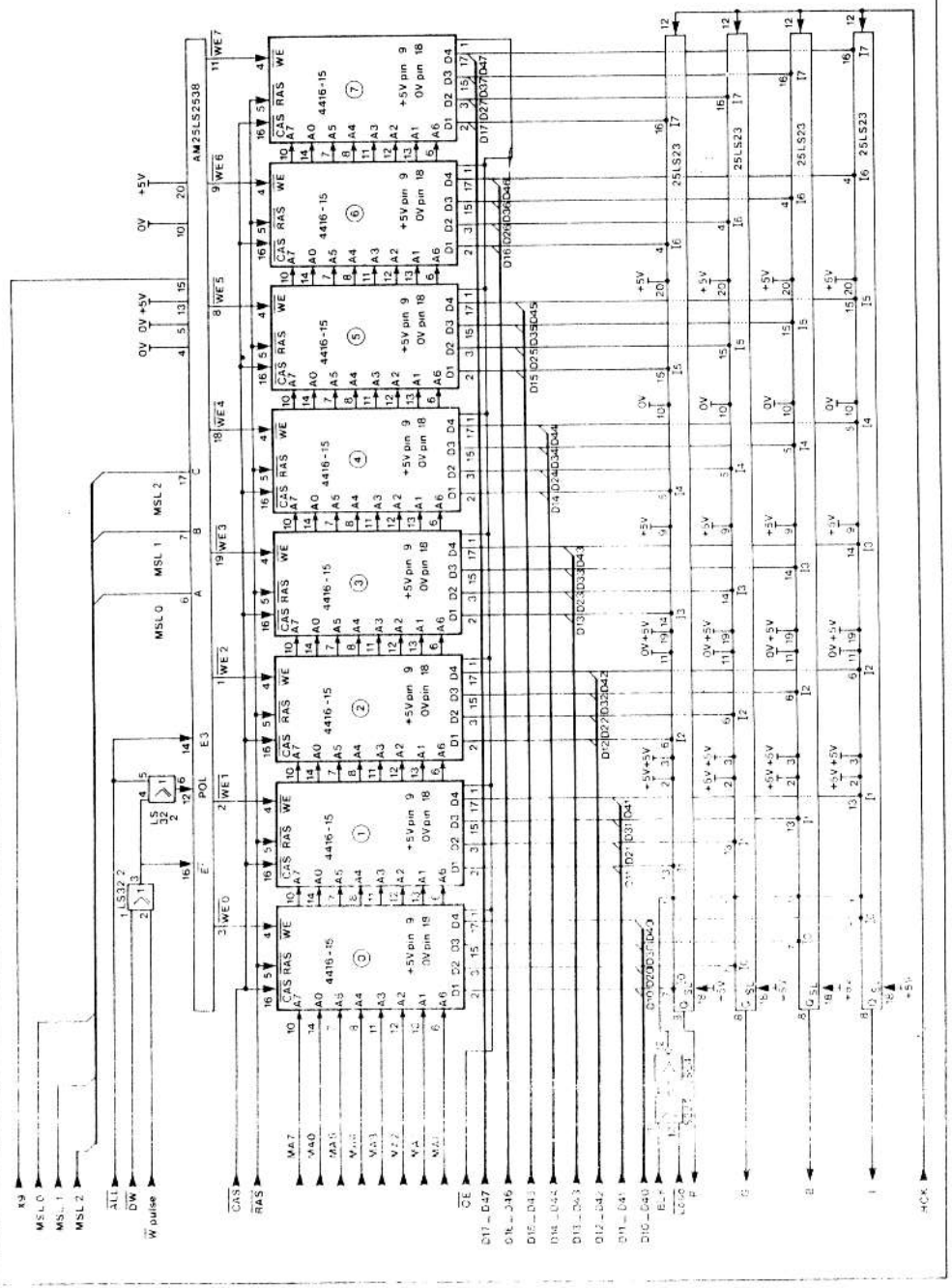


FIGURE 16 – APPLICATION DIAGRAM CONTINUED

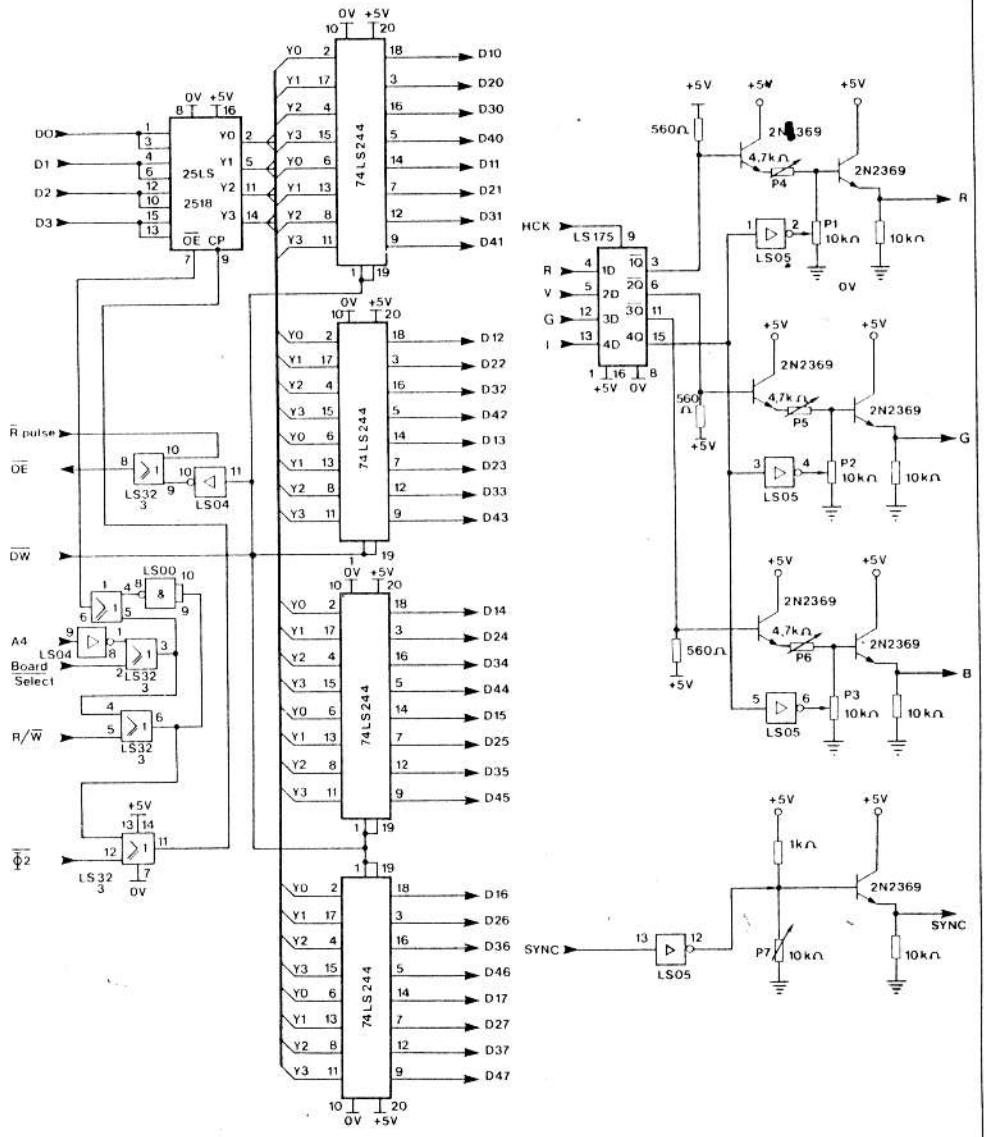
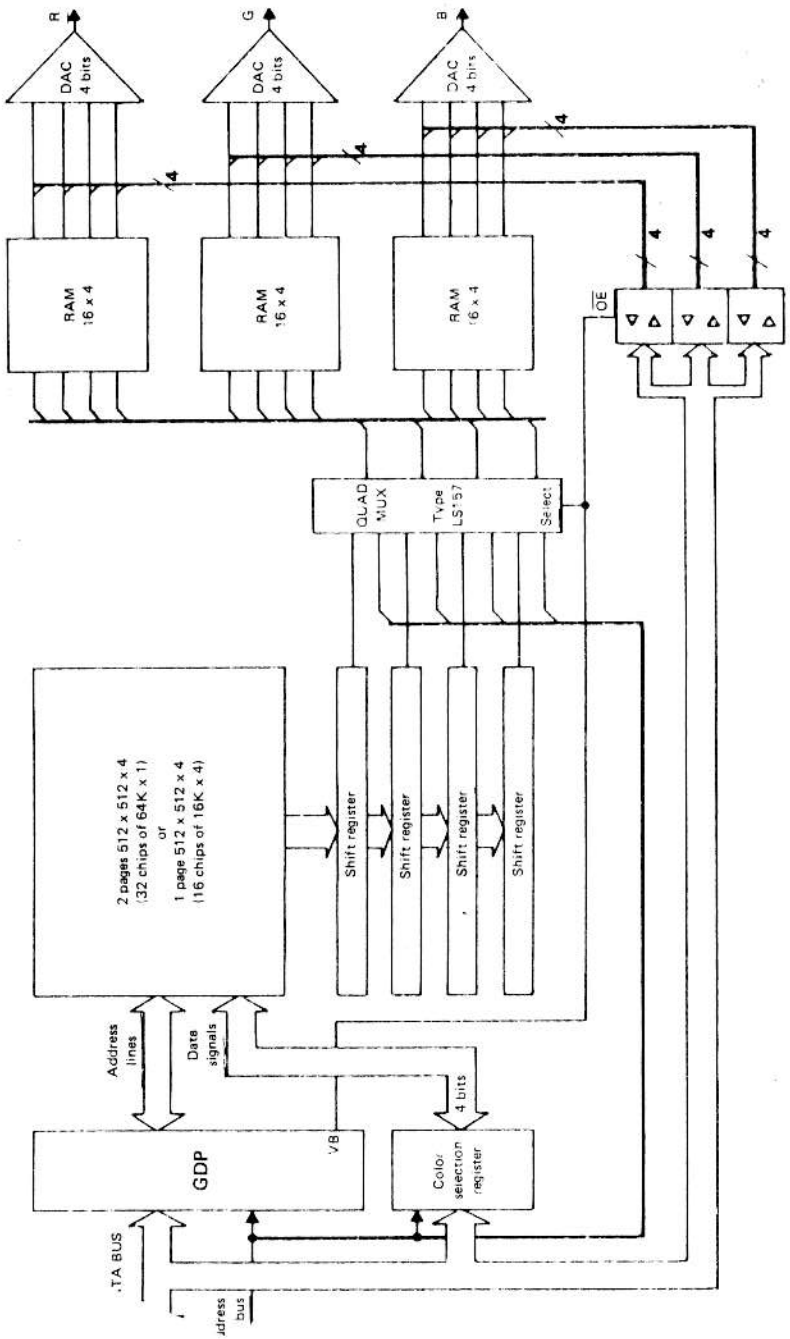


FIGURE 17 – APPLICATION BLOCK DIAGRAM FOR 16 OUT OF 4096 COLOR SELECTION (512 x 512 x 4 resolution)



Remarks concerning the application of Figure 17.

- For the sake of simplicity, the following functions were omitted in the functional diagram of Figure 17, but must be implemented :
  - Read Write control of RAMs (16 x 4) by the microprocessor during vertical blanking and by the display during frame cycle.
  - Address decoding of colour selection register.
  - Memory address decoding of RAMs (16 x 4) during microprocessor access and during display cycle.
  - Data latching at the inputs of DACs (if they do not provide this function).

- Speed of the RAMs must be compatible with the dot frequency of 12 MHz (e.g. 74S189 or SFC 80S703 type).
  - Speed of DACs must be compatible with dot frequency (e.g. HDG 0405 type).

- Implementing this application, it is possible to obtain a wide range of different colors. For example, in 256 x 256 resolution, using :
  - 8 memory chips of 16K x 4,
  - 3 memory chips of 256 x 8 and
  - 3 DAC circuits of 8 bits

  It is possible to obtain 256 different colors out of over 16 million (2^{24}) possible combinations.