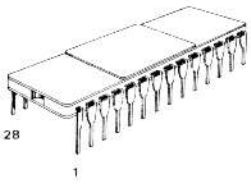
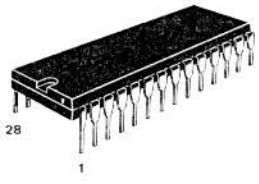
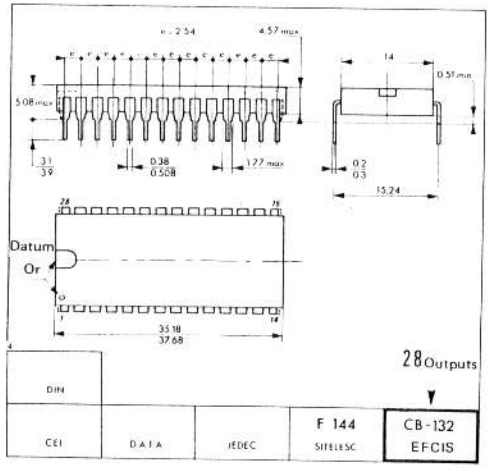
CASE CB-132



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



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Please inquire with our sales offices about the availability of the different packages.

EFCIS

THOMSON-EFCIS MOS Integrated Circuits

mosmosmosmosmosmosmosmosmosmosmos

EF9365
EF9366

PRODUCT PREVIEW

MOS

(N - CHANNEL, SILICON-GATE)

GRAPHIC DISPLAY PROCESSOR (GDP)

GRAPHIC DISPLAY PROCESSOR (GDP)

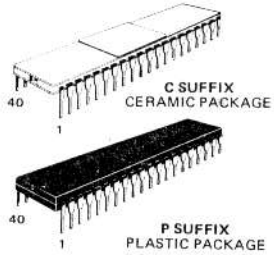
The GDP is a true high resolution graphic display processor, which contains all the functions required to process vector generation at a very high speed and to generate all the timing signals required for interfacing interlaced or non interlaced video data on a raster scan CRT display compatible with the CCIR 625 lines 50 Hz standard.

The GDP flexibility results from its direct interfacing with any 8-bit MPU bus and its 11 internal registers.

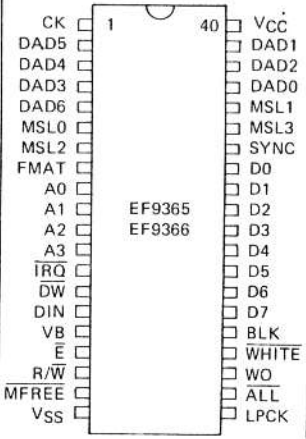
The GDP's main features are :

- Selectable resolutions in black and white or color :
  EF9365 : 512 x 512 (interlaced scan)
  256 x 256, 128 x 128, 64 x 64 (non interlaced scan)
  EF9366 : 512 x 256 (non interlaced scan)
- High speed vector plot well suited for animation (up to 1500 000 dots/sec and an average value of 900 000 dots/sec) - 4 types of lines.
- Multiplexed address and refresh for 16K or 4K dynamic RAMs
- On-chip full ASCII character generator (96) - maximum alphanumeric screen density : 85 x 57 - programmable sizes and orientations
- Direct interfacing with the monitor through the composite synchro and blanking signals
- Automatic allocation of display memory in refresh, write, dump, and display cycles
- Single + 5 volt supply
- Light pen registers and control
- Three types of interrupt request
- Fully static design
- TTL-LS compatible I/O.

CASE CB-182



PIN ASSIGNMENT



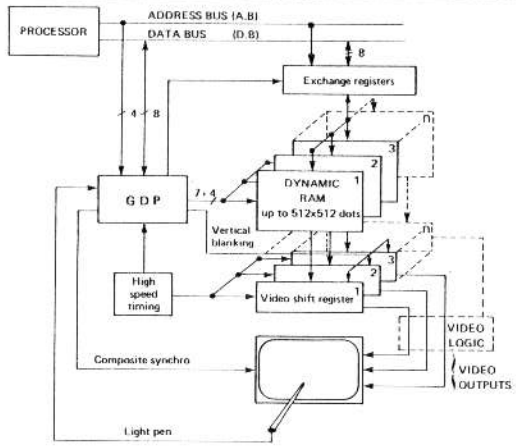


FIGURE 1 – TYPICAL APPLICATION

PP01-A
1/6

EFCIS
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78140 VELIZY
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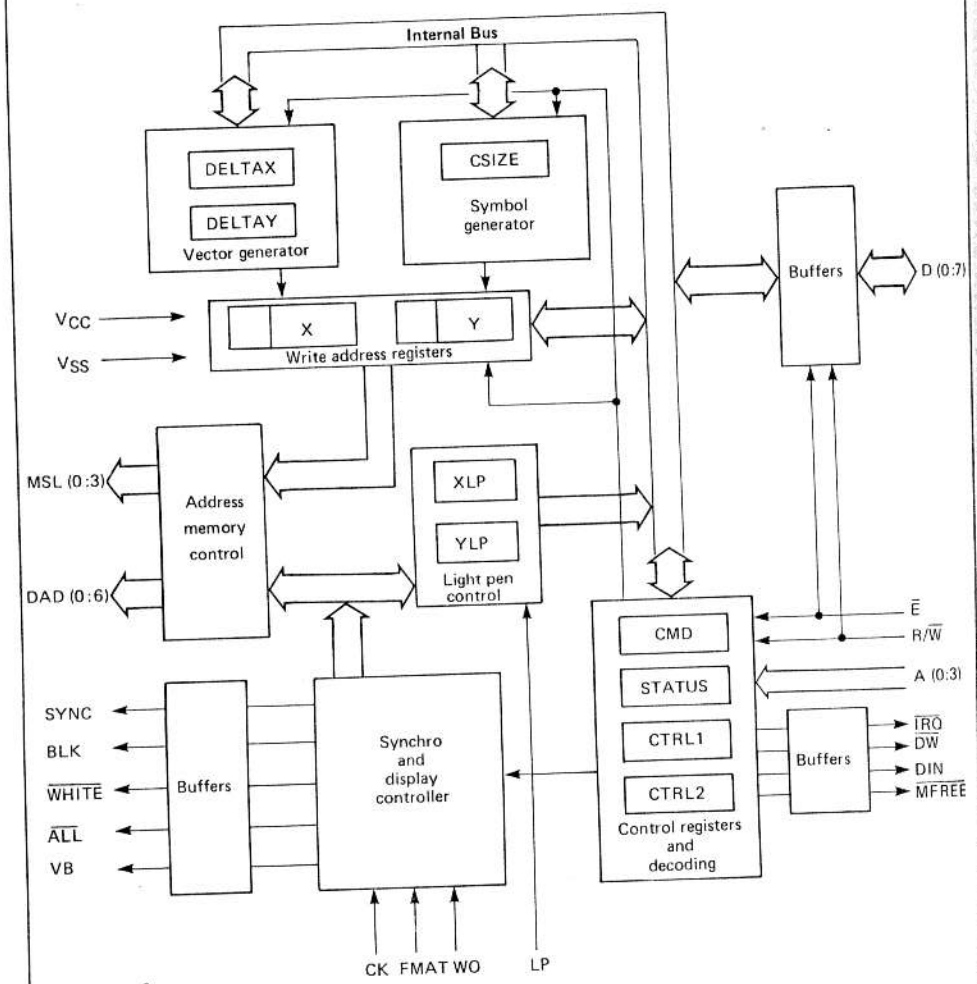
BLOCK DIAGRAM



PIN DESCRIPTION

V_{SS}, V_{CC}	:	Power supply	
CK	:	Clock (TTL level ; 1.75 MHz for the CCIR standard : 625 lines 50 Hz	
FMAT, WO	:	Inputs for selectable functions	
SYNC, BLK, VB	:	Synchro and blanking signals	
DAD (0:6), MSL (0:3), $\overline{ALL}$	:	Display memory address signals	
DIN	:	Data in	Display memory control signals
$\overline{DW}$	:	Display write	
$\overline{MFREE}$	:	Memory free	
D (0:7)	:	Data	MPU Bus
A (0:3)	:	Address	
R/W, $\overline{E}$, $\overline{IRQ}$	:	Control signals	
$\overline{WHITE}$, LPCK	:	Light pen signals	

GENERAL DESCRIPTION

The EF9365 family circuits are true graphic display processors, programmable via an 8-bit microprocessor bus. Besides all the necessary logic needed to perform a complete interface to raster scan CRT displays, the GDP includes two hardwired display processors, i.e. a vector and a character generator.

This unique feature allows an ultra fast screen writing speed (the diagonal may be written in less than 700µs) at almost no microprocessor processing cost.

The GDP is particularly well fitted to all applications in which the memory display is not directly addressed by the MPU. This feature allows a total asynchronism between the MPU and the GDP memory cycles and preserves the whole MPU memory addressing space.

Nevertheless, in the case where direct exchange between the microprocessor and the memory is necessary, the on-chip allocation controller will allow this exchange without display interference. The GDP interfaces to the processor bus on an 8-bit bidirectional data bus, a 4-bit address bus and an interrupt request line, using a Read/Write and an Enable as control signals.

DESCRIPTION OF THE 11 INTERNAL REGISTERS
(see table 1)

COMMAND REGISTER : CMD (see table 2)
Each writing in the CMD register triggers the corresponding action, i.e. :
- Vector plot sequence
- Symbol plot sequence
- Erase sequence
- Light pen sequence
- External memory access
- Writing in the internal registers.

STATUS REGISTER (see table 3)
This 8-bit read-only register gives the current status of the GDP. It should be tested to insure that an instruction which needs several cycles has been completed before sending a new one.

CTRL1 and CTRL2 CONTROL REGISTERS (see table 3)
These two 7 and 4-bit registers are used to control the GDP activity :
- Write (or erase) display memory inhibition (similar to "pen up", "pen down")
- Display write (or erase) modes
- Inhibition of the 3 MSBs of the X and Y registers (512 x 512 cyclic screen)
- Interrupt mask
- Type of line to be written (continuous, dotted, dashed and dotted-dashed)
- Character position (on the X axis, on the Y axis ; vertical or italic characters)
- Image memory write only mode. In this case, the display possibilities of the GDP are inhibited and only the write and dynamic RAM refresh cycles are provided.

C-SIZE REGISTER (see table 3)
This register contains the X and Y scaling factors used to program the size of the symbols. The 96 symbols (see table 4) are contained in a 96 x 5 x 8 dot matrix internal ROM. In the standard version of the GDP, the ROM contains the alphanumeric characters of the ASCII code. The two scaling factors are independent integers which may vary each from 1 to 16. The symbol generation sequence is started after writing the ASCII code of the symbol to be represented in the CMD register.

X and Y REGISTERS. These two 12-bit registers indicate the position of the dot to be written in the display memory. They have no relation with the current video spot position on the screen but these two registers are incremented or decremented by the internal vector and symbol generators before any writing in the display memory. They may be set to a value through direct writing of the microprocessor. These two registers define a 4096 x 4096 working address space. But only a 512 x 512 addressing space will be memorized and therefore only the 9 LSBs of each register are used. The MSBs are either ignored (cycling screen of 512 x 512) or used (cycling screen of 4096 x 4096). Due to this feature, the real display may be considered as a small window in the full addressing space. As vector coding may be completely relative, vector cutting at the edges of the screen need not be calculated but is clearly achieved by the GDP alone.

DELTA X and DELTA Y REGISTERS.
These two 8-bit registers represent the projection, on the X and Y axes respectively, of the vector to be plotted. They are unsigned values. The direction of the vector must be written in the command register : CMD.

XLP and YLP REGISTERS
These two 7 and 8-bit read-only registers contain the address of the light pen. This address is latched by the first rising edge of LPCK during the light pen sequence.

TABLE 1 – REGISTER ADDRESS

ADDRESS REGISTER					REGISTER FUNCTIONS		Number of bits
Binary				Hexa	Read R/$\overline{W}$ = 1	Write R/$\overline{W}$ = 0	
A3	A2	A1	A0				
0	0	0	0	0	STATUS	CMD (Command)	8
0	0	0	1	1	CTRL 1 (Write control and interrupt control)		7
0	0	1	0	2	CTRL 2 (Vector and symbol type control)		4
0	0	1	1	3	CSIZE (Character size)		8
0	1	0	0	4	Not used		—
0	1	0	1	5	DELTAX		8
0	1	1	0	6	Not used		—
0	1	1	1	7	DELTAY		8
1	0	0	0	8	X Most significant bits		4
1	0	0	1	9	X Least significant bits		8
1	0	1	0	A	Y Most significant bits		4
1	0	1	1	B	Y Least significant bits		8
1	1	0	0	C	XLP (Light-pen)	Not used	7
1	1	0	1	D	YLP (Light-pen)	Not used	8
1	1	1	0	E	Not used		—
1	1	1	1	F	Not used		—

TABLE 2 – COMMAND REGISTER

b3 b2 b1 b0		b7 b6 b5 b4 = 0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 0 0	0	Set bit 1 of CTRL1 : Pen select	Vector generation (for b2, b1, b0 see small vector definition)	SPACE	0	@	P	`	p								
0 0 0 1	1	Clear bit 1 of CTRL 1 : Eraser select		!	1	A	Q	a	q								
0 0 1 0	2	Set bit 0 of CTRL1 : Pen/Eraser down select		"	2	B	R	b	r								
0 0 1 1	3	Clear bit 0 of CTRL 1 : Pen/Eraser up select		#	3	C	S	c	s								
0 1 0 0	4	Clear screen		$	4	D	T	d	t								
0 1 0 1	5	X and Y registers reset to 0		%	5	E	U	e	u								
0 1 1 0	6	X and Y reset to 0 and clear screen		&	6	F	V	f	v								
0 1 1 1	7	Clear screen, set CSIZE to code "minsize" All other registers reset to 0 (except XLP, YLP)		'	7	G	W	g	w								
1 0 0 0	8	Light-pen initialization	Special direction vectors (for b2, b1, b0 see small vector definition)	(	8	H	X	h	x								
1 0 0 1	9	Light-pen initialization		)	9	I	Y	i	y								
1 0 1 0	A	5 x 8 block drawing (size according to CSIZE)		*	:	J	Z	j	z								
1 0 1 1	B	4 x 4 block drawing (size according to CSIZE)		+	;	K	[	k	{								
1 1 0 0	C	Screen scanning : Pen or Eraser as defined by CTRL1		,	<	L	\	l	¦								
1 1 0 1	D	X registers reset to 0		–	=	M	]	m	}								
1 1 1 0	E	Y registers reset to 0		.	>	N	↑	n	¬								
1 1 1 1	F	Direct image memory access request for the next free cycle.		/	?	O	←	o	▒								

SMALL VECTOR DEFINITION :

b7	b6 b5	b4 b3	b2 b1 b0
1	|ΔX|	|ΔY|	Direction

Dimension

ΔX or ΔY		Vector length
0	0	0 step
0	1	1 step
1	0	2 steps
1	1	3 steps

Direction

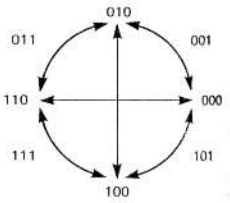
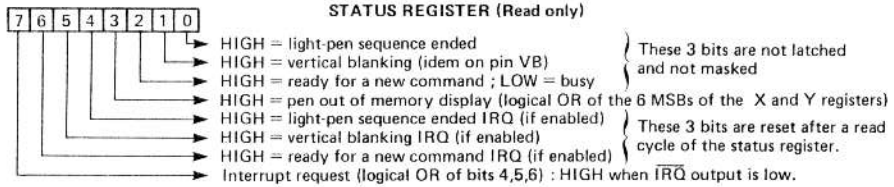
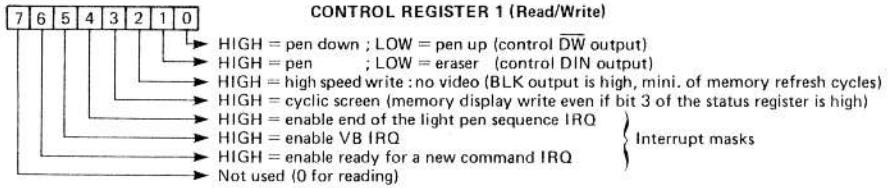


TABLE 3 : OTHER REGISTERS

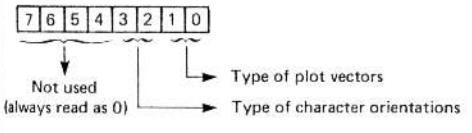
STATUS REGISTER (Read only)



CONTROL REGISTER 1 (Read/Write)



CONTROL REGISTER 2 (Read/Write)

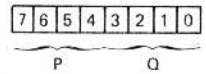


b_1	b_0	Type of plot vector	
0	0	——— continuous	
0	1	------- dotted	2 dots on, 2 dots off
1	0	– – – dashed	4 dots on, 4 dots off
1	1	—·—· dotted-dashed	10 dots on, 2 dots off, 2 dots on, 2 dots off.

Types of character orientations

$b_3 = 0, b_2 = 0$ $b_3 = 0, b_2 = 1$ $b_3 = 1, b_2 = 0$ $b_3 = 1, b_2 = 1$

C-SIZE REGISTER (Read/Write)



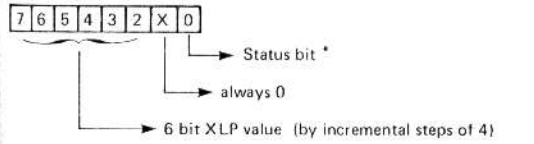
P : Scaling factor on X axis
Q : Scaling factor on Y axis

P and Q may take any value between 1 and 16. This value is given by the leftmost or rightmost 4 bits for P and Q respectively. Binary value (0) means 16.

X and Y REGISTERS

The 4 MSBs of X and Y are located in the LSB positions of addresses 8 and A respectively (the 4 leftmost bits are always 0). The 8 LSBs of X and Y are located in addresses 9 and B respectively.

LIGHT PEN REGISTER (XLP Register)

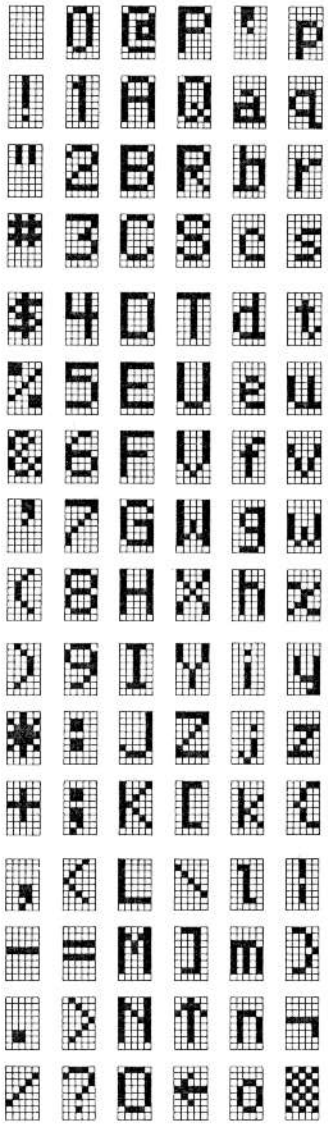


* Set if a rising edge occurs on the LPCK during the frame of a light pen sequence. The status bit is reset after reading of XLP or YLP.

TABLE 4 – ASCII CHARACTER GENERATOR (5 x 8 matrix)

b7	0	0	0	0	0	0
b6	0	0	1	1	1	1
b5	1	1	0	0	1	1
b4	0	1	0	1	0	1

b3	b2	b1	b0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



This circuit has been designed and developed in conjunction with the ENS - Paris.

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Bipolar peripheral circuits

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