PRELIMINARY

iPCB-75 PC-BUBBLE™ CARD 4-MEGABIT BUBBLE MEMORY EVALUATION PACKAGE

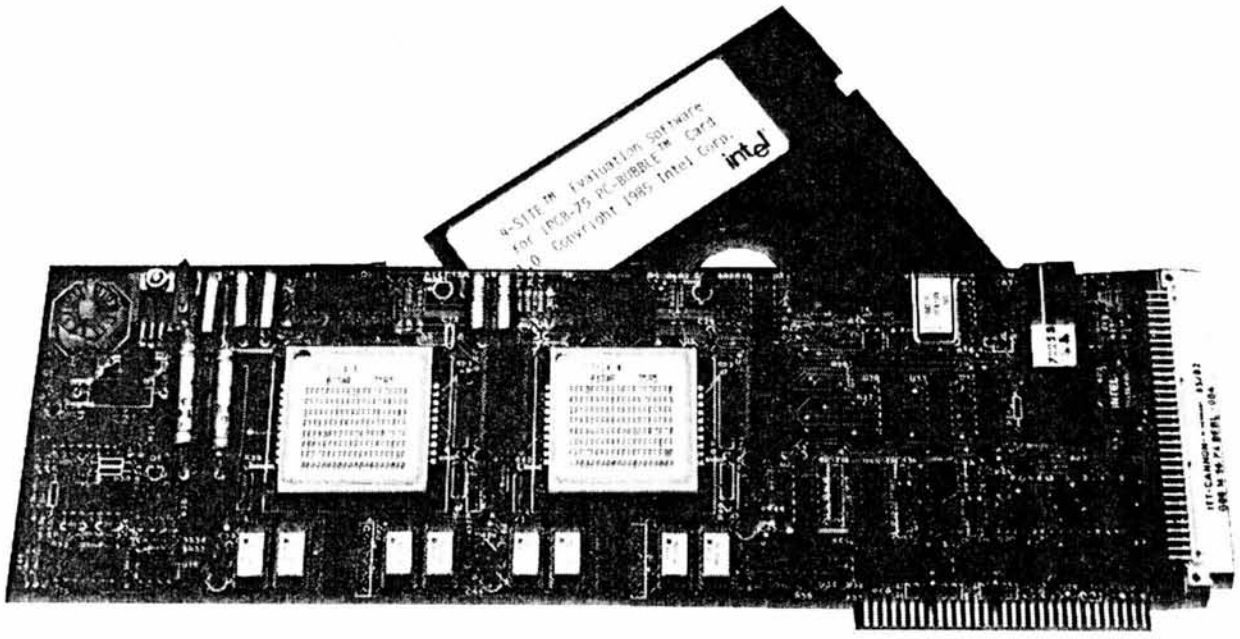
- **Hosted on IBM* PC, PC/XT, or PC/AT (or Compatible Systems)**
- **Available with One or Two 7114 Bubble Memory Devices (512K Bytes or 1-Megabyte)**
- **Polled, Interrupt, or DMA Data Transfer Capability**
- **Industry's Most Advanced Bubble Memory Controller with 128-Byte FIFO**
- **LEDs for Monitoring Coil Activity and Write-Protect Status**
- **Interactive 4-SITE™ Software for Learning to Program the Bubble Memory Controller**
- **Color Mode for Systems with Color Monitor (Monochrome Mode for Use with Monochrome Monitors)**
- **Expansion Connector for Use with Non-IBM Host Systems, Monitoring BMC Signals, or Evaluating Four- and Eight-Bubble Configurations**
- **Operates from Standard +5Vdc ±5% Supply**

The iPCB-75 PC-BUBBLE™ Card Evaluation Package is a complete hardware and software package for evaluating Intel 4-Megabit Magnetic Bubble Memory architecture and components. Hosted on an IBM PC, PC/XT, PC/AT, or other compatible systems, PC-BUBBLE card is available with one or two 7114 devices, yielding storage densities of 512K bytes or 1-Megabyte, respectively.

The interactive 4-SITE™ software evaluation program allows a design engineer to quickly learn to program the 7225 Bubble Memory Controller (BMC). All fundamental bubble memory operations can be performed in response to simple commands entered at the keyboard. 4-SITE includes color mode and a graphic representation of the BMC registers (shown in hex and binary), FIFO, and data buffers to allow a user to verify configuration and programming. A design engineer can monitor command execution and BMC status, and can display data buffers for comparison or verification.

A 96-pin DIN connector allows direct access to BMC signals for use with non-IBM systems. The connector can also be used to monitor BMC signals or to daisy-chain additional PC-BUBBLE Cards for evaluation of four- and eight-MBM configurations. Jumpers are used to change hardware configuration. LEDs are used to monitor coil activity and write-protect status.

*IBM is a trademark of International Business Machines Corporation.
**Microsoft is a trademark of Microsoft Corporation.



290100-1

October 1985

Order Number: 290100-001

HARDWARE DESCRIPTION

Like many high-density peripheral devices, bubble memory data is accessed serially as pages of data rather than as individually addressed bytes. Pages can be 64, 128, 256, or 512 bytes in size (larger page sizes require multiple MBMs operating in parallel). Data transfers between system memory and the 7114 devices are performed under control of the host CPU and the on-board 7225 BMC. Data transfer between the BMC and system memory can also be performed by the host system DMAC (Direct Memory Access Controller).

Advanced Bubble Memory Controller

The 7225 BMC contains a 128-byte FIFO, five parametric registers, a command register, and a status register. The parametric registers are loaded with address, block length, and execution mode information prior to issuing many BMC commands. A set of 18 separate commands can be issued to the command register to initialize and access bubble memory devices (only a few basic commands are typically used for reads/writes). Current status of the BMC and the results of BMC commands are determined by reading the status register. The 7225 BMC supports three data transfer modes and two command execution modes.

The three data transfer modes are: DMA mode, interrupt mode, and polled mode. In DMA mode, the host system 8237 DMAC works together with the 7225 BMC to transfer data beween the BMC FIFO and system memory at high speeds to eliminate almost all CPU overhead. In interrupt mode, the 128-byte FIFO provides full page bufferring to eliminate real-time programming constraints. Polled mode allows a very simple driver to be developed for applications where CPU time can be dedicated to data transfer operations.

The two command execution modes are: interrupt mode and polled mode. In interrupt mode, the BMC indicates command completion or termination by generating an interrrupt to the CPU. In polled mode, the CPU polls the BMC Status Register to determine command completion or termination.

PC-BUBBLE™ Card Features

The iPCB-75 PC-BUBBLE Card includes the following additional hardware features that increase its flexibility and/or enhance its usefulness as an evaluation tool:

- PC bus interface logic buffers all signals and provides user-selectable I/O address, interrupt request, and DMA request/acknowledge signals
- DIN expansion connector allows use with non-IBM systems. It also allows BMC signals to be monitored by a logic analyzer or scope. Finally, the connector allows additional PC-BUBBLE Cards to be connected in a daisy chain for evaluating four or eight bubbles controlled by one BMC. (A custom cable is required to connect additional PC-BUBBLE Cards.)
- Automatic power-fail circuit provides data protection
- Write-protect jumpers allow 7114s to be individually write-protected
- LEDs indicate write-protect status and MBM coil rotation for each MBM present

An on-board +12Vdc step-up switching regulator allows the board to draw power from only the host system's +5Vdc ±5% power supply.

4-SITE™ SOFTWARE DESCRIPTION

The iPCB-75 evaluation package includes 4-SITE, an interactive software program that speeds development of I/O drivers for bubble memory by allowing a user to quickly learn to program the 7225 BMC. 4-SITE software provides an on-line graphic representation of BMC registers and offers a simple command language for communicating with the BMC. With the 4-SITE program, a design engineer can read/write the BMC registers and FIFO, issue commands to perform MBM operations, monitor status, operate bubbles in serial or parallel (at least two MBMs are required for parallel operation), fill, alter, and display data buffers, verify hardware operation, etc. Color mode supports multi-color displays for IBM PCs with color monitors (monochrome mode is used for monochrome monitors).

4-SITE software is partitioned into two layers: low-level BMC command routines written in ASM86, and a higher-level command processor written in BASIC. ASM86 source code is provided for the low-level routines to allow modification and reassembly for evaluaton of custom applications. (The ASM86 source code can be assembled on Version 3.0 or greater of Microsoft's 8086 Macro Assembler.) The higher-level command processor runs under Version 2.0 or greater of IBM's BASIC Interpreter. A copy of the 4-SITE command processor can be modified as required for the custom applications. 4-SITE software executes in an IBM PC, PC/XT, PC/AT, or compatible systems. (4-SITE does not directly support systems that interface to the BMC through the DIN connector.)