SERVICE PC / DOCUMENTATION

Documentation Update

List of Affected Pages

vii & viii

3.2 2-3 & 3.2 2-4

3.2 5-1 & 3.2 5-2
3.2 5-3 & 3.2 5-4
3.2 5-5 & 3.2 5-6

3.2 6-3 & 3.2 6-4

3.2 7-1 & 3.2 7-2

3.2 13-9 & 3.2 13-10
3.2 13-11 & 3.2 13-12

Circuit diagram 5103 108 0271 (Mainboard)
3 sheets (130-01, 02 and 03)

3.3 10-1 & 3.3 10-2

3.7 1-1 & 3.7 1-2

4.2 1-1 & 4.2 1-2

Order Form

4.2 2-1 & 4.2 2-2

4.2 6-3 & 4.2 6-4

Manual Status Form

Comment Form

SERVICE PC / DOCUMENTATION

Documentation Update

MANUAL : P2000C System Reference and Service Manual

12 NC : 5103 993 30421

AMENDMENT : 1

DATE : 20th April 1984

NOTE : 12 NC becomes 5103 993 30422 after incorporating this amendment.

INSTRUCTIONS

Remove and replace the pages indicated in the 'List of Affected Pages'.

Update the 12 NC number on the Front Page and the Spine Label to reflect the change of 12 NC number.

Significant changes to the text (or illustrations) are marked with a line in the outer margin.

The deletion of text is marked with the symbol '*'.

Incorporation of Amendment 1 to 5103 993 30421 will bring the document to the same technical standard as 5103 993 30422, released at the same time.
Minor typographical errors have not been corrected.

Please file this sheet behind the Front Page to indicate that the amendment has been incorporated.

CHAPTER 2 - HARDWARE CONFIGURATION AND PERIPHERAL EXTENSIONS

PART 3
DETAILED DESCRIPTION AND SERVICING

INTRODUCTION

CHAPTER 1 - POWER SUPPLY

CHAPTER 2 - MAINBOARD

3 CIRCUIT DESCRIPTIONS

3.1 Data Bus and Address Bus

As shown in figure 2.2, the system data bus is partly buffered. Although the CPU (item 7437) is able to drive four LS TTL loads, this buffering ensures that a maximum of three loads are on the data bus at any time. The Address bus is fully buffered. The CPU address bus and the DMA address lines are simultaneously buffered by the same two I.C. drivers 74 LS 244 (items 7435/7436).

3.2 Control Bus

Two components on the Mainboard (DMA and USART) require special compound signals, which are produced by items 7457, 7419 and 7420 as follows:

IORD-N signal formed from the RD-N & IORQ-N signals.
IOWR-N signal formed from the WR-N & IORQ-N signals.

In order to prevent any possibility of timing problems between a RAM access and a Refresh, the MREQ-N signal is "precharged" using a circuit consisting of two D-FF's (Item 7461).
RAS Precharge Time - worst case = 60 ns.

Precharge logic timing is shown with the DMA/CPU Timing Diagram on page 3.2 3-6.

Note : This circuit only functions during an Opcode fetch (activated by M1-N). Correct function is only guaranteed if no wait states are used. In memory write or read and I/O cycles, this circuit remains idle.

The Control Bus signals are fully buffered.

For situation of CPU in relation to other Mainboard circuits, please refer to the full circuit diagrams.

3.3 Additional Signals

The signals RES-N and NMI-N can be activated by external debounced switches. Only the RESET switch is implemented.
At each power-up the RES-N signal is automatically activated. The signal NMI-N is also activated during the power up phase but is of shorter duration (due to the use of a smaller CR time constant) than the RESET and does not affect the CPU operation.

The DMA is programmed by, and works under the control of, the CPU. A handshake routine, in the form of a simple data exchange, is used to allocate use of the data bus to the DMA as required and to ensure that only one device attempts to use the bus at any time. BUSAK-N controls the tristate outputs of the Bus buffer, offering a high impedance to the bus. BUSAK-N and BUSRQ-N work with the 8257 DMA. Both of these signals are available on the Bus plug.

The priority logic ensures that internal DMA (bus request HRQ) has priority over additional, external DMA on the bus extension (bus request BRE), in the event of contention. However, once either internal or external DMA has initiated a transfer, no interruption is allowed.

The Z80A can be used in three interrupt modes - 0, 1 and 2. The P2000C uses Interrupt mode 2, which is supported by two CTCs (used as Interrupt controllers) and the SIO. If the basic unit is extended, via the 120 way Bus plug, only one additional Z80 Interrupt device is allowed. This is because a maximum of four devices are allowed with the 4 MHz configuration due to delay times in the interrupt daisy chain. Further details of the Z80A Interrupt Modes are given in the CPU Data Sheet.

The Wait line is not used on the Mainboard, and must not be used on the optional extension board in combination with an Opcode fetch cycle. It can be used on the extension board to slow down I/O transfers when working with slower devices.

Detailed Description and Servicing
Mainboard - Clock Generator

1 GENERAL

All frequencies which are needed on the Mainboard are produced by the Clock Generator, including some special signals:

16 MHz
8 MHz
4 MHz
2 MHz
1 MHz
615,38 kHz
Write clock for the FDC (WCK)

2 BLOCK DIAGRAM

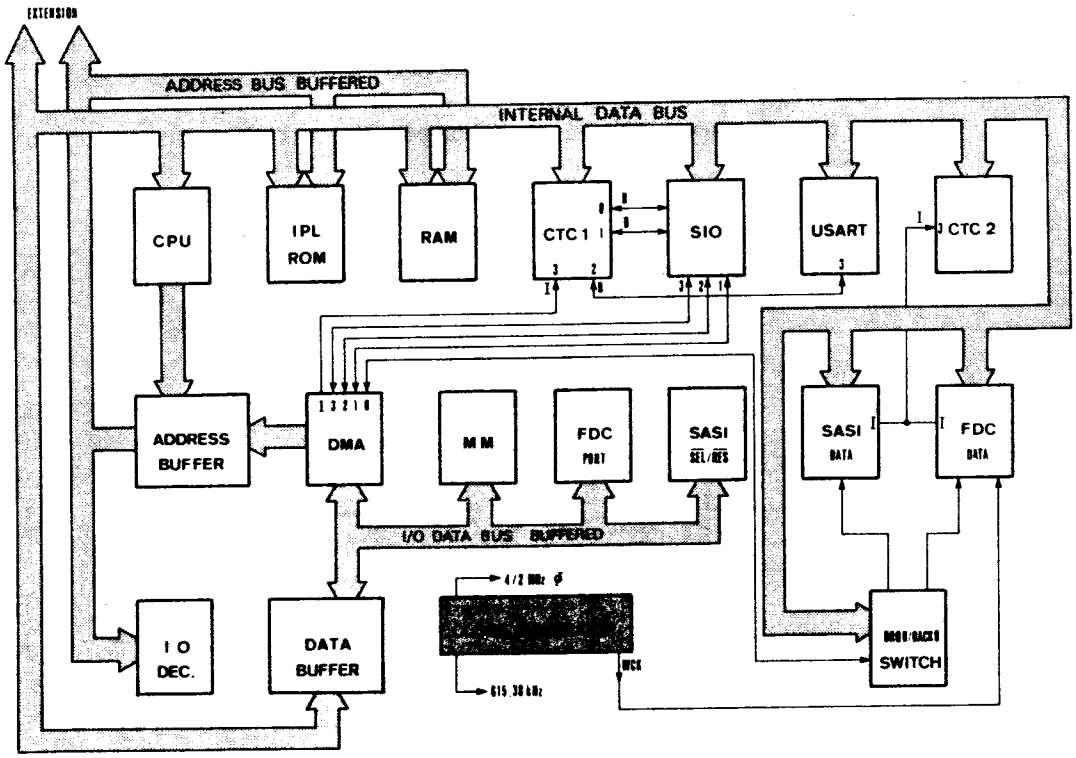


Figure 2.7 P2000C - Clock Generator Block Diagram

Detailed Description and Servicing
Mainboard - Clock Generator

3 CIRCUIT DESCRIPTION

A quartz stabilised Colpits-Oscillator generates a frequency of 16 MHz. It is followed by a TTL-buffer (item 7467) with a Schmitt-trigger input. The outputs are obtained, by division, from a 4 bit binary counter (items 7489/7490). See figure 2.10.

The 4 MHz signal is used as the system clock. Due to the use of slower ROMs, the system clock is switched over to 2 MHz when the Memory Manager accesses ROM. (MM2 = 0).
The circuit with two flip-flops (item 7488) ensures that no spikes can be produced in the clock during switch over. (Both input clocks are "0" during the switch-over, making the following Open Collector Drivers (item 7487) inactive.)
(See Timing Diagram - A)

The 8 MHz signal is used to clock a second 4 bit counter. It is wired to count down from 12 to 0 in order to create the input frequency of 615.38 kHz used for the Baud Rate Generators. (Note: 19 200 x 32 = 614.4 kHz, a deviation of 0.16%).
(See Timing Diagram - B)

The 1 MHz signal is used to generate an asynchronous 500 kHz signal (2us cycle-time). This signal is combined with the 2 MHz signal (250 ns one half-cycle) to produce the timing for the Floppy Disk Write Clock WCK (using item 7486). The two inverters (item 7467) are used to delay the 500 KHz signal to avoid spikes in the WCK signal. (See Timing Diagram - C)

Timing diagrams for the Mainboard Clock Generator are shown in figure 2.9.

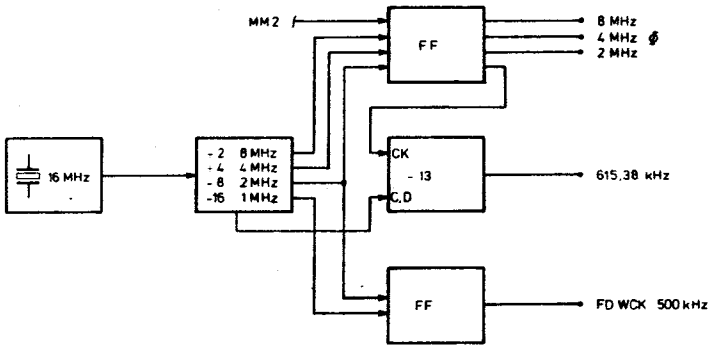
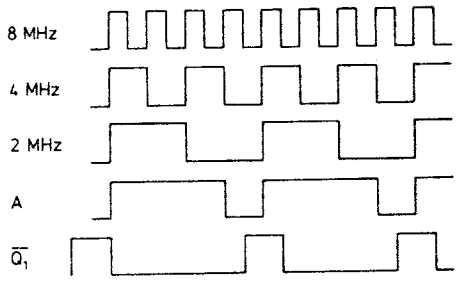


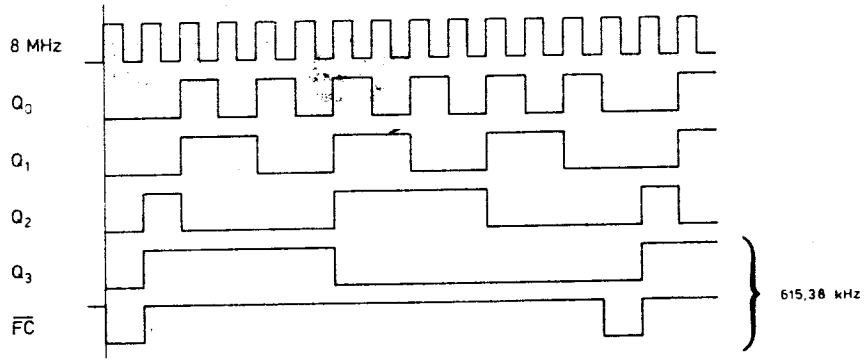
Figure 2.8 Clock Generator - Detailed Block Diagram

Detailed Description and Servicing
Mainboard - Clock Generator

A - System Clock



B - Baudrate Generation



C - FDC WCK Generation

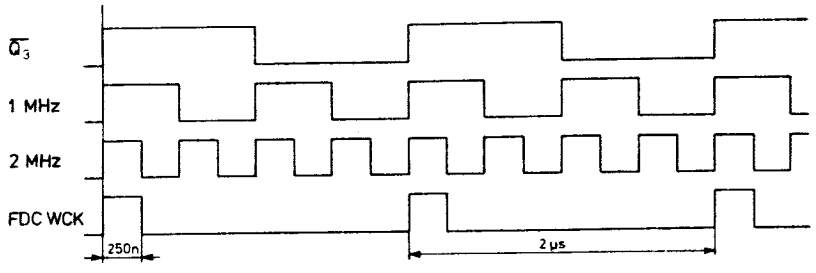


Figure 2.9 P2000C Clock Generator - Timing Diagrams

5-4

Detailed Description and Servicing
Mainboard - Clock Generator

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Detailed Description and Servicing
Mainboard - Clock Generator

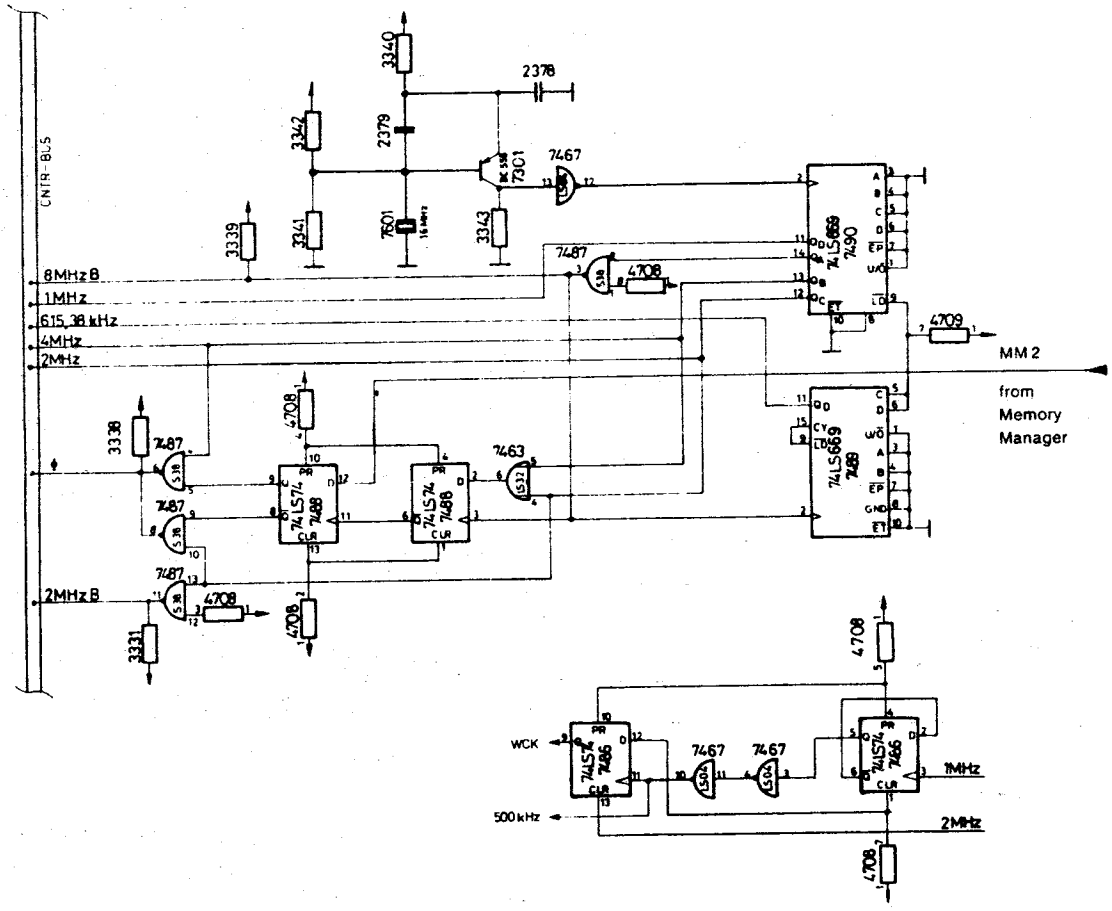
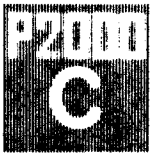


Figure 2.10 Circuit Diagram - Clock Generator



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Detailed Description and Servicing
Mainboard - I/O Decoder

The decoding is shown table 2.13:

Table 2.13 - I/O Decoding

IF AB0-AB7 ARE SET	ADDR	CIRCUIT DECODES	GIVING
AB 7 6 5 4 3 2 1 0		AB7,6,5,4	
0 0 0 0 X X X X	0X	S2,M1B-N	CSDMA-N
AB 7 6 5 4 3 2 1 0			
0 0 0 1 1 1 1 0	1EH	IOWRB-N	CSMM-N
0 0 0 1 1 1 1 1	1FH	AB0	CSFD-N
AB 7 6 5 4 3 2 1 0		AB3,2,1	
0 0 0 1 0 0 0 1	11H		CS0-N
0 0 0 1 0 1 0 1	15H		CS2-N
0 0 0 1 0 1 1 1	17H		CS3-N
0 0 0 1 1 0 0 1	19H		CS4-N
0 0 0 1 1 0 1 1	1BH		CS5-N

AB0 is hard wired to the device.

AB 7 6 5 4 3 2 1 0		AB3,2	
0 0 1 0 0 0 1 1	23H		CS8-N
0 0 1 0 0 1 1 1	27H		CS9-N
0 0 1 0 1 0 1 1	2BH		CSA-N

AB0, AB1 are hard wired to the device.

Detailed Description and Servicing
Mainboard - I/O Decoder

3.1 Mainboard I/O Addresses

The Mainboard I/O addresses are given below:

Address	Signal	Device	Direction
00 - 08	CSDMA-N	Intel 8257 DMA	read & write
09 - 0F		Do not use	
10, 11	CS0-N	Trigger IC 7443 (74LS107)	
12, 13	CS1-N	not used	
14, 15	CS2-N	8251A USART (for printer)	read & write
16, 17	CS3-N	SASI Data	read & write
18, 19	CS4-N	SASI Control	read & write
	read:	write:	
	bit 0 : REQ	-	
	bit 1 : C/D-N	-	
	bit 2 : MSG	SEL-N	
	bit 3 : BSY	RES-N	
	bit 4 : I/O-N	-	
	bit 7 : C/D-N	-	
1A	CS5-N	NEC 765 FDC (status)	read & write
1B		NEC 765 FDC (data)	read & write
1C, 1D	CS6-N	not used	
1E	CSMM-N	Memory Manager	write only
	bit 0 to bit 3 giving MM1 to MM4		
	(Set to 0 for IPL ROM; set to 2 for System RAM)		
	(On RESET, IPL ROM is activated)		
1F	CSFDP-N	FDC Output Port	write only
	bit 4 : NEC 765 reset (active '0')		
	bit 5 : MOTON		
	bit 6 : DS4EN (must be '1' to select Drive 4)		
	bit 7 : SFSEL ('0' : FDC)		
	('1' : SASI)		
20 - 23	CS8-N	CTC I	read & write
24 - 27	CS9-N	CTC II	read & write
28 - 29	CSA	SIO (Communication)	read & write
2A - 2B		SIO (Terminal)	read & write
2C - 2F	CSB	not used	

Detailed Description and Servicing
Mainboard - Memory Manager

1 GENERAL

The memory manager is used to control the bank switching procedures:
- to switch between internal ROM and external RAM arrays and
- to switch over between internal RAM and the IPL ROM.

In all cases it is necessary, within each of the parallel storage areas, to have a common storage area kept free for possible information interchange between the blocks. An exception to this is external RAM access, where the function of the memory manager is handled by the external hardware.

The memory manager uses a 1024-Bit Bipolar Prom (256 x 4) 82 S 129.

2 BLOCK DIAGRAM

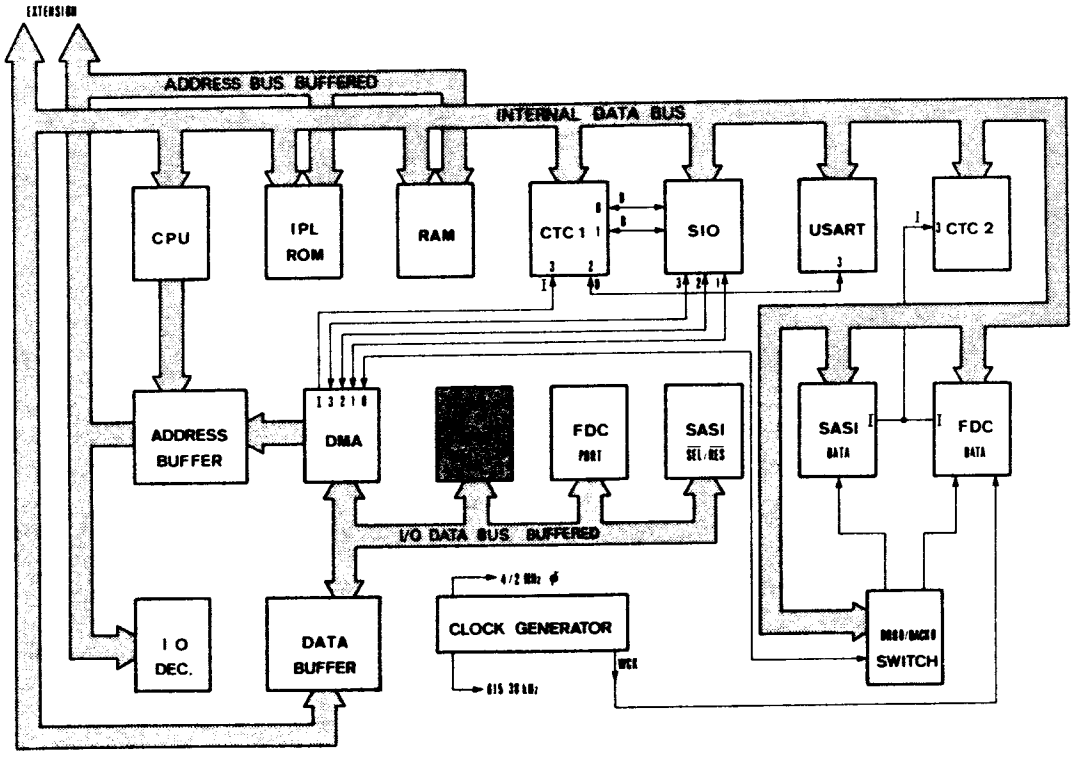

Figure 2.13 P2000C - Memory Manager Block Diagram

3 CIRCUIT DESCRIPTION

The memory manager (item 7462) is controlled by:
- two memory manager signals
  MM1 and MM2, (produced from two D-FF's 74 LS 74 - item 7446) reachable via software with an output command to I/O address 1EH: bit 0 and bit 1
- the signal EXDIS-N
- the four highest address lines.

With these signals 3 memory activities can be selected. Combinations of MM1, MM2 and EXDIS-N not shown below are not allowed:

MM2	MM1	EXDIS-N	address area	activity
0	0	1	0 - 4 k	read from IPL ROM, write to internal RAM
0	0	1	above 4 k	internal RAM access
1	0	1	all	internal RAM access
1	1	0	all	external RAM access

Memory manager decoding is shown in table 2.14, on the following page.

Detailed Description and Servicing
Terminalboard - Character Generator ROM

1 GENERAL

The character generator ROM is a 4K x 8 bit device - 2632, (item 7450) giving 256 characters in a 16 x 8 matrix. Only the first 12 x 8 bits are used to define a character, the contents of the remaining 4 x 8 bits being undefined and not addressed by the CRTC. See Appendix A for the Character Generator listing.

2 BLOCK DIAGRAM

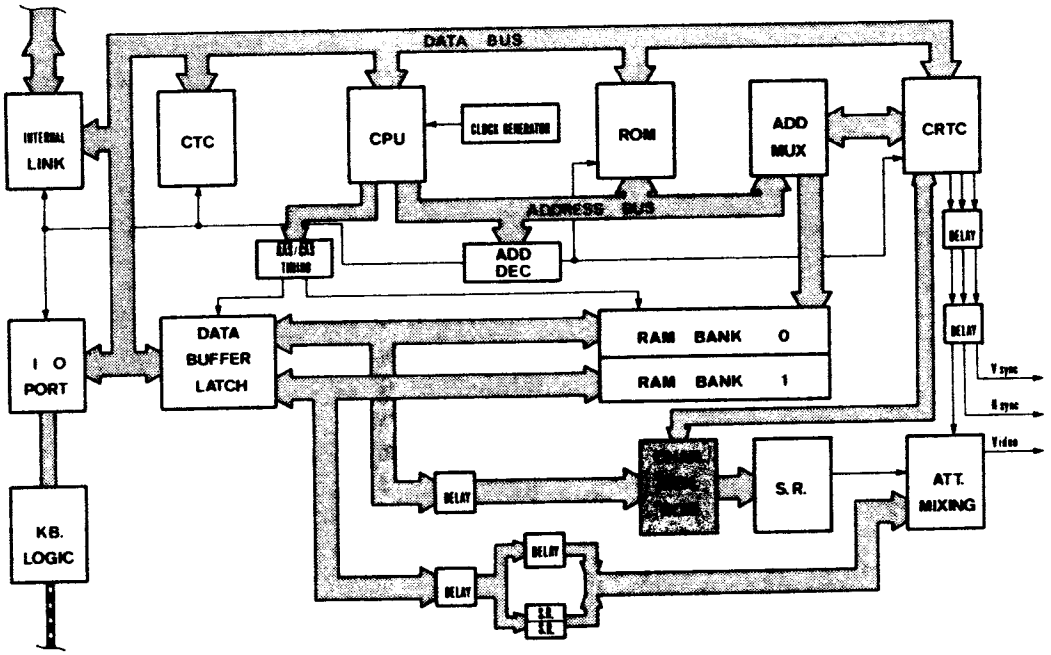

Figure 3.17 P2000C - Character Generator ROM Block Diagram

3 ADDRESSING

A character is read out of the ROM by clocking out, byte by byte, the 12 bytes that are used to represent that character.

Address lines ID0 - ID7 are first latched from Ram Bank0. (A4 - A11 on the character generator = 000x - 0FFx). This identifies the start address in ROM of the required character.

The Row Address lines RA0 - RA3 are then activated in sequence by the CRTC (A0 - A3 on the character generator = 0 - F, but programmed within the CRTC to count to 12; i.e., 0 - B). One byte of ROM is clocked out to the shift register (item 7449) with each increment of the character clock.

Subsequently the information is shifted out of the shift register, bit by bit, with the least significant bit first.

3.1 Character Representation in ROM

As an example of the ROM contents, the following is the information that represents the letter 'B':

FF C1 BD BD C1 BD BD C1 FF FF FF FF

where 0 (● in illustration below) = bright in normal character display and 1 (• in illustration) = dark.

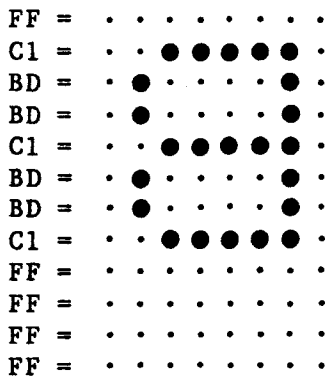

Figure 3.18 Character Representation in ROM

Detailed Description and Servicing
Monitor

1 GENERAL

The P2000C incorporates a Mitsubishi Electronic Corporation Model NT-1002XU, 9" Monochrome (Green) Monitor. The maintenance philosophy for this unit is that it should be 'serviced by replacement' and, consequently, full technical details will not be supplied. However, this section outlines the safety precautions to be taken when handling and using the unit and will give instructions on any adjustments that may needed.

2 SAFETY PRECAUTIONS

HIGH VOLTAGE WARNING

Parts of the CRT PCB are supplied with **HIGH VOLTAGE** (700V), and extreme care must be taken in handling the unit when it is switched 'ON'.

Even after switching 'OFF', the CRT **ANODE** may be at a dangerous voltage level. This high voltage should be discharged to ground after the ANODE CAP has been carefully removed.

HIGH VOLTAGE WARNING

In addition to precautions against fatal electric shock, the following points should be considered when handling or using the Monitor:

- Although an anti-explosive type CRT is used in the Monitor, any damage to the tube is potentially dangerous. Care must be taken in handling the Monitor to ensure that the surface of the CRT is not damaged. Remember that any damage to the tube will affect both SAFETY and PICTURE QUALITY.

- The anode cap is held firmly in place by the cap spring. Ensure that this item is always fitted.

- To preserve 'tube life', it is advisable to use the lowest acceptable brightness level for the display. This will lessen the effect of phosphor burn on the tube.

1-2

Detailed Description and Servicing
Monitor

- Avoid moving the sub-magnets on the deflection yoke, which compensate for linearity and raster distortion. Extreme care should be taken when handling the deflection yoke to avoid damage to the wiring.

3 ADJUSTMENTS

HIGH VOLTAGE WARNING

Adjustments to the Monitor must only be carried out by a qualified Service Technician.

HIGH VOLTAGE WARNING

Connect appropriate power source and TTL signals to the module as follows:

Power Source	DC 12V +/-0.2V
Video	TTL positive 5V P-P
Vertical Sync	TTL negative 5V P-P
Horizontal Sync	TTL positive 5V P-P

The following procedures outline adjustments for individual stages:

3.1 Horizontal Frequency (VR501)

- Disconnect input signal
- Connect a frequency counter (loose coupling) to horizontal output
- Adjust VR501 for output of 15.67 KHz

3.2 Vertical Frequency (VR401)

- Connect input signal
- Adjust VR401 to stabilize picture in vertical plane

P2000 C

SPARE PART CATALOGUE
4x64k RAM-BOARD

1984-04-14

ITEM	QTY	DESCRIPTION	CODE NUMBER	SERVICE NUMBER
7001	1	I.C. 74 LS 11	9332 869 80112	* 5103 109 31060
7002	1	I.C. 74 S 123 N (7002) RAM	5103 108 52370	* 5103 109 31150
7003	1	I.C. 74 LS 174 B	9332 874 80112	4822 209 50008
7004	1	I.C. 74 LS 244	9334 307 60112	5322 209 86017
7005	1	I.C. 74 S 00 N	9332 813 80112	5322 209 84167
7006	1	I.C. 74 S 04 N	9332 617 40112	5322 209 84475
7007	1	I:C. 74 LS 02 A	9332 886 70112	5322 209 85312
7008	1	I.C. 74 S 00 N	9332 813 80112	5322 209 84167
7009	1	I.C. 74 LS 30 A	9332 870 80112	5322 209 84985
7010	1	I.C. 82 S 129 N (7010) RAM	5103 108 52380	* 5103 109 31160
7011	1	I.C. 82 S 126 N (7011) RAM	5103 108 52520	* 5103 109 31170
7012	1	I.C. 74 S 157 N	9332 878 90112	5322 209 85669
7013	1	I.C. 74 S 157 N	9332 878 90112	5322 209 85669
7014	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7015	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7016	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7017	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7018	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7019	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7020	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7021	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7022	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7023	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7024	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7025	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7026	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7027	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7028	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7029	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7030	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7031	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7032	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7033	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7034	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7035	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7036	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7037	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7038	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7039	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7040	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7041	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7042	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7043	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7044	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977
7045	1	I.C. HM 4864-2 (HITJ)	9336 043 10682	5322 209 80977

6-4

SPARE PART CATALOGUE
4x64k RAM-BOARD

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SPARE PART CATALOGUE

1984-04-14

1 GENERAL

This Spare Part Catalogue includes all electrical and the more important mechanical components and parts of the P2000C Portable Computer, covering both P 2010 and P 2012 and Options.

This catalogue is arranged in order of ITEM NUMBER under each heading, where the correct description and the SERVICE CODE of the item will be found.

ITEM ..... part number of component on service print
QTY ..... quantity per item number
DESCRIPTION .. definition and/or component value
CODE NUMBER .. 12NC used in manufacturing
SERVICE CODE . 12NC must be used for ordering

Special components and units, which are indicated in the part lists with an "*", are held on stock in the factory in Vienna. All other components are held on stock in the Concern Service in Eindhoven.

For ordering the following addresses must be used:

for "*" marked components and units:

Österreichische Philips Ind. G.m.b.H
EFW-Microelectronics

Service Department
Breitenseerstr. 116

A-1140 W I E N
A U S T R I A

Telex: EFPHI 131724

for standard components

Philips Export B.V.
Concern Service
Building SBP 5

Eindhoven Holland

1-2

1983-10-14

SPARE PART CATALOGUE
ORDER FORM

1.1 Order Form

If you would like to be kept informed about any updates to this System Reference and Service Manual, please complete the form on the following page and return it to the address indicated.

Please fill in your name and address in CAPITALS.

As each update becomes available you will be informed of its content and of any costs that may be incurred, covering administration and postal charges.

Osterreichische Philips Ind. G.m.b.H
EFW-Microelectronics

Service Department
Breitenseerstr. 116.

A-1140 W I E N
A U S T R I A

SPARE PART CATALOGUE
MAINBOARD

1984-04-14

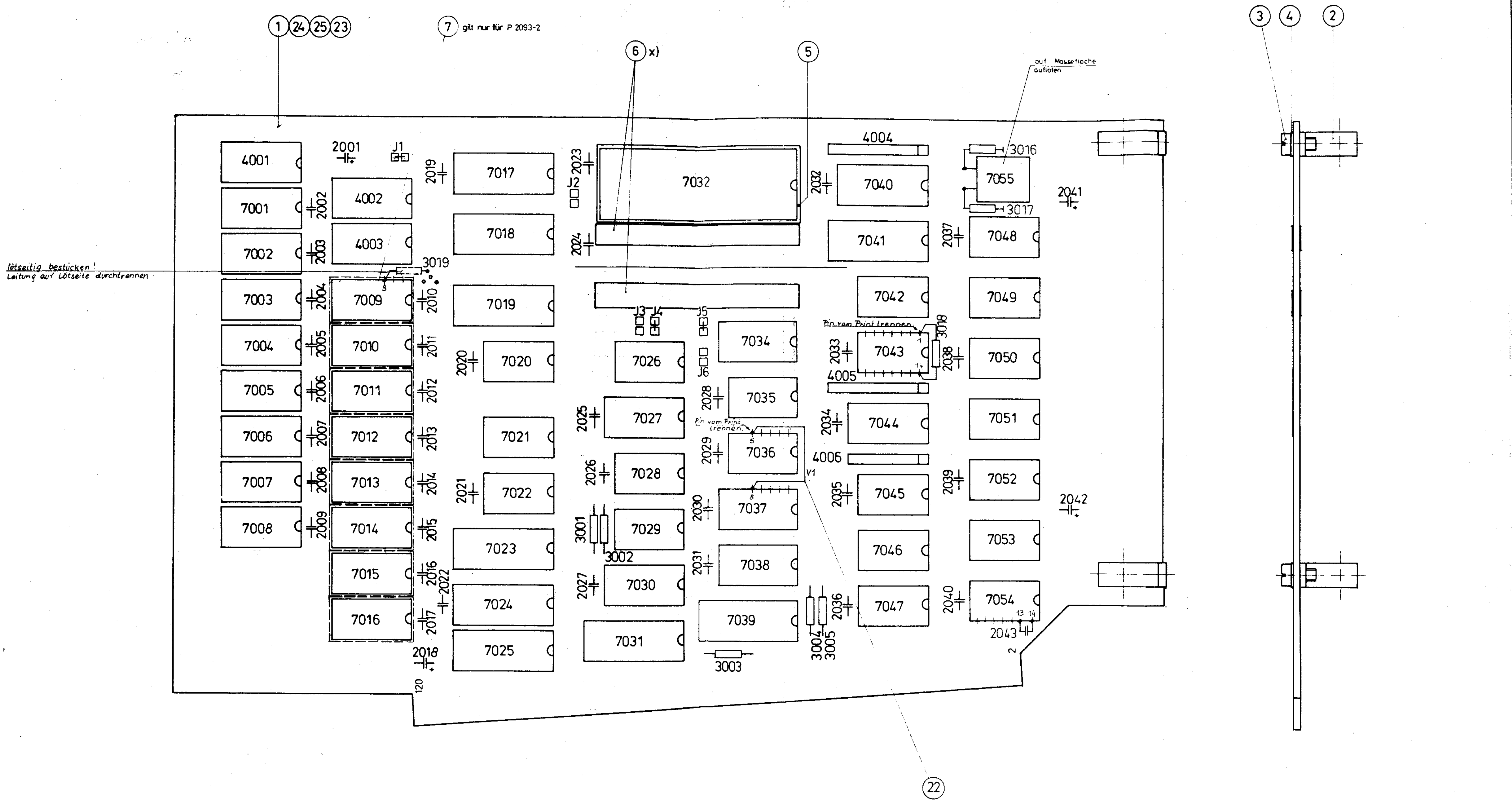
ITEM	QTY	DESCRIPTION	CODE NUMBER	SERVICE NUMBER
61	1	MAINBOARD PCB ASSY	5103 108 02710	* 5103 109 30000
2	1	SOCKET 8-pin 0-826375-8 (AMP)	2422 025 04093	* 5103 109 30400
3	1	SOCKET 6-pin 0-826375-6 (AMP)	2422 038 00122	* 5103 109 30400
4	1	SOCKET 4-pin 0-826375-4 (AMP)	2422 025 04092	* 5103 109 30400
5	1	CABLE ASSY 34-way 3FD1/2	5103 107 81230	* 5103 109 31420
6	1	SOCKET CONNECTOR 7-pin PRINTER	5103 108 73600	* 5103 109 30360
7	1	SOCKET CONNECTOR 11-pin COMMS.	5103 108 73620	* 5103 109 30370
31	2	IC-SOCKET 40-pin	3103 238 73270	5322 255 44217
32	1	IC-SOCKET 24-pin	3103 238 73250	5322 255 44171
33	1	IC-SOCKET 16-pin	5103 108 70200	5322 255 44107
37	1	CONNECTOR 2 x 60-pin	2422 023 98122	* 5103 109 30390
2301	1	CER-CAP CL.1 56 P G 100 V	2222 682 34569	5322 122 34205
2302	1	CER-CAP CL.1 56 P G 100 V	2222 682 34569	5322 122 34205
2303	1	CER-CAP CL.1 56 P G 100 V	2222 682 34569	5322 122 34205
2304	1	CER-CAP CL.1 56 P G 100 V	2222 682 34569	5322 122 34205
2305	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2306	1	CER-CAP CL.1 56 P G 100 V	2222 682 34569	5322 122 34205
2307	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2308	1	EL-CAP 4 M 7 63 V	2222 035 38478	4822 124 40246
2309	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2310	1	CER-CAP CL.1 56 P 100 V	2222 682 34569	5322 122 34205
2311	1	CER-CAP CL.1 56 P 100 V	2222 682 34569	5322 122 34205
2312	1	CER-CAP CL.1 56 P 100 V	2222 682 34569	5322 122 34205
2313	1	EL-CAP 4 M 7 63 V	2222 035 38478	4822 124 40246
2314	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2315	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2320	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2321	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2322	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2323	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2324	1	EL-CAP 4 M 7 63 V	2222 035 38478	4822 124 40246
2325	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2326	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2327	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2328	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600
2329	1	CER-CAP 100 N S 63 V SIEM.	2012 572 10028	* 5103 109 30600

2-2

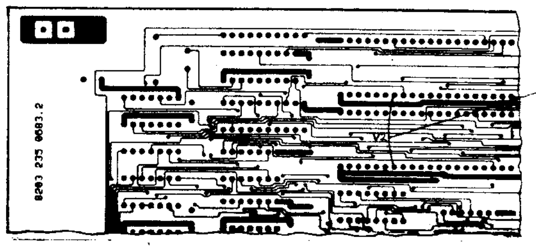
1983-10-14

SPARE PART CATALOGUE
MAINBOARD

ITEM	QTY	DESCRIPTION			CODE	NUMBER	SERVICE NUMBER
2330	1	EL-CAP	4 M 7	63 V		2222 035 38478	4822 124 40246
2331	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2332	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2333	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2334	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2335	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2336	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2337	1	EL-CAP	4 M 7	63 V		2222 035 38478	4822 124 40246
2338	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2339	1	PP-CAP	1 N3 G	250 V		2222 457 71302	* 5103 109 30630
2340	1	PP-CAP	1 N3 G	250 V		2222 457 71320	* 5103 109 30630
2341	1	PP-CAP	47 N G	63 V		2222 455 74703	* 5103 109 30640
2342	1	PP-CAP	47 N G	63 V		2222 455 74703	* 5103 109 30640
2343	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2344	1	CER-CAP	100 P G	100 V		2222 682 28101	* 5103 109 30540
2345	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2346	1	EL-CAP	4 M 7	63 V		2222 035 38478	4822 124 40246
2347	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2348	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2349	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2350	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2351	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2352	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2353	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2354	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2356	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2357	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2358	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2359	1	EL-CAP	4 M 7	63 V		2222 035 38478	4822 124 40246
2360	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2361	1	EL-CAP	4 M 7	63 V		2222 035 38478	4822 124 40246
2362	1	EL-CAP	4 M 7	63 V		2222 035 38478	4822 124 40246
2363	1	EL-CAP	4 M 7	63 V		2222 035 38478	4822 124 40246
2364	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2365	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2366	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2367	1	EL-CAP	4 M 7	63 V		2222 035 38478	4822 124 40246
2368	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2369	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2371	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2372	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2373	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2374	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2375	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2376	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2377	1	CER-CAP	100 N S	63 V	SIEM.	2012 572 10028	* 5103 109 30600
2378	1	CER-CAP	68 P G	100 V		2222 682 28689	* 5103 109 30530
2379	1	CER-CAP	27 P G	100 V		2222 682 04279	* 5103 109 30510



Lötseite



x) Lötaugen mit Pos 6 abkleben (nachträgliches einlöten des 8067 Coprocessors möglich)

Gezeichnete Jumperung für 64K-RAM'S.

Jumperung bei Verwendung von 256K-RAM'S
J1 — offen
J2 — geschlossen
J3 — offen
J4 — geschlossen
J5 — offen
J6 — geschlossen

printed board,assy
Printpl. Zus. (16 Bit-Ext.)

5103 108 0327

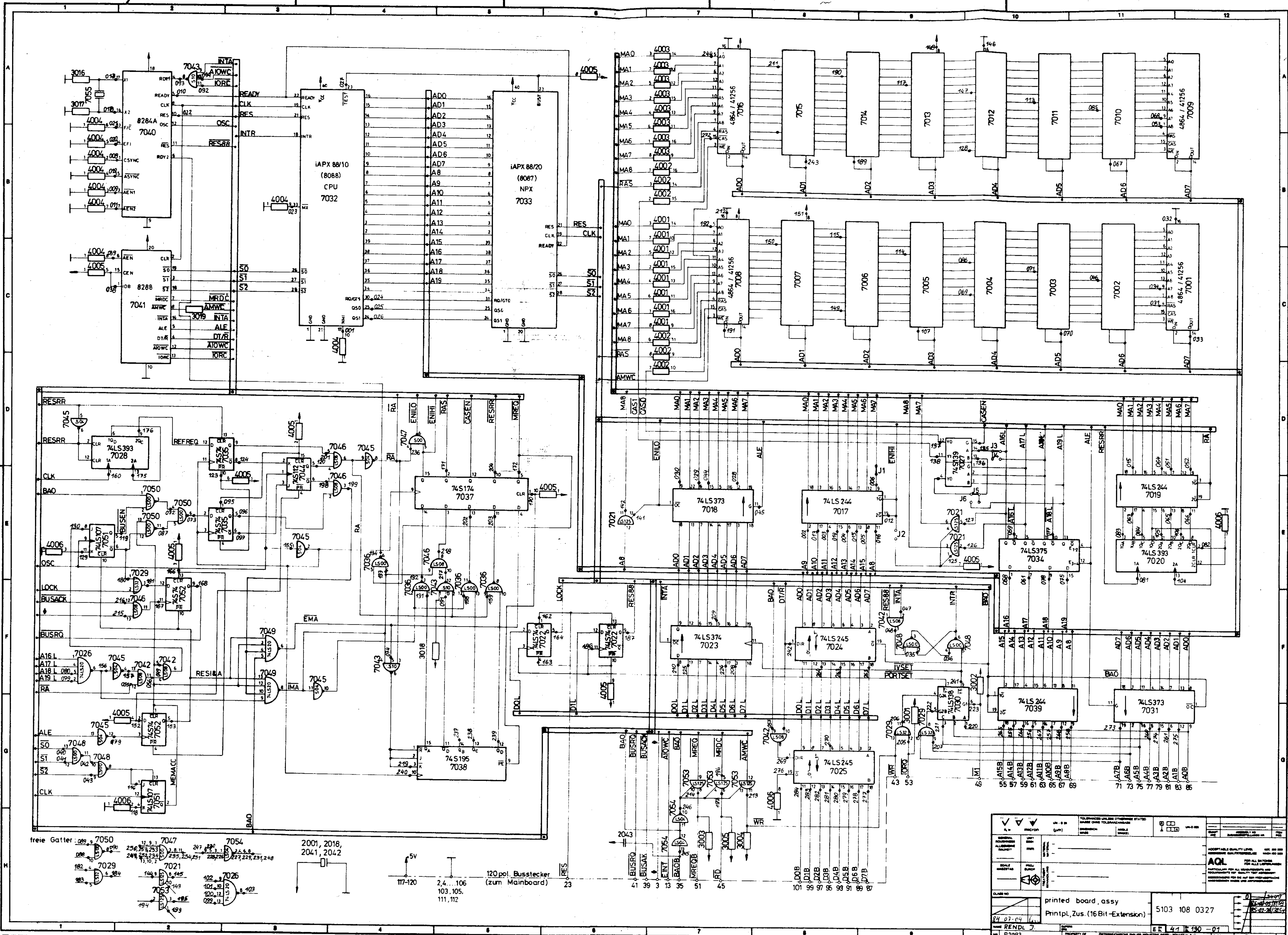
2:1

Schoberl

P 2093

84-07-02

AQL



printed board, assy

Printpl. Zus. (16 Bit-Extension)

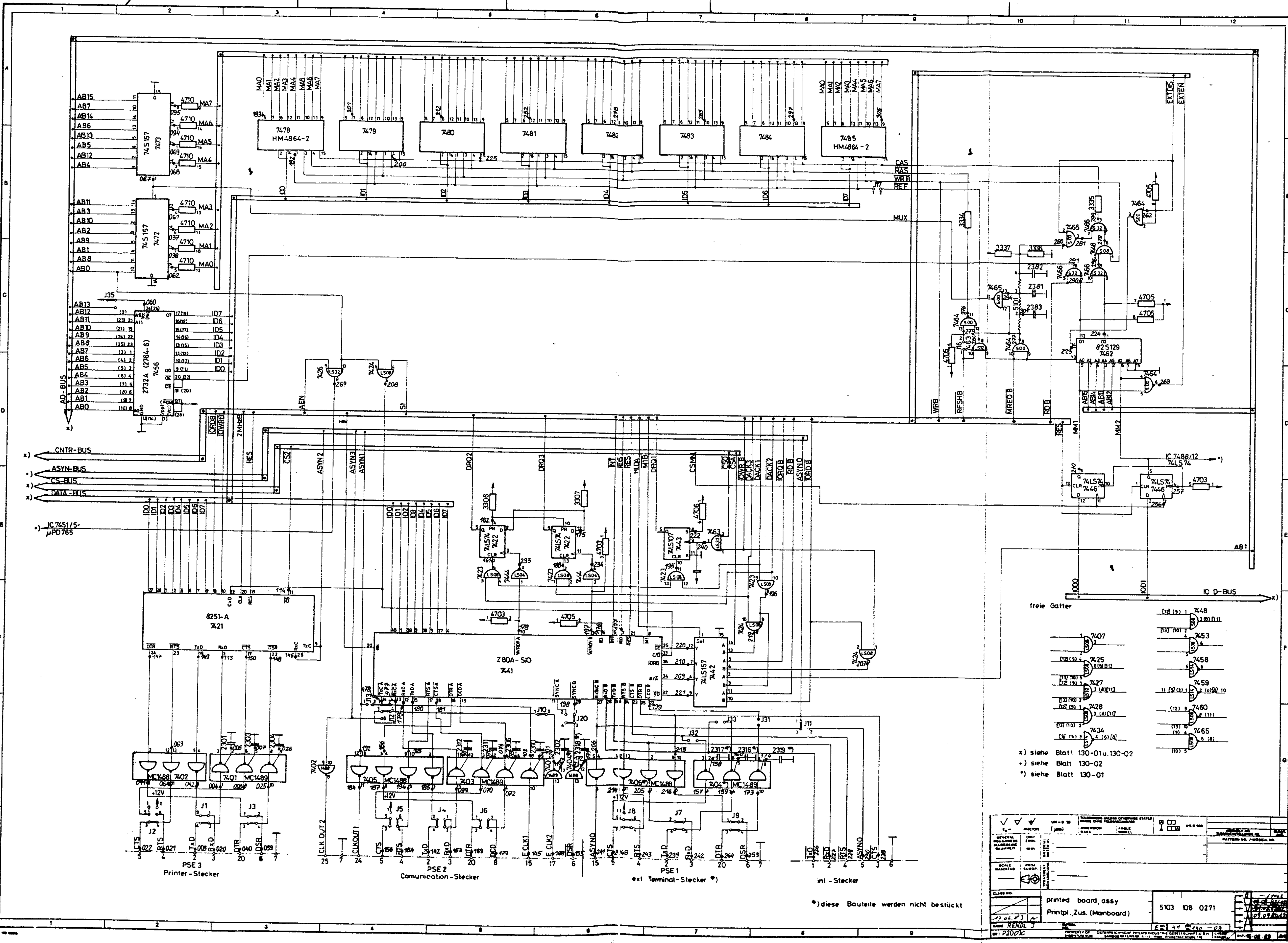
5103 108 0327

AQL

84-07-04

RENDL J.

P2093



8251-A
Z80A-SIO
2732A (2764-6)
HM4864-2
82S129
AD-BUS
CNTR-BUS
ASYN-BUS
CS-BUS
DATA-BUS
IO D-BUS
PSE 3
Printer-Stecker
PSE 2
Comunication-Stecker
PSE 1
ext Terminal-Stecker *)
int.-Stecker
freie Gatter
x) siehe Blatt 130-01u.130-02
+) siehe Blatt 130-02
*) siehe Blatt 130-01
*) diese Bauteile werden nicht bestückt
printed board, assy
Printpl. Zus. (Manboard)
5103 108 0271
RENDL J
P2000C

x) CNTR-BUS

DATA-BUS x)

IOD-BUS

CS-BUS x)

AD-BUS x)

4MHz 1MHz 2MHz

DISC CHG 461
TRK0 440
WRT PR 439
2 SIDE 431
GND
DIRECTION 448
STEP 447
SIDE 433
WRT GT 444
INDEX 455
DS4 456
DS3 461
DS2 452
DS1 454
WD 465
MOTON 450
HDL 460

74LS244 7454
FDC / µPD765 7451
74LS373 7470
74LS153 7469
MC4024/VCO 7417
74LS293 7433
µA741CN 7491
74LS112 7416
74LS221 7415

250kHz
500kHz
TP1 1µsek
TP2 500ns

34pol. Floppy-Disc Stecker

ID0 ID1 ID2 ID3 ID4 ID5 ID6 ID7

74LS175 7468

74LS373 7432
74LS240 7412
74LS367 7431
74LS240 7410
74LS38 7413
74LS38 7411

DRQ FDC
INT FDC
DOUT
DIN
CNT IN

Z80A-CTC (1) 7449
Z80A-CTC (2) 7450

INT RES RDB IORQB MTB CS0 AB1 AB0

ASYN0
ASYN1
615,38 kHz
ASYN2
TC
IEI S
ASYN3
E INT
IEO
DRQ 0

DRQ SAS
SASI INT

50pol. SASI-Stecker

SEL RES DO D1 D2 D3 D4 D5 D6 D7 ACK

I/O C/D MSG REQ

1,3...49
18,20,...34

x) siehe Blatt 130-01 u. 130-03
•) siehe Blatt 130-03
*) diese Bauteile werden nicht bestückt!

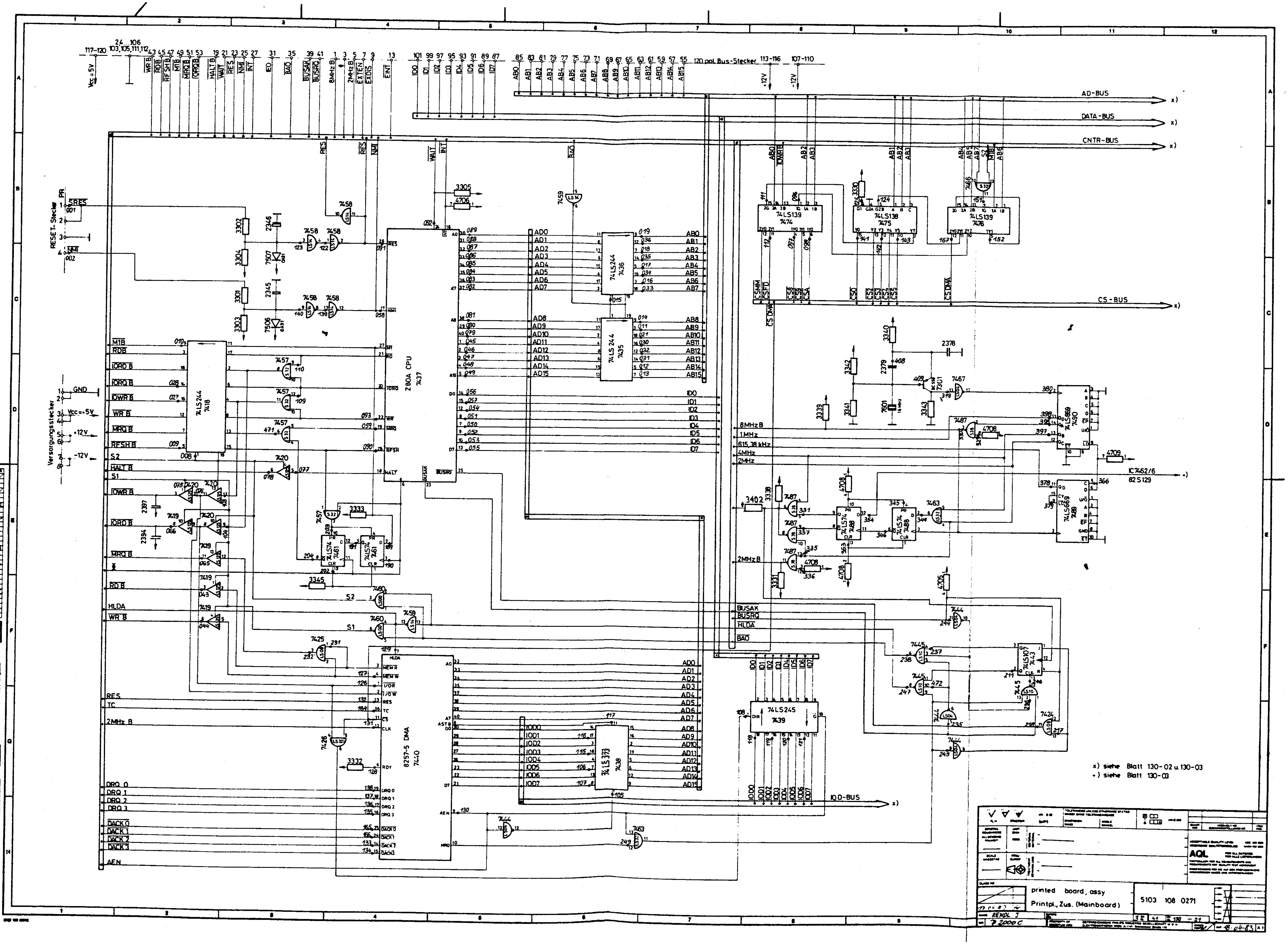
AQL

printed board, assy
Printpl., Zus. (Mainboard)

5103 108 0271

RENDL J
P2000C

130 -02



120 pol. Bus-Stecker
AD-BUS
DATA-BUS
CNTR-BUS
CS-BUS
IOD-BUS
RESET-Stecker
Versorgungsstecker
Z80A CPU 7437
74LS244 7418
74LS244 7436
74LS 244 7435
74LS139 7474
74LS138 7475
74LS139 7476
74LS669 7490
74LS669 7489
74LS74 7481
74LS74 7461
74LS74 7488
74LS107 7443
74LS245 7439
74LS 373 7438
8257-5 DMA 7440
IC7462/6
82S129
x) siehe Blatt 130-02 u. 130-03
+) siehe Blatt 130-03
printed board, assy
Printpl., Zus. (Mainboard)
5103 108 0271
RENDL J
P 2000 C