LNW80 Technical Reference Manual

5000/5200-882

LNW80 MICRO COMPUTER

TECHNICAL REFERENCE MANUAL

BY

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FIRST EDITION - 1982

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INTRODUCTION

This book was written for those people who have the technical knowledge to understand how a computer operates. This requires that the reader has a through understanding of digital logic. Armed with a TTL DATA BOOK and this manual such a person can understand the complex internal operation of the LNW80 COMPUTER.

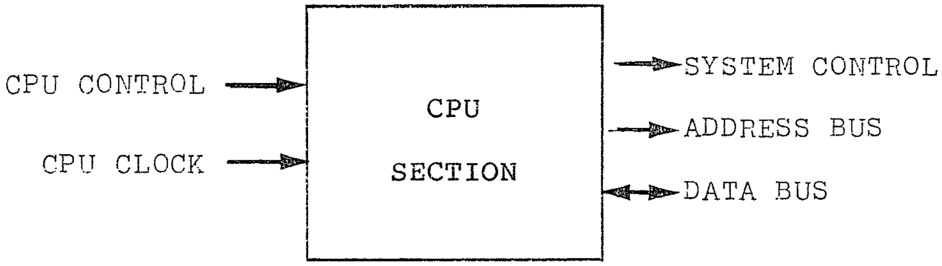
Remember that any work you do to your LNW80 voids all warranties, implied or expressed. Also we will not repair or correct owner modifications. We cannot possibly support owner hardware/circuit ideas on how to customize the LNW80.

In the following sections refer closely to the schematics and the system block diagram which can be found at the end of the manual. Good luck and have fun.

SYSTEM OVERVIEW

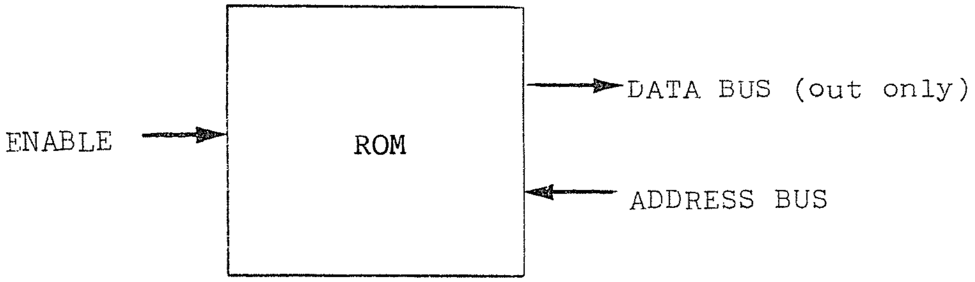
CENTRAL PROCESSING UNIT (CPU)

The heart of the LNW80 is the Z80A CPU. The Z80A has 16 address lines and therefore 65536 addressable memory locations. The Z80A receives instructions from the ROM or RAM and proceeds to execute them. Only the CPU interacts with all other sections within the computer. The CPU section includes not only the Z80A but also the data and address buffers, wait logic, and system control logic.



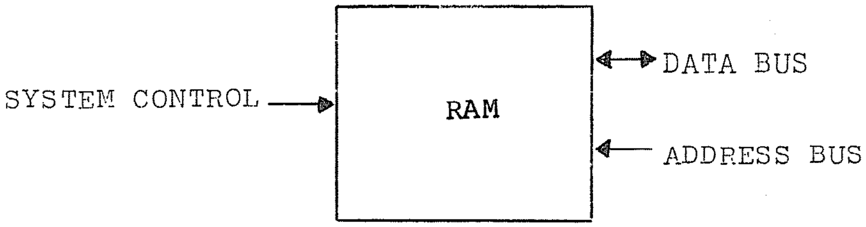
READ ONLY MEMORY (ROM)

The ROM contains non-erasable data that is used to provide the CPU with instructions necessary for the system's operation. Upon power up the CPU outputs to the ROM for its first instruction after which the ROM takes over and instructs the CPU exactly how to perform the necessary funtions to get the system operating.



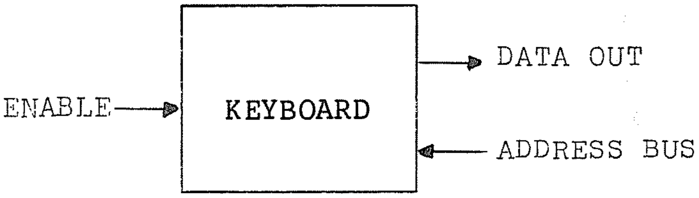
RANDOM ACCESS MEMORY (RAM)

The RAM is where the CPU stores data. This data may consist of program information. The RAM differs from the ROM in that data may be written to as well as read from the RAM by the CPU.



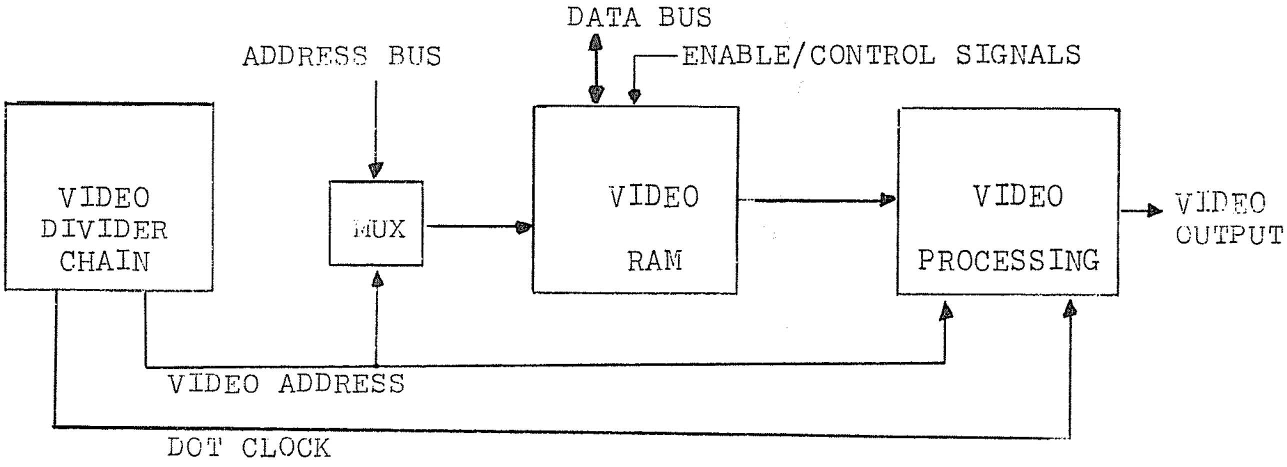
KEYBOARD

The keyboard is used to input instructions from the user to the CPU.



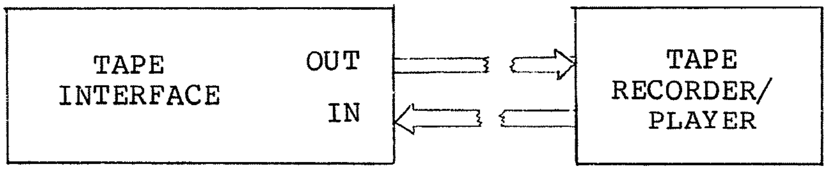
VIDEO RAM AND PROCESSING

The video is used to inform the user what the system is doing. All data that is stored in the video ram is automatically displayed on the CRT by the video processing unit. The data within the video ram is stored in ASCII. Utilizing the Character Generator the ASCII is translated into a dot pattern that represents the desired character.



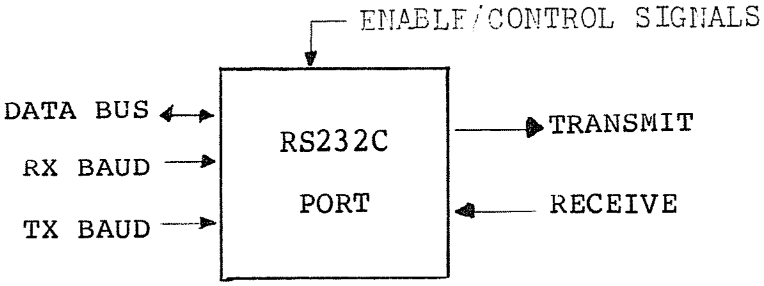
TAPE INTERFACE

The tape interface stores data on tape so that it can be recovered at a later date.



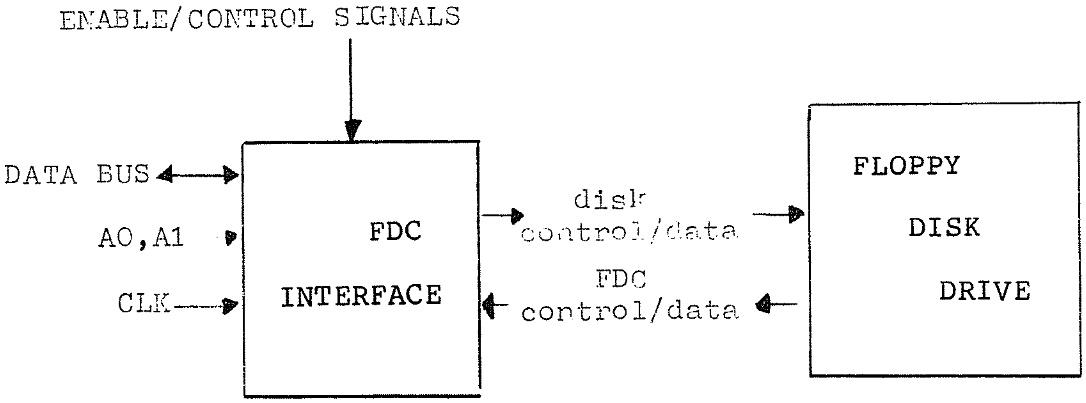
SERIAL INTERFACE

The RS232C serial interface sends and receives data in serial fashion and converts that data to parallel form to be received by the CPU. This section is used to connect to such devices as modems and serial printers.



FLOPPY DISK CONTROLLER (FDC)

The FDC stores large amounts of data and thus increases the storage copacity of the system.



THEORY OF OPERATIONS
LNW80 BOARD

SYSTEM CLOCK

The system clock is a 16MHz oscillator utilizing Y1 and U1 to form a series resonant circuit. U87, a synchronous 4-bit counter, is used to perform the divide by four for the 4MHz and a divide by nine for the 1.77MHz CPU operation. When the HI/LO switch is depressed, the signal FORCELO* (U29-5) is a logic "0" resulting with a preset of 1,0,0 at U87 pins 3,4, and 5 respectively. This preset will program U87 to divide by nine resulting in a 1.77MHz CPU clock at U2-6.

During 4MHz operation, U87 will be preset with 0,1,1 at pins 3,4, and 5 respectively resulting in a divide by four of the system clock. At 4MHz, the signal NHI* (U15-2) will be a logic "0". Thus when ROMRD* (U15-1) is active, a WAIT* will be generated through U31 to the CPU pin 24 allowing for the relatively slow access time of the ROM.

During automatic switching (SW1=1) when the floppy address (37EC) is decoded along with a logic "0" at IMREQ*, the one-shot at U120 will be triggered forcing U120-4 low. This results with a logic "0" at U29-4 resulting in a CPU speed of 1.77MHz as when the HI/LO switch was depressed. The clock speed will remain at this state until the one-shot expires at which time the CPU automatically and synchronously returns to 4MHz.

CPU ADDRESS LINES

The Z80A provides 16 address lines which define the 64K of addressable memory locations. These address lines are buffered from the Z80A through U3 and U5. U3-1 and U5-1 should be a logic "0" thus enabling their outputs at all times. The upper addresses are latched through U5, an LS373, to prevent the address from changing prematurely. During refresh time, the lower 7 bits contain a valid refresh address.

CPU DATA BUS

The CPU utilizes an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices. The data is buffered through U4 and U17. DBIN (U1-10) is used for directional control. When DBIN is a logic "1" the CPU is receiving data. When DBIN is low the CPU is sending data.

WAIT*, INT*, and TEST*

The WAIT* input to the Z80A CPU will cause the Z80A to extend its cycle, resulting in slowing down the CPU. The LNW80 utilizes one WAIT function when a ROM read is in process and one or two waits when accessing the video memory. These waits are required in the hi-speed mode of 4MHz to ensure data validity when accessing the slower memory devices. There are no wait states when accessing the program memory (RAM) on the LNW80 (requiring 200ns or faster RAM's).

The wait term is generated by U31. U31-3, the clock, is delayed by U16. This clock delay results in proper data setup time to U31. U61-3 is WAITHLD. This will increase the wait from the usual one wait state for the Level II ROM's, to multiple wait states when reading from the video memory. Pin 33 of J1 is the bus WAIT signal. This input may be utilized by other external devices that may wish to pose a wait condition on the Z80A procesor.

The INT* signal is a maskable interrupt to the Z80A pin 16. The Level II Basic ROM utilizes interrupt mode 1. When the CPU is interrupted, a restart to location 0038H is executed.

Pin 23 of J1 is TEST* which is a busrequest signal to the Z80A CPU. The CPU responds by tri-stating its data, address and output control signals. Since the Z80A CPU is fully buffered, all the buffers (U3, U4, U5, U17, and U18) will also be tri-stated. Once these buffers are tri-stated, any device on the expansion bus may control the function of the LNW80 board. One important consideration is that the dynamic program RAM's are refreshed by the Z80A processor. Therefore, any controlling device on the expansion bus must consider memory refresh.

CPU CONTROL SIGNALS

The ZRD* signal is a tri-state output, active low. ZRD* indicates that the CPU is ready to receive data from memory or an I/O device. It is input to U36 pins 4 and 12. When U36-12 goes low it enables DBIN. When ZRD* and ZMREQ* go low, they enable IRD* (U36-6). RDOUT* will also be enabled if RDWRDIS (U51-8) is true. Note that RDWRDIS is used to disable the lower 16K when the HI RESOLUTION GRAPHICS RAM are enabled.

ZWR* indicates that the CPU holds valid data to be stored in memory or an I/O device. When ZWR* and ZMREQ* both go low, IWR* (U36-3) is enabled. WROUT* (U36-11) will also be enabled if RDWRDIS is true.

ZMREQ* indicates that the address bus holds a valid address for a read or write operation. Note that it is also used for memory refreshing.

ZIORQ* indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. It is used as the enable at U35-15. When combined with a WR*, IOUT* will be enabled (U35-9). When ZIORQ* is combined with a RD*, IIN* will be enabled (U35-11). ZIORQ* is also combined with ZM1* when an interupt is being acknowledged.

RFSH* indicates that the lower 7 bits of the address contains a refresh address for dynamic memories and the current MREQ* signal is used to do a refresh read to all dynamic memories. Note that it is used to clear U46-5 during refresh time. Resulting in the selection of the lower seven address lines and a logic "1" for the CAS* signal.

ADDRESS DECODING CIRCUIT

The address decoding circuit consists of U6 and U35. The decoding circuit uses the higher order address bits to enable the locations within the memory map which the CPU wishes to access. U6 is a 3 to 8 line decoder. It uses A15 and IMREQ* as enables and A12, A13, and A14 as inputs. Refer below for a listing of the memory mapped sections of the LNW80 along with their decoded addresses.

LNW80 MEMORY MAP

ADDRESS		
DECIMAL	HEX	DEVICE
0	0	
12288	3000	BASIC ROM
12289	3001	
14301	37DD	UNUSED
14302	37DE	COMMUNICATION STATUS ADDRESS
14303	37DF	COMMUNICATION DATA ADDRESS
14304	37E0	INTERUPT BATCH ADDRESS
14305	37E1	DISK DRIVE SELECT LATCH
14308	37E4	CASSETTE SELECT LATCH
14312	37E8	PARALLEL PRINTER ADDRESS
14316	37EC	FLOPPY DISK CONTROLLER ADDRESS
14336	3800	
14591	38FF	KEYBOARD
15360	3C00	
16383	3FFF	LO-RES VIDEO RAM
16384	4000	
32767	7FFF	16K PROGRAM RAM
32768	8000	
65535	FFFF	32K RAM (EXPANSION BOARD)

ROM

The LNW80 ROM consists of six EPROMs. ROMA is memory mapped from 0 to 2K, ROMA1 from 2K to 4K, ROMB from 4k to 6K, ROMB1 from 6K to 8K, ROMC from 8K to 10K, and ROMC1 from 10K to 12K.

Each ROM has three enables. Pin 21 is an active high enable and pins 18 and 20 are active low enables. Pin 21 is pulled high on all ROMs with 33 ohm pull-up resisters.

ROMA and ROMA1, pins 20 are enabled by "0-4K*" (U6-15). "0-4K*" goes low when U6 pins 1,2,3,4, and 5 are at logic levels "0","0","0","0, and "0" respectively. RA11 is inverted at U50-8 and enables either ROMA and ROMA1 at pins 18.

ROMB and ROMB1, pins 20 are enabled by "4-8K*" (U6-14). "4-8K*" goes low when U6 pins 1,2,3,4, and 5 are at logic levels "1","0","0","0", and "0" respectively. RA11 enables either ROMB or ROMB1 at pins 18.

ROMC and ROMC1, pins 20 are enabled by "8-12K*" (U6-13). "8-12K*" goes low when U6 pins 1,2,3,4, and 5 are at logic levels "0 ,"1","0","0", and "0" respectively. RA11 enables ROMC or ROMC1 at pins 18.

Addresses A0 through A11 are buffered through U62 and U65, LS244's. The data bus out is buffered through U63 and is enabled by "RAM/ROM*" (U52-6). "RAM/ROM*" goes low when RD* occurs with either "0-4K*", "4-8K*", or "8-12K*".

PROGRAM RAM

The LNW80 utilizes the 16Kx1 dynamic memories (4116 type) with maximum access time of 200ns. The 14 address lines are multiplexed into the 7 address inputs. The addressing sequence is RAS* (Row Address Select), MUX (Multiplex), and then CAS* (Column Address Select). The timing diagram for a write operation of the memory control signals is displayed in the following diagram. The RAM data bus out is enabled by "RAM/ROM*" at U63 when RAM* is decoded at U19-6 during a read operation.

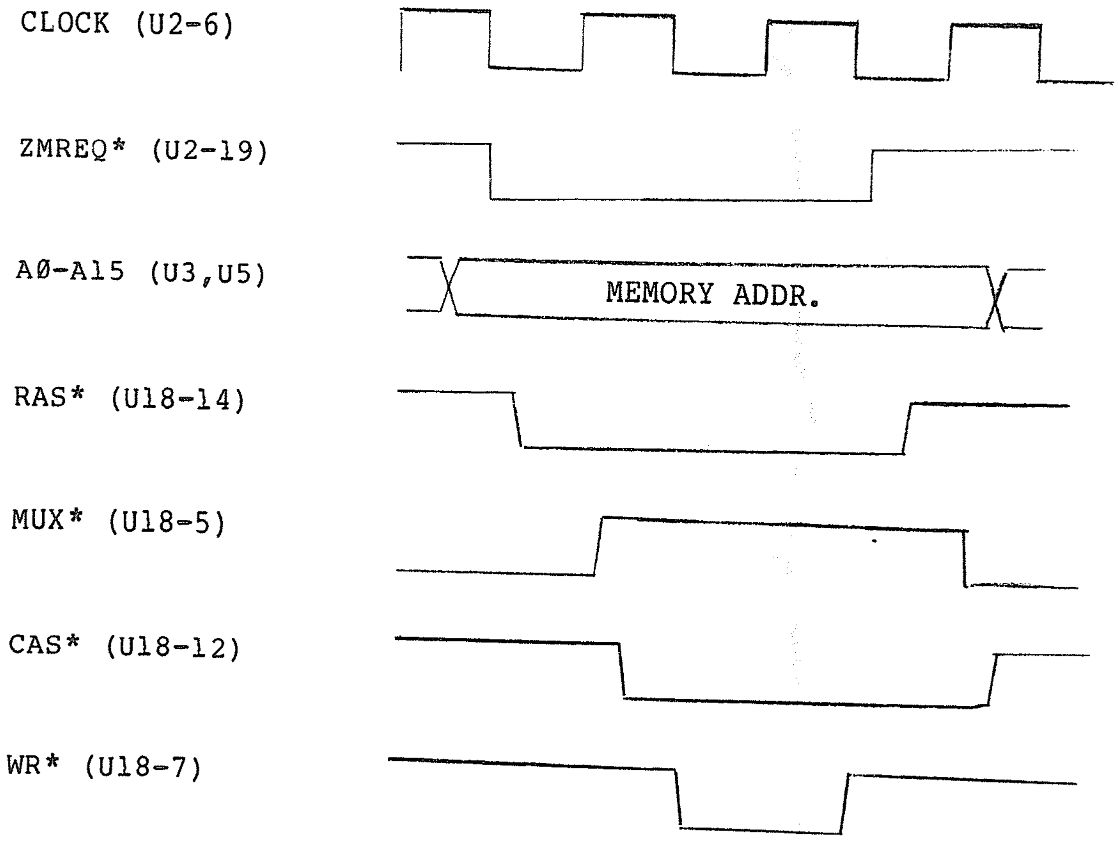


FIGURE 1. MEMORY WRITE TIMING DIAGRAM

RAM REFRESH

Dynamic RAM require periodic refreshing to retain data information. If the system does not receive periodic refreshing the dynamic RAMs will begin to "forget" data.

The LNW80 utilizes the Z80A CPU to generate the refresh to the RAM's. The memory refresh address is output on the lower 7 address bits during refresh time. An instruction fetch will increment the refresh register.

The LNW80 uses a "RAS*" only refresh, where RAS* will be low and CAS* will be high during refresh. At refresh time MUX will be low selecting A0-A7 as the RAM address.

KEYBOARD

The LNW80 keyboard is designed specifically for the LNW80 computer providing a 62 keypad, an 11 key numeric keypad, and all the special functions that are available to you through the LNW80 computer.

The keyboard is a scanning type keyboard based on an eight by eight matrix. Normally, all lines are floating until the KYBD* signal goes low which turns Q1 on and pulls all signals high indicating a keyboard scan operation. KYBD* is decoded through U35 when a keyboard address is placed on the address bus and RD* is active.

Note that lower case is enabled only with software driver routines such as those available in DOS+, NEWDOS80, and ELECTRIC PENCIL.

SPECIAL KEYBOARD FUNCTIONS

RESET (RST):	Both RST keys must be depressed to reset the computer.
HIGH LOW:	Forced LOW Speed switch. When depressed the system will operate in LOW speed. Otherwise the system will operate in forced high speed.
CONTROL:	This is a special software controlled key. It is used in software such as the ELECTRIC PENCIL word processing program.
CAPS LOCK:	Disables lower case characters.
F1, F2:	User definable keys. Needs special software driver.

VIDEO DIVIDER CHAIN

The video divider chain provides the necessary logic for video processing, including video ram addressing, and vertical and horizontal timing pulses. The basis of the video divider chain is the 10.738MHz clock at U119-6. This signal appears as a sine wave and is exactly 3 times the color frequency of 3.579MHz. U121 executes a divide by 2. This results in 2 input frequencies to the divider chain at U122.

In the standard 64 character mode, 32CHAR*(U122-1) will be high so that the B inputs to U122 will be selected therefore the clock input at U138-9, CLKT, will be 10.738MHz. U138 provides the basic timing signals for video processing. Figure 2 represents a timing diagram for the outputs of U138 and U155 in the 64 character mode.

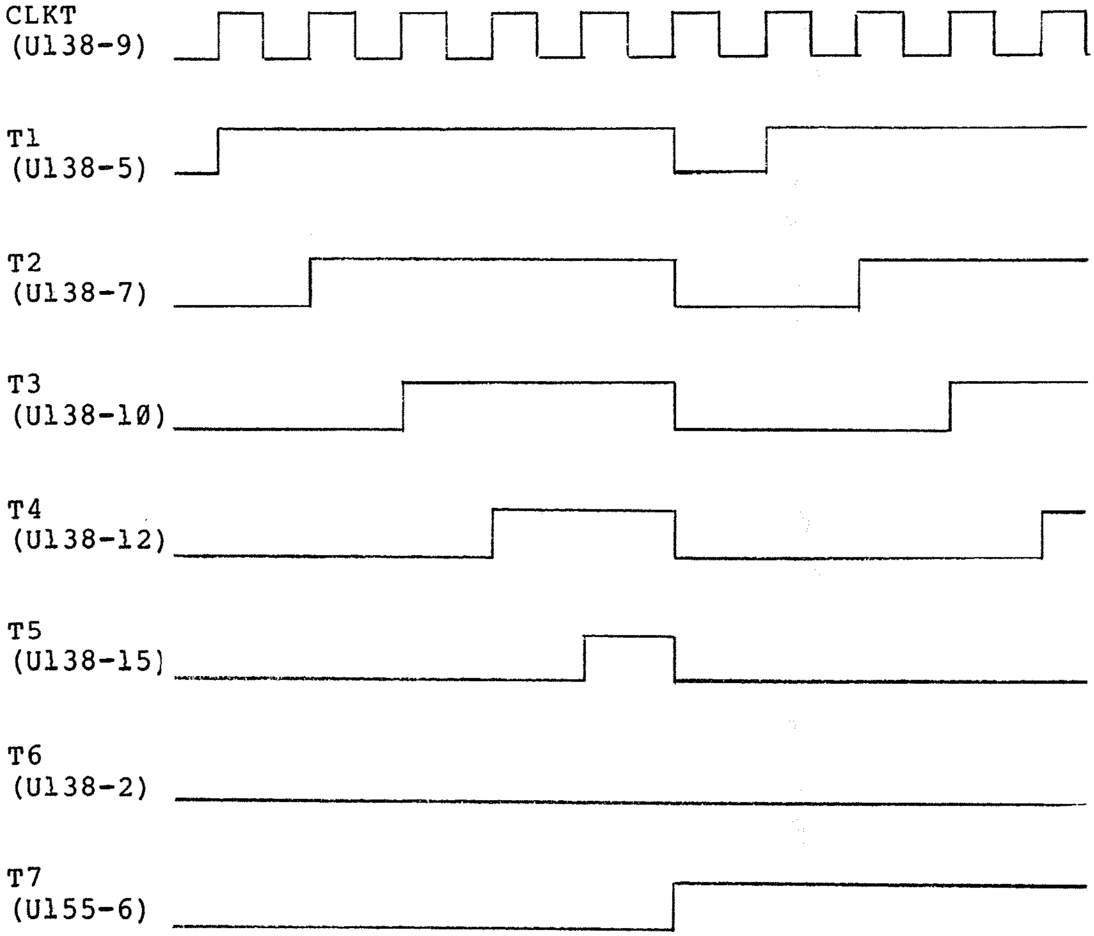


FIGURE 2

During 64 character mode, T7* is selected as the control clock(CNTRCLK) for the video timing chain(U122-12). The circuitry of U138 and U155 effectively produces a divide by 12 such that T7* is 10.738MHz/12 or 894.8KHz. Note also that T7 is selected as CHAR1(U122-9). CNTRCLK is the clock input to U160 and U161(S161's). Figure 3 illustrates the outputs of U160 and U161.

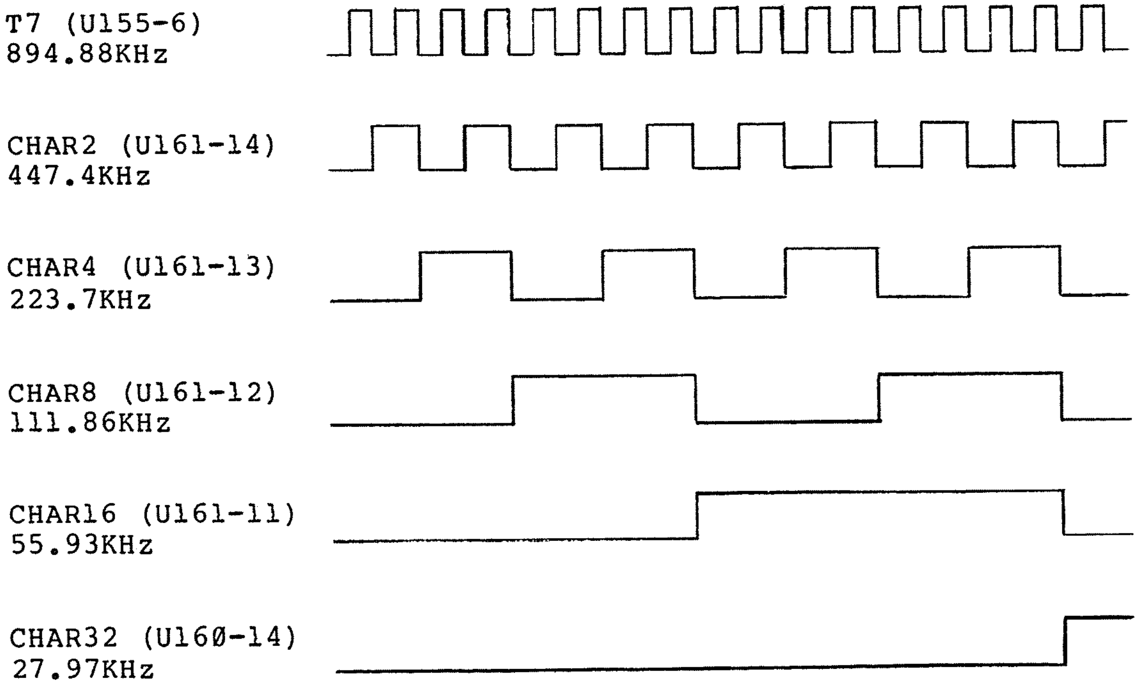


FIGURE3

Note that HORTP(U160-13) is not half the frequency of CHAR32(U160-14). T6INH*(U155-9) prevents the completion of its period by clearing U160 and U161 at the end of each horizontal line. The frequency of HORTP is 15.750KHz resulting in a period of 63.49us for each line.

Each line consists of 112 characters. Allowing one CHAR1 period for each 2 characters the time span for 112 characters is 62.58us. Note that we are left with 0.91us at the end of each horizontal line. T6INH* is used to delay the timing chain to "waste" this additional time before starting the next cycle. U167 is used to add the additional delay in T6INH*. It is ANDed with T6 at U154 thus delaying T6*(U154-8) from clearing U138.

HSTP(U168-11) is the ORing of CHAR16 and CHAR32, ANDed with HORTP. This is the horizontal sinc timing pulse. Its frequency is 15.750KHz. Refer to figure 4 for the timing diagram.

U159-12 is also displayed in figure 4. It goes low after the 112th character and also has a frequency of 15.750KHz. It serves 2 important purposes. 1st, it is the data input to U124 which when clocked clears U155 and thus enabling T6INH*. Also it is the input to U156-13 and thus increments the row count.

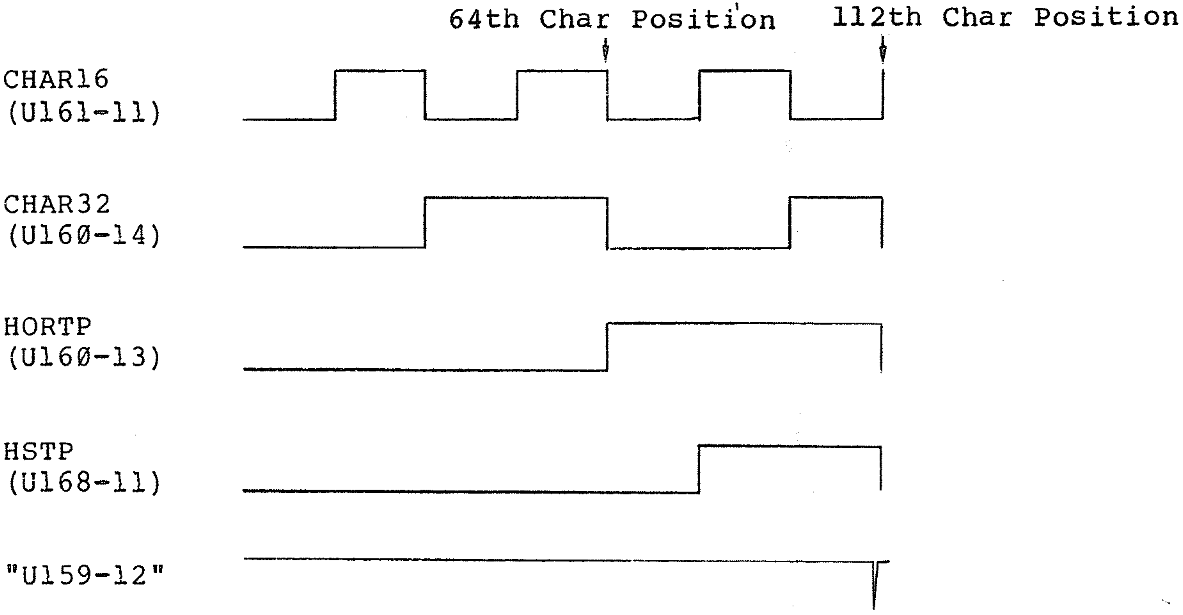


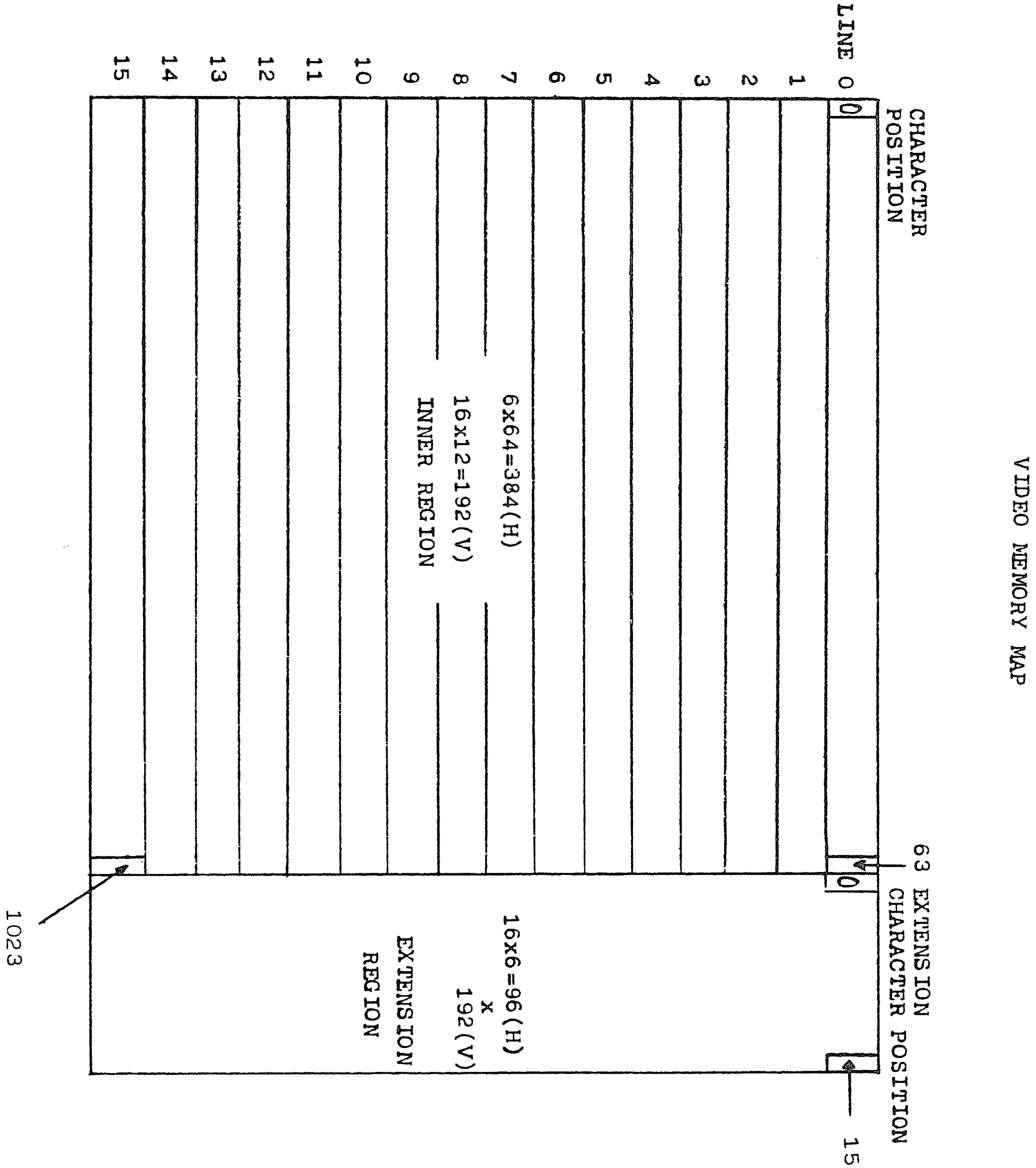
FIGURE 4.

Each character position consists of a 6x12 matrix. Six dots and 12 horizontal rows. U156 increments by one after each horizontal scan. When the row count is equal to 12, U168-3 will go high thus clearing U156 setting the row count back to zero and also clocking U153-11 and incrementing the line count by one.

Note that the screen consists of 22 lines (only 16 are displayed) and each line has 12 rows. LINE1, the least signicicant bit of the line counter, changes state every 2nd line and thus has the same period as 24 rows or 24x63.49us or 1.524ms. Its frequency is therefore 656.3Hz. Using similar logic, you can find that LINE2=328.1Hz, LINE4=164.1Hz, and LINE8=82.0Hz.

A similar situation exists for VERTP(U156-6) as did for HORTP in that U156 is cleared before VERTP, which represents line16, completes its full period. When the total line count is 22 the inputs to U169 pins 3,4 and 5 are high, thus its output pin6 clears the line count back to zero. In 22 lines LINE1 changes state 11 times so that the period of VERTP is 11 times that of LINE1 or 16.76ms. The resultant VERTP frequency is 59.66Hz.

In the 32 character mode, U122-1 goes low selecting the 5.369MHz clock for CLKT. The result is that all of the outputs of U138 are exactly one half the frequency that they



VIDEO MEMORY MAP

FIGURE 5

were in 64 character mode. T5* is selected as CNTRCLK and CHAR1 is ground. Note that because T7* is 1/2 the frequency of T5*, by selecting T5* in 32 character mode CNTRCLK does not change and therefore nor does the resulting logic of U160 and U161.

The signals that did change, T2 through T5 and CHAR1, are very important to the video processor section. CHAR1 determines whether the video ram have 1024 or512 usable addresses. T2 through T5 determine how many characters may be processed to the character generator per line.

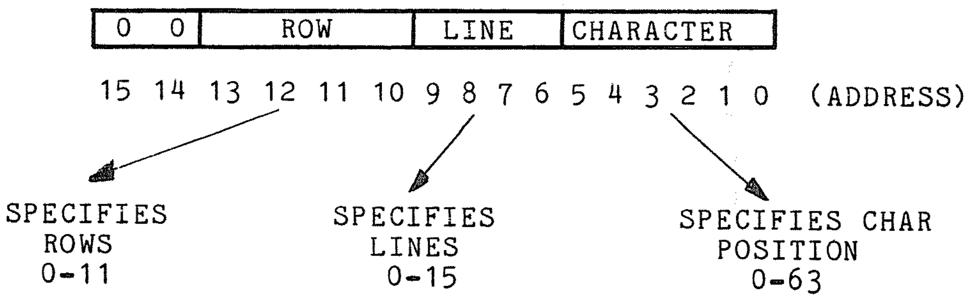
VIDEO RAM ADDRESSING

The video rams are addressed by 2 sources. The video divider chain addresses the video ram so that data contained in memory can be processed and displayed on the screen. The CPU must address the video ram so that data can be read from or writen to specific locations. Multiplexers are used to select either the video chain or CPU address.

For the following discussion refer to figure 5, the VIDEO MEMORY MAP. Note that the low resolution video is defined only within the inner region and that A10-A13, which specify the row count are not used by the low resolution video ram. By definition A10-A13 are at a logic "1" voltage state during CPU access of the low resolution video ram.

The inner region represents the standard TRS80* video display. This region is memory mapped at locations 15360 through 16383. It has 63 characters and 16 lines, each line with 12 rows. The video addressing of this region is represented by the following:

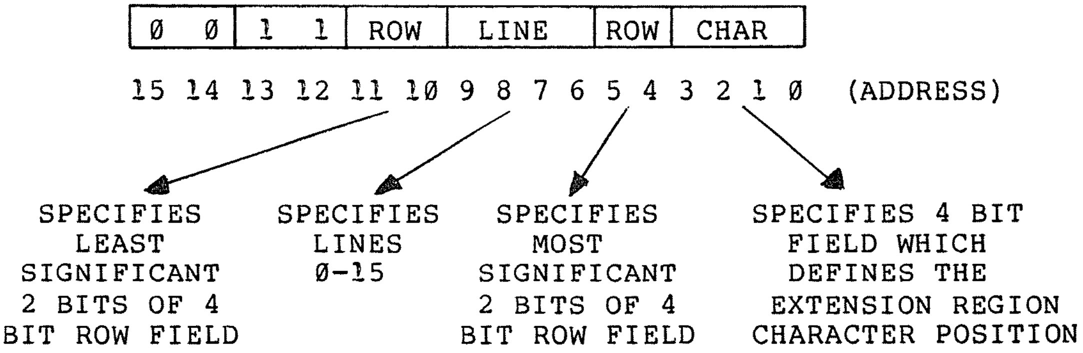
384 X 192 INNER REGION



A0-A5 specify character position 0-63, A6-A9 specify line position 0-15, and A10-A13 specify row position 0-11. A14 and A15 will be low.

The extension region, refer to figure 5, adds an additional 16 character positions for a total of 80. The following illustrates the addressing of this region:

96 X 192 EXTENSION REGION



A0-A3 specify character 0-15 of the extension region, A4-A5 specify the most significant 2 bits of the 4 bit row field, A6-A9 specify lines 0-15, and A10-A11 specify the least significant 2 bits of the 4 bit row field. A12 and A13 are high. Note that the extension region is uniquely defined by a logic"1" at A12 and A13 because in the inner region this would specify a row count greater than 11.

When the CPU is not accessing the video ram, the video addresses are controlled by the video divider chain. The selects at U139, U140, U144, and U145 will be high selecting the B inputs.

U142 specifies whether we are in the inner or extension region. Prior to the 64th character HORTP(U142-1) will be low, selecting the A inputs. At the 64th character HORTP will go high selecting the B inputs thus selecting the extension region addresses.

CPUACC*(U121-8) is the select for U139, U140, U144, and U145. When the CPU is accessing the video ram, CPUACC* will go low selecting the A inputs. The procedure by which CPUACC* goes low and the CPU addresses are latched into the address multiplexers will be covered in a following section.

LOW RESOLUTION VIDEO RAM

The Low-Resolution Video Ram consists of two 2114 type 1Kx4 static ram chips. For either read or write operations the select (pin 8) must be low. They have an active low write enable, 10 address lines, and 4 data lines each. U114 uses the least 4 significant data bits and U115 the 4 most significant data bits.

When the CPU wishes to access the video ram it must execute a read or write operation while placing a video address on the address bus. For the Low-Resolution (LORES) Video Ram this address must be from (3C00-3FFF)Hex. The following illustrates the sequence of events during a LORES video write.

During the execution of a LORES video write, the CPU will place a video address on the address bus. This address will be decoded at U6 and U35 resulting with a logic "0" at VID*(U35-7). WR* will be low. These are the inputs to U152 pins 4 and 5 respectively. When both are low the output, VIDWRT*(U152-6), will go low. This is the input to U154, a four input nand gate. Note that the four inputs represent LORES video write, LORES video read, HIRES video write, and HIRES video read. When any of the four inputs goes low the output, pin6 will go high clocking U153. DATALAT(U153-5) will be high and U153-6 will be low. CLKADRSDTA (U137-6) will go high latching U98, U141, and U143. Thus the CPU addresses, the CPU data, and VIDWRT* are latched. VIDWRT* is latched at U141-4. It becomes LVIDWRT*. LVIDWRT* and T2* are input at U151 pins 12 and 13 respectively. T2* prevents the LORES video ram to be written to before the video addresses are stabilized. At the beginning of the next video timing cycle T1 will clock DATALAT into U121 resulting in a logic "0" at CPUACC*(U121-8). CPUACC* is the select of the video address multiplexers and when it is low the CPU addresses are selected. At T2*, LVIDWRT* will be output to WRT2114* (U139-12). WRT2114* enables the data output of U98 through U81 and is the write enable to the LORES rams. The write operation is completed when T6* clears U153, and the resulting low signal at DATALAT clears U121. CPUACC* goes high and the video address is returned to the video divider chain.

A LORES video read is very similar to the write. VID* will be decoded from the video address. RD* will be low. These are the inputs to U152 pins 1 and 2 respectively. This will place a low input to U154 as before and the same signals will result except VIDWRT* will be high and VIDRD* will be low. At the end of the operation DATALAT will go low latching in data at U99 and U125. VIDRD* enables the output of U99 from which the CPU will read the data.

HI RESOLUTION GRAPHICS RAM

The Hi Resolution (HIRES) Graphics Ram are located at the lower 16K of the LNW80 address space. Note that this is also where the Roms, keyboard, LORES video ram, and miscellaneous I/O are mapped. I/O port 254 bit-D3 selects which devices are enabled. With D3=1, the graphics memory is enabled. Note that since the Roms are also disabled by D3=1, using the OUT command in basic to turn on this bit will be fatal to the computer, since the computer will execute out of graphics Ram instead of Rom.

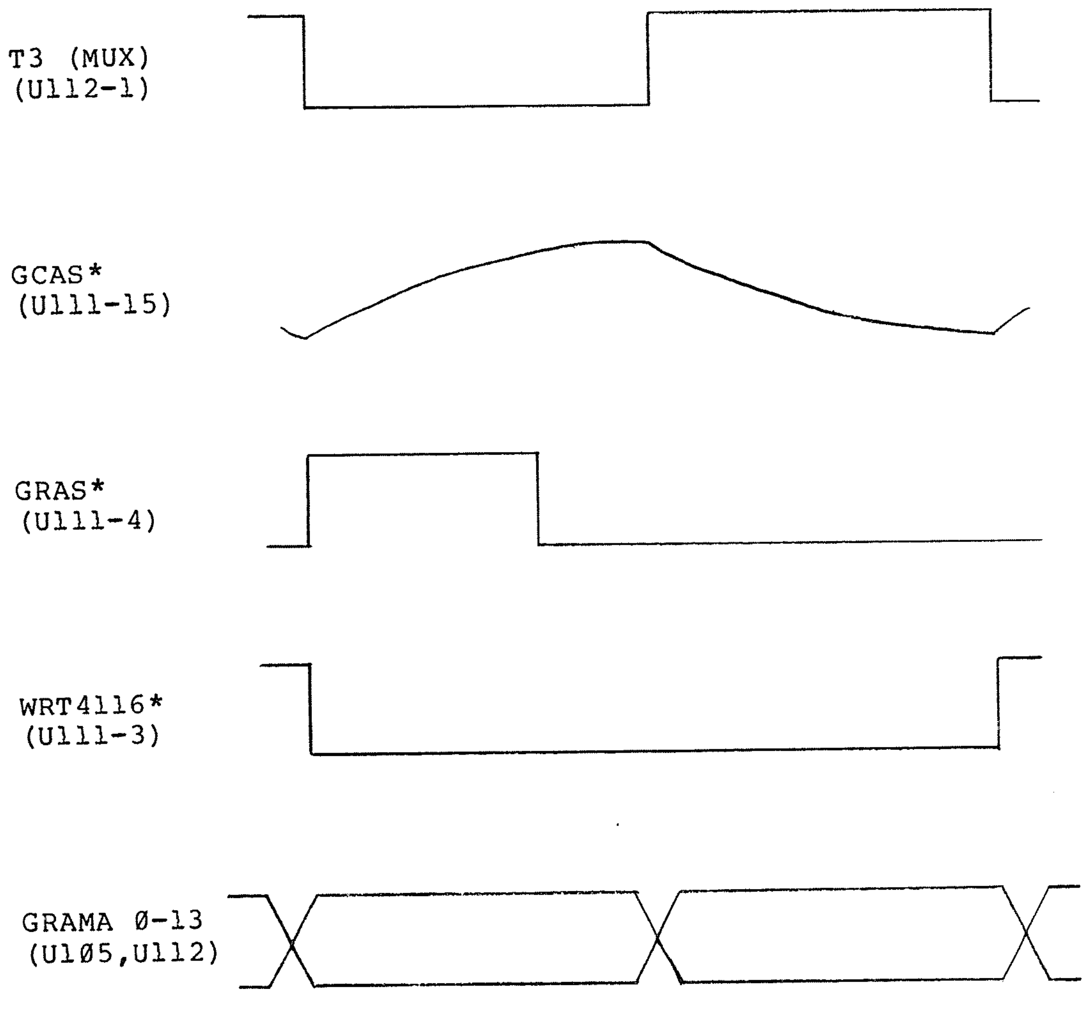


FIGURE 6. HIRES GRAPHICS RAM WRITE TIMING DIAGRAM

The HIRES Ram utilizes six, 16Kx1 dynamic memories. The addressing sequence of events is GRAS*(row address select), T3(multiplex), then GCAS*(column address select) to multiplex the 14 bits of address into 7-bit parts. The sequence of events during a write operation are as follows.

I/O Port 254 is decoded by U33 and U54. FEOUT* (U54-12) is used to clock U67. When U67 is clocked and D3=1, GRRDEN* (U67-6) becomes logic "0". This inputs to U66-12. When the CPU places an address of the lower 16K on the address bus, A14 and A15 will be low at U66 pins 10 and 9 respectively. This is used to decode the lower 16K. The output of U66-8 goes low and inputs to U66-13. This enables GLWR16K* at U66-11. GLWR16K* is inverted at U51 and becomes RDWRDIS (read write disable). RDWRDIS disables RDOUT*(U36-8) and WROUT*(U36-11) preventing a conflict on the data bus. GLWR16K* is input to U152 pins 9 and 12. When accompanied with either IRD* or IWR* a read or write operation will occur at the HIRES Ram. Suppose that IWR* (U152-10) goes low. Then GRAMWRT* (U152-8) will enable U154-4. The video address and data control signals are the same as for the LORES write operation. WRT4116* (U139-4) is inverted through U118 to disable the LORES Ram. Figure 6 illustrates the timing diagram during a write operation.

The read operation is very similar except that GRAMWRT* remains high and GRAMEN* goes low enabling U154. Refer to the write operation for complete details of the address latching and multiplexing. The data is latched into U125 from pin 14 of the HRES Ram by DATALAT, and the outputs of U125 are enabled by GRAMEN*. The CPU reads the data from U125. Note that D6 and D7 have inputs HORTP and VERTTP. In the present usage these bits are not used.

VIDEO DATA LATCH

The first step of the video processing is the data latch. For the LORES video this occurs at U116 and U117 (LS174's). U116 latches the lower 5 data bits. U117 latches D6 and D7, also the video control signals. D0-D5 and D7 are latched directly at the end of the timing chain cycle by T5*. D6 passes through U81 and U82. When CAPS* (U82-4) is true D6 is disabled, and DLYD6 becomes a function of D5 and D7. The purpose of the CAPS* key is to disable lower case characters. The ASCII code for lower case is within (60-7F)Hex. D6 is a "1" for all lower case characters. When a lower case character is decoded and the CAPS* key is depressed, DLYD6 will be "0" thus disabling lower case. The HIRES video also uses an LS174, U126, and it too is clocked by T5*.

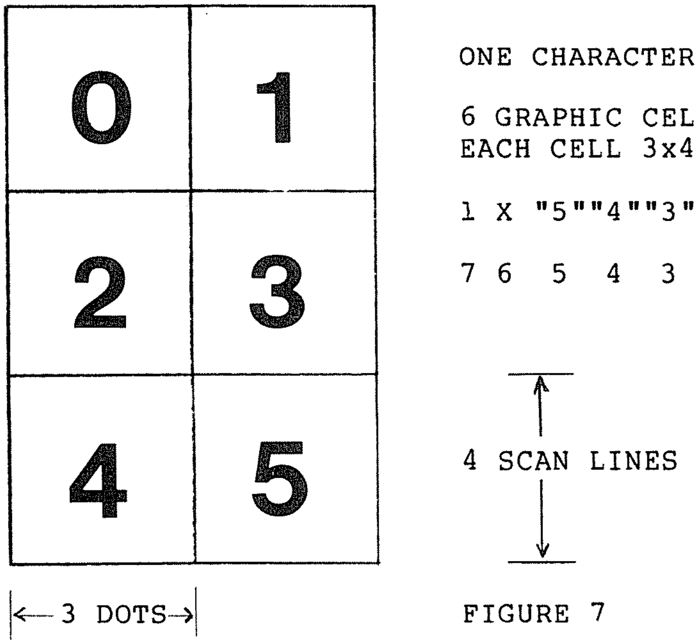
CHARACTER GENERATOR

Each character consists of a 5x7 dot matrix. Between any two characters there is a dot that is never turned on. Vertical spacing between dots is determined by CLKT. Note that in 32 character mode CLKT is 1/2 the 64 character mode CLKT frequency. This means that in 32 character mode there will be twice the vertical spacing between dots.

U100 is the Character Generator. The ASCII word is presented to U100 pins 1 through 7 from U116 and U117. U100 uses the ROW count to determine which patern of five dots to print on each row. It must output 7 times to complete one character after which five rows of blanks are output and the line increments and we're ready to output the first row of dot information to the 2nd character line.

GRAPHICS GENERATOR

U83 functions as the Graphics (LORES) Generator. The Graphics Character may use the entire character position, a 6x12 dot matrix. This matrix is divided into six rectangles as shown in figure 7. U83 is a dual 4x1 data multiplexer. It uses ROW4 and ROW8 as selects. Each 3x4 rectangle is either "on" of "off". When the ROW count is between 0 and 3, DLYD0 AND DLYD1 are selected. When the ROW count is between 3 and 7, DLYD2 and DLYD3 are selected. And finally for a ROW count between 8 and 11, DLYD4 and DLYD5 are selected. Each scan line, 3 dots may be written in each of two rectangles per graphic character. Each rectangle is defined by one data bit. DLYD7 defines a graphics character when true.



ONE CHARACTER POSITION 6x12 DOTS

6 GRAPHIC CELLS
EACH CELL 3x4

1 X "5""4""3""2""1""0"

7 6 5 4 3 2 1 0 (DATA BIT)

FIGURE 7

ALPHANUMERIC/GRAPHIC SHIFT REGISTERS

U101 is the alphanumeric shift register, U84 is the LORES graphic shift register, and U127 is the HIRES graphic shift register. All three receive parallel data and shift that data out to the video display in serial form.

All three behave in the same manner but have different restrictions that if not met will prevent data from being serialized.

The inputs to U102 pins 1,2,4, and 5 represent the restrictions to the alphanumeric shift register. If any of the inputs go low, the output will go high thus preventing the loading of data. DLYROW8* provides the blanking of ROWs 8 through 11 for alphanumeric characters. DLYBLANK* provides blanking beyond the 64th character position and below the 16th line. DLYD7* defines an alpha numeric

character when true. And CTRLT5(U81-8) provides that data in not loaded during CPU access time. Note that there are only 5 inputs to U101. This is because the sixth bit is tied to gnd to blank the sixth dot between characters.

The inputs to U85 pins 1,2, and 13 represent the restrictions to the LORES graphics shift register. If any of its inputs go low its output will go high preventing data from being loaded. There are two differences in the restrictions of the LORES graphics and the alphanumeric shift registers. The first is that for graphics characters the entire character position may be used therefore ROWs 8 through 11 are not blanked out. And DLYD7 defines a graphics character when true. The restriction regarding CTRLT5 still applies.

The inputs to U85 pins 3,4, and 5 represent the restrictions to the HIRES graphics shift register. CTRLT5 has the same purpose as described for the alphanumeric shift register. DLYLDHDG* provides blanking after the 80th character and below the 16th line. DLYLDINH* prevents loading during CPU access time.

INVERSE VIDEO

Inverse Video is controlled through Port 254. When D0 is set to a one and output to Port 254, VIDEOINV (U67-10) becomes a logic one. VIDEOINV drives U82-1 an input of an exclusive or gate (74LS86). When VIDEOINV is a "1" the combined video output of U68-4 (VIDEO "NORed" with HRESVID) is complemented thus inverting the video content. This is full screen video. When VIDEOINV is low the combined video information passes unchanged (standard video). The output of U82-3 COMBINED VIDEO (COMBVID*) drives both the high resolution B/W video output circuitry (U9-6,7) and the NTSC color channel (in the non-color display modes) at U68-11.

HORIZONTAL AND VERTICAL SYNC TIMING

U20 and U37 form the sync generator circuit. The horizontal and vertical sync generator circuits take the timing pulses from the divider chain, delays are applied to them, and the pulses are one-shot to fix the pulse width. This allows the vertical and horizontal positions to be adjustable and the correct pulse width is supplied to the video monitor to provide the correct horizontal and vertical synchronization.

The VERTICAL TIMING PULSE (VERTTP) from the divider chain is buffered by U20-8 (a CMOS exclusive or acting as a buffer only) and drives potentiometer R145. When R145 is set for some resistance U20-10 directly drives an RC timing delay circuit formed by R145 and C23. When VERTTP goes to a logic "1", C23 begins to charge. As it charges, the voltage at the input of U37-5 (74C04) rises. When the voltage reaches the threshold of a logic "1" (around 4 volts since this is CMOS logic), the output of U37-6 becomes a logic 0 (U37 is an inverter). The logic 0 output of U37-6 drives the input of the next inversion stage of U37-9. The logic 0 is inverted and the output of U37-8 becomes a logic "1" and stays that way until VERTTP returns to a logic "0". By changing the "R" of the R145 and C23 "RC" circuit the vertical sync pulse is varied. This allows the adjustable vertical screen position to compensate for variance in video monitors. The output of U37-8 is now given a fixed pulse width by the monostable circuitry of C22, R49 and the input of U37-1.

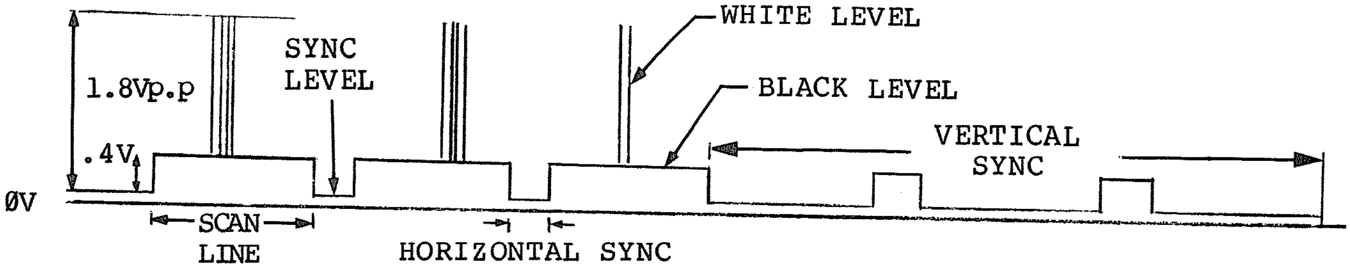
The horizontal sync circuits work in a similar manner with the HORIZONTAL SYNC TIMING PULSE (HSTP) driving U20-13. R144 and C24 form the RC delay, and C21 and R48 form the pulse shaping and width.

The horizontal and vertical sync pulses are mixed by two EXCLUSIVE OR gates of U20. The output of U20-3 directly drives the video mixing circuits of the Hi-resolution B/W video output. U20-4 drives the Sync input to the NTSC Prom.

U118-9,8 buffers the horizontal sync circuits to signal the Burst one-shot (U133-1) of the horzontal sync period. The Burst one-shot is described further in the section entitled "COLOR VIDEO".

COMPOSITE VIDEO MIXING CIRCUITS (HI-RES)

The following drawing illustates what the black and white video output would look like with an oscilloscope.



The "sync level" extends from 0 volts to .4 volts. This .4 volt level is commonly referred to as the "black level" or the voltage that would leave the display black. Above 1.2 volts is the white level. Between these levels are shades of gray. When a pixel is displayed on the CRT, the voltage goes above 1.2 volts for just enough time to display the dot. If most of the screen is blanked, looking at the video signal with an oscilloscope should show few very thin pulses extending to 1.2 volts with most of the time the voltage staying below .4 volts.

The combined sync output of U20-3 directly drives the base of Q2. When there is sync, U20-3 is high and Q2 is turned off. This provides no drive to Q1 and thus the video output is 0 volts. During the non-sync period U20-3 is "low" and "turns on" Q2. This causes 5 volts to be driven into voltage divider R19 and R16 and the base of Q1. The COMBINED VIDEO output (COMBVID*) drives peripheral and driver U9. When the video dot is to be displayed (COMBVID*=0) then the output transistor in U9 is "off" thus high impedance. This means that R17 has no effect in the circuit and around 2.5 volts drives the base of emitter-follower Q1. With around .7 volts drop the output of Q1 (75 ohms impedance) is 1.8 volts. When the video dot is NOT to be displayed, COMBVID* is high and R17 now appears in the circuit from the base of Q1 to ground. This causes the voltage at the base of Q1 to be reduced to around 1 volt thus with a .7 volt drop at Q1 (base to emitter) the output is at the "black level" or .4 volts. C7, R22, and C8 serve to filter, reduce power dissipation in Q1, and serve as short-circuit protection. R121 serves to set the output impedance of the video signal.

NTSC COLOR VIDEO

NTSC stands for the television standard first developed and implemented in the United States. Japan, Canada, and Mexico also adopted this (the first) television standard. NTSC color video uses the same timing and levels as Black and White video. It has a 60 hz vertical sync rate which corresponds to 262 scanned lines (including sync). The LNW80 refreshes the screen at a rate of 60 hz with 262 lines. Countries which have AC power frequencies of 50hz use PAL, SECAM, or other color systems with 312 scanned lines at a 50hz vertical rate. These systems are not compatible with the LNW80 set up for NTSC at 60hz.

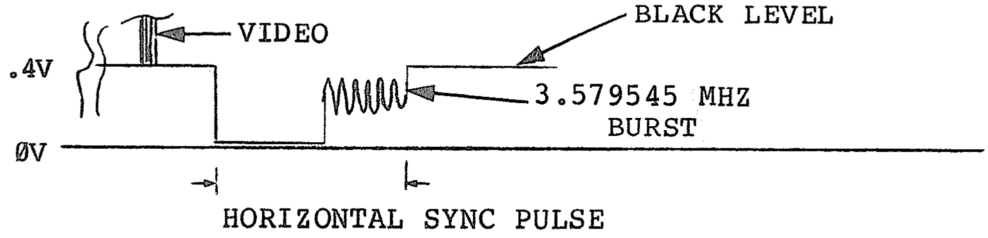
Color video works much the same as black and white. The video signal also is 1.8v p-p and .4 v is the black level and 1.2v is the white level. Horizontal and vertical sync are identical. Here are the differences:

1. COLOR ENCODING

In order to encode color information on the video signal there is a COLOR CARRIER. This color carrier allows the luminance information to be encoded with a PHASE relationship with the carrier thus specifying the color to be displayed.

2. COLOR BURST

The color carrier cannot be present during the displayed video period and thus is maintained by the monitor (or TV). This 3.579545 MHz signal is transmitted only for a small period of time by the computer (or TV station) to keep the color oscillator in the monitor (or TV) "locked in at the same exact frequency". This "burst" of color carrier is transmitted only for about 8 cycles and only at the very end of the horizontal sync pulse. This is commonly referred to as the "back porch" of the horizontal sync or the COLOR BURST and is illustated below:



COLOR MODES

In the LNW80 there are two possible color modes-low resolution and high resolution. The bandwidth of NTSC video only allows the low resolution mode to be displayed. In order to display the high resolution color, an RGB type direct drive monitor must be used and the optional RGB interface circuitry must be installed.

Port 254 data bit 2 selects whether or not color is enabled. COLOR (U67-2) and COLOR* (U67-3) do the logic switching to enable or disable color operation.

LOW RESOLUTION COLOR

In low resolution color mode, HRES will be low and HRES* will be high. This causes U129 to be enabled and U131 to be disabled via two gates of U52. U52-13 (COLOR) is high, U52-2 (HRES*) is high and U52-1 is VIDEO, thus the output of U52-12 which allows U129 to be selected to drive color information to U130 (NTSC ROM) will go low along with VIDEO. This means that the low resolution text and graphics information from the MODE 0 display will select whether or not the color information is to be passed on the NTSC ROM or the display will be black. When U129 is not enabled (it is a tri-state) gate pull-up resistors R101, R100, and R93 pull the floating inputs of the NTSC ROM to a logic "1". A logic "1" on all three bits of the color code or a 7 is defined as the color black. This means that there are two ways that the screen can be programmed black. One by putting 7 as the color information in the color memory or by blanking the low res screen.

Color information is stored in the same memory as the high resolution graphics memory U106-U111. The 6 bits of data, instead of being fed into a shift register (U127) to be sent out one bit at a time (as in high resolution graphics), is latched again into U128. It is fed to U128 for another level of delay to syncronize the Black and White video information (being shifted out of U101 or U84). Once latched into U128, the 6 bits represent two 3 bit (1 of 7 colors and black) fields. During the period that the first 3 dots (of the character position time) are being shifted out of U84 or U101, T3 is a logic 0. This drives the least significant 3 bits of U128 into the NTSC ROM to define the color. During the next 3 dot periods, T3 is a logic 1 and the most significant 3 bits of U128 are driven into U130 to define the color. Remember that if VIDEO was false, U129 is disabled completely thus overriding the contents of U128 (displaying black).

NTSC COLOR ROM

The NTSC COLOR ROM translates a 3 bit color code (0-7), SYNC and BURST (timing) into the proper R-Y (COLORB), B-Y (COLORA), and LUMINANCE (LUM) that the MC1372 requires to do the color encoding. The NTSC ROM (U130) is a high speed bipolar open collector prom. U130 combined with ladder resistors R85-92, R94, R99 and R102-105 form a high speed digital to analog converter to translate the digital color codes and sync information into the analog levels needed by the MC1372.

The following is the truth table for the NTSC ROM and the voltage levels developed for COLORA, COLORB, and LUM.

ADDRESS						DATA(Hex)		COLORA	COLORB	LUM
(Hex)	COLOR			SYNC	BURST					
	A0	A1	A2	A3	A4		COLOR			
00	0	0	0	0	0	6C	WHITE	1.5V	1.5V	.38
01	1	0	0	0	0	D5	GREEN	1.0	1.0	.5
02	0	1	0	0	0	CC	YELLOW	1.5	1.0	.38
03	1	1	0	0	0	7A	RED	2.0	1.5	.62
04	0	0	1	0	0	FD	MAGENTA	2.0	2.0	.50
05	1	0	1	0	0	EA	BLUE	1.5	2.0	.62
06	0	1	1	0	0	75	CYAN	1.0	1.5	.50
07	1	1	1	0	0	6B	BLACK	1.5	1.5	.70
08	0	0	0	1	0	6F	SYNC	1.5	1.5	1.00
to										
0F	1	1	1	1	0	6F	SYNC	1.5	1.5	1.00
10	0	0	0	0	1	AE	BURST	1.5	1.25	.75
to										
17	1	1	1	0	1	AE	BURST	1.5	1.25	.75
18	0	0	0	1	1	6F	SYNC	1.5	1.5	1.00
to										
1F	1	1	1	1	1	6F	SYNC	1.5	1.5	1.00

COLOR BURST ONE-SHOT

When HSYNC transitions from high to low (the end of the horizontal sync pulse) U133-13 strobes, using R80 and C83 for RC timing. The one-shot time is approximately 2usec. During this time, BURST is high and drives A4 of U130, the NTSC ROM. When A4 is high, the correct analog levels are supplied to U146 (MC1372) to output a burst reference signal with the correct phase and amplitude.

U146-MC1372 COLOR ENCODER

The MC1372 is a linear IC which contains both a chroma oscillator and the necessary chroma (color) encoder. U146 pins 1 and 2 along with Y2 the 3.579545 MHz crystal, C94 and 95, and R106 form the complete color reference oscillator (chroma oscillator) circuit. C95 is the chroma frequency trimmer adjustment. U146-1 is the square wave output of the 3.579 MHz color frequency and drives one-shot U133-10 to provide the color to luminance dot clock synchronization signal (COLORSYNC). U133 with timing resistor R107 (and no timing capacitor) forms a 50-70 nanosecond pulse generator. U133-5 drives open-collector inverter U162-11. Inverted and pulled up by R97, this generates COLORSYNC.

COLORA, COLORB, and LUM information from U130 determines the luminance level and the phase encoding of the video information that is output by the MC1372 on pin 12. R109 sets the output bias and CR1 selects the composite video polarity. The output of U146-12 (COLOROUT) is amplified and level shifted by Q13, R123 and R129. Q14 is an emitter follower to provide current amplification and 75 ohm impedance matching.

The MC1372 has the chroma encoder circuit separate from the final composite video mixing circuit. The chroma encoder output (U146-10) is fed back into U146-8 through R117 and blocking capacitor C110. U162-12, C111, and R118 form the chroma killer circuit that disables any chroma content in the video signal when COLOR is disabled. It does this by shorting the chroma signal to ground (through open-collector U162-12).

For more details on the operation of U146 refer to the data sheets on the MC1372.

HIGH RESOLUTION COLOR

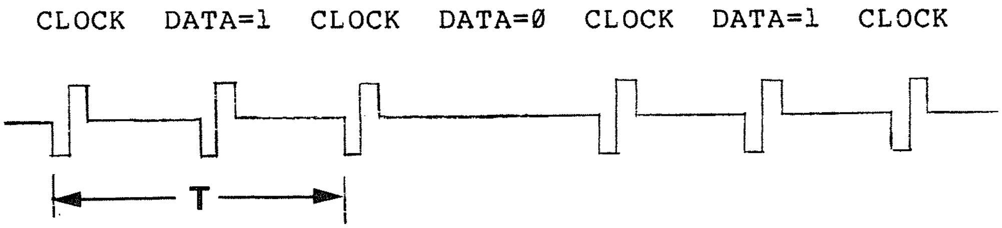
Assuming that the RGB ROM is installed, wired, and usable, then high resolution color is possible. In high resolution color U129 is disabled and U131 is enabled via U52-8 when HRESVID (U52-10), COLOR (U52-11), and HRES (U52-9) are true. In the high resolution color mode the dot information is supplied by the high resolution memory (480x192) and the color information is supplied by the low resolution memory (128x16 lines). U132 latches the output of the text memory and drives the multiplexer U131. U131 provides the RGB ROM with the least 3 bits of the text data (DLY0-DLY2) during the first half of the character position when T3 is "low" (first 3 dots) and then switches the output of U131 to the most significant 3 bits of the text data for the last 3 dot clocks (T3 is high).

BLACK AND WHITE DISPLAY THROUGH THE NTSC CHANNEL

In the low or high resolution black and white display modes, COLOR is low (U68-12). This disables both U131 and U129. Thus U130 receives no color or luminance information from U131 or U129. U130 still receives Sync information. Since U68-12 is low, video information passes directly through to U68-13 to drive the open-collector driver, U162-1. This through R95 then feeds dot information (luminance) directly into the MC1372 (U146) while U130 supplies the correct information to luminance during sync.

CASSETTE

Programs are loaded onto tape in serial fashion. The serial data contains both clock and data information as shown below:

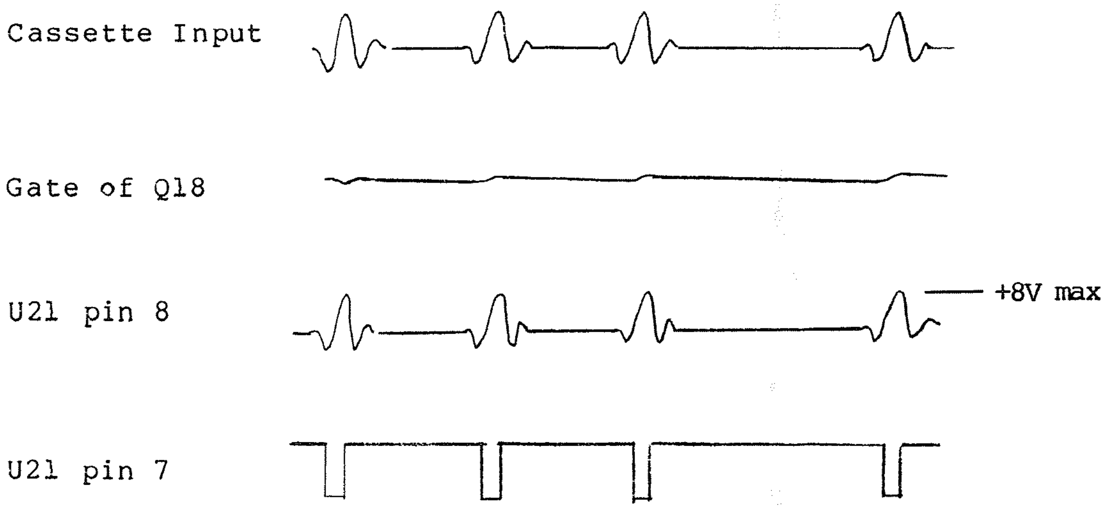


The time "T" is dependent upon whether the computer is in high speed or low speed. In low speed the time "T" is 2 ms. In high speed this time is 1 ms. This timing results in a transfer rate of 500 baud and 1000 baud respectively.

The cassette routines are resident in the Level II ROM's and cassette is accessed as an I/O port. When a CSAVE is entered, the address FF is placed on the address bus along with OUT* (U18-3) going low. The result is that FFOUT* (U54-11) goes low. When this happens D2 will go high and will be clocked into U8. This will turn U9 on and therefore the relay K1. This shorting of pins 1 and 3 of the cassette connector through K1 will turn the cassette motor on. D0 and D1 also get clocked into U8 with timing that results in the above diagram.

The cassette loading operation is accomplished through U21 A, B, and C. Refer to the figure below.

CASSETTE WAVEFORMS



The signal from the cassette is voltage divided by R24 and R25. U21A is a two pole active high pass filter which will eliminate noise. U21B along with U18 function as an automatic gain controlled (AGC) amplifier. The amplitude at U21B is peak detected by CR2 and C119 to get an average signal level. The voltage at the gate of Q18 will then be higher as the signal amplitude goes higher. The higher the voltage at the gate, the higher the resistance between the source and drain which will have the effect of lowering the gain of this stage. The lower the gate voltage, the lower the drain to source resistance and the higher the gain. The voltage level of U21B will be controlled to a maximum of about 8.0 volts. U21C is a comparator who's trip level is dependent upon the voltage at U21C pin 5. The output at pin 7 is normally high which will go low when a data or clock signal is encountered.

U38 is a flip flop who is set and reset by U21C pin 7 and FFOUT* respectively. The decoded signal FFIN* will then place the cassette information onto D7.

POWER SUPPLY

The LNW80 power supply section is designed to power both the LNW80 computer board and the LNW expansion board.

The LNW80 transformer is 9 volts AC rated at 4 amps and 18 volts AC rated at 2 amps. The unregulated AC voltage of the transformer is rectified by CR17 and filtered by the 15,000 ufd capacitor. This capacitor must be located somewhere off the LNW80 board. Q3, Q7, Q8, Q9, and Q10 provide the regulated +5 volt supplies. All +5 volt outputs are connected through diodes to a summing point at thte anode of Q12. If any of these voltages exceeds approximately 6.2V then CR24 will begin to conduct. While the gate of Q12 remains unchanged, the anode voltage will begin to rise higher than the gate. This will cause Q12 to begin conducting which will fire SCR1 causing F1 to open. This overvoltage protection prevents damage to components due to high voltage.

CR15 rectifies the AC signal which is then filtered by C121. Q4 regulates thte voltage to +12 volts. If the voltage at JP9 exceeds 13 volts, CR11 will begin to conduct. While the gate of Q6 remains unchanged, the anode will rise above the gate voltage. This will cause Q6 to begin conducting and result in turning SCR2 on and F2 will open.

R138 limits the current, C137 provides DC blocking and CR19 and CR16 provide a voltage doubler. Q11 will then provide a -12 volt regulated output which supplies both the LNW80 computer and expansion board.

The voltage at the negative lead of C131 is regulated by R133 and CR14 and it is then filtered by C130. This -5 volts is used both for the LNW80 computer and expansion board.

THEORY OF OPERATIONS
EXPANSION BOARD

The Expansion board is merely an extension of the main computer board. A number of the functions of the LNW80 Computer are performed on the expansion board. These functions include additional memory, real time clock, floppy disk controller, parallel printer, and RS232C serial port. The expansion bus is a 40 pin connector that contains all of the necessary control, data, and address lines necessary for operation.

LNW80 EXPANSION BUS

The 40 pin bus is equivalent to the TRS80's 40 pin expansion bus. The following are the signals and their descriptions for the expansion bus:

PIN #	SIGNAL NAME	DESCRIPTION
1	RAS*	ROW ADDRESS STROBE
2	SYSRES*	SYSTEM RESET
3	CAS*	COLUMN ADDRESS STROBE
4	A10	ADDRESS INPUT
5	A12	ADDRESS INPUT
6	A13	ADDRESS INPUT
7	A15	ADDRESS INPUT
8	GND	GROUND
9	A11	ADDRESS INPUT
10	A14	ADDRESS INPUT
11	A8	ADDRESS INPUT
12	OUT*	I/O WRITE STROBE
13	WR*	WRITE STROBE
14	INTACK*	INTERUPT ACKNOWLEDGE
15	RD*	READ STROBE
16	MUX	ADDRESS MULTIPLEXER
17	A9	ADDRESS INPUT
18	D4	DATA BUS
19	IN*	I/O READ STROBE
20	D7	DATA BUS
21	INT*	MASKABLE INTERUPT REQUEST
22	D1	DATA BUS
23	TEST*	BUS REQUEST
24	D6	DATA BUS
25	A0	ADDRESS INPUT
26	D3	DATA BUS
27	A1	ADDRESS INPUT
28	D5	DATA BUS
29	GND	GROUND
30	D0	DATA BUS
31	A4	ADDRESS INPUT
32	D2	DATA BUS
33	WAIT*	Z80A CPU WAIT
34	A3	ADDRESS INPUT
35	A5	ADDRESS INPUT
36	A7	ADDRESS INPUT
37	GND	GROUND
38	A6	ADDRESS INPUT
39	GND	GROUND
40	A2	ADDRESS INPUT

MEMORY EXPANSION

The Expansion Board contains 16 additional 4116 type RAM chips at U42-49 and U53-60. U37 and U38 (LS241's) are used to multiplex the address lines. U34 and U35 are used to buffer the data lines both input and output.

RAS* is buffered to all of the RAMs while CAS* is gated by U29 with 48KRAMEN* and 32KRAMEN*. When the CPU wishes to access the upper memory it places an address from 7FFF to FFFF on the expansion bus. The address is decoded at U30. When A15 and A14 are high and RAS* is low, 48KRAMEN* (U30-7) will go low enabling CAS* to the upper bank of memory. When A15 is high and A14 and RAS* are low, 32KRAMEN* (U30-6) will go low enabling CAS* to the lower bank.

The data bus is buffered by U34 and U35. These buffers will pass data from the memory onto the data bus when pin 1 of U34 and U35 is low. 32KRAMEN* and 48KRAMEN* are fed into U11 pins 2 and 1 respectively. When either goes low the output (U11-3) will go low. This signal is used to gate RD* through U29 pins 9 and 10 respectively. U29-8 is then fed into U34 and U35 and is used to enable memory data onto the data bus. U34 and U35 is tied to gnd thus enabling data from the data bus to the data input of the memory array at all times.

For further information on the operation of 4116 type dynamic rams refer to the section on program memory in the theory of operations of the LNW80 computer board.

FLOPPY CONTROLLER AND PRINTER DECODING

U19 is used to decode the various signals involved in the floppy disk and parallel printer circuits. All addresses memory mapped within the range 37E0 to 37EC (HEX) are decoded through U19.

When the CPU places an address in this range on the address bus RAS* (U30-1) will go low indicating a valid address. All of the inputs to U31 will go high resulting in a logic "0" at U31-8. A11, A14, and A15 will be low such that all of the inputs to U30, pins 1,2,3,13, and 14, will be low. U30-4 will go low enabling U30-12 which will also go low. U30-12 is used to enable the outputs of U19 which effectively produces a "double" 2/4 line decoder.

The outputs of U19 are used as control signals for both the Floppy Controller and the Parallel Printer Interfaces. Explanations of these signals and the addresses that decode them may be found below:

PIN#	FUNCTION	ADDRESS DECODE	WR*	RD*
7	INTERUPT RESET	37E0H	1	0
6	N/C	37E4	1	0
5	PRINTER STATUS READ	37E8	1	0
4	FLOPPY READ	37EC	1	0
9	MOTOR ON/DRIVE SELECT	37E0	0	1
10	CASSETTE	37E4	0	1
11	PRINTER WR STROBE	37E8	0	1
12	FLOPPY WRITE	37EC	0	1

PARALLEL LINE PRINTER PORT

The expansion board contains an interface to the Radio Shack/Centronic Printer. This Printer Interface consists of an eight bit output port and a four bit input port.

This I/O port is accessed by either writing or reading from address 37E8 Hex. This address is decoded at U30, U31, and U19.

When reading the memory address 37E8, the printer status is read through U3. Only the 4 most significant data bits contain valid information. The meaning of each data bit is as follows:

Data Bit	Printer Status
D7	Printer Busy
D6	Paper Empty
D5	Unit Select
D4	Fault

The Radio Shack's parallel printer has wire ORed internally, the printer busy status, and the paper empty signal. When using the Radio Shack/Centronic Printer, only one of these two bits, D6 or D7, needs to be checked. The printer busy indication is issued by asserting a logic "1". When this occurs, the paper empty status will also be a logic "1". The unit select and fault status bits are not used by the Radio Shack's printer.

A write to memory location 37E8 will load the output latch U4 and U5 to the line printer's internal data buffer and also generate a signal through U7 called DATA STROBE (U7-4). DATA STROBE will be a low-going pulse of approximately
1.5us.

The Radio Shack's printer is set up to recognize the following control characters for the line feed and carriage return:

Character	Function
0A(Hex)	Line Feed
0D	Carriage Return

When either of these control characters are received by the printer, the printer will assert a logic "1" at the printer busy status.

CLOCK CIRCUIT

The Expansion Board Main Clock is a 4 MHz oscillator, utilizing Y1 and U18 to form a series resonant circuit. The 4MHz clock is input to U9-14 and U24-2.

U9 provides a divide by 2 resulting in a 2 MHz clock at U9-12, which is then input to U22-3 which again divides by 2 resulting in the 1 MHz clock input to the FLOPPY CONTROLLER (U14).

U24 effectively produces a divide by 13 of the 4 MHz clock resulting in a 307 KHz clock at U24-11. This is used to clock U25, a 4 bit binary counter. Its output produces 4 of the 8 baud rates used for the SERIAL INTERFACE. The frequencies of the outputs can be calculated by multiplying the baud frequency by 16 for the frequency in Hz.

U17 is clocked by U25-12 (38.4KHz) and provides a divide by 11 resulting in a 3.49KHz clock at U17-11. This is input to U10-14, which does a divide by two such that U10-12 is a 1.75KHz clock.

The 2nd half of U10 is clocked by U25-11 (19.2KHz) and does a divide by 8. The outputs of U10 provide the other 4 baud rate clock signals. Baud rate clocks will be discussed in the section entitled "SERIAL INTERFACE".

U10-11 (2.4KHz) is clocked into U9-1 which set for a divide by 6 resulting in an output of 400Hz. This is then input to U12 which is set for a divide by ten resulting in the 40Hz clock signal used to provide the REAL TIME CLOCK.

FLOPPY DISK INTERFACE

The function of interfacing to a floppy disk drive is performed primarily by the Western Digital's FD1771B-01 Floppy Disk Formatter/Controller chip. Note that when using double density adapters, the "doubler" performs the duties of the controller chip. The LNDOUBLER 5/8 will be explained in a further section.

The FD1771, a MOS/LSI device which performs much of the housekeeping involved in reading and writing data to and from the disk has the following internal features:

1. Cyclic redundancy check and generation for error checking.
2. Internally seperates disk head outpput into data.
3. Checks for desired section, check ID field and locate it's data address mark.
4. Accounts for track number of the current read/write head position

The interface to the processor is accomplished through the eight Data Access Line (DAL) and the associated control signals.

When reading from the DAL, the address decoder U19-4 (37EC READ*) will be low enabling U8 and U15 to buffer data from U14 to the data bus. U8 and U15 are LS240's, OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS with inverted 3-state outputs.

When writing from the data bus to the DAL, the address decoder U19-12 (37EC WRITE*) will be low enabling U8 and U15 to buffer data from the data bus to the floppy controller.

The least two significant addresses, A0 and A1, are decoded by the floppy controller to interpret the selected registers of the read and write operations. These registers are decoded as follows:

A1-A0	READ	WRITE
0 0	STATUS REG.	COMMAND REG.
0 1	TRACK REG.	TRACK REG.
1 0	SECTOR REG.	SECTOR REG.
1 1	DATA REG.	DATA REG.

The interrupt request (INTRQ) of the FDC (U14-39) indicates the completion or termination of any operation. INTRQ presets U22A presenting a high to U1 pins 4 and 5, which is reset by reading the FDC Status Register. Reading from 37E0H will reset the interupt signal (U1-6) by clocking a low at the output of U22A.

The FDC requires a 1 MHz clock input to U14-24 which is generated from the 4 MHz main clock circuit and is explained in the clock discription of the expansion board.

Drive Selection through Data Lines D0-D3 is clocked into U13 by 37E0 WRITE* (U19-9). This also triggers the one-shot, U7A, generating the motor on signal. The drive selection is only activated when the motor on signal (U7-5) is high.

When U7-5 is low, clearing U13, a high is generated at U11-8. This signal is then inverted at U20-10 providing a low command and indicating that the floppy status is ready.

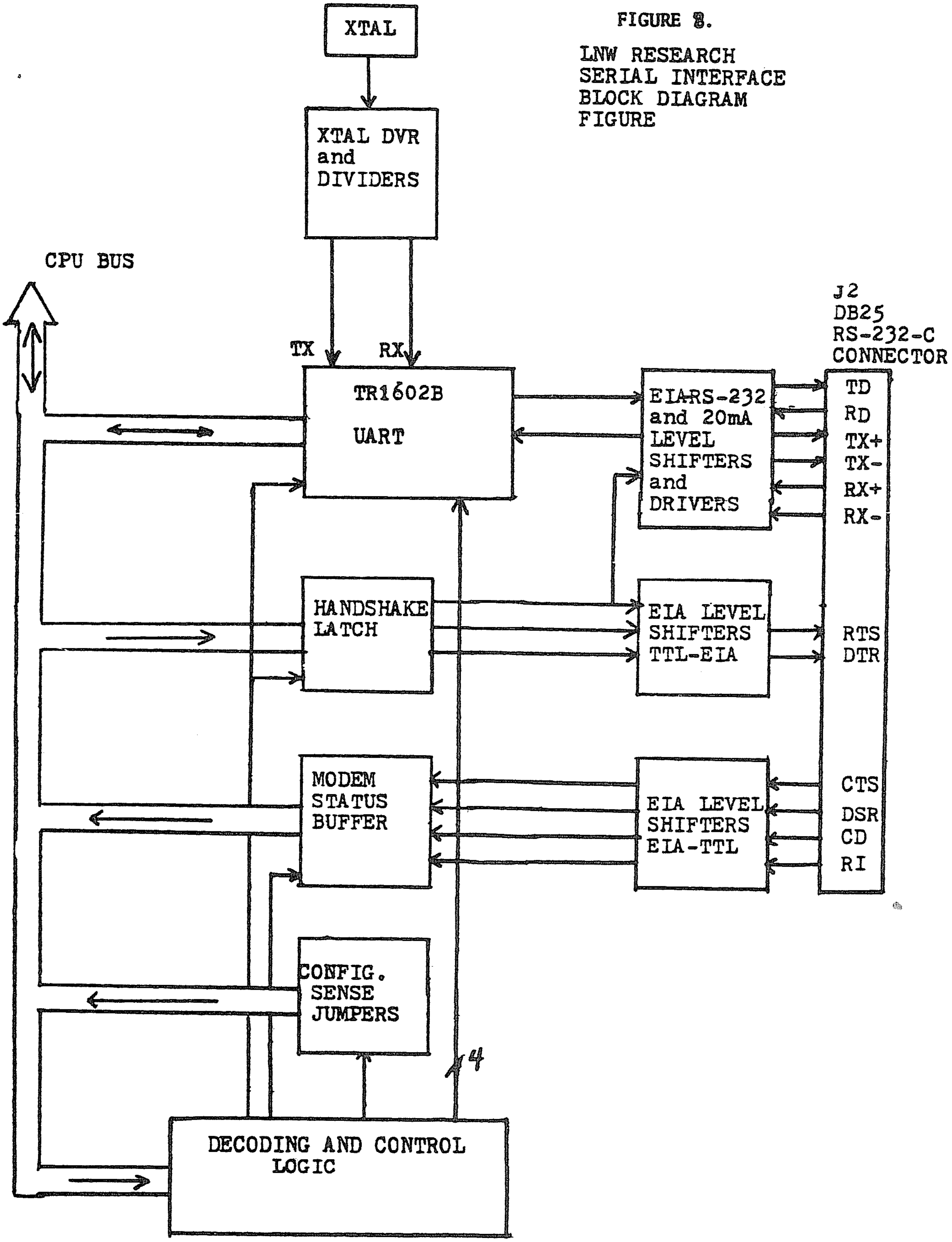
U14-19 is the MASTER RESET, and is driven by SYSRES* from the main computer board. When MR* goes low, the FDC is reset and HEX 03 is loaded into the command register and the system will proceed to reboot. For further details of the internal operations and the programing of the FDC refer to the data sheets.

SERIAL INTERFACE

The Block Diagram (figure 8) outlines the major sections of the Serial Interface. For the following circuit description, use the schmatics along with the Block Diagram to aid in visualizing the circuit theory.

FIGURE 8.

LNW RESEARCH
SERIAL INTERFACE
BLOCK DIAGRAM
FIGURE



BAUD RATE GENERATION

In order to provide the receive and transmit baud clocks for the UART, the 4 MHz clock is divided down. Details of the clock divider circuitry is given in the section entitled CLOCK CIRCUIT.

The Baud Rate is programmed by jumpering A,B,C,D,E,F,G, or H to the RX and TX line. (Note that on the pre-assembled LNW80 Systems, these have been jumpered using two 8-pin dip switches.) These RX and TX lines are used by the UART for the RECEIVE and TRANSMIT BAUD CLOCKS.

TR1602B UART

The TR1602B Universal Asynchronoous Receiver/Transmitter (UART) is the heart of the serial interface. It takes parallel data from the CPU BUS and converts it to serial data and at the same time can receive serial data and convert it to parallel. It has two registers which can be read--one for the status and the other with received data. It has two registers which can be loaded--one with transmit data and the other with control information (word length,parity,stop bits). Refer to the Data Sheet of the Western Digital TR1602B for further details of operation.

EIA RS232C and 20mA LEVEL SHIFTERS AND DRIVERS

The serial output of U40 is pin25 (TRQ). It drives U18 for buffering to EIA Driver U61-9 and the 20mA driver U50-6. Serial data can be output by U26-10 which drives both U50-7 and U61-10. U50, R23, and R24 provide the 20mA interface. When U50 conducts it allows about 20mA of current to flow (20mA=mark,0mA=space). Received serial data is brought in to U51-4. U51 is an EIA to TTL receiver. The 20mA serial input is accomplished by the current to voltage conversion of R25 and R26. The TTL received data is fed to the Receive Data (RI,U40-20) of the UART and is fed to U33-12 to be read as part of the Modem Status Buffer.

HANDSHAKE LATCH

U26 is the handshake latch. D0-D2 inputs to U26 pins 4, 5, and 12 respectively. The latch is loaded when OUT EAH (U16-5) goes low which is input to U26-9. The outputs of U26 are fed to U61-12,13 and U61-4,5 for level conversion to EIA standards.

MODEM STATUS BUFFER

U33 is the modem status buffer. U52, an EIA receiver, converts EIA levels to TTL. This is input to U33 and enabled to the data bus when IN E8H (U16-7) goes low. In addition, the Serial Input (TTL) is fed to U33-12 to allow the CPU to directly input the serial data.

CONFIGURATION SENSE JUMPERS

Jumper wires from K,N,P,M, and J connected to E5 or E6 select whether the associated data bit is a "1" or a "0" when U28 is enabled onto the data bus. It is enabled by IN E9H (U16-6) and is used by serial driver programs so that stop bits, parity, and word length can be selected by hardware configuration.

DECODING AND CONTROL LOGIC

The port address decoding (IN,OUT-E8,E9,EA,EB) is accomplished by U41 and U16. U41 decodes the upper 6 bits (E8) and outputs to the strobe inputs of U16. The lower two address bits (A1,A0) feed to the A and B inputs of U16. U16 is a 2/4 line decoder and its outputs (active low) select which port is addressed and whether it is an IN or OUT instruction. U23 pins 1 and 2 are driven by INEAH and INEBH such that whenever the Receive Register and the Status Regiser of the UART are read, U39 drives the data onto the data bus. Below is a summary of the address decoding:

IN E8H - Modum Status Register
IN E9H - Configuration Jumpers
IN EAH - UART Status Register
IN EBH - UART Receive Register, Data Received Reset

OUT E8H - Master Reset
OUT E9H - Not Used
OUT EAH - Control Register Load, Handshake Latch Load
OUT EBH - Transmit Holding Register Load

SERIAL INTERFACE PORT ADDRESSING

Data Bit	Jumper Letter	Configuration Jumpers	UART Control Register Handshake Latch	UART Status Register	Modem Status Register
D7	j	Even/Odd Parity 1=Even 0=Odd	Even/Odd Parity	Data Received 1=True	Clear to send Pin 5 DB-25
D6	m	Word Length 1	Word Length 1	THRE 1=True	DSR Pin 6 DB-25
D5	p	Word Length 2	Word Length 2	OverrunError 1=True	CD Pin 8 DB-25
D4	n	Stop Bit Slct. 1=2bits,0=1bit	Stop Bit Slct. 1=2bits,0=1bit	Framing Err. 1=True	Ring Indctor. Pin 22 DB-25
D3	k	Parity Inhibit 1 disabled par.	Parity Inhibit 1 disabled par.	Parity Error 1=True	
D2			Break,0 Disable Transmit Data		
D1			Request to Send Pin 4 DB-25		Receiver In. UART Pin 20
D0			Data Terminal Ready Pin 20 DB-25		
		IN 0E9H	OUT 0EAH	IN 0EAH	IN 0E8H

REAL TIME CLOCK

The 40 Hz Real Time Clock is output from U12-11 and used to clock U21B. This clocks a logic "0" to U21-9 which presets U21A. This places a logic "1" at U21-5 which is input to U29-4. If U29-4 goes high then its output U29-6 will go high. U29-6 is inverted through U20 and thus presets U22B. U22-9 goes high and is inverted through U1 which sends a maskable interupt request to the CPU. The CPU responds by decoding 37E0RD* at U19-7. 37E0RD* presets U21B, clocks a logic "0" into U21A, and enables the output of U3B. If bit D7 is a logic "1", then the RTC generated the interupt request.

The programming of the Real Time Clock can be by DOS or in a User's Machine Program. Note the DOS Manual for commands.

THEORY OF OPERATIONS
LNDOUBLER 5/8

The LNDOUBLER 5/8 has as its heart two floppy controller IC's--the FD1771 (single density controller) and the FD1791 (single and double density controller). The reason that the FD1771 is still needed is that the commands are slightly different and the BOOT in the level II Roms would not work. The two floppy controllers are tied together so that only one of the two can be enabled at one time.

SINGLE/DOUBLE DENSITY OPERATION

Single density operation is enabled when memory location 37EC is written to with data FE. Double density operation is enabled when memory location 37EC is written to with data FF.

The controlling signals for single/double density operation are DOUBLE* and DOUBLE, U16 pins 9 and 8 respectively. U5 and U6, open collector inverters, are tied together to create an 8-input nor gate whose common output is inverted through U7 and again through U12. U12-8 is used to clock DAL0* into U16-12. Double density operation is selected when DOUBLE and DOUBLE* are high and low respectively.

The signal DOUBLE is input to U10-3, U11-1, and U2-2. When U10-3 is low, the FD1771 is enabled. U11 is used to select the STEP, DIRC, WD, and WG signals to be output to the Floppy from either the FD1771 or FD1791. When U11-1 is low the single density controller outputs will be selected. U2 enables VFOE* (U2-3). This signal is input to the WD1691 and will be explained later.

The signal DOUBLE* is input to U9-3, U9-37, and U8-15. When U9-3 is low, the FD1791 is enabled. U9-37 enables the FD1791 for double density. And U8-15 enables the WD1691 for double density.

CLOCK CIRCUIT

The LNDOUBLER 5/8 uses a series resonant circuit utilizing Y1 and U12 to provide a 4MHz clock at U12-12. This is then input to U14-13 which performs a divide by 2 resulting in a 2MHz clock at U14-5. Both the 4MHz and 2MHz clocks are input to U13 pins 5 and 6 respectively. In 5.25" operation the 2MHz clock is selected and then divided by 2 at U14 to become CLKI (U14-9). In 8" operation the 4MHz clock is selected and then divided by 2. CLKI is used to clock both the FD1771 and the FD1791 pins 24, and is 1MHz in 5.25" operation and 2MHz in 8" operation.

5.25" & 8" SELECTION

On power up or reset, the LNDOUBLER 5/8 switches to 5.25" or 8" drive operation depending on the setting of the 5/8 switch.

When the 5/8 switch is in the 5 position, U17 will be preset upon power up or reset and the control signals FIVE (U17-9) and FIVE* (U17-8) will go high and low respectively enabling 5.25" operation. When the 5/8 switch is in the 8 position U17 will be cleared upon power up or reset and FIVE and FIVE* will go low and high respectively enabling 8" operation.

5.25" and 8" operation may also be selected through software switching. When memory location 37EE is written to with data bits D7=1 and D6=1 the LNDOUBLER will switch to 8" operation. When memory location 37EE is written to with data bits D7=1 and D6=0 the LNDOUBLER will switch to 5.25" operation.

5.25" & 8" OPERATION

FIVE* is input to U4-7 through R6 and determines the pulse width of the one-shot used for RDIN* (U4-12). In 8" operation RDIN* has a pulse width of approximately 225us. In 5.25" operation RDIN* has a pulse width of approximately 450us.

FIVE is input to U13-1, an LS158, and is used to select the various signals associated with either 5.25" or 8" operation.

The inputs to U13 associated with 5.25" operation are a 2MHz clock (U13-6), a 2MHz voltage controlled oscillator (U13-10), and gnd (U13-13).

The inputs to U13 associated with 8" operation are a 4MHz clock (U13-5), a 4MHz voltage controlled oscillator (U13-11), and TG43MUX* (U13-14)

TG43 indicates that the RD/WR head is positioned between tracks 44-76 and is valid only during RD and WR commands. It is output from the FD1771 and FD1791 as STG43 and DTG43 respectively. STG43 and DTG43 are then inverted through U5, an open collector inverter, and the outputs are tied together producing TG43MUX*. In 5.25" operation TG43 is always enabled. In 8" mode TG43 is enabled only for tracks 44-76.

ANALOG PHASE LOCK LOOP DATA SEPARATION

U15, an LS629, provides the VCO, voltage controlled oscillator frequency of 4MHz (2MHz for 5.25" operation) for the WD1691 (U8). In order to guarantee that it is not sensitive to power supply variations, VR1 (78L05) provides a regulated supply to the LS629 and the adjustment controls R25 and R26. R25 is a multiturn pot to adjust the frequency range and R26 adjusts the bias voltage for the VCO. The WD1691 and the 74LS629 make up the ANALOG PHASE LOCK LOOP DATA SEPERATION. For further details refer to the data sheets supplied in this manual.

PRECISION WRITE PRECOMPENSATION

The WD2143 provides an accurate write precompensation value according to the adjustment of R24. A negative true pulse of the actual precompensation value can be observed with an ascilloscope at U8-4. Write precompensation is factory aligned to 200ns +/- 25ns and is enabled only for double density operation (all tracks 5.25" and tracks above 43 for 8"). For further details of the interface between the WD2143 and the WD1691 refer to the data sheets.

WAIT LOGIC

The "wait" logic circuitry consists of U1, U2, U6, U7, and U18.

The "wait" logic allows 8" disk drive operation under a slow CPU speed. This logic is used by several operating systems and is maintained for compatibility reasons.

When the memory location 37EE is written to with data bits D7=1 and D5=1 then the "wait" logic is turned on. When memory location 37EE is written to with data bits D7=1 and D5=0 then the "wait" logic is turned off.

Although the "wait" logic need not be invoked for single density operation for 8" drives at the 1.77MHz CPU speed an explanation of its operation follows:

1. The "wait" logic is turned on
2. The FDC is initialized and registers set
3. The command is given to the FDC to read or write
4. The status register is read causing the "wait" logic to issue a "wait" to the CPU until:
    a. the busy bit in the status register goes false
    b. DRQ on the FDC goes true
    c. IRQ on the FDC goes true

If the condition that removed the "wait" was (a) or (b) then the "wait" logic is still "on" but the CPU wait was removed until the next time the status register of the FDC is read. If the condition that turned off the wait was (c) then the wait logic is turned off.

TROUBLESHOOTING

It is not within the scope of this manual to provide a complete and detailed procedure for troubleshooting the LNW80. But for those with technical experience in digital electronics, this section may provide some helpful hints.

POWER SUPPLY

The first step in troubleshooting is to check the supply voltages. The following voltages should be verified at the corresponding test point.

REGULATED VOLTAGE	TEST POINT
+5V +/- .3V	JP1;JP3;JP5
+12V +/- .5V	JP9
-12V +/- .5V	JP7
-5V +/- .3V	JP11

Note that the -5V supply is critical to the RAM's. If it is not present damage may occur to those parts. Therefore check the -5V supply first. If it is not present then disconnect the other supplies before troubleshooting further.

If the fuses continually blow you may disable the overvoltage protection by removing the SCR's. But before doing so disconnect the power supplies. Be ready to turn off power if any component begins smoking.

VIDEO OUTPUT/ADJUSTMENTS

After the power supplies have been verified proceed to check that there is a video output. If there is a video output but it seems unstable or out of sync, then try adjusting C140. If that doesn't work then check the video divider chain noting in particular the horizontal and vertical sync pulses. If there is no video, then first check for sync pulses. If all the sync pulses seem correct then check the alphanumeric and graphic shift registers. Keep in mind that the CPU may be instructing the VIDEO to clear the screen.

SYSTEM CLOCK

Check that the Z80A has a clock at U2-6. If not then follow the circuitry back to find out why. It should be either 4MHz (high speed) or 1.77MHz (low speed).

CPU/CPU TEST

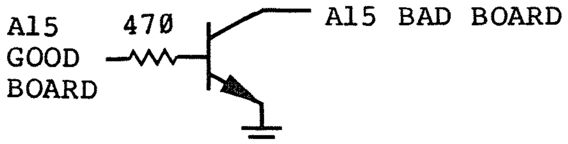
There is a method by which you may test the RAM, BASIC ROM, VIDEO RAM, and KEYBOARD. This procedure requires two computers. One must be a known good 16K level 2 TRS80 or 16K LNW80.

A special cable must be created in which A15 is inverted from the good board to the bad board to enable the good board to take over control. By doing so the bad board will be perceived by the good to occupy the upper 32K of memory space.

SPECIAL CABLE

Materials:
40 pin cable, 2N3906 transister, 470 ohm resiser

Procedure:
Break lines 7 and 8 on the cable. Line 7 corresponds to pin 8 on the connector and line 8 corresponds to pin 7 on the connector. Pin 8 is ground and pin 7 is A15. Connect pin 8 from the good board to the emitter of the transistor. Connect pin 7 from the good board through a 470 ohm resistor to the base of the transistor. And connect the collector to pin 7 of the bad board. Connect the two computers together and ohm out the connections to verify proper connection.



ENABLING THE BUS

If the bad board was preassembled by LNW RESEARCH then no further modifications must be made except pulling U2-25 to ground and reducing noise on the MUX line by placing a parallel combination of a 180 ohm resister and a 330 pf capacitor from U18-5 to ground.

If the bad board was purchased as a bare board and built as a kit then the following modifications must also be made: lift the pins of U36-3 and U46-5; jumper U36-12 to U18-7, U18-9 to U18-14, and U18-5 to U18-15.

CPU TO CPU TEST PROGRAM

```
  5 CLS:PRINT"CPU TO CPU TEST":PRINT:PRINT:PRINT
 10 INPUT"TEST ROM,RAM,VID,KEY";ZX$
 20 IF ZX$="ROM" THEN 100 ELSE IF ZX$="RAM" THEN 200
    ELSE IF ZX$="VID" THEN 300 ELSE IF ZX$="KEY" THEN 400
 30 GOTO10
100 INPUT"SELECT ROM NUMBER(A,A1,B,C1,ALL,LOOP)";ZX$
105 C=-32767
110 IF ZX$="A" THEN 120 ELSE IF ZX$="A1" THEN 121 ELSE
    IF ZX$="B" THEN 122 ELSE IF ZX$="B1" THEN 123 ELSE
    IF ZX$="C"   THEN 124 ELSE IF ZX$="C1" THEN 125 ELSE
    IF ZX$="ALL" THEN   126 ELSE IF ZX$="LOOP" THEN 127
    ELSE 10
120 Y=0:GOTO150
121 Y=2048:GOTO150
122 Y=4196:GOTO150
123 Y=6144:GOTO150
124 Y=8192:GOTO150
125 Y=10240:GOTO150
126 FOR X=-32767 TO -20480:IF PEEK(X)=PEEK(Y) THEN 130
    ELSE 140
127 INPUT"LOCATION DESIRED(DECIMAL 0-12287)";Z:LET
    Z=Z-32768
128 ?PEEK(Z):GOTO128
130 ?Y:Y=Y+1:NEXTX:PRINT"TEST COMPLETE":GOTO10
140 PRINT"TEST FAILED":PRINT"LOC.     EXPECTED    ACTUAL":
    PRINT Y,PEEK(Y),PEEK(X):Y=Y+1:STOP:NEXTX
150 A=Y+C:B=A+2047:FOR X=A TO B:IF PEEK(X)=PEEK(Y) THEN 130
    ELSE 140
151 ?Y:Y=Y+1:NEXTX:?"TEST COMPLETE":GOTO10
200 Y=170:FOR X=-16384 TO -1:POKE X,170:IF PEEK(X)=170 THEN
    NEXT X ELSE 220
210 Y=85:FOR X=-16384 TO -1:POKE X,85:IF PEEK(X)=85 THEN
    NEXT X ELSE 220
215 ?"TEST COMPLETE":GOTO10
220 ?"TEST FAILED":?"LOC.     EXPECTED       ACTUAL":
    ? X+32768,Y,PEEK(X):STOP:NEXTX
300 Y=0:FOR X=-17408 TO -16385:?X+32767:POKEX,Y:Y=Y+1:
    IFY=192 THEN Y=0
302 NEXTX
310 Y=0:FOR X=-17408 TO -16385:?X+32767:Z(3)=0:GOSUB600:
    IF Z(1)=Y THEN 320 ELSE 350
320 Y=Y+1:IF Y=192 THEN Y=0
322 NEXTX:?"TEST COMPLETE":GOTO10
350 ?"VIDEO RAM FAILED TEST":?"LOC.   EXPECTED    ACTUAL":
    ?X+32768,Y,PEEK(X):Y=Y+1:IF Y=192 THEN Y=0
351 NEXT X:?"TEST COMPLETE":GOTO10
400 ?PEEK(-18177):GOTO400
600 Z(3)=Z(3)+1:Z(1)=PEEK(X):Z(2)=PEEK(X):IF Z(1)=Z(2)
    THEN RETURN ELSE IF Z(3)=25 THEN RETURN ELSE 600
```

CPU/CPU TEST PROGRAM

The previously listed program will enable you to test the program RAM, ROM, LORES VIDEO RAM, and KEYBOARD on the "bad" board. Remember that the bad board will be perceived by the good board from locations 32768 to 65535. Remember also that writing to or reading from the upper 32K requires that you use negative numbers. The following is a simple formula for translating the actual location to the location to be poked to peeked:

POKE OR PEEK ADDDRESS = ACTUAL ADDRESS - 32768

The simplest procedure for loading this program is to type it in and save to cassette. This will prevent you from having to retype it if the system crashes. Connect the two computers together, power up the good board and load level 2 basic. Then load the program from cassette and then turn on the power on the bad board. The program will not load if the power to the bad board is already on.

The program will display a simple menu. Respond with ROM and the program will ask you whether you wish to test ROM A1, A, B1, B, C1, C, or all. You may also loop on any one location. The way the ROM test works is that it peeks the same location on both the good and the bad board and compares. Note that if you are using a TRS80 as your "good" board then some of the ROM locations will disagree. You may continue by typing "CONT".

The RAM part of the CPU test pokes data=170 to all 16K of the program RAM and peeks those locations to verify. Then data is set equal to 85 and the process repeats itself. These values are selected because they represent two patterns of alternating "ones" and "zeros" in binary. The entire RAM test takes about 5 minutes. Upon completion the program will respond with "TEST COMPLETE".

The video part of the CPU test first writes to every location. You may observe this by connecting the CRT to the bad board. Afterwards it reads back to verify that the correct information was stored. An occasional error may occur due to noise. A good signal to loop on while accessing the video memory is "CPUACC*" (U139-1).

The KEYBOARD part of the CPU test will loop continuously peeking a keyboard address. For this part of the test you must connect a kybd to the "bad" board. With no keys depressed zero's should be displayed on the CRT. When a key is depressed the value displayed should correspond to a "1" at the data bit which corresponds to that particular key. Refer to the kybd schematic. To escape the KYBD test you must depress the break key on the "good" board.

If there is a failure you may loop at the location of the failure and trigger on the appropiate enabling signal to verify that the data and address are correct. Two sample programs are:

```
1 A=PEEK(-32768):GOTO1
1 POKE -16384,0:GOTO1
```

The 1st program will loop on a read of the 1st location of ROM. The 2nd will loop on a write to the 1st location of RAM with data equal to zero. In the 1st case you should trigger on ROMRD* (U66-6). In the 2nd case, trigger on CAS* (U96-15).

If you have verified that the ROM, RAM, VID RAM, and KYBD sections are good then you may assume that the problem is in the CPU section. All you can do is check to see that all the control lines, address lines, and data lines are functioning. If the CPU is "hanging up", ie. getting locked on a RD*, you may "trick" it by lifting the RD* and MREQ* lines on the Z80A.

"SCOTCH TAPE TRICK"

Sometimes the CPU/CPU test will not work because connecting to the "bad" board causes the good board to hang-up. An example of this would be if any of the critical bus lines were shorted. You may be able to determine which line or lines are causing the problem by covering the 40 pin connector with scotch tape and removing it pin by pin. If removing the scotch tape from a pin causes the good board to hang-up then you may assume that something is either shorted to that line, driving that line, or possibly loading that line down.

HI RESOLUTION GRAPHICS

The HRES GRAPHICS can be tested by running the HRES GRAPHICS TEST on the following page. If the program fails you must troubleshoot the associated circuitry. There is no easy way to loop on the HRES GRAPHICS RAM to see if the address and data are correct. You may allow the test program to continue without stopping by deleting line 220. While the program is running you can check the signals with an oscilloscope to see that they are active. If the program is writing to two or more lines at a time you may assume you have an addressing problem. If no data is being written check the write line. If after running, the CRT does not display an eighty character screen check HRES (55-5). If the test does not fail but the information on the screen seems incorrect check the shift register at U127.

```
10 REM      HIGH RESOLUTION GRAPHICS TEST
20 REM           CASSETTE VERSION
30 CLS
40 PRINT"LNW RESEARCH HRES GRAPHICS TEST"
50 FOR Z=0 TO 1000
60 NEXT Z
70 OUT 254,2
80 FOR X=32512 TO 32533
90 READ D
100 POKE X,D
110 NEXT X
120 POKE 16526.0:POKE 16527,127
125 LET Y=1
130 FOR Z=0 TO 4
140 REM NOW POKE DATA TO BE OUTPUT TO USR ROUTINE
150 POKE 32522,Y
155 GOSUB 170
160 LET Y=Y*2
161 NEXTZ
162 LET Y=0
166 POKE 32522,0
167 GOSUB 170
168 PRINT "ALL MEMORY LOCATIONS TESTED"
169 END
170 FOR X=0 TO 16383
180 A=USR(X)
190 LET A=A AND 63
200 IF A=Y THEN GOTO 230
205 PRINT"MEMORY LOCATION FAILED TO READ OR WRITE
CORRECTLY"
207 PRINT"ADDRESS     EXPECTED DATA     ACTUAL DATA"
210 PRINT X;Y;A
220 STOP
230 NEXT X
240 RETURN
270 DATA 205,127,10,219,254,246,8,211,254,54,0,0,110,38,0
280 DATA 230,247,211,245,195,154,10
```

COLOR GRAPHICS TEST AND ADJUSTMENTS

1.Run "COLOR BAR TEST PROGRAM" and wait for it to complete.
2.Measure the voltage at pin 6 of U146. Record this value, it should be between 1.25 and 1.75 volts.
3.While measuring the voltage at pin 5 of U146 adjust R99 so that the voltage is the same as the recorded value.
4.While measuring the voltage at pin 7 of U146 adjust R98 so that the voltage is the same as the recorded value.
5.Adjust R94 for best picture.Note that this effects the luminance level and be observed at pin 9 of U146. The observed level should be between .75 and 1.1 volts.

```
10 REM          COLOR BAR TEST PROGRAM
20 REM             CASSETTE VERSION
30 REM THIS TEST SHOULD GENERATE THE FOLLOWING COLORS:
35 REM WHITE GREEN YELLOW RED MAGENTA BLUE BLUE-GREEN BLACK
36 CLS:PRINTCHR$(23)
40 PRINT "LNW RESEARCH COLOR BAR TEST"
45 REM DELAY BEFORE STARTING TEST
50 FOR Z=0 TO 1000
60 NEXT Z
70 OUT 254,4
72 FOR X=15360 TO 16383
74 POKE X,255
76 NEXT X
80 FOR X=32512 TO 32533
90 READ D
100 POKE X,D
110 NEXT X
120 POKE 16526,0:POKE 16527,127
125 FOR X=0 TO 12288
130 FOR Y=0 TO 7
135 FOR Z=0 TO 7
150 POKE 32522,Y*9
180 A=USR(X)
190 LET X=X+1
200 NEXT Z
210 NEXT Y
220 LET X=X-1
230 NEXT X
240 END
270 DATA 205,127,10,219,254,246,8,211,254,54,0,0,110,38,0
280 DATA 230,247,211,254,195,154,10
```

TROUBLE-SHOOTING THE EXPANSION INTERFACE

If connecting the expansion interface to the main computer board causes the system to lock up refer to the "SCOTCH TAPE TRICK" in the previous section.

POWER SUPPLY

As stated previously, the first step in trouble-shooting is to verify the power supply. So proceed to verify the following voltages at the following reference points:

REGULATED VOLTAGE	TEST POINT
+5V +/- .3V	JP2,JP4
+12V +/- .5V	JP12
-12V +/- .5V	JP10
-5V +/- .3V	JP8

Note that the -5V supply is critical to the RAMs. If it is not present damage may occur to those parts.

32K MEMORY EXPANSION

The same procedure as used in the CPU/CPU TEST may be used to trouble-shoot the additional 32K of program memory. A sample program to test the memory is:

```
10 Y=170
20 FOR X=-32767 TO -1
30 POKE X,Y
40 A=PEEK(X)
50 IF A=Y THEN NEXT X ELSE 60
51 Y=85:Z=Z+1:IF Z=2 THEN 55 ELSE 20
55 PRINT"TEST COMPLETE":STOP
60 PRINT"LOCATION",X+65536;"ACTUAL",A;"EXPECTED",Y
70 STOP
80 NEXTX
```

Before running this program "set" the memory size to 32767. This will prevent the program from being stored in the upper 32K of memory. If there is a failure you may PEEK or POKE at that location using a simple loop statement. By triggering on CAS* you may verify that the correct address and data are present. Remember that the following relationship exists between the actual location and that poked or peeked:

ACTUAL ADDRESS = POKE OR PEEK ADDRESS + 65536

FLOPPY DISK CONTROLLER

If the FDC is not working, check that the 1MHz clock input to U14-24 is present. Check that when reset MR* (U14-19) goes low. If the motor on the drive does not go on, or if it stays on continuously then the problem may be related to U19 or U7. Note that if the motor stays on continuously the problem is likely to be a reversed floppy cable. By looping on POKE and PEEK statements and checking with an oscilloscope you may verify that the decoder at U19 is operating correctly. Follow the interupt logic from U14-39 to U1-6. Verify that U13 is selecting drive 0 and that U14-23 goes high indicating that the status register is ready. Check the gates of U1, U2, and U6 to see that they're inverting their inputs. Remember that these are 7438's (open collector) and that the outputs must be pulled up by the disk drive.

RS232 HANDSHAKING

To test the handshaking short the following points together on J2:

J2-4 to J2-5 to J2-6
and J2-8 to J2-20 to J2-22

Load the following program:

```
10 FOR Y=0 TO Y=3:OUT234,Y:A=INP(232)
20 PRINT "Y=";Y,"A=";A:NEXTY
30 PRINT"FOR Y=0, A SHOULD BE 0000XXXX BINARY"
40 PRINT"FOR Y=1, A SHOULD BE 1100XXXX BINARY"
50 PRINT"FOR Y=2, A SHOULD BE 0011XXXX BINARY"
60 PRINT"FOR Y=3, A SHOULD BE 1111XXXX BINARY"
```

This program latches data through U26 and back again through U33. OUT234 clocks the data out through U26 and INP(232) clocks it back through U33. Refer to the schematics.

RS232 SEND/RECEIVE

To test or troubleshoot the send/receive functions of the RS232 port load the SERIAL CRT TERMINAL PROGRAM and short E1 to E3. If the serial port is functioning properly then as letters are typed on the keyboard they are routed out through E3 and then back again through E1 and placed on the CRT. If this is not occuring then check U40-25 to see if data is being passed out through the UART. If so then

```
10 REM      SERIAL CRT TERMINAL PROGRAM-CASSETTE VERSION
20 REM
30 REM      THIS PROGRAM ALLOWS THE USE OF THE LNW SYSTEM
40 REM      EXPANSION CIRCUIT BOARD AS A CRT TERMINAL. THIS
50 REM      PROGRAM MAY ALSO BE USED FOR TESTING THE SERIAL
60 REM      INTERFACE BY SHORTING E1 AND E3 TOGETHER
65 REM
70 FOR X=28672 TO 28764
80 READ D
90 POKE X,D
100 NEXT X
110 POKE 16526,0
120 POKE 16527,112
130 A=USR(N)
200 DATA 62,28,205,51,0,62,31,205,51,0,62,14,205,51,0,211
210 DATA 232,219,233,230,248,246,5,211,234,219,234,203,127
220 DATA 40,23,219,235,183,40,18,230,127,254,96,250,45,112
230 DATA 230,95,254,10,40,232,205,51,0,24,227,205,43,0,183
240 DATA 40,221,254,5,242,73,112,33,88,112,79,6,0,9,126
250 DATA 254,26,40,204,79,219,234,203,119,40,249,121,211
260 DATA 235,24,192,3,27,124,127
```

```
10 REM      SERIAL PRINTER DRIVER PROGRAM-CASSETTE VERSION
20 REM
30 REM      THIS PROGRAM ALLOWS THE USE OF A SERIAL PRINTER
40 REM      WITH THE LNW RESEARCH SYSTEM EXPANSION CIRCUIT
50 REM      BOARD. THIS DRIVER PROGRAM IS LEFT IN MEMORY AT A
60 REM      LOCATION WHICH IS UNALTERED BY BASIC AND BY USER
70 REM      PROGRAMS. THE PROGRAM IS EXECUTED DURING EVERY
80 REM      LPRINT AND LLIST FOR EACH CHARACTER TO BE PRINTED
90 REM      HANDSHAKING IS SUPPORTED AS THE SOFTWARE READS
100 REM     THE PRINTER BUSY (DSR) BEFORE OUTPUTING A
110 REM     CHARACTER.  NOTE: IN ORDER FOR THIS PROGRAM TO BE
120 REM     EXECUTED, THE LINE PRINTER CONTROL BLOCK AT HEX
130 REM     4025 TO 4027 MUST BE ALTERED BEFORE PRINTING TO
140 REM     IDENTIFY THE PRINTER TYPE AND DRIVER ADDRESS.
150 REM     THE FOLLOWING LIST GIVES YOU THESE VALUES.
160 REM     16421D   4025H    DCB TYPE            02H 002D
170 REM     16422D   4026H    LSB DRIVER ADDR.    00H 000D
180 REM     16423D   4027H    MSB DRIVER ADDR.    7FH 127D
190 REM
200 FOR X=32512 TO 32560
210 READ D
220 POKE X,D
230 NEXT X
240 POKE 16526,0
250 POKE 16527,127
260 A=USR(N)
300 DATA 245,58,48,127,254,1,40,15,62,1,50,48,127,211,232
310 DATA 219,233,230,248,246,4,211,234,241,219,232,203,119
320 DATA 32,250,121,211,235,254,13,32,4,14,10,24,233,201,0
```

proceed to follow the logic until you're back to U40-20 where the data is received by the UART. If no data is being sent or if the data is not correct then return to LEVEL II BASIC and using IN and OUT commands enable the decoder at U16. Verify with an oscilloscope that the decoder is functioning and that the signals are present at their destination points. Problems may also occur at U23 and U39, especially in relation to incorrect data.

RS232 BAUD RATES

On the LNW80, BAUD RATES may only be controlled through hardware switches. On the factory assembled models this is accomplished through the use of dip switches. If there is any problems in the baud rates first check that no more than one switch is on at a time. In troubleshooting the RS232 check the baud rates with a frequency counter or oscilloscope. Refer to the THEORY OF OPERATIONS for the expected frequencies.

LNDOUBLER 5/8 ALIGNMENT

DO NOT ATTEMPT ALIGNMENT ON AN LNDOUBLER 5/8 WHICH IS UNDER WARRANTY AND APPEARS NOT TO FUNCTION AFTER IT WAS FIRST INSTALLED. ATTEMPTING TO DO SO WILL VOID YOUR 180 DAY LIMITED WARRANTY

Alignment should not be necessary for the life of the LNDOUBLER 5/8 unless the controls have been tampered with or ONE of the following parts has been replaced: VR1, IC15, IC3, IC8, R25, R26, R18, R13, R1, R24, C10.

The LNDOUBLER 5/8 may be returned to the factory for alignment if required. Contact the Service Department for the cost of alignment. For those with the equipment and knowhow to do the alignment, the following procedure should only be done in the event that returning the LNDOUBLER 5/8 is a problem AND the LNDOUBLER 5/8 NEEDS ALIGNMENT!

Equipment Required:
Digital Voltmeter 1% accuracy >1megohm input impedance
Frequency Counter .1% accuracy >1Kohm input >5MHz
Oscilloscope >15MHz bandwidth, triggered

DO NOT ATTEMPT ALIGNMENT IF YOU DO NOT HAVE ALL THE EQUIPMENT LISTED ABOVE!!!

1. Preset the controls and switch settings:
   a. R26- fully counterclockwise
   b. R24- fully clockwise
   c. SW1- "5" position
   d. R25- does not matter

2. Install the LNDOUBLER 5/8 into the expanion interface and apply power to the interface.

3. Adjust R26 for 1.40 volts at IC8 pin 13

4. Adjust R25 for a frequency measurement of 4.00MHz at IC15 pin 7

5. Boot a disk and set up to format a DOUBLE DENSITY DISK. While it is writing to the disk, measure with the oscilloscope a negative true pulse at IC8 pin 4. Adjust R24 for a pulse width of 200ns. This value corresponds to the amount of write precompensation.

DISASSEMBLY/ASSEMBLY

The most important part of disassembling the computer is to be able to put it back together again. This computer has many cables and power connectors and it is vital that they be put back together in the same way as they are taken apart. Great care should be taken. Reversed cables or connectors may cause either unreliable operation, no operation, or even serious damage to electrical and electronic components.

Therefore I strongly advise that some systematic method be used to ensure that the cables and connectors be put back together in the same way as they are taken apart. One method would be to mark both the connector and the circuit board with a permanent marking pen.

REMOVING THE LID

There are 5 screws holding the lid to the chassis, 3 on the back panel and 2 in the front beneath the keyboard. When removing the lid be careful as the LED is connected to the keyboard with wires approximately 8" in length. The LED can be removed from the lid by prying the donut shaped backing off the LED. Then simply push the LED down and remove it.

REMOVING THE KEYBOARD

The KEYBOARD is connected by a 40 pin cable and held in place by 4 screws into the supporting brackets. To remove the 40 pin cable take a firm grip on the plastic part and pull straight back taking care not to bend the pins on the keyboard.

REMOVING THE EXPANSION INTERFACE

The expansion interface is connected by a 40 pin cable and a power connector to the main computer board, and the cables for the RS232 to the chassis. You may remove the EI without disconnecting the RS232 cables, though not completely. There are 4 screws connecting the EI to the supporting rods. Note that only 3 of these screws have lock washers. The forth does not so as to prevent shorting to nearby signals.

REMOVING THE LNDOUBLER 5/8

If you turn the expansion board over you will see a small board plugged into it and tied with plastic tie wraps. This board is the LNDOUBLER 5/8. To remove the doubler you must cut the plastic tie wrap. Then simply pull the doubler straight back being careful not to bend the gold pins beneath.

REMOVING THE LNW80 COMPUTER BOARD

To remove the main computer board you must 1st remove the expansion interface. Then unscrew the 4 cylindrical rods used to support the EI. Note that beneath 3 of these rods there are small nylon spacers. Remove these also. Before you can remove the computer board you must cut the tie wraps holding the large orange capacitor to the case, disconnect the power connector from the transformer, cut the tie wraps on the video connectors, disconnect the video cables, and unsolder or cut the wires connecting to the auto switch on the back panel.

REASSEMBLING THE COMPUTER

If you marked the connectors and paid attention when you disassembled the computer you should have little difficulty in reassembling it. Merely proceed with the above directions in reverse.

ECN's- ENGINEERING CHANGE NOTICES

The following ECN's are not necessary for a functional operating computer. If you have a computer that simply does not operate-ie. garbage appears on the screen-then these changes will not help. These changes have been made to improve operation in various areas. Factory assembled units have had all or most of these changes installed.

These ECN's refer to making jumpers and etch cuts. When making jumpers, use 30 gauge wire (unless otherwise specified) and verify that you are connecting the correct points. When making etch cuts, use a sharp pointed razor knife and be very careful to cut only the etch specified.

It is advisable to make the appropiate changes in the schematics as you install these ECN's. Use a colored ink or pencil so that you can clearly see the ECN changes.

Note: Expansion Board ECN's begin with ECN 2000.

ECN 1000. These changes enable BUS REQUEST for the LNW80.

a. etch cuts

1. U46-5 (solder side)
2. U152-10 (component side)
3. U36-12 (component side, above pin 12)

b. jumpers

1. U18-5 to U97-1
2. U18-7 to U89-3
3. U6-4 to U6-5
4. U36-3 to U152-10

ECN 1001. Purpose: To eliminate jitter in the display.

a. change the following parts:

	PART	FROM:	TO:
1.	U138	74LS174	74S174
2.	U122	74LS157	74S157
3.	U139	74LS157	74S157
4.	U160	74S161	74LS161

b. install the following capacitors:

1. 330pf ceramic from U37-6 to U37-7
2. 47pf ceramic from U138-9 to U138-8

ECN 1002. Purpose: To eliminate screen "hash" from display when reading or writing out of text/graphics RAM or HIRES Graphics RAM.

a. etch cuts

1. U168-6 just above feedthrough below the number "1" of the "U168" (component side).
2. U153-5 (solder side)

b. jumpers

1. U153-6 to U170-11
2. U170-8 to U170-9
3. U170-12 to U170-1
4. U170-13 to U121-12

ECN 1003. Purpose: To reduce "ringing" on the MUX and CAS* lines.

a. install parts

1. Add a 330 ohm resister from U88-1 to GND.
2. Add 100 pf cap at R140 (RAM side) to GND.

ECN 1004. Purpose: To delay GRAS* approximately 20ns allowing DRAD0-DRAD5 to stabilize prior to GRAS* going active.

a. Install 150pf ceramic cap from R83 (right side) to GND.

ECN 1005. Purpose: Ensures that the video wait gets to the Z80.

a. change R143 from 4.7K to 470 ohms

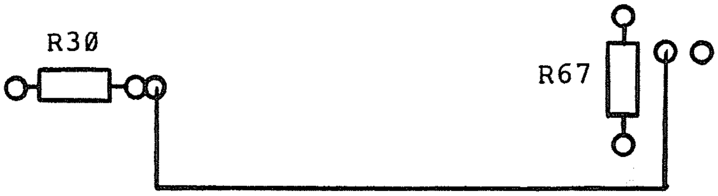
b. remove C138

c. jumper

1. U61-3 to U16-9
2. U16-8 to U29-9

ECN 1006. Purpose: To create a wait state for Disk I/O to increase reliability at high speed.

a. add jumper from feedthrough closet to R67 to feedthrough at R30.



b. cut etch to U73-1 (component side)
cut etch to U74-6 (solder side)

c. jumper U73-1 to U60-7
jumper U74-6 to U74-5

ECN 1007. Purpose: To eliminate double clocking at U156-13 resulting in double vertical display

a. add 220pf ceramic capacitor from U159-12 to U159-14

ECN 1008. Purpose: To eliminate the possibility of heat damage to board due to heat resulting from CR17.

a. remove the Bridge at CR17 from board

b. mount Bridge on case using case chassis as heat sink

c. connect the 9VAC outputs from the transformer directly to the AC inputs of the Bridge

d. connect the "+" output of the bridge to pin 1 of the female molex connector that fits on J5 (use 19 gauge wire)

f. connect the "-" output of the bridge to pin 4 of the female molex connector that fits on J5 (use 19 gauge wire)

g. connect pin 1 of the male molex connector on J5 to the feedthrough marked "+" within the silk-screened area marked for CR17 (use 19 gauge wire)

ECN 1009. Purpose: to avoid ripple on the -12V supply due to heat damage to C131 and C125.

a. remove C131 and C125.

b. install a 220 ufd +- 20% 25VDC with the "-" leg to the "IN" of Q11 and the "+" leg to gnd.

ECN 1010. Purpose: To improve video stability and to remove potentiometers at R98, R99, and R129, thereby eliminating some of the video adjustments in the NTSC color video output.

a. Change the following components:

1. R129 from a 10K pot to 4.7K ohms
2. R98 from a 1K pot to 750 ohms
3. R99 from a 1K pot to 750 ohms
4. R124 from 220 to 10 ohms
5. R94 from a 1K pot to a 2.2K pot
6. R109 from 2K to 1.2K ohms
7. C113 from 220pf to 47pf MICA
8. U119 from 74S04 to 74LS19
9. C84 from 100pf to a 10.738MHz CRYSTAL

NOTE: 10-14 ARE OPTIONAL

10. U122 from 74S157 to 74LS157
11. U121 from 74S74 to 74LS74
12. U124 from 74S74 to 74LS74
13. U160 from 74S161 to 74LS161
14. U161 from 74S161 to 74LS161

b. remove the following parts completely

1. C140, L2, R62, R63, and R67

c. install the following

1. 15pf ceramic capacitor from bottom side of R62 to top side of R63
2. 20K ohms 1/4W 5% from U103-8 to C140 (left side)
3. 6.8 ufd tant. elect. parallel with R110, with the "+" side facing C95.

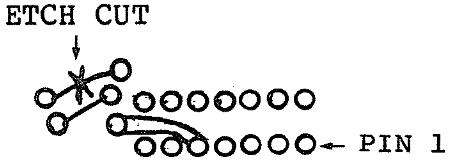
d. cut the etch to U119-12 (solder side).

e. jumper from U1-5 to U103-9.

ECN 2000. Purpose: Reduce noise on RAS*, CAS*, RD*, and MUX and thereby increase memory reliability.

a. Regenerate MUX from RAS*

1. Verify the removal of all termination resisters on J3, also R68, R69, and C14
2. cut etch near U10 (solder side) such that MUX is open circuited from U36-13 to J3-16



U10 (solder side)

3. install the following jumpers:

   from U36-14 to U20-3
   from U36-13 to U20-4

b. Cut etch between the following points:

1. R34 and R46 (near J3)
2. R35 and R47 (near J3)

c. Install the following components:

1. 100pf ceramic cap from U36-6 to U36-10
2. 100pf ceramic cap from U36-15 to U36-10
3. 330pf ceramic cap from U36-8 to U36-10
4. 75 ohm resistor from R34 to R46
5. 75 ohm resistor from R35 to R47

d. Use J3 when connecting from the main computer to the expansion board

RGB OPTION

The following components and jumpers must be installed to obtain the RGB video output.

A. INSTALL THE FOLLOWING COMPONENTS

RGB VIDEO CONNECTOR- 6 pin din jack
U131- 74LS257
U132- 74LS174
U158- RGB ROM
C146- 680 pf ceramic cap(from U129-1 to U129-8)

B. INSTALL THE FOLLOWING JUMPERS

1. USE 24 GAUGE STRANDED WIRE TO CONNECT TO RGB 6 PIN DIN JACK

U162-9 TO RGB-1*	VERTICAL SYNC
U158-1 TO RGB-2	BLUE
U158-6 TO RGB-3	GREEN
U158-4 TO RGB-4	RED
U162-5 TO RGB-5*	HORIZONTAL SYNC
U158-8 TO RGB-6	GROUND

2. USE 30 GAUGE NON-STRANDED WIRE

U20-5 TO U162-3
U118-8 TO U162-5
U162-4 TO U162-9
U68-12 TO U158-14
U68-11 TO U158-13
U130-12 TO U158-12
U130-11 TO U158-11
U130-10 TO U158-10
U158-15 TO U158-8

C. INSTALL THE FOLLOWING RESISTORS

1K ohms from U162-4 to U162-14
1k ohms from U162-6 to U162-14
1k ohms from U162-8 to U162-14

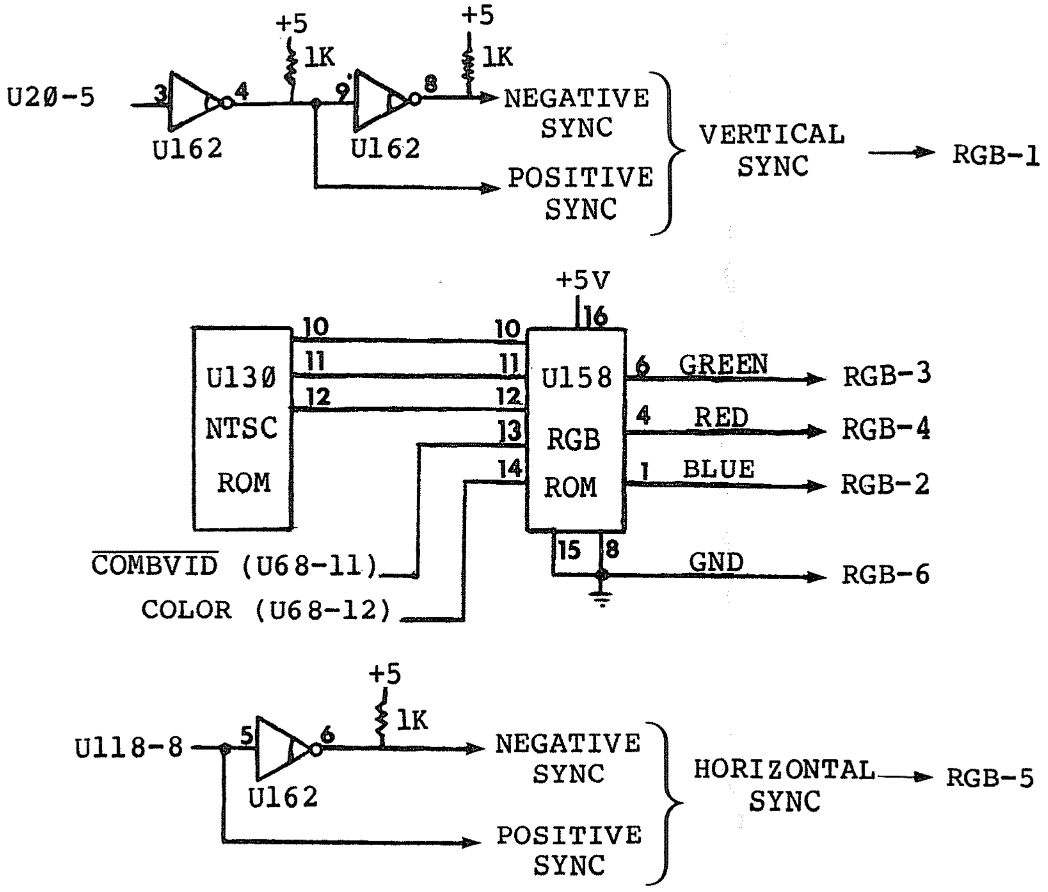
* Note that factory built LNW80's are set up for both positive horizontal and vertical syncs. Negative sync pulses may be obtained by moving the following jumpers:

RGB-1 from U162-9 to U162-8
RGB-5 from U162-5 to U162-6

Because U162 has open collector gates, a combined negative sync may be obtained by setting up for negative syncs and then connecting the sync outputs together.

Because the RGB ROM also has open collector gates it may be necessary to install 330 ohm pull-up resistors on it's outputs, pins 1, 4, and 6. Note that this is only necessary with monitors that do not internally pull up the RED, GREEN, and BLUE lines. This is not necessary with the AMDEC COLOR II RGB MONITOR.

RGB CIRCUIT LOGIC DIAGRAM



PARTS LIST

LNW80 COMPUTER BOARD

SYMBOL	DESCRIPTION	PART NUMBER
	PRINTED CIRCUIT BOARD	97002
	*****INTEGRATED CIRCUITS*****	
U1	74S04	10003
U2	Z80A	10042
U3	74LS244	10061
U4	74LS241	10031
U5	74LS373	10032
U6	74LS138	10020
U7	not used	
U8	74LS175	10028
U9	75452	10036
U10	not used	
U11	not used	
U12	not used	
U13	not used	
U14	not used	
U15	74LS32	10012
U16	74LS05	10006
U17	74LS241	10031
U18	74LS244	10061
U19	74LS11	10009
U20	74C86	10015
U21	TL084	10041
U22	not used	
U23	not used	
U24	not used	
U25	not used	
U26	not used	
U27	not used	
U28	74LS08	10007
U29	74LS08	10007
U30	74LS05	10006
U31	74S74	10014
U32	74LS241	10031
U33	74LS30	10011
U34	74LS240	10030
U35	74LS139	10021
U36	74LS32	10012
U37	74C04	10002
U38	74LS132	10019
U39	not used	
U40	not used	

SYMBOL	DESCRIPTION	PART NUMBER
U41	not used	
U42	not used	
U43	not used	
U44	not used	
U45	not used	
U46	74S74	10014
U47	74S74	10014
U48	74LS04	10004
U49	not used	
U50	74LS04	10004
U51	74LS00	10000
U52	74LS10	10008
U53	74LS244	10061
U54	74LS139	10021
U55	74LS08	10007
U56	not used	
U57	not used	
U58	not used	
U59	not used	
U60	74LS00	10000
U61	74LS02	10001
U62	74LS244	10061
U63	74LS244	10061
U64	not used	
U65	74LS244	10061
U66	74LS32	10012
U67	74LS175	10028
U68	74LS02	10001
U69	not used	
U70	not used	
U71	not used	
U72	not used	
U73	74LS138	10020
U74	74LS30	10011
U75	ROM A1	10040
U76	ROM B1	10040
U77	ROM C1	10040
U78	ROM A	10040
U79	ROM B	10040
U80	ROM C	10040
U81	74LS08	10007
U82	74LS86	10016
U83	74LS153	10022
U84	74166	10026
U85	74LS10	10008
U86	SPARE	
U87	74S161	10025
U88	74LS157	10023
U89	4116 (200ns)	10039
U90	4116 (200ns)	10039
U91	4116 (200ns)	10039

SYMBOL	DESCRIPTION	PART NUMBER
U92	4116 (200ns)	10039
U93	4116 (200ns)	10039
U94	4116 (200ns)	10039
U95	4116 (200ns)	10039
U96	4116 (200ns)	10039
U97	74LS157	10023
U98	74LS374	10033
U99	74LS373	10032
U100	2716 CHAR GEN	10065
U101	74166	10026
U102	74LS20	10010
U103	74S175	10029
U104	74S74	10014
U105	74LS157	10023
U106	4116 (200ns)	10039
U107	4116 (200ns)	10039
U108	4116 (200ns)	10039
U109	4116 (200ns)	10039
U110	4116 (200ns)	10039
U111	4116 (200ns)	10039
U112	74LS157	10023
U113	SPARE	
U114	2114 (450ns)	10063
U115	2114 (450ns)	10063
U116	74LS174	10027
U117	74LS174	10027
U118	74LS04	10004
U119	74S04	10003
U120	74LS123	10018
U121	74S74	10014
U122	74S157	10044
U123	not used	
U124	74S74	10014
U125	74LS373	10032
U126	74LS174	10027
U127	74166	10026
U128	74LS174	10027
U129	74LS257	10045
U130	NTSC COLOR ROM	10046
U131	not used	
U132	not used	
U133	74123	10017
U134	not used	
U135	not used	
U136	not used	
U137	74LS04	10004
U138	74S174	10043
U139	74S157	10044
U140	74LS157	10023
U141	74LS374	10033
U142	74LS157	10023
U143	74LS374	10033

SYMBOL	DESCRIPTION	PART NUMBER
U144	74LS157	10023
U145	74LS157	10023
U146	MC1372	10037
U147	not used	
U148	not used	
U149	not used	
U150	not used	
U151	74LS32	10012
U152	74LS32	10012
U152	74LS32	10012
U153	74LS74	10013
U154	74LS20	10010
U155	74S74	10014
U156	74LS393	10035
U157	SPARE	
U158	RGB ROM (optional)	10049
U159	74LS10	10008
U160	74LS161	10024
U161	74S161	10025
U162	7405	10005
U163	not used	
U164	not used	
U165	not used	
U166	not used	
U167	74LS161	10024
U168	74LS08	10007
U169	74LS11	10009
U170	74LS02	10001
U171	74LS32	10012
U172	SPARE	

****RESISTORS (1/4 watt, 5% unless otherwise indicated)****

R1	150 ohm	20007
R2	680	20030
R3	4.7K	20036
R4	680	20030
R5	4.7K	20036
R6	4.7K	20036
R7	220	20010
R8	220	20010
R9	4.7K	20036
R10	1K	20016
R11	1K	20016
R12	10K	20021
R13	1K	20016
R14	4.7K	20036
R15	1K	20016
R16	330	20012
R17	120	20006
R18	1.8K	20033

SYMBOL	DESCRIPTION	PART NUMBER
R19	270	20027
R20	10K	20021
R21	75	20004
R22	47	20003
R23	100	20005
R24	1K	20016
R25	180	20009
R26	not used	
R27	20K	20022
R28	3.6K	20019
R29	1K	20016
R30	4.7K	20036
R31	10	20025
R32	10K	20021
R33	1.2K	10017
R34	7.5K	20020
R35	7.5K	20020
R36	1K	20016
R37	220K	20024
R38	20K	20022
R39	20K	20022
R40	1.8K	20033
R41	4.7K	20036
R42	3K	20035
R43	10	20025
R44	20K	20022
R45	4.7K	20036
R46	10K	20021
R47	4.7K	20036
R48	10K	20021
R49	10K	20021
R50	33	20026
R51	33	20026
R52	4.7K	20036
R53	10K	20021
R54	10K	20021
R55	33	20026
R56	33	20026
R57	1K	20016
R58	33	20026
R59	33	20026
R60	33	20026
R61	33	20026
R62	150	20007
R63	470	20014
R64	200K	20023
R65	33	20026
R66	33	20026
R67	470	20014
R68	4.7K	20036
R69	100	20005

SYMBOL	DESCRIPTION	PART NUMBER
R70	33	20026
R71	33	20026
R72	33	20026
R73	33	20026
R74	33	20026
R75	1K	20016
R76	33	20026
R77	33	20026
R78	1K	20016
R79	1K	20016
R80	56K	20038
R81	1K	20016
R82	1K	20016
R83	33	20026
R84	1K	20016
R85	910	20032
R86	470	20014
R87	270	20027
R88	910	20032
R89	270	20027
R90	910	20032
R91	390	20029
R92	1.2K	20017
R93	470	20014
R94	1K POT	21000
R95	470	20014
R96	1K	20016
R97	220	20010
R98	1K POT	21000
R99	1K POT	21000
R100	470	20014
R101	470	20014
R102	470	20014
R103	470	20014
R104	470	20014
R105	1.5K	20018
R106	5.6K	20037
R107	4.7K	20036
R108	360	20028
R109	2K	20034
R110	47	20003
R111	470	20014
R112	75	20004
R113	not used	
R114	not used	
R115	1.5K	20018
R116	3.6K	20019
R117	750	20031
R118	330	20012
R119	not used	

SYMBOL	DESCRIPTION	PART NUMBER
R120	not used	
R121	not used	
R122	not used	
R123	1K	20016
R124	220	20010
R125	not used	
R126	not used	
R127	not used	
R128	not used	
R129	10K POT	21001
R130	1K	20016
R131	100	20005
R132	1K	20016
R133	430	20013
R134	3.3 ohm 1 watt	20002
R135	1K	20016
R136	33	20026
R137	1K	20016
R138	1 ohm 1 watt	20001
R139	150 ohm 1 watt	20008
R140	100	20005
R141	1K	20016
R142	1K	20016
R143	4.7K	20036
R144	50K POT	21003
R145	100K POT	21004
****CAPACTORS (CERAMIC 25V+- 20% UNLESS OTHERWISE NOTED****		
C1	47pf	30000
C2	.1ufd	30010
C3	.1ufd	30010
C4	.1ufd	30010
C5	.1ufd	30010
C6	.1ufd	30010
C7	.1ufd	30010
C8	10ufd ELECT. 15VDC, AXIAL MOUNT	32002
C9	.01ufd	30009
C10	.01ufd	30009
C11	.1ufd	30010
C12	.1ufd	30010
C13	.1ufd	30010
C14	.1ufd	30010
C15	.1ufd	30010
C16	.1ufd	30010
C17	.1ufd	30010
C18	.1ufd	30010
C19	.1ufd	30010
C20	.1ufd	30010
C21	.001ufd POLY FILM	30100
C22	.022ufd MYLAR 25V	30101

SYMBOL	DESCRIPTION	PART NUMBER
C23	.047ufd MYLAR	30103
C24	.001ufd POLY FILM	30100
C25	.1ufd	30010
C26	.1ufd	30010
C27	.1ufd	30010
C28	.1ufd	30010
C29	.1ufd	30010
C30	.1ufd	30010
C31	.1ufd	30010
C32	.1ufd	30010
C33	.1ufd	30010
C34	6.8ufd TANTALUM ELECT 15V	32001
C35	.1ufd	30010
C36	.1ufd	30010
C37	.1ufd	30010
C38	.1ufd	30010
C39	.1ufd	30010
C40	.1ufd	30010
C41	6.8ufd TANTALUM ELECT 15V	32001
C42	.1ufd	30010
C43	.1ufd	30010
C44	.1ufd	30010
C45	.1ufd	30010
C46	.1ufd	30010
C47	6.8ufd T.E. 15V	32001
C48	.1ufd	30010
C49	.1ufd	30010
C50	.1ufd	30010
C51	.1ufd	30010
C52	.1ufd	30010
C53	.1ufd	30010
C54	.1ufd	30010
C55	.1ufd	30010
C56	6.8ufd T.E. 15V	32001
C57	.1ufd	30010
C58	.1ufd	30010
C59	.1ufd	30010
C60	6.8ufd T.E. 15V	32001
C61	.1ufd	30010
C62	.1ufd	30010
C63	.1ufd	30010
C64	.1ufd	30010
C65	6.8ufd T.E.15V	32001
C66	.1ufd	30010
C67	33ufd ELECT AXIAL MOUNT 15V	32006
C68	330pf	30007
C69	.1ufd	30010
C70	6.8ufd T.E. 15V	32001
C71	.1ufd	30010
C72	.1ufd	30010
C72	.1ufd	30010
C73	.1ufd	30010
C74	.1ufd	30010

SYMBOL	DESCRIPTION	PART NUMBER
C75	.1ufd	30010
C76	6.8ufd T.E. 15V	32001
C77	.1ufd	30010
C78	.1ufd	30010
C79	.1ufd	30010
C80	.1ufd	30010
C81	.1ufd	30010
C82	.1ufd	30010
C83	150pf	30005
C84	100pf MICA +-5%	30004
C85	.1ufd	30010
C86	.1ufd	30010
C87	.1ufd	30010
C88	.1ufd	30010
C89	.1ufd	30010
C90	.1ufd	30010
C91	.1ufd	30010
C92	.1ufd	30010
C93	not used	
C94	50pf MICA +-5% 25V	30002
C95	9-35pf VARIABLE CAP	33000
C96	.1ufd	30010
C97	.1ufd	30010
C98	.1ufd	30010
C99	.1ufd	30010
C100	.1ufd	30010
C101	.1ufd	30010
C102	not used	
C103	not used	
C104	.1ufd	30010
C105	not used	
C106	not used	
C107	not used	
C108	.1ufd	30010
C109	.1ufd	30010
C110	.1ufd	30010
C111	.1ufd	30010
C112	not used	
C113	220pf	30006
C114	.1ufd	30010
C115	not used	
C116	.1ufd	30010
C117	not used	
C118	6.8ufd T.E. 15V	32001
C119	4.7ufd ELECT 15V	32000
C120	10ufd ELECT 15V	32003
C121	2200ufd 25V ELECT AXIAL	32009
C122	6.8ufd T.E. 15V	32001
C123	6.8ufd T.E. 15V	32001
C124	.1ufd	30010
C125	22ufd TANTALUM ELECT 20V	32005
C126	.1ufd	30010

SYMBOL	DESCRIPTION	PART NUMBER
C127	6.8ufd T.E. 15V	32001
C128	6.8ufd T.E. 15V	32001
C129	6.8ufd T.E. 15V	32001
C130	.1ufd	30010
C131	100ufd ELECT 16V	32007
C132	6.8ufd T.E. 15V	32001
C133	6.8ufd T.E. 15V	32001
C134	6.8ufd T.E. 15V	32001
C135	.1ufd	30010
C136	22ufd ELECT 15V	32004
C137	100ufd ELECT 25V	32008
C138	150pf	30008
C139	470pf	30008
C140	9-35pf VAR CAP	33000
C141	15000ufd ELECT 15V	32030
C142	not used	
	*****MISCELLANEOUS SEMICONDUCTORS*****	
Q1	2N3904	11000
Q2	2N3906	11001
Q3	7805 5V REGUL	11005
Q4	7812 12V REGUL	11006
Q5	not used	
Q6	MPU131	11002
Q7	7805 5V REGUL	11005
Q8	7805 5V REGUL	11005
Q9	7805 5V REGUL	11005
Q10	7805 5V REGUL	11005
Q11	79L12 -12V .1A REG	11007
Q12	MPU131	11002
Q13	2N3906	11001
Q14	2N3904	11000
Q15	not used	
Q16	not used	
Q17	not used	
Q18	J175 (NATIONAL) FET	11004
SCR1	4A 50VRMS SCR (R/S NO 276-1067)	11100
SCR2	4A 50VRMS SCR	11100
CR1	1N4001 1A 50PIV	11101
CR2	1N914 SILICON SIG 75PIV	11102
CR3	not used	
CR4	1N914	11102
CR5	1N914	11102
CR6	1N914	11102
CR7	1N914	11102
CR8	1N914	11102
CR9	1N914	11102
CR10	1N914	11102
CR11	14V ZENER 1N5244	11106
CR12	1N4001	11101

SYMBOL	DESCRIPTION	PART NUMBER
CR13	1N4001	11101
CR14	5.1V ZENER 1N5231	11103
CR15	BRIDGE 50V 2A	11108
CR16	1N4001	11101
CR17	BRIDGE 50V 4A	11107
CR18	not used	
CR19	1N4001	11101
CR20	1N4001	11101
CR21	1N4001	11101
CR22	1N4001	11101
CR23	1N4001	11101
CR24	6.2V ZENER 1N5234	11104
	*****IC SOCKETS*****	
	14 PIN LOW PROFILE	40001
	16 PIN LOW PROFILE	40002
	18 PIN LOW PROFILE	40003
	20 PIN LOW PROFILE	40004
	24 PIN LOW PROFILE	40005
	40 PIN LOW PROFILE	40006
	40 PIN MACHINE	40500
	*****MISCELLANEOUS*****	
L2	.56 uH INDUCTOR	37000
CASSETTE JACK	5 COND DIN RT ANGLE PC	42000
J6	2 COND MOLEX HDR	43000
J2	6 COND MOLEX HDR	43001
J5	6 COND HDR .156 R/A AMP	43003
HI-RES B/W VIDEO	2 COND MOLEX HDR	43000
J4	2X20 MALE HDR .1 AP	43700
SW1	SWITCH SPST 5A 220V CHA	45010
K1	5VDC RELAY	45500
F1	4A FAST BLO 32V	47001
F2	2A FAST BLO 32V	47002
	HEATSINK T0220 5306B-13	69000
	HEATSINK T0220 5307B-14	69001
Y1	16.0 MHz CRYSTAL	35001
Y2	3.579 MHz CRYSTAL	35002
	10.738 MHz CRYSTAL	35003

PARTS LIST

LNW EXPANSION INTERFACE

SYMBOL	DESCRIPTION	PART NUMBER
	PRINTED CIRCUIT BOARD	97012
****RESISTORS (1/4 watt, 5% unless otherwise indicated)****		
R1	not used	
R2	not used	
R3	not used	
R4	not used	
R5	not used	
R6	not used	
R7	not used	
R8	not used	
R9	not used	
R10	not used	
R11	not used	
R12	10K	20021
R13	10K	20021
R14	1K	20016
R15	200K	20023
R16	150	20007
R17	150	20007
R18	150	20007
R19	150	20007
R20	4.7K	20036
R21	4.7K	20036
R22	20K	20022
R23	not used	
R24	not used	
R25	not used	
R26	not used	
R27	150	20007
R28	680	20030
R29	680	20030
R30	1K	20016
R31	1K	20016
R32	not used	
R33	not used	
R34	not used	
R35	not used	
R36	not used	
R37	not used	
R38	not used	
R39	not used	
R40	not used	
R41	not used	

SYMBOL	DESCRIPTION	PART NUMBER
R42	not used	
R43	not used	
R44	not used	
R45	not used	
R46	not used	
R47	not used	
R48	not used	
R49	not used	
R50	not used	
R51	not used	
R52	not used	
R53	not used	
R54	not used	
R55	not used	
R56	not used	
R57	not used	
R58	100	20005
R59	100	20005
R60	100	20005
R61	100	20005
R62	100	20005
R63	100	20005
R64	100	20005
R65	100	20005
R66	33	20026
R67	not used	
R68	not used	
R69	not used	

******CAPACITORS (all caps are 25VDC +-20% unless otherwise indicated)******

SYMBOL	DESCRIPTION	PART NUMBER
C1	not used	
C2	not used	
C3	not used	
C4	not used	
C5	not used	
C6	not used	
C7	not used	
C8	not used	
C9	not used	
C10	not used	
C11	not used	
C12	33 ufd ELECT AXIAL 6VDC	32006
C13	220 PF CERAMIC	30006
C14	not used	
C15	47 PF CERAMIC	30000
C16	.1 ufd CERAMIC	30010
C17	.1 ufd CERAMIC	30010
C18	.1 ufd CERAMIC	30010
C19	.1 ufd CERAMIC	30010
C20	.1 ufd CERAMIC	30010
C21	.1 ufd CERAMIC	30010

SYMBOL	DESCRIPTION	PART NUMBER
C22	.1 ufd CERAMIC	30010
C23	.1 ufd CERAMIC	30010
C24	.1 ufd CERAMIC	30010
C25	.1 ufd CERAMIC	30010
C26	.1 ufd CERAMIC	30010
C27	.1 ufd CERAMIC	30010
C28	.1 ufd CERAMIC	30010
C29	.1 ufd CERAMIC	30010
C30	.1 ufd CERAMIC	30010
C31	.1 ufd CERAMIC	30010
C32	.1 ufd CERAMIC	30010
C33	.1 ufd CERAMIC	30010
C34	6.8 ufd TANTALUM	32001
C35	6.8 ufd TANTALUM	32001
C36	.1 ufd CERAMIC	30010
C37	6.8 ufd TANTALUM	32001
C38	.1 ufd CERAMIC	30010
C39	6.8 ufd TANTALUM	32001
C40	.1 ufd CERAMIC	30010
C41	6.8 ufd TANTALUM	32001
C42	.1 ufd CERAMIC	30010
C43	.1 ufd CERAMIC	30010
C44	.1 ufd CERAMIC	30010
C45	.1 ufd CERAMIC	30010
C46	.1 ufd CERAMIC	30010
C47	.1 ufd CERAMIC	30010
C48	.1 ufd CERAMIC	30010
C49	.1 ufd CERAMIC	30010
C50	.1 ufd CERAMIC	30010
C51	.1 ufd CERAMIC	30010
C52	.1 ufd CERAMIC	30010
C53	6.8 ufd TANTALUM	32001
C54	.1 ufd CERAMIC	30010
C55	6.8 ufd TANTALUM	32001
C56	.1 ufd CERAMIC	30010
C57	6.8 ufd TANTALUM	32001
C58	.1 ufd CERAMIC	30010
C59	6.8 ufd TANTALUM	32001
C60	not used	
C61	.1 ufd CERAMIC	30010
C62	.1 ufd CERAMIC	30010
C63	.1 ufd CERAMIC	30010
C64	not used	
C65	6.8 ufd TANTALUM	32001
C66	not used	
C67	not used	

SYMBOL	DESCRIPTION	PART NUMBER
	*****INTEGRATED CIRCUITS*****	
U1	7438	10064
U2	7438	10064
U3	74LS367	10054
U4	74LS175	10028
U5	74LS175	10028
U6	7438	10064
U7	74LS123	10018
U8	74LS240	10030
U9	7492	10051
U10	7493	10052
U11	74LS08	10007
U12	7490	10050
U13	74LS175	10028
U14	FD1771B-01	10059
U15	74LS240	10030
U16	74LS155	10053
U17	7493	10052
U18	74S04	10003
U19	74LS155	10053
U20	74LS14	10047
U21	74LS74	10013
U22	74LS74	10013
U23	74LS08	10007
U24	74163	10066
U25	74163	10066
U26	74LS175	10028
U27	not used	
U28	74LS367	10054
U29	74S32	10048
U30	74LS139	10021
U31	74LS30	10011
U32	74LS14	10047
U33	74LS367	10054
U34	74LS244	10061
U35	74LS244	10061
U36	74LS244	10061
U37	74LS241	10031
U38	74LS241	10031
U39	74LS244	10061
U40	TR1602-B	10062
U41	74LS30	10011
U42	4116 200ns	10039
U43	4116 200ns	10039
U44	4116 200ns	10039
U45	4116 200ns	10039
U46	4116 200ns	10039
U47	4116 200ns	10039
U48	4116 200ns	10039
U49	4116 200ns	10039

SYMBOL	DESCRIPTION	PART NUMBER
U50	not used	
U51	1489 EIA RECEIVER	10056
U52	1489 EIA RECEIVER	10056
U53	4116 200ns	10039
U54	4116 200ns	10039
U55	4116 200ns	10039
U56	4116 200ns	10039
U57	4116 200ns	10039
U58	4116 200ns	10039
U59	4116 200ns	10039
U60	4116 200ns	10039
U61	1488 EIA DRIVER	10055
U62	not used	
U63	not used	
U64	not used	
U65	not used	
U66	not used	
	*****MISCELLANEOUS*****	
Y1	4.000 MHZ CRYSTAL	35000
U40	40 PIN DIP IC SOCKET	40006
U14	40 PIN MACHINE SOCKET	40500
	DIP SWITCH 6 POS	45100
	DIP SWITCH 8 POS	45101
	CABLE 16C 12" HDR-WIRE	85100
	PCB RS232 CONFIG FOR SE	97042
	CONNECTOR 25 PIN D TYPE	42500
	SOCKETS FOR RS232 CONN	43255
	WIRE 24 AWG STRANDED	86500
	6 COND MOLEX CONNECTOR	43501
	MOLEX PINS	43250
	18 GA. PVC WIRE	85002

PARTS LIST

LNDOUBLER 5/8

SYMBOL	DESCRIPTION	PART NUMBER
	PRINTED CIRCUIT BOARD	97067
	****RESISTORS (1/4 Watt, 5%)****	
R1	2K	20034
R2	4.7K	20036
R3	not used	
R4	4.7K	20036
R5	1.0K	20016
R6	10K	20021
R7	4.7K	20036
R8	not used	
R9	680	20030
R10	150	20007
R11	1.0K	20016
R12	1.0K	20016
R13	47K	20040
R14	4.7K	20036
R15	4.7K	20036
R16	4.7K	20036
R17	not used	
R18	47K	20040
R19	47	20003
R20	10K	20021
R21	4.7K	20036
R22	not used	
R23	10K	20021
R24	10K MINI PC MINI POT	21001
R25	50K MULTITURN POT	21006
R26	100K MINI PC POT	21005
	******CAPACITORS******	
C1	.1 ufd ceramic	30010
C2	.1 ufd ceramic	30010
C3	6.8ufd TANT ELECT 15V	32001
C4	.1 ufd ceramic	30010
C5	.1 ufd ceramic	30010
C6	not used	
C7	47 pf MICA +- 5%	30001
C8	6.8 TANT ELECT 15V	32001
C9	47 pf ceramic	30000
C10	47 pf MICA +- 5%	30001
C11	.1 ufd ceramic	30010
C12	.47 ufd MYLAR	31999
C13	not used	
C14	.1 ufd ceramic	30010
C15	.1 ufd ceramic	30010
"R8"	47 pf ceramic	30000

*****INTEGRATED CIRCUITS*****

U1	74LS27	10057
U2	74LS08	10007
U3	WD2143	10068
U4	74LS123	10018
U5	74LS05	10006
U6	74LS05	10006
U7	74LS00	10000
U8	WD1691	10067
U9	MB8876 (FUJ-1791 COM)	10060
U10	40 PIN SOCKET	40006
U11	74LS157	10023
U12	74LS04	10004
U13	74LS158	10034
U14	74LS74	10013
U15	74LS629	10069
U16	74LS74	10013
U17	74LS74	10013
U18	74LS08	10007

*****MISCELLANEOUS*****

Y1	4.0 MHZ CRYSTAL	35000
	20 PIN SOCKET STRIP(2)	41000
SW1	SPDT SW R/A PC MNT	45000

PARTS LIST

CASE ASSEMBLY

SYMBOL	DESCRIPTION	PART NUMBER
	KEYBOARD	45002
	LED RED	12000
	TRANSFORMER LNW80	55000
	SHIELDED CABLE	85000
	KEYBOARD CABLE	85001
	LNW80 CASE TOP PANEL	60002
	LED BEZEL	12050
	KYBD BRACKET LEFT	65013
	KYBD BRACKET RIGHT	65012
	FAN 3" ROTRON SPRITE	80000
	LNW80 CASE BOTTOM PANEL	60000
	LNW80 CASE REAR PANEL	60005
	PHONO PLUG CHASSIS MNT	42300
	FUSE HOLDER CHASSIS MNT	44000
	SWITCH SPST 5A 220V	45010
	1/2A SLOBLO FUSE 220V	47006
	STRAIN RELIEF FOR LCORD	48700
	CORD PWR LINE 120V	82000
	RUBBER BUMPER	78000
	TERMINAL STRIP 5 POS GND	43900
	LNW80 CASE SUPPORT BRK	65010
	6 COND MOLEX CONNECTOR	43501
	2 COND MOLEX CONNECTOR	43500
	MOLEX PINS (9)	43250
	COAX WIRE RG174/U	86550
	24 GAUGE WIRE STRANDED	86500
	20 GAUGE WIRE STRANDED	86510
	WIRE TIES 3.5"	48710
	SHRINK TUBING 1/4"	49000
	SHRINK TUBING 3/8"	49001
	4-40 NUT	71000
	4-40 INTERNAL TOOTH WASHER	73000
	4-40x3/4 MACHINE SCREW	70000
	4-40x1/4 MACHINE SCREW	70001
	4-40x1/2 NYL SPACER	72202
	4-40 X 1/4 RND PH SPCR	72000
	4-40x 1.5 RND SPACER	72200
	4-40 1/8 NYLON SPACER	72100
	#6-32 NUT	71001
	#6-32 X 1/4 SHT MTL SCREW	70004
	#6 INTERNAL TOOTH WASH	73001
	#6 FLAT WASHER	73005
	6-32 X 3/8 MASH SCREW	70003
	6-32 X 3/8 NYLON SCREW	70005
	6-32 NYL NUT	71002

APPENDIX 1 DATA SHEETS

THE FOLLOWING DATA SHEETS ARE REPRINTED WITH THE PERMISSION OF WESTERN DIGITAL, ZILOG, MOTOROLA, AND TEXAS INSTRUMENTS, AND MAY NOT BE REPRODUCED IN ANY FORM WITHOUT THEIR EXPRESSED WRITTEN PERMISSIONS.

DATA SHEET INDEX

MOTOROLA

MCM2114
MCM21L14

4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM2114 is a 4096-bit random access memory fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of fully static operation. Data access is particularly simple, since address setup times are not required. The data out has the same polarity as the input data.

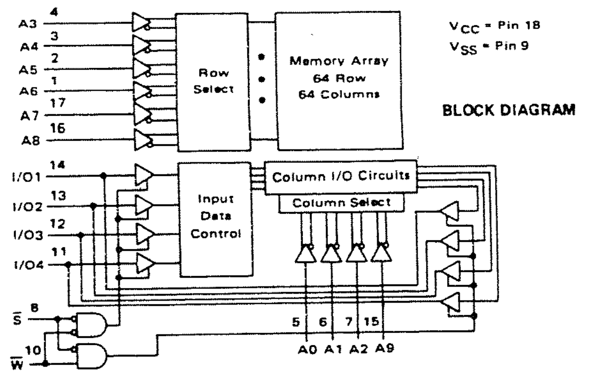
The MCM2114 is designed for memory applications where simple interfacing is the design objective. The MCM2114 is assembled in 18-pin dual in-line packages with the industry standard pin-out. A separate chip select ($\overline{S}$) lead allows easy selection of an individual package when the three-state outputs are OR-tied.

The MCM2114 series has a maximum power dissipation of 525 mW. Low power versions (i.e., MCM21L14 series) are available with a maximum power dissipation of less than 370 mW.

- 1024 Words by 4-Bit Organization
- Industry Standard 18-Pin Configuration
- Single +5 Volt Supply
- No Clock or Timing Strobe Required
- Fully Static: Cycle Time = Access Time
- Fully TTL/DTL Compatible
- Common Data Input and Output
- Three-State Outputs for OR-Ties
- Low Power Version Available — 370 mW (Max)

MAXIMUM ACCESS TIME/MINIMUM CYCLE TIME

MCM2114-20 MCM21L14-20	200 ns	MCM2114-30 MCM21L14-30	300 ns
MCM2114-25 MCM21L14-25	250 ns	MCM2114-45 MCM21L14-45	450 ns

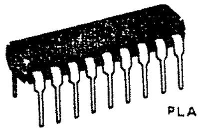


BLOCK DIAGRAM

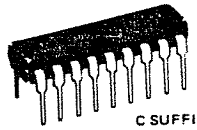
MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

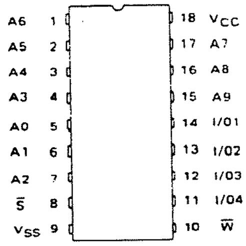


P SUFFIX
PLASTIC PACKAGE
CASE 707



C SUFFIX
FRIT SEAL
CERAMIC PACKAGE
CASE 701

PIN ASSIGNMENT



PIN NAMES

A0-A9	Address Input
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
I/O1 - I/O4	Data Input/Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Value	Unit
Temperature Under Bias	-10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	-0.5 to +7.0	Vdc
DC Output Current	5.0	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

Note: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5.0 V ± 5% unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	MCM2114			MCM21L14			Unit
		Min	Nom	Max	Min	Nom	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{LI}	–	–	10	–	–	10	μA
I/O Leakage Current ($\overline{S}$ = 2.4 V, $V_{I/O}$ = 0.4 V to V_{CC})	$\lvert I_{LO} \rvert$	–	–	10	–	–	10	μA
Power Supply Current (V_{in} = 5.5, $I_{I/O}$ = 0 mA, T_A = 25°C)	I_{CC1}	–	80	95	–	–	65	mA
Power Supply Current (V_{in} = 5.5 V, $I_{I/O}$ = 0 mA, T_A = 0°C)	I_{CC2}	–	–	100	–	–	70	mA
Input Low Voltage	V_{IL}	-0.5	–	0.8	-0.5	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	6.0	2.0	–	6.0	V
Output Low Current V_{OL} = 0.4 V	I_{OL}	2.1	6.0	–	2.1	6.0	–	mA
Output High Current V_{OH} = 2.4 V	I_{OH}	–	-1.4	-1.0	–	-1.4	-1.0	mA
Output Short Circuit Current	I_{OS} (2)	–	–	40	–	–	40	mA

Note: 2. Duration not to exceed 30 seconds.

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Input/Output Capacitance ($V_{I/O}$ = 0 V)	$C_{I/O}$	5.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

Input Pulse Levels	0.8 Volt to 2.4 Volts
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5 Volts
Output Load	1 TTL Gate and C_L = 100 pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

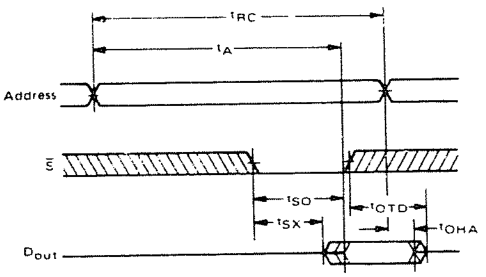
Read (Note 3), Write (Note 4) Cycles

RECOMMENDED AC OPERATING CONDITIONS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 5%)

Parameter	Symbol	MCM2114-20 MCM21L14-20		MCM2114-25 MCM21L14-25		MCM2114-30 MCM21L14-30		MCM2114-45 MCM21L14-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200	–	250	–	300	–	450	–	ns
Access Time	t_A	–	200	–	250	–	300	–	450	ns
Chip Selection to Output Valid	t_{SO}	–	70	–	85	–	100	–	120	ns
Chip Selection to Output Active	t_{SX}	20	–	20	–	20	–	20	–	ns
Output 3 State From Deselection	t_{OTD}	–	60	–	70	–	80	–	100	ns
Output Hold From Address Change	t_{OHA}	50	–	50	–	50	–	50	–	ns
Write Cycle Time	t_{WC}	200	–	250	–	300	–	450	–	ns
Write Time	t_W	120	–	135	–	150	–	200	–	ns
Write Release Time	t_{WR}	0	–	0	–	0	–	0	–	ns
Output 3-State From Write	t_{OTW}	–	60	–	70	–	80	–	100	ns
Data to Write Time Overlap	t_{DW}	120	–	135	–	150	–	200	–	ns
Data Hold From Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns

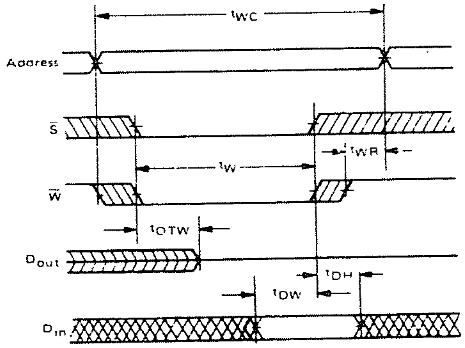
Notes: 3. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.
4. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

READ CYCLE TIMING (Note 5)



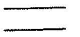
Notes: 5. $\overline{W}$ is high for a Read cycle

WRITE CYCLE TIMING (Note 6)



6. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transition, the output buffers remain in a high impedance rate.

WAVEFORMS

Waveform Symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

WESTERN DIGITAL
C O R P O R A T I O N

MOS/LSI

TR1602A & TR1602B

ASYNCHRONOUS RECEIVER/TRANSMITTER

WESTERN DIGITAL CORPORATION • 19242 RED HILL AVENUE • NEWPORT BEACH, CALIFORNIA 92663 • (714) 557-3550

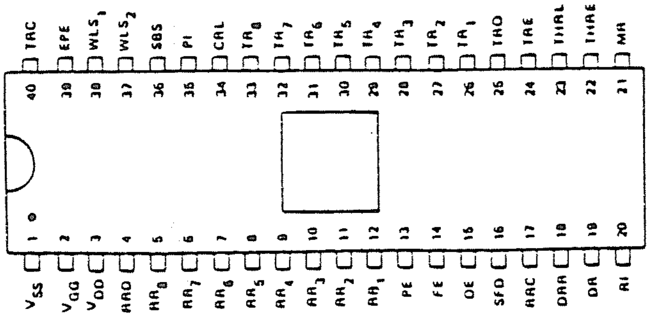
FEATURES

- SILICON GATE TECHNOLOGY — LOW THRESHOLD CIRCUITRY
  Directly TTL and DTL Compatible — External Resistors Eliminated
- D. C. STABLE (STATIC) CIRCUITRY
- FULL DUPLEX OR HALF DUPLEX OPERATION
  Transmits And Receives Serial Data Simultaneously Or Alternately
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- BUFFERED RECEIVER AND TRANSIMITTER REGISTERS
- FULLY PROGRAMMABLE — EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  Parity Inhibit — Verification/Generation
  One, One and One-Half, or Two Stop Bit Generation
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- AVAILABLE IN CERAMIC OR HERMETIC PLASTIC CAVITY PACKAGES

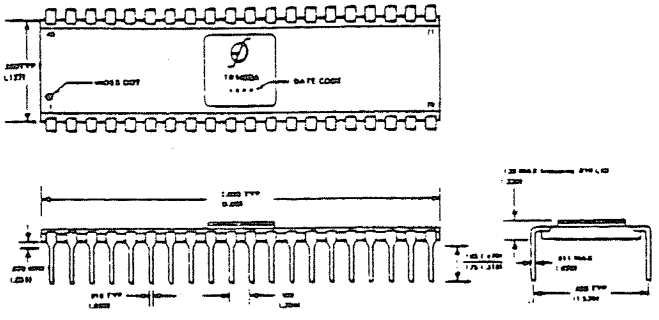
APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES

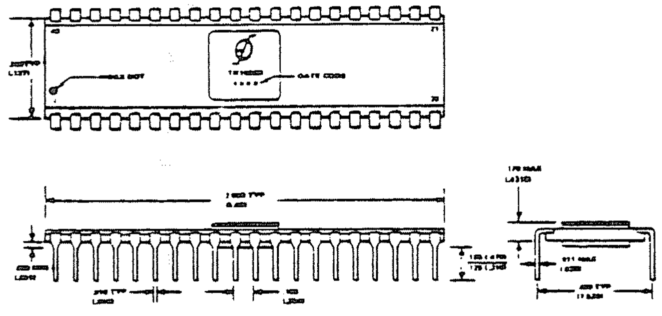
PIN CONNECTIONS



TR1602A CERAMIC PACKAGE OUTLINE



TR1602B HERMETIC PLASTIC CAVITY PACKAGE OUTLINE

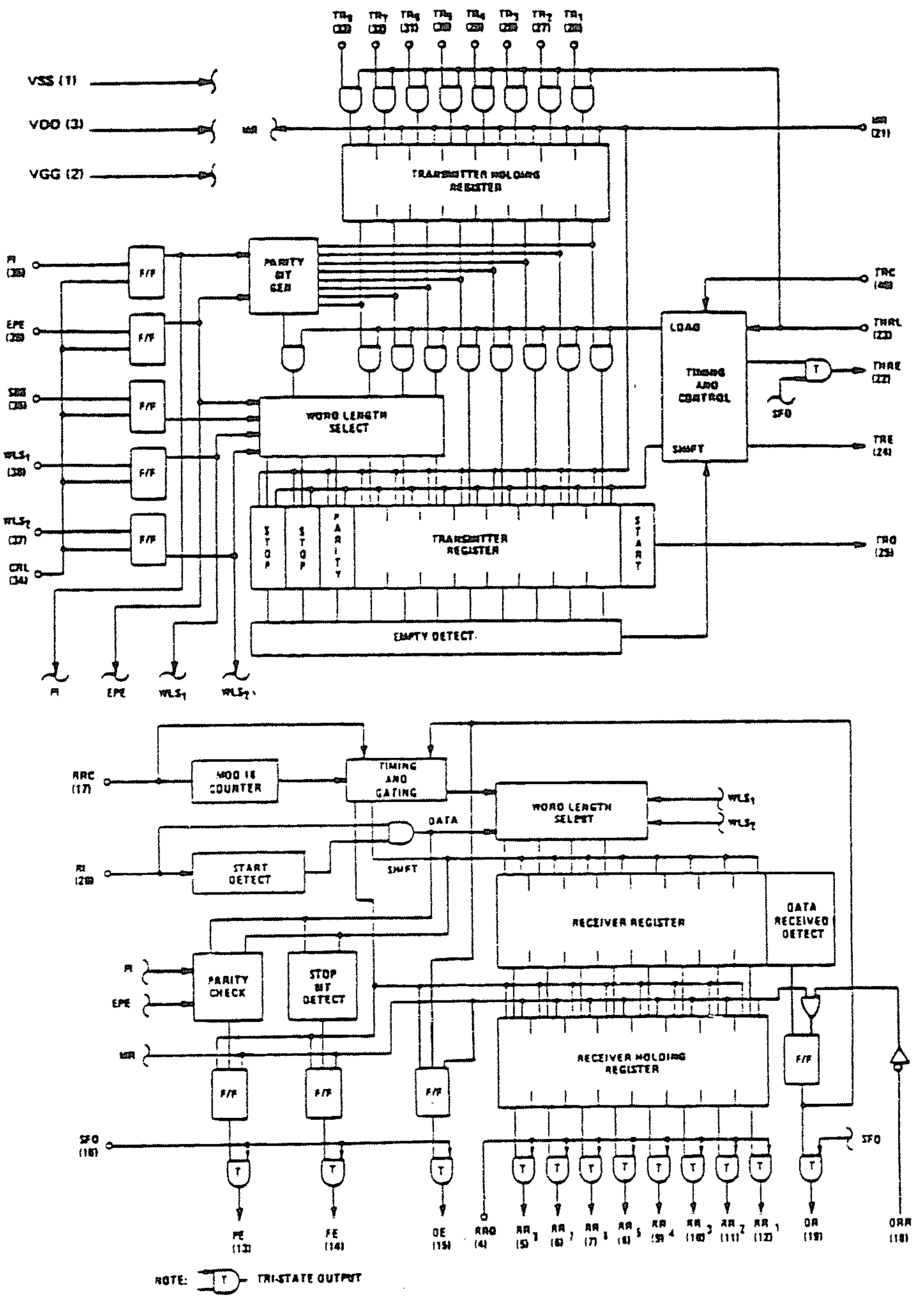


GENERAL DESCRIPTION

The TR1602A & the TR1602B are ASYNCHRONOUS RECEIVER/TRANSMITTER sub-systems using silicon gate process technology. The use of this low threshold process provides direct compatibility with all forms of current sinking logic. Interfacing restraints, such as external resistors, drivers and level shifting circuitry, are eliminated. All output lines have been designed to drive TTL directly.

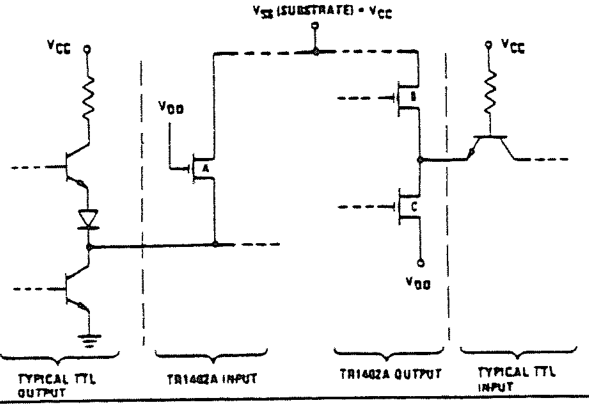
The ASYNCHRONOUS RECEIVER/TRANSMITTER is a general purpose, programmable MOS/LSI device for interfacing an asynchronous serial data channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial word which contains the data along with start, parity, and stop bits. The receiver section converts a serial word with start, data, parity, and stop bits, into parallel data, and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both the receiver and the transmitter are double buffered. The array is compatible with bipolar logic. The array may be programmed as follows: The word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited, the parity may be even or odd; and the number of stop bits may be either one or two, with one and one half when transmitting a 5 bit code. Note: See TR1402A Data Sheet for operation with 5 level code-2 stop bits.

ADVANCE ENGINEERING INFORMATION



INPUT STRUCTURE

MOS DEVICE "A" ACTS AS AN INTERNAL PULL-UP RESISTOR TO $V_{SS} = V_{CC}$ WHICH BIASES OFF THE CASCODE DEVICE OF THE TTL OUTPUT IN THE HIGH-LEVEL OUTPUT STATE. IN THE LOW-LEVEL OUTPUT STATE THE TTL OUTPUT DEVICE SINKS THE CURRENT SUPPLIED BY DEVICE "A".



OUTPUT STRUCTURE

DEVICES "B" & "C" COMPRISE A PUSH-PULL OUTPUT BUFFER. IN THE LOW-LEVEL STATE, OUTPUT TRANSISTOR "C" IS "ON" AND CASCODE DEVICE "B" IS OFF. IN THE HIGH-LEVEL STATE, THE OPPOSITE IS TRUE. IN THE DISCONNECTED STATE, BOTH "B" AND "C" ARE TURNED OFF CAUSING THE OUTPUT NODE TO FLOAT.

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{SS} Power Supply	V_{SS}	+5 volts supply
2	V_{GG} Power Supply	V_{GG}	-12 volts supply
3	V_{DD} Power Supply	V_{DD}	Ground
4	Receiver Register Disconnect	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_8-RR_1 data outputs (pins 5-12).
5—12	Receiver Holding Register Data	RR_8– RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR_1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	Parity Error	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	Framing Error	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	Overrun Error	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data REceived Flag (pin 19) was not reset before the next character was transferred to the REceiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	Status Flags Disconnect	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	Receiver Register Clock	RRC	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	Data Received Reset	DRR	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	Data Received	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	Receiver Input	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	Master Reset	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the Transmitter and Receiver Registers, the Receiver Holding Register, FE, OE, PE, DRR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	Transmitter Holding Register Empty	THRE	A high-level output Voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.

PIN DEFINITIONS (CONT)

<table>
<tr><th>PIN NUMBER</th><th>NAME</th><th>SYMBOL</th><th>FUNCTION</th></tr>
<tr><td>23</td><td>Transmitter Holding Register Load</td><td>THRL</td><td>A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.</td></tr>
<tr><td>24</td><td>Transmitter Register Empty</td><td>TRE</td><td>A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.</td></tr>
<tr><td>25</td><td>Transmitter Register Output</td><td>TRO</td><td>The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage, V_{OH}, to a low-level output voltage, V_{OL}.</td></tr>
<tr><td>26–33</td><td>Transmitter Register Data Inputs</td><td>TR_1 – TR_8</td><td>The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, RR1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.</td></tr>
<tr><td>34</td><td>Control Register Load</td><td>CRL</td><td>A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.</td></tr>
<tr><td>35</td><td>Parity Inhibit</td><td>PI</td><td>A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited the STOP bit(s) will immediately follow the last data bit on transmission.</td></tr>
<tr><td>36</td><td>Stop Bit(s) Select</td><td>SBS</td><td>This line selects the number of STOP bits to be transmitted after the PARITY bit. A high-level input voltage, V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. Selection of two STOP bits when programming a five (5) bit word generates 1.5 STOP bits.</td></tr>
<tr><td>37–38</td><td>Word Length Select</td><td>WLS_2 – WLS_1</td><td>These two lines select the character length (exclusive of parity) as follows:
<table>
<tr><th>WLS_2</th><th>WLS_1</th><th>Word Length</th></tr>
<tr><td>V_{IL}</td><td>V_{IL}</td><td>5 bits</td></tr>
<tr><td>V_{IL}</td><td>V_{IH}</td><td>6 bits</td></tr>
<tr><td>V_{IH}</td><td>V_{IL}</td><td>7 bits</td></tr>
<tr><td>V_{IH}</td><td>V_{IH}</td><td>8 bits</td></tr>
</table></td></tr>
<tr><td>39</td><td>Even Parity Enable</td><td>EPE</td><td>This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.</td></tr>
<tr><td>40</td><td>Transmitter Register Clock</td><td>TRC</td><td>The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.</td></tr>
</table>

WESTERN DIGITAL
MOS/LSI

TR1602/TR1863

APPLICATION NOTE

ASYNCHRONOUS RECEIVER/TRANSMITTER

FEB. 1978

INTRODUCTION

The transfer of digital data over relatively long distances is generally accomplished by sending the data in serial form thru a single communications channel using one of two general transmission techniques; *asynchronous* or *synchronous*. Synchronous data transmission requires that a clock signal be transmitted with the data in order to mark the location of the data bits for receiver. A specified clock transition (either rising or falling) marks the start of each data bit interval as shown in Figure 1. In addition, special synchronization data patterns are added to the start of the transmission in order for the receiver to locate the first bit of the message. With synchronous transmission, each data bit must follow contiguously after the sync word, since one data bit is assumed for every clock period.

With asynchronous transmission, a clock signal is not transmitted with the data and the characters need not be contiguous. In order for the receiver to properly recover the message, the bits are grouped into data characters (generally from 5 to 8 bits in length) and synchronizing start and stop elements are added to each character as shown in Figure 2.

The start element is a single logic zero (space) data bit that is added to the front of each character. The stop element is a logic one (mark) that is added to the end of each character. The stop element is maintained until the next data character is ready to be transmitted. (Asynchronous transmission is often referred to as start-stop transmission for obvious reasons). Although there is no upper limit to the length of the stop element, there is a lower limit that depends on the system characteristics. Typical lower limits are 1.0, 1.42 or 2.0 data bit intervals, although most modern systems use 1.0 or 2.0. The negative going transition of the start element defines the location of the data bits in one character. A clock source at the receiver is reset by this transition and is used to locate the center of each data bit.

The rate at which asynchronous data is transmitted is usually measured in *baud*, where a baud is defined to be the reciprocal of the shortest signal element (usually one data bit interval). It is interesting to note

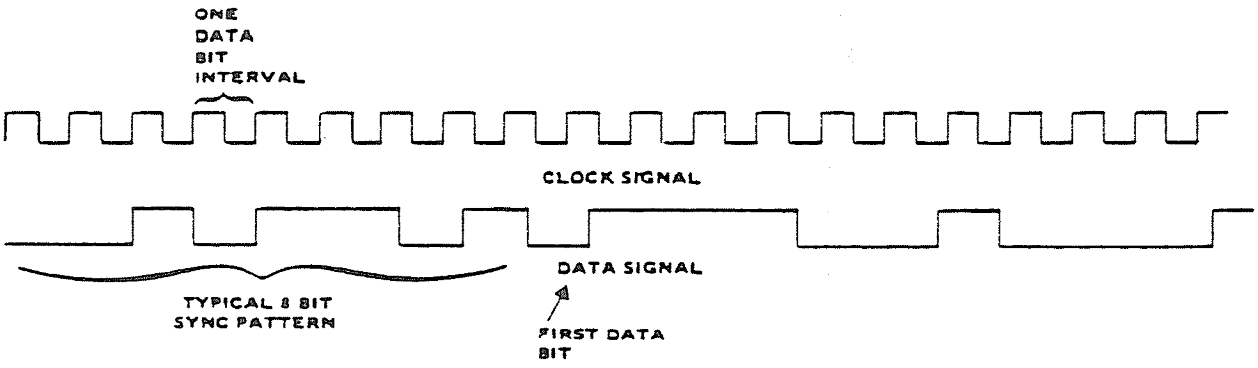


Figure 1. Synchronous Data

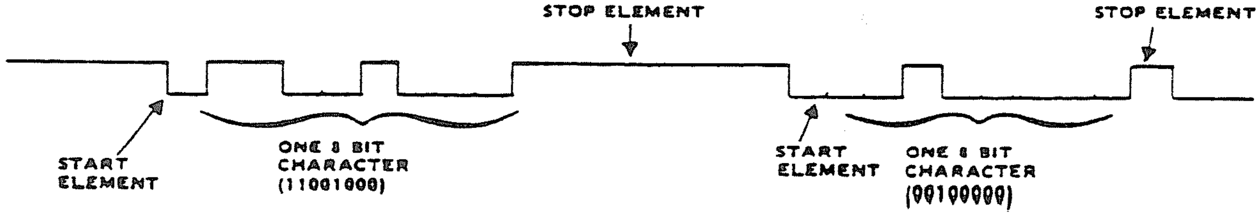


Figure 2. Asynchronous Data

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that the variable stop length is what makes the baud rate differ from the bit rate. For synchronous transmission, each element is one bit in length so that the baud rate equals the bit rate. The same is true for asychronous transmission if the stop element is always one bit in duration (this is referred to as *isochronous* transmission). However, when the stop code is longer than one bit, as shown in Figure 3, the baud rate differs from the bit rate.

Each character in Figure 3 is 11 data bit intervals in length, and if 15 characters are transmitted per second, then the shortest signal element (one data bit interval) is 66.6 ms/11 = 6.06 ms; giving a rate of 1/6.06 ms = 165 baud. However, since only 10 bits of information (8 data bits, one start bit and 1 stop bit) are transmitted every 66.6 msec, the bit rate is 150 bit/sec. (Even though the stop element lasts for two data intervals, it still is only one bit of information)

There are several reasons for using asychronous transmission. The major reason is that since a clock signal need not be transmitted with the data, transmission equipment requirements are greatly simplified. (Note, however, that an independent clock source is still required at both the transmitter and receiver). Another advantage of asynchronous transmission is that characters need not be contiguous in time, but are transmitted as they become available. This is a very valuable feature when transmitting data from manual entry devices such as a keyboard. The major disadvantage of asynchronous transmission is that it requires a very large portion of the communication channel bandwidth for the synchronizing start and stop elements (a much smaller portion of the bandwidth is required for the sync words used in synchronous transmission).

Asynchronous transmission over a simple twisted wire pair can be accomplished at moderately high baud rates (10K baud or higher depending on the length of the wire, type of line drivers, etc.) while it is generally limited to approximately 2K baud over the telephone network. When operating over the telephone network, a modem is required to convert the data pulses to tones that can be transmitted through the network.

One of the major limiting factors in the speed of asynchronous transmission is the distortion of the signal elements. Distortion is defined as the time displacement between the actual signal level transition and the nominal transition (Δt), divided by the nominal data bit interval (See Figure 4).

The nominal data bit interval is equal to the reciprocal of the nominal transmission baud rate and all data transitions should ideally occur at an integer number of intervals from the start bit negative going transition. Actual data transitions may not occur at these nominal points in time as shown in the lower waveform of Figure 4. The distortion of any bit transition is equal to Δt × NOMINAL BAUD RATE.

This distortion is generally caused by frequency jitter and frequency offset in the clock source used to generate the actual waveform as well as transmission channel, noise, etc. Thus, the amount of distortion that can be expected on any asynchronous signal depends on the device used to generate the signal and the characteristics of the communication channel over which it was sent. Electronic signal generators can be held to less than 1% distortion while electromechanical devices (such as a teletype) typically generate up to 20% distortion. The transmission channel may typically add an additional 5% to 15% distortion.

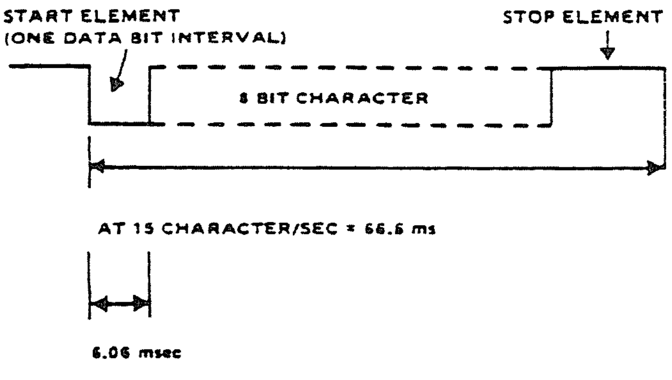


Figure 3.

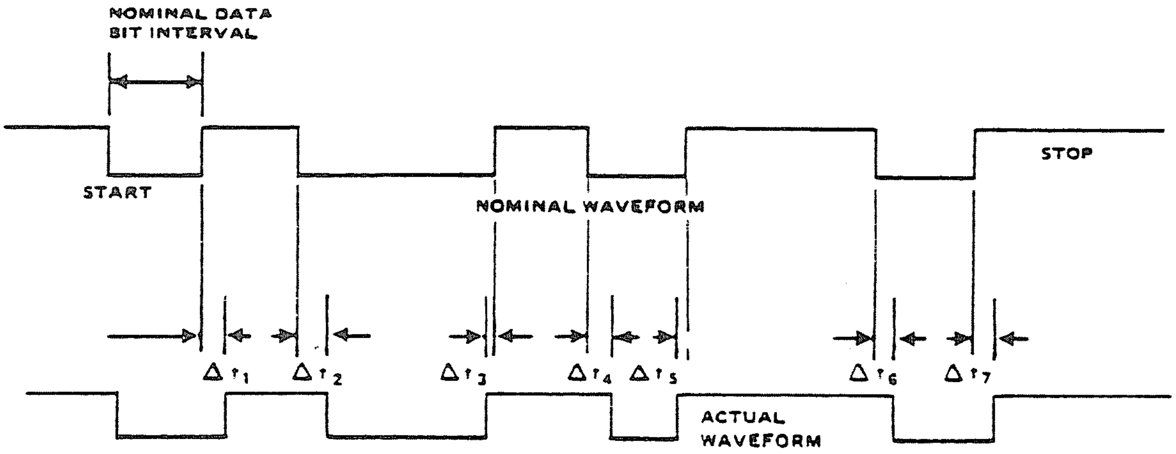


Figure 4A

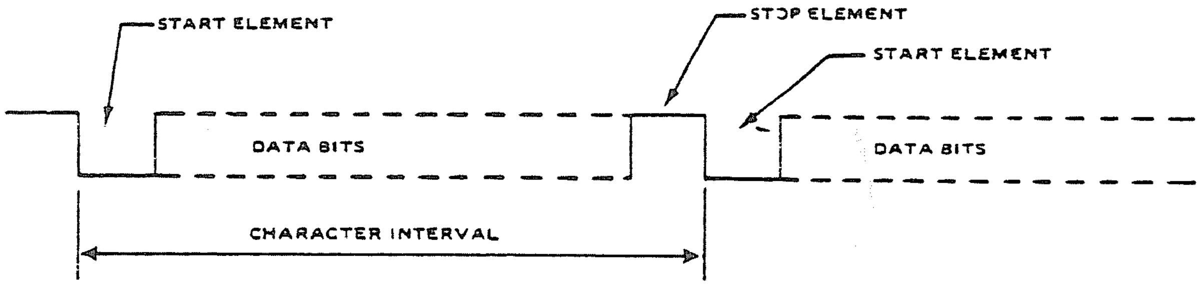


Figure 4B

The distortion previously described referred only to a single character as all measurements were referenced to the start element transition of that character. However, there may also be distortion between characters when operating at the maximum possible baud rate (i.e., stop elements are of minimum length). This type of distortion is usually measured by the minimum character interval as shown in Figure 4B.

The minimum character interval distortion is generally specified as the percentage of a nominal data bit interval that any character interval may be shortened from its nominal length. Since many of the same parameters that cause distortion of the data bits are also responsible for the character length distortion, the two distortions are often equal. However, some systems may exhibit character interval distortions of up to 50% of a data bit interval. This parameter is important when operating at the maximum baud rate since the receiver must be prepared to detect the next start bit transition after the minimum character interval.

Asynchronous receivers operate by locating the nominal center of the data bits as measured from the start bit negative going transition. However, due to receiver inaccuracies, the exact center may not be properly located. In electromechanical devices such as teletypes, the inaccuracy may be due to mechanical tolerances or variations in the power line frequency. With electronic receivers, the inaccuracies are due to frequency offset, jitter and resolution of the clock source used to find the bit centers. (The bit centers are located by counting clock pulses). For example, even if the receiver clock had no jitter or offset, and it was 16 times the baud rate, then the center of the bit could only be located within 1/16 of a bit interval (or 6.25%) due to clock resolution. However, by properly phasing the clock, this tolerance can be adjusted so that the sample will always be within ±3.125% of the bit center. Thus, signals with up to 46.875% distortion could be received. This number (the allowable receiver input distortion) is often referred to as the receiver distortion margin. Electromechanical receivers have distortion margins of 25 to 30%. The receiver must also be prepared to accept a new character after the minimum character interval. Most receivers are specified to operate with a minimum character interval distortion of 50%.

TR1602 Operation**

The WDC TR1602 is designed to transmit and receive asynchronous data as shown in Figure 5. Both the transmitter and the receiver are in one MOS CHIP, packaged in a 40 lead ceramic DIP. The array is capable of full duplex (simultaneous transmission and reception) or half duplex operation.

The transmitter basically assembles parallel data characters into a serial asynchronous data system. Control lines are included so that the characters may be 5, 6, 7 or 8 bits in length, have an even or odd parity bit, and have either one or two* stop bits. Furthermore, the baud rate can be set anywhere between DC and 20K baud by providing a transmit clock at 16 times the desired baud rate.

The receiver disassembles the asynchronous characters into a parallel data character by searching for the start bit of every character, finding the center of every data bit, and outputing the characters in a parallel format with the start, parity and stop bits removed. Three error flags are also provided to indicate if the parity was in error, a valid stop bit was not decoded or the last character was not unloaded by the external device before the next character was received (and therefore the last character was lost). The receiver clock is set at 16 times the transmitter baud rate.

Both the transmitter and receiver have double character buffering so that at least one complete character interval is always available for exchange of the characters with the external devices. This double buffering is especially important if the external device is a computer, since this provides a much longer permissible interrupt latency time (the time required for the computer to respond to the interrupt).

The status of the transmitter buffer and the receiver buffer (empty or full) is also provided as an output.

Another feature of the TR1602 is that the control information can be strobed into the transmitter and receiver and stored internally. This allows a common bus from a computer to easily maintain the controls for a large number of transmitter/receivers.

*1-1/2 with 5 bit code

**All references to the TR1602 operation also apply to the TR1863 operation.

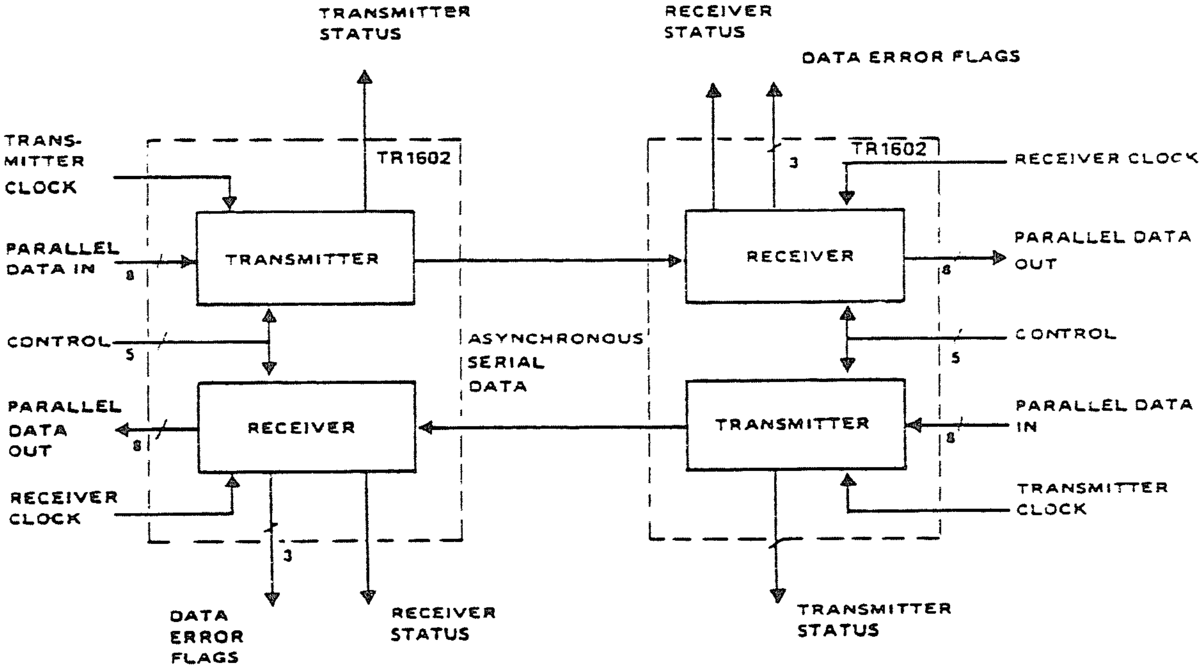


Figure 5

The TR1602 data and error flag outputs are designed for direct compatibility with bus organized systems. This feature is achieved by providing completely TTL compatible Three-state outputs (no external components are required). Three-state outputs may be set to a logic one or logic zero when enabled, or set to an open circuit (very high impedance) when disabled. A separate control line is provided to enable the data outputs and another one to enable the error flags so that the data outputs can be tied to a separate bus from the flag outputs.

The TR1602 inputs are also directly compatible with TTL logic elements without any external components.

TR1602 Description

Figure 6 is a block diagram of the transmitter portion of the TR1602. Data can be loaded into the Transmitter Holding Register whenever the Transmitter Holding Register Empty (THRE) line is at a logic one, indicating that the Transmitter Holding Register is empty. The data is loaded in by strobing the Transmitter Holding Register Load (THRL) line to a logic zero. The data is automatically transferred to the Transmitter Register as soon as the Transmitter Register becomes empty. The desired start, stop and parity bits are then added to the data and serial transmission is started. The number of stop bits and the type of parity bit is under control of the Control Register. The state of the control lines is loaded into the Control Register when the Control Register Load (CRL) line is strobed to a logic one. The 5 control lines allow 24 different character formats as shown in Table 1. These 24 formats cover almost all of the transmission schemes presently in use.

A Master Reset (MR) input is provided which sets the transmitter to the idle state whenever this line is strobed to a logic one. In addition, a Status Flag Disconnect (SFD) line is provided. When this signal is at a logic one, the THRE output is disabled and goes to a high impedance. This allows the THRE outputs of a number of arrays to be tied to the same data bus.

Figure 7 illustrates the relative timing of the transmitter signals. After power turn-on, the master reset should be strobed to set the circuits to the idle state. The external device can then set the transmitter register data inputs to the desired value and after the data inputs are stable, the load pulse is applied. The data is then automatically transferred to the Transmitter Register where the start, stop and parity (if required) bits are added and transmission is started. This process is then repeated for each subsequent character as they become available. The only timing requirement for the external device is that the data inputs be stable during the load pulse (and 20 nsec after).

TABLE 1
CONTROL DEFINITION

CONTROL WORD					CHARACTER FORMAT			
W L S 2	W L S 1	P I	E P E	S B S	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	x	0	1	5	NONE	1
0	0	1	x	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	x	0	1	6	NONE	1
0	1	1	x	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	x	0	1	7	NONE	1
1	0	1	x	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	x	0	1	8	NONE	1
1	1	1	x	1	1	8	NONE	2

The TR1602 Transmitter output will have less than 1% Distortion at baud rates of up to 20K baud (assuming the Transmitter Register Clock is perfect) and is, therefore, compatible with virtually all other asynchronous receivers.

Figure 8 is a block diagram of the Receiver portion of the TR1602. Serial asynchronous data is provided to the Receiver Input (RI). A start bit detect circuit continually searches for a logic one to logic zero transition while in the idle state. When this transition is located, a counter is reset and allowed to count until the center of the start bit is located. If the input is still a logic zero at the center, the signal is assumed to be a valid start bit and the counter continues to count to find the center of all subsequent

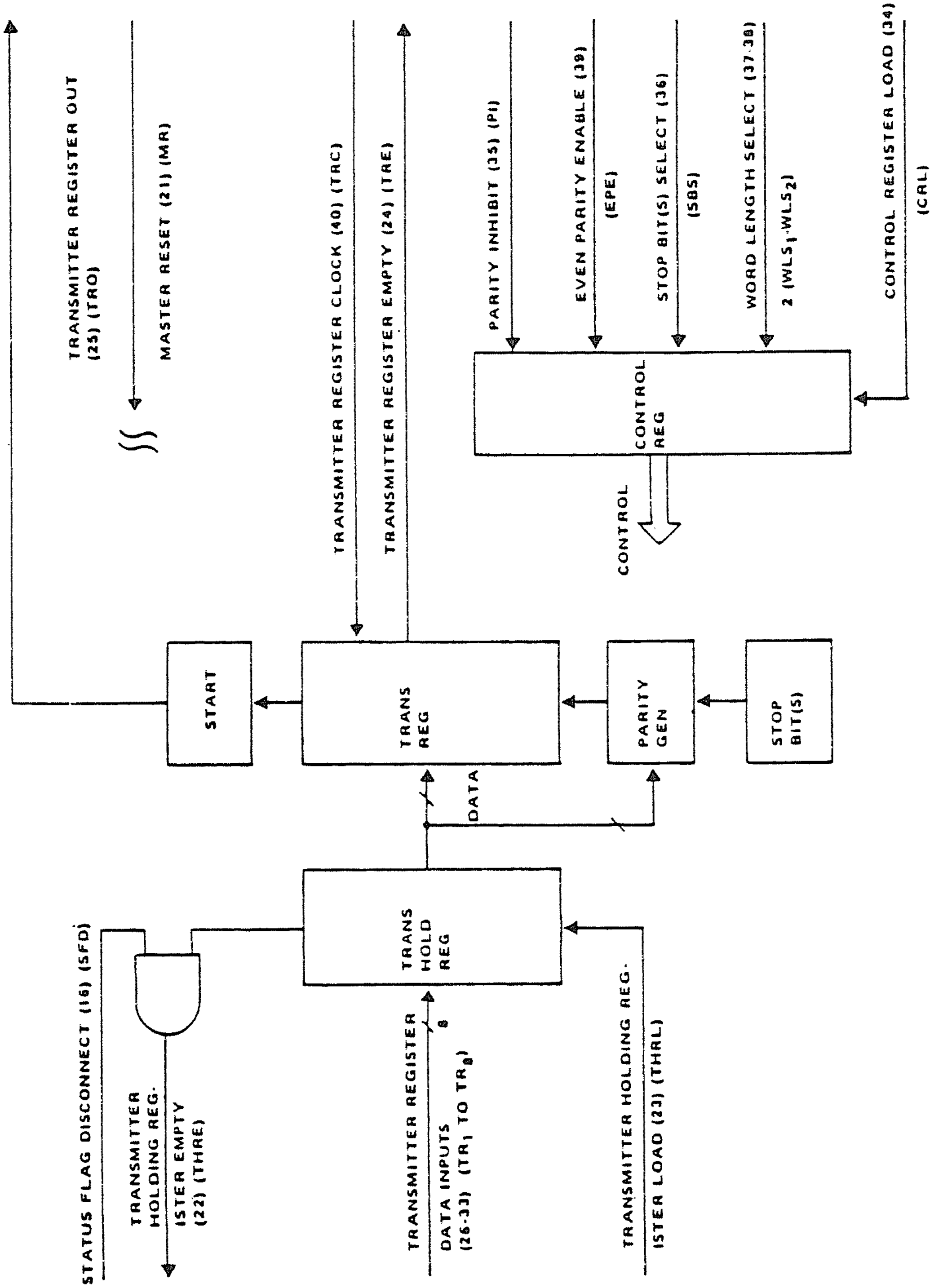


Figure 6. Transmitter Block Diagram

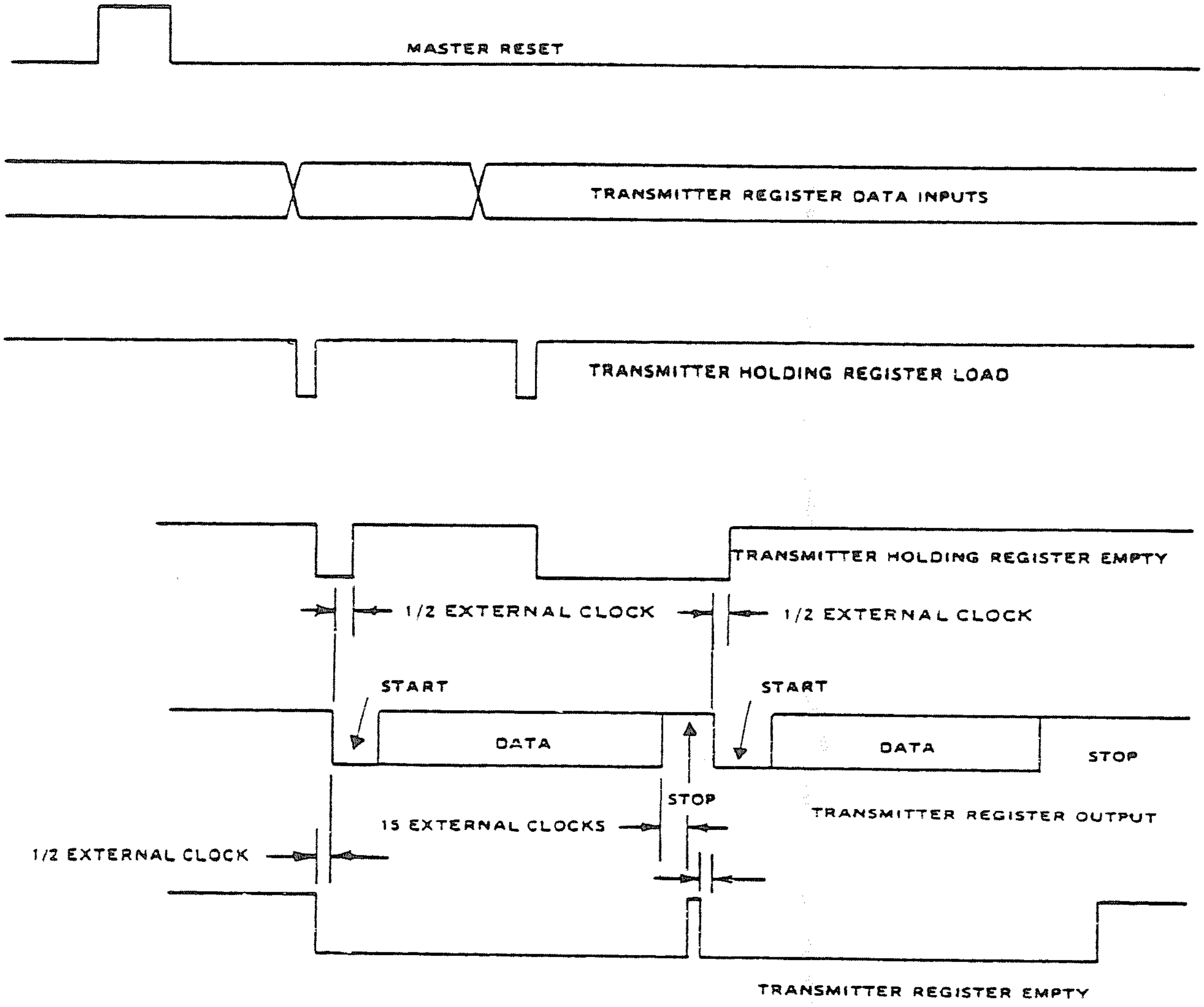


Figure 7. Transmitter Timing Diagram

data and stop bits. (Verification of the start bit prevents the receiver from assembling an erroneous data character when a logic zero noise spike is presented to the Receiver Input). The Receiver is under control of the Control Register described in the previous paragraph. This register controls the number of data bits, number of stop bits, and the type of parity as described in Table 1. The word length gating circuit adjusts the length of the Receiver Register to match the length of the data characters. A parity check circuit checks for even or odd parity if parity was added by the Transmitter. If parity does not check a Parity Error signal will be set to a logic one and this signal will be held until the next character is transferred to the Holding Register. A circuit is also provided that checks the first stop bit of each character. If the stop bit is not a logic one, the Framing Error line will be set to a logic one and held until the next character is transferred to the Holding Register. This feature permits easy detection of a break character (null character with no stop element). As each received character is transferred to the Holding Register, the Data Received (DR) line is set to a logic one indicating that the external device may sample the data output. When the external device samples the output, it should strobe the Data Received Reset (DRR) line to a logic zero to reset the DR line. If the DR line is not reset before a new character is transferred to the Holding Register (i.e., a character is lost) the Overrun Error line will be set to a logic one and held until the next character is loaded into the Holding Register. The timing for all of the Receiver functions is obtained from the external Receiver Register Clock which should be set at 16 times the baud rate of the transmitter.

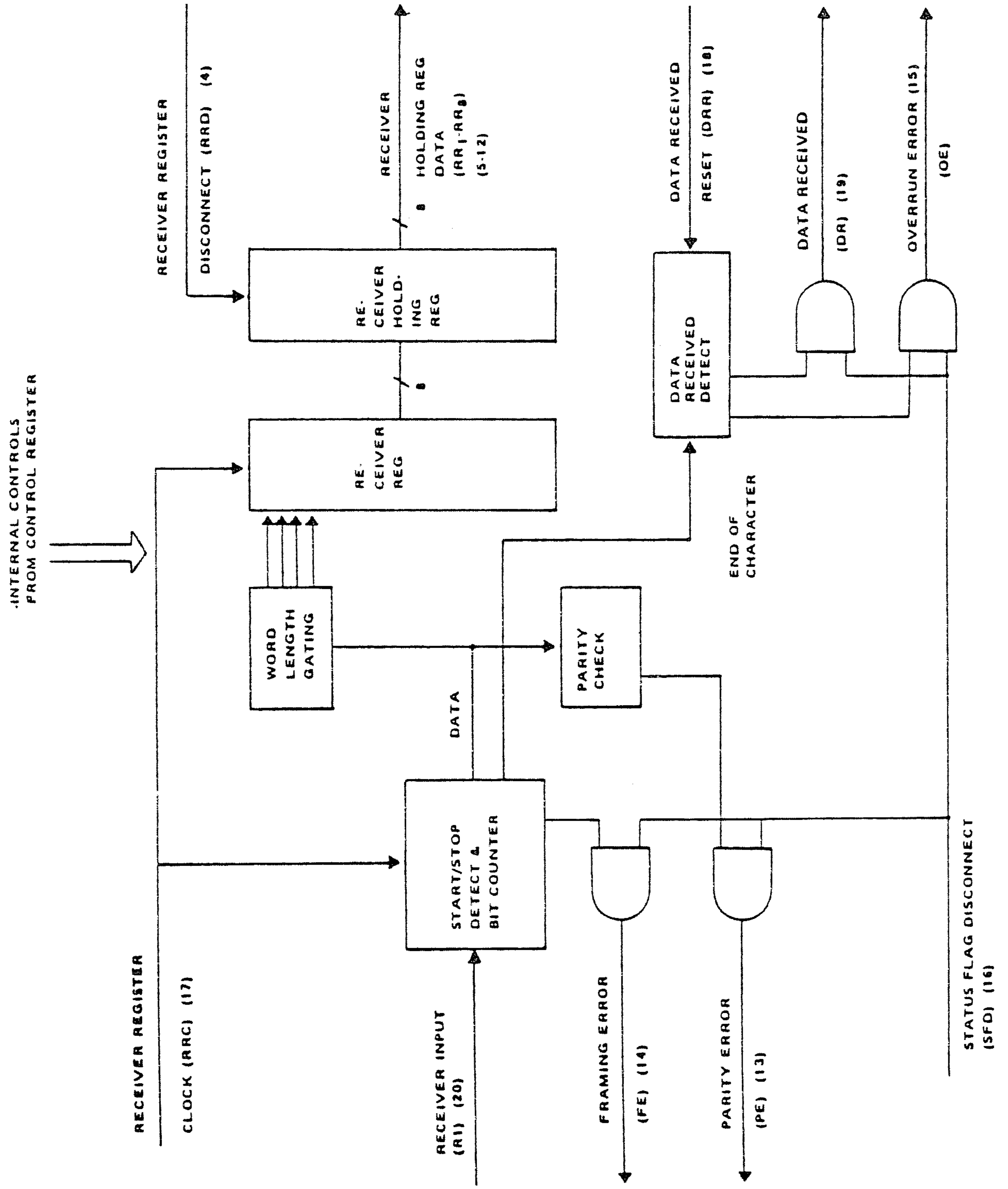


Figure 8. Receiver Block Diagram

Figure 9 illustrates the relative timing of the Receiver signals. A Master Reset strobe places the unit in the idle mode and the Receiver then begins searching for the first start bit. After a complete character has been decoded, the data output and error flags are set to the proper level and the Data Received (DR) line is set to a logic one. Although it is not apparent in Figure 9, the data outputs are set to the proper level one half clock period before the DR and error flags, which are set in the center of the first stop bit. The Data Received Reset pulse resets the DR line to a logic zero. Data can be strobed out at any time before the next character has been disassembled.

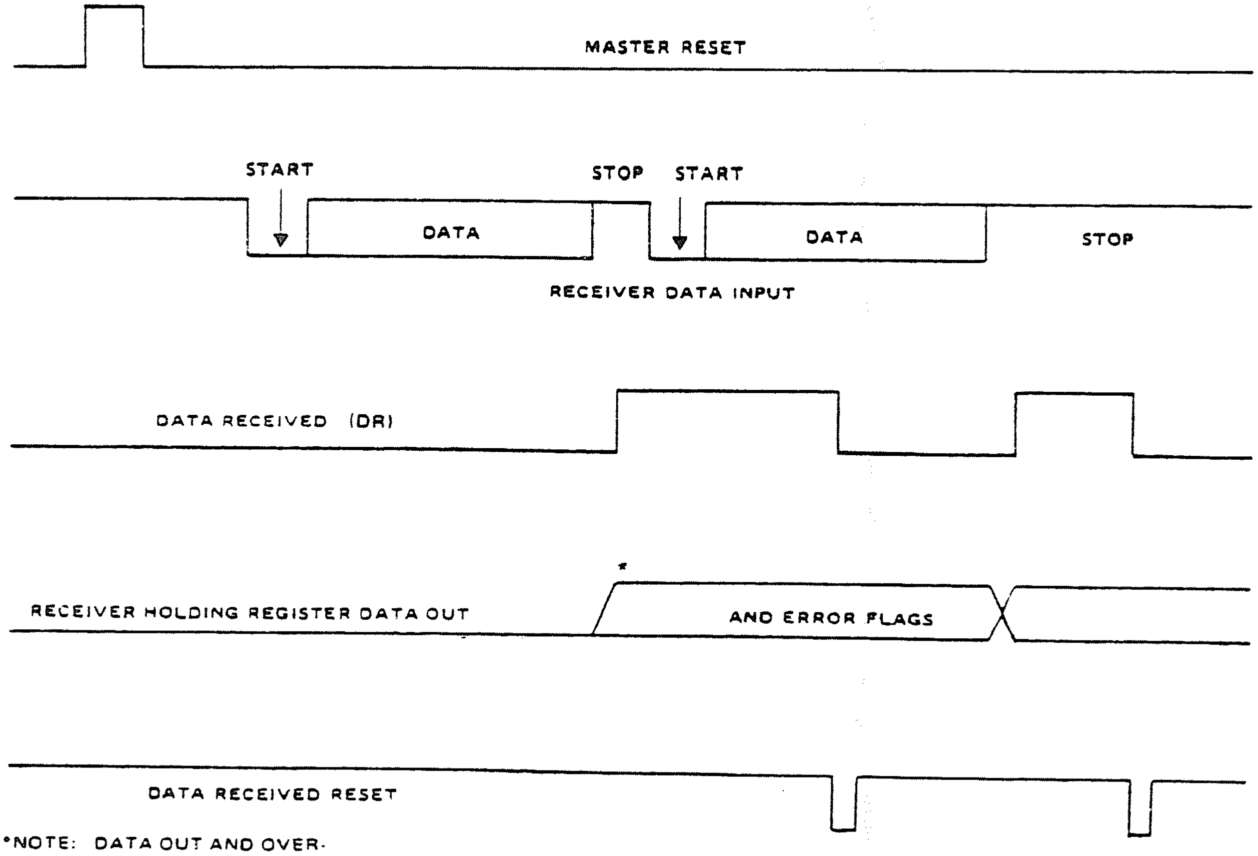
The TR1602 Receiver uses a 16X clock for timing purposes. Furthermore, the center of the start bit is defined as clock count 7-1/2. Therefore, if the receiver clock is a symmetrical square wave as shown in Figure 10, the center of the bits will always be located within ±3.125% (assuming a perfect input clock) thus giving a receiver margin of 46.875%.

In Figure 10, the start bit could have started as much as one complete clock period before it was detected, as indicated by the shaded area of the negative going transition. Therefore, the exact center is also unknown by the shaded area around the sample point. This turns out to be ±1/32 = ±3.125%.

If the receiver clock is not perfect, then the receiver distortion margin must be further reduced. For example, if the clock had 1.0% jitter, 0.1% offset and the positive clock pulse was only 40% of the clock cycle; then, for a 10 element character, the clock would add:

1.0%	+	(0.1% × 10)	+	0.1 (1/16)	=	2.3% Distortion
(Jitter)		(Offset)		(Non-symmetrical Clock)		

(The frequency offset was multiplied by the number of elements per character since the offset is cumulative on each element).



*NOTE: DATA OUT AND OVER-RUN ERROR PRECEDES DR & ERROR FLAGS BY 1/2 CLOCK

Figure 9. Receiver Timing Diagram

WESTERN DIGITAL
MOS/LSI

FD1771

APPLICATION NOTE

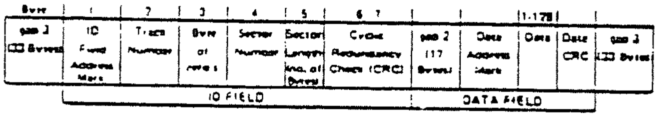
FLOPPY DISK FORMATTER/CONTROLLER

MARCH, 1978

FLOPPY DISK CONTROLLER
APPLICATION NOTE

Introduction

The FD1771 is a MOS/LSI device that performs the function of interfacing a processor to a flexible (Floppy) diskette drive. This single chip replaces nearly 80% of the required disk drive interface electronics. (See figure 1-1). It provides the data accessing controls and the bidirectional transfer of information between the processor's memory and the magnetically stored data on the diskette. The diskette data is stored in a data entry format compatible with the IBM 3740 specification (other formats may be used providing more data storage). In this format all information is recorded on tracks (radial paths) in sectors (arc sections) defined by a programmed header as shown below:



The FD1771 handles single density frequency modulated (FM) data. Each data cell is defined by clock pulses. A pulse recorded between clock pulses identifies the presence of a logic 1 bit; the absence of this pulse is interpreted as a logic 0 bit. The Address Marks for Index, ID, and Data are identified by a particular pattern not repeated in the remainder of the ID field or Data field. This is accomplished by reading patterns that are recorded with missing clock bits (logic 0) as shown below:

Index Address Mark	Data	1 1 1 1 1 1 0 0	=FC
	Clock	1 1 0 1 0 1 1 1	=D7
ID Address Mark	Data	1 1 1 1 1 1 1 0	=FE
	Clock	1 1 0 0 0 1 1 1	=C7
Data Address Mark	Data	1 1 1 1 1 0 1 1	=FB
	Clock	1 1 0 0 0 1 1 1	=C7
Deleted Data Address Mark	Data	1 1 1 1 1 0 0 0	=F8
	Clock	1 1 0 0 0 1 1 1	=C7

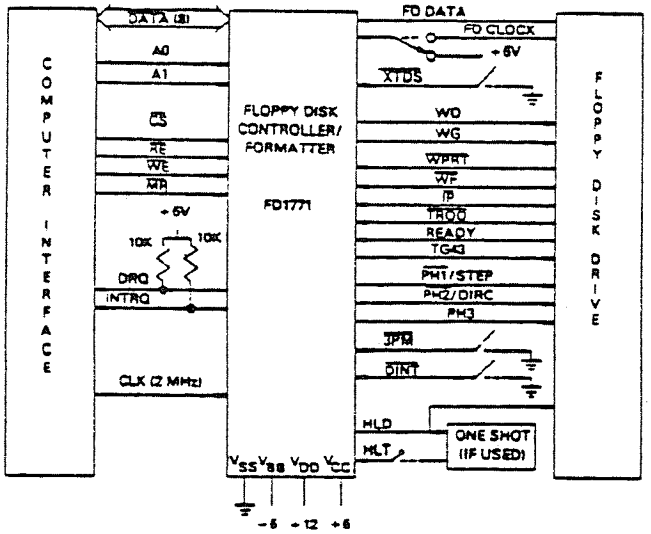
These patterns are used as synchronization codes by the FD1771 when reading data and are recorded by the formatting command, Write Track, when the FD1771 is presented with data F7 through FE.

SECTION I FD1771 DESCRIPTION

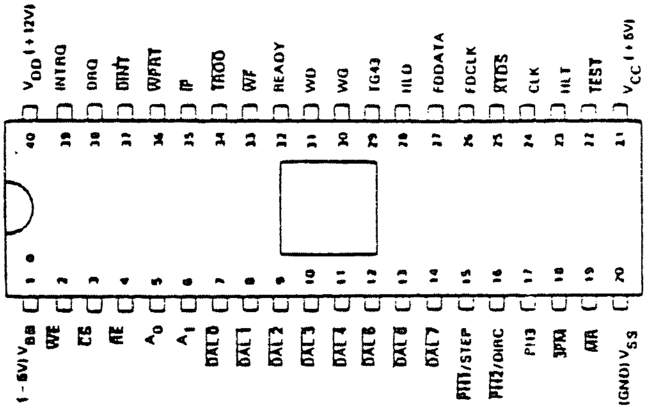
1.1 FD1771 — Flexible Drive Interface (Refer to Figure 1-1 FD1771 Block Diagram)

The FD1771 generates all controls to position the read/write head over the desired track. The FD1771 has the capability of sending successive three phase pulses over the lines PH1, PH2, and PH3 for 3 phase stepping motors or by sending a level over the PH2 line and pulses over the PH1 lines to determine direction and stepping rate for step-direction motors. The particular motor interface is chosen by hardwiring the external pin, 3PM.

ALL REFERENCE TO FD1771 DENOTES FD1771-01 VERSION



FD1771 SYSTEM BLOCK DIAGRAM
FIG 1



A Suffix = Ceramic
B Suffix = Plastic

FD1771 PIN CONNECTIONS
FIG 2

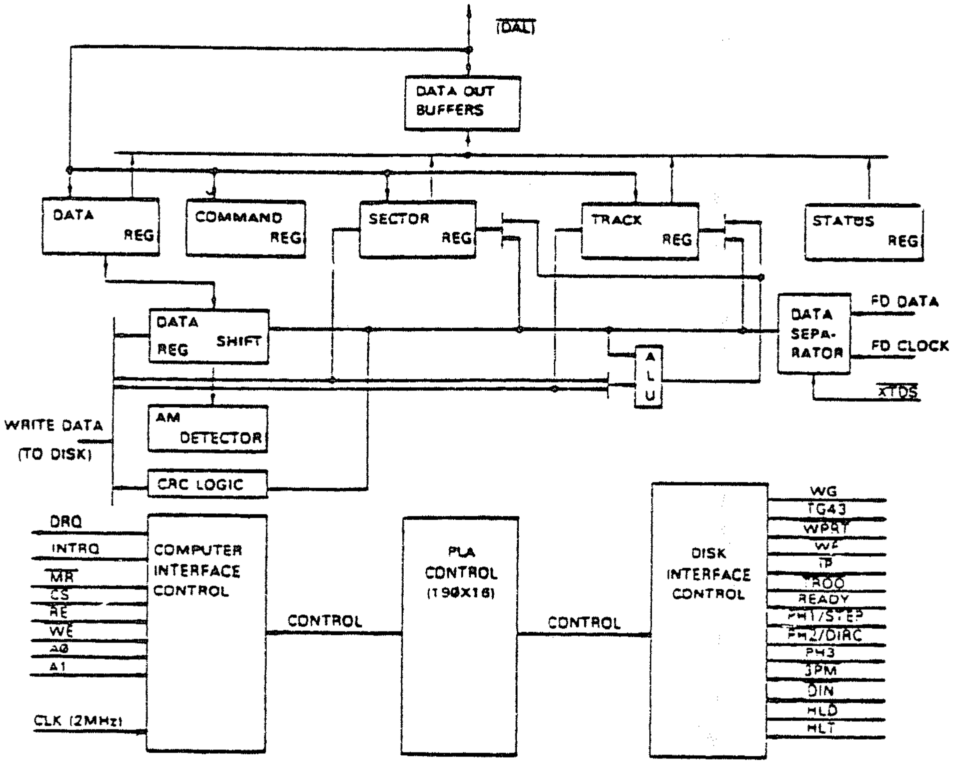


FIGURE 1-1

The head is loaded against the recording media (diskette) by the HLD (Head Load) signal from the FD1771. A read or write operation does not occur until a logic high signal is sampled at the HLT (Head Load Timing) input. This input is sampled after a 10 msec internal delay. This input may be wired high if 10 msec time is sufficient or a one shot may be used to extend this time. If the head is already engaged from a previous operation the resetting of bit 2 in the Read or Write Command (see Processor Interface) will disable the HLT functions and the 10 ms delay.

When reading the serial data from the disk the FD1771 will look for the desired sector to be read, check its ID field and locate its data address mark. All subsequent serial data is assembled in parallel form and presented to the processor interface. The serial data read from the Floppy Driver may be input as composite data, both clock and data present at the FDDATA input, or as separated data in which the data is input to the FDDATA pin and the clock is input to the FD Clock pin.

When writing, information is presented as composite of serial clock and data pulses of 500 nsec periods. With data present at the WD output the WG (Write Gate) signal is activated to allow current to flow in the Read/Write head.

The remaining interface between the FD1771 and the Floppy Drive concerns status information.. The $\overline{\text{IP}}$ (Index Pulse) and $\overline{\text{TR00}}$ (Track 00) signals are outputs of the drive to indicate when the index mark is encountered (once per revolution of the disk) or when the Read/Write head is located over Track 00 respectively.

The $\overline{\text{WPRT}}$ (Write Protect), $\overline{\text{DINT}}$ (Disk Initialization), and Ready signals reflect the drive condition. The Write Protect signal, when a logic low, prevents the FD1771 from executing a Write Command. The Disk Initialization input, when a logic low, prevents a Write Track Command and essentially disables the rewriting of a format over a previously formatted diskette. The Ready signal indicates Floppy Drive readiness and a logic low on this input prevents any Read or Write command from being executed.

Other status interface signals are $\overline{\text{WF}}$ (Write Fault) from the Drive which signifies a write operation fault such as failure to detect write current when WG is turned on terminating the Current Write command; and the TG43 signal to the drive indicating the track to be written on is located between Track 44 and Track 76. This latter signal is used by the drive to lower the write current on inner tracks and compensate for the higher density recording of these tracks.

1.2 FD1771 – Processor Interface (See figure 1-1)

All commands, status and data are transferred over the 3 state bidirectional $\overline{\text{DAL}}$ (Data Access) lines. These 8 lines present an open circuit to the common processor peripheral bus until activated by the $\overline{\text{CS}}$ (Chip Select) signal. An active $\overline{\text{CS}}$ combined with $\overline{\text{RE}}$ (Read Enable) sets the $\overline{\text{DAL}}$ into the transmitter mode while the $\overline{\text{CS}}$ combined with an active WE (Write Enable) sets the $\overline{\text{DAL}}$ in the receiver mode. The information in the FD1771 resides in 5 accessible 8 bit registers. These registers are: (1) The bidirectional Data Register which acts as a parallel buffer for read or write operations, and receives the desired track number to be accessed in seek operation. (2) the Command register which receives and stores commands from e processor, (3) The sector register which receives the desired sector number to be accessed, (4) The track register which contains the present Track position, (5) The Status Register containing information about the present operation.

The accessing of the registers is accomplished by a combination of active levels on the $\overline{\text{CS}}$, $\overline{\text{RE}}$, or $\overline{\text{WE}}$, and the register address lines A1 and A0. The Command Register can only receive information and the Status Register can only transmit information.

Two signals are available to aid in program response to the FD1771. The INTRQ (Interrupt Request) is activated by the controller whenever an operation is completed successfully or terminated by a fault. The DRQ (Data Request) signal is available as an indication of the chips readiness to transfer a byte of data during read or write operations.

A 2MHZ clock is required by the chip as a reference for all timed signals such as motor controls and data transfers. The $\overline{\text{MR}}$ (Master Reset) clears the command register and initiates a Restore (seek track 00) Command when the $\overline{\text{MR}}$ line is returned to an inactive state.

1.3 FD1771 Instructions

The FD1771 can be considered a specialized microprocessor with its own instruction repertoire. These are listed in the Tables below.

The Restore, Seek, and the three Step commands position the Read/Write head over the desired track. The Restore positions it over Track 00, the Seek poisitions it over the track specified in the Data Register, and the Step Commands position the head over an adjacent track to its present position.

The Step In moves the head inward toward the center of the disk while the Step Out moves it outward from the center. The Step Command moves the head one step in the same direction as the previous command.

The Read and Write commands are the normally executed commands when transferring information. The Read command initiates a search for a track and sector code in the ID field equal to that in the track and sector registers. When found, the data is formatted from serial to parallel and presented to the Data Register along with the setting of the DRQ signal. By setting of bit 4 in the Read (or Write) command all data records from the desired sector until the last sector on the track are sequentially assembled. The setting of bit 3 allows other combinations of byte count per sector than the standard IBM format.

The Write Command operates similar to the Read Command in multiple sector and variable sector length. All received words in the Data register are transferred to the shift register at which time the DRQ line is set. Four separate Data address marks are selectable through bits 1 and 0 which are written on the diskette prior to writing the sector data.

The Read Address command provides the next encountered ID field (6 bytes) on the diskette to the processor. This can be used to identify the track over which the head resides and can be used if one were to multiplex between two or more drives and wish to return to the first drive. This could also be accomplished by storing the track register in memory and returning it when reactivating the first drive.

The Write Track command is basically used for formatting. Once the index position is located the FD1771 will request data and transfer it to the disk including all ID fields, gaps, and Data fields. Special address marks and the CRC characters are written by detecting certain data patterns. The Read track command allows the reading of the entire recorded pattern on a track including gaps. (Refer to Data Sheet for formatting details)

The final command is the Force interrupt which can be loaded into the Command register at any time. This will terminate any present operation and can also generate an interrupt under four selectable conditions.

1.4 Status Register (See Table 1, page 16)

This register contains status information associated with each of the command instructions. Bit 7 always reflects the Ready condition of the Drive while bit 0 (Busy) always defines the status of the FD1771 concerning present operations.

COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\bar{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

COMMAND FLAG SUMMARY

TYPE I

h = Head Load flag (Bit 3)

h=1, Load head at beginning
h=0, Do not load head at beginning

V = Verify flag (Bit 2)

V=1, Verify on last track
V=0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

r_1r_0=00,	6ms between steps
r_1r_0=01,	6 ms between steps
r_1r_0=10,	10ms between steps
r_1r_0=11,	20ms between steps

u= Update flag (Bit 4)

u=1, Update Track register
u=0, No update

In general bit 1 reflects the state of the external DRQ signal while bit 2 indicates lost data due to overrun or underrun conditions. The Type 1 or head positioning instructions use bit 1 and 2 as a reflection of the $\overline{\text{IP}}$ and $\overline{\text{TR00}}$ inputs respectively.

Bit 3 normally indicates the encounterance of a CRC error in the ID or Data fields except for Read Track and Write Track commands in which the CRC is not checked. Bit 4 indicates that the desired track or sector was not correctly located. Bit 6 reflects the $\overline{\text{WP}}$ input on Seek and Write Commands and combines with bit 5 to identify the encountered data address mark on the Read command. Bit 5 also indicates the head engaged status on Seek commands and Write fault or Write commands.

TYPE II

m = Multiple Record flag (Bit 4)

m=0, Single Record
m=1, Multiple Records

b = Block length flag (Bit 3)

b=1, IBM format (128 to 1024 bytes)
b=0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1-0)

a_1a_0=00,	FB (Data Mark)
a_1a_0=01,	FA (Data Mark)
a_1a_0=10,	F9 (Data Mark)
a_1a_0=11,	F8 (Data Mark)

TYPE III

s = Synchronize flag (Bit 0)

$\bar{s}$=0, Synchronize to AM
$\bar{s}$=1, Do not synchronize to AM

TYPE IV

I_i = Interrupt Condition flags (Bits 3-0)

I_0=1, Not Ready to Ready Transition
I_1=1, Ready to Not Ready Transition
I_2=1, Index Pulse
I_3=1, Immediate Interrupt

E=Enable HLD and 10 msec Delay

E=1, Enable HLD, HLT and 10 msec Delay
E=0, Head is assumed Engaged and there is no 10 msec Delay

Computer Interface:

PIN NO	PIN NAME	SYMBOL	FUNCTION
7-14	$\overline{\text{DATA ACCESS LINES}}$	$\overline{\text{DAL0-DAL7}}$	• Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{\text{WE}}$ or a transmitter enabled by $\overline{\text{RE}}$.
3	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	• A logic low on this input selects the chip and enables computer communication with the device.
5,6	REGISTER SELECT LINES	A0, A1	•These inputs select the register to receive/transfer data on the DAL lines under RE and WE control:

A1	A0	$\overline{\text{RE}}$	$\overline{\text{WE}}$
0	0	Status Reg	Command Reg
0	1	Track Reg	Track Reg
1	0	Sector Reg	Sector Reg
1	1	Data Reg	Data Reg

PIN NO	PIN NAME	SYMBOL	FUNCTION
4	$\overline{\text{READ ENABLE}}$	$\overline{\text{RE}}$	•A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{\text{CS}}$ is low.
2	$\overline{\text{WRITE ENABLE}}$	$\overline{\text{WE}}$	•A logic low on this input gates data on the DAL into the selected register when $\overline{\text{CS}}$ is low.
38	DATA REQUEST	DRQ	•This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	•This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
24	CLOCK	CLK	•This input requires a free-running 2 MHz ± 1% square wave clock for internal timing reference.

Floppy Disk Interface:

PIN NO	PIN NAME	SYMBOL	FUNCTION
25	$\overline{\text{EXTERNAL DATA SEPERATION}}$	XTDS	•A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	•This input receives the externally separated clock when $\overline{\text{XTDS}}$ = 0. If $\overline{\text{XTDS}}$ = 1, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	•This input receives the raw read disk data if XTDS = 1, or the externally separated data if XTDS = 0.
31	WRITE DATA	WD	•This output contains both clock and data bits of 500 ns duration.
28	HEAD LOAD	HLD	•The HLD output controls the loading of the Read-Write head against the media the HLT input is sampled after 10 ms. When a logic high is sampled on the HLT input the head is assumed to be engaged.
23	HEAD LOAD TIMING	HLT	
15	Phase 1/Step	PH1/STEP	•If the 3PM input is a logic low the three phase motor control is selected and PH1, PH2, and $\overline{\text{PH3}}$ outputs form a one active low signal out of three. PH1 is active low after MR. If the 3PM input is a logic high the step and direction motor control is selected. The step output contains a 4usec high signal for each step and the direction output is active high when stepping: active low when stepping out.
16	Phase 2/Direction	PH2/DIRC	
17	Phase 3	$\overline{\text{PH3}}$	
18	3 Phase Motor Select	3PM	

PIN NO.:	PIN NAME:	SYMBOL:	FUNCTION
29	Track Greater Than 43	TG43	•This output informs the drive that the Read-Write head is positioned between track 44-76. This output valid only during Read and Write Commands.
30	WRITE GATE	WG	•This output is made valid when writing is to be performed on the diskette.
32	Ready	READY	•This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	•This input detects writing faults indications from the drive. When WG = 1 and $\overline{\text{WF}}$ goes low the current Write command is terminated and the Write Fault status bit is set. The $\overline{\text{WF}}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	•This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	•Input, when low for a minimum of 10 usec, informs the FD1771 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	•This input is sampled whenever a Write Command is received. A logic low terminated the command and sets the Write Protect Status bit.
37	$\overline{\text{DISK INTIALIZATION}}$	$\overline{\text{DINT}}$	•The input is sampled whenever a Write Track command is received. If $\overline{\text{DINT}}$ = 0, the operation is terminated and the Write Protect Status bit is set.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	•This input is used for testing purposes only and should be tied to +5V or left open by the user.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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C O R P O R A T I O N

FD 179X-02 Floppy Disk Formatter/Controller Family

MAY 1980

FEATURES

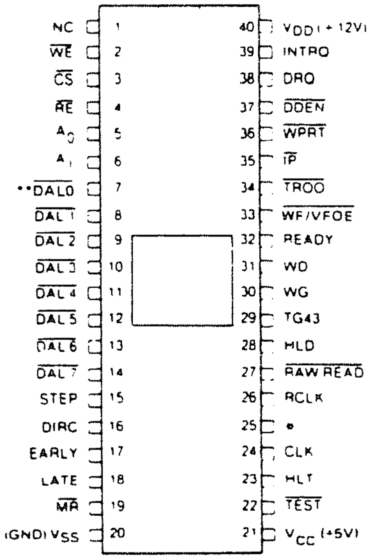
- TWO VFO CONTROL SIGNALS
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  IBM 3740 Single Density (FM)
  IBM System 34 Double Density (MFM)
- READ MODE
  Single/Multiple Sector Read with Automatic Search or Entire Track Read
  Selectable 128 Byte or Variable length Sector
- WRITE MODE
  Single/Multiple Sector Write with Automatic Sector Search
  Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  DMA or Programmed Data Transfers
  All Inputs and Outputs are TTL Compatible
  On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  Selectable Track to Track Stepping Time
  Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1793	1795	1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

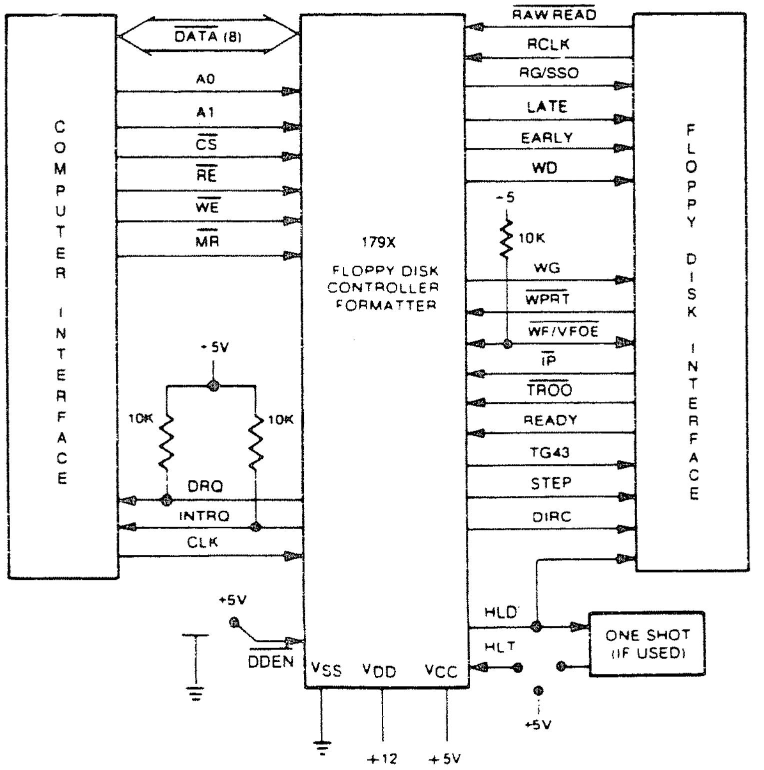
APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
NEW MINI-FLOPPY CONTROLLER



*1791/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS

PIN CONNECTIONS



FD179X SYSTEM BLOCK DIAGRAM

GENERAL DESCRIPTION

The FD179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793. On these devices, DDEN must be left open.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{\text{MR}}$ ACTIVE. When $\overline{\text{MR}}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	$\overline{\text{WRITE ENABLE}}$	$\overline{\text{WE}}$	A logic low on this input gates data on the DAL into the selected register when $\overline{\text{CS}}$ is low.
3	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	A logic low on this input selects the chip and enables computer communication with the device.
4	$\overline{\text{READ ENABLE}}$	$\overline{\text{RE}}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{\text{CS}}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{\text{RE}}$ and $\overline{\text{WE}}$ control: A1 A0 $\overline{\text{RE}}$ $\overline{\text{WE}}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
7-14	$\overline{\text{DATA ACCESS LINES}}$	$\overline{\text{DAL0}}$-$\overline{\text{DAL7}}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{\text{WE}}$ or transmitter enabled by $\overline{\text{RE}}$.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference. 2 MHz for 8" drives, 1 MHz for mini-drives.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF}}/\overline{\text{VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FD179X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected. This line must be left open on the 1792/4

ORGANIZATION

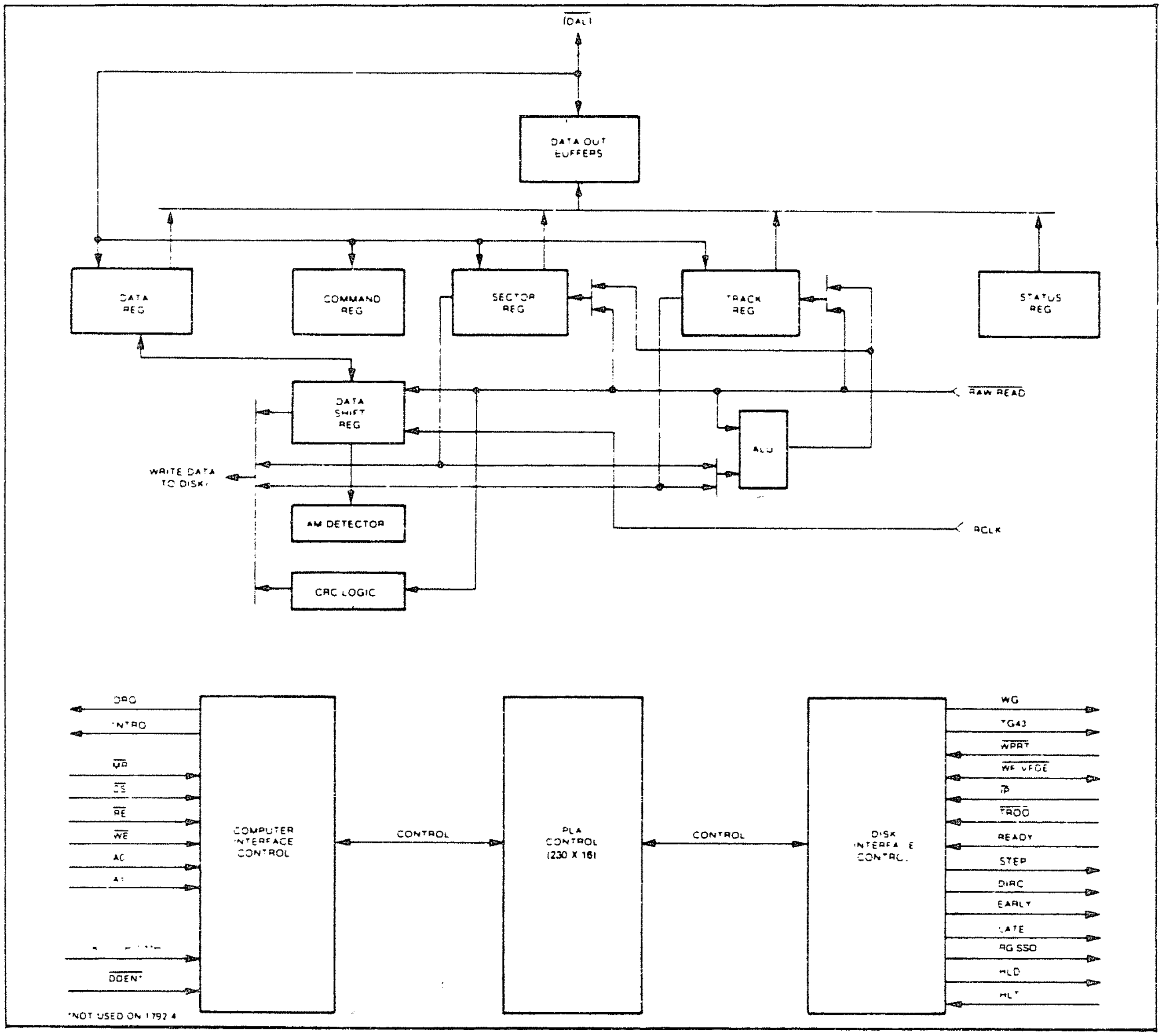
The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.



FD179X BLOCK DIAGRAM

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^{5} + 1$. The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791/3 has two different modes of operation according to the state of $\overline{\text{DDEN}}$. When $\overline{\text{DDEN}} = 0$ double density (MFM) is assumed. When $\overline{\text{DDEN}} = 1$, single density (FM) is assumed.

AM Detector—The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{\text{DAL}}$) and associated control signals. The $\overline{\text{DAL}}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{\text{DAL}}$ are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable ($\overline{\text{RE}}$) are active (low logic state) or act as input receivers when $\overline{\text{CS}}$ and Write Enable ($\overline{\text{WE}}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{\text{CS}}$ is made low. The address bits A1 and A0, combined with the signals $\overline{\text{RE}}$ during a Read operation or $\overline{\text{WE}}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{\text{RE}}$)	WRITE ($\overline{\text{WE}}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The 179X has two modes of operation according to the state of $\overline{\text{DDEN}}$ (Pin 37). When $\overline{\text{DDEN}}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

HEAD POSITIONING

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{\text{TEST}}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 µs (MFM) or 4 µs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 µs before the first stepping pulse is generated.

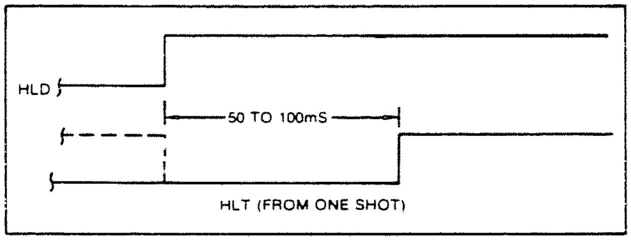
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

Table 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{\text{DDEN}}$	0	1	0	1	x	x
R1 R0	$\overline{\text{TEST}}$=1	$\overline{\text{TEST}}$=1	$\overline{\text{TEST}}$=1	$\overline{\text{TEST}}$=1	$\overline{\text{TEST}}$=0	$\overline{\text{TEST}}$=0
0 0	3 ms	3 ms	6 ms	6 ms	184µs	368µs
0 1	6 ms	6 ms	12 ms	12 ms	190µs	380µs
1 0	10 ms	10 ms	20 ms	20 ms	198µs	396µs
1 1	15 ms	15 ms	30 ms	30 ms	208µs	416µs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations, the FD179X requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{\text{WF}}/\overline{\text{VFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$ = 1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

Table 2. COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	F_2	E	F_1	0
II	Write Sector	1	0	1	m	F_2	E	F_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrrupt	1	1	0	1	I_3	I_2	I_1	I_0

Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I COMMANDS

h = Head Load Flag (Bit 3)

h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on destination track
V = 0, No verify

$r_1 r_0$ = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

Table 4. FLAG SUMMARY

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

a_0 = Data Address Mark (Bit 0)

a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)

E = 1, 15 ms delay
E = 0, no 15 ms delay

(F_2) S = Side Select Flag (1791/3 only)

S = 0, Compare for Side 0
S = 1, Compare for Side 1

(F_1) C = Side Compare Flag (1791/3 only)

C = 0, disable side select compare
C = 1, enable side select compare

(F_1) S = Side Select Flag

(Bit 1, 1795/7 only)

S = 0 Update SSO to 0
S = 1 Update SSO to 1

(F_2) b = Sector Length Flag

(Bit 3, 1975/7 only)

	Sector Length Field			
	00	01	10	11
b = 0	256	512	1024	128
b = 1	128	256	512	1024

Table 5. FLAG SUMMARY

TYPE IV COMMAND

Ii = Interrupt Condition flags (Bits 3-0)

I0 = 1, Not-Ready to Ready Transition
I1 = 1, Ready to Not-Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate Interrupt
$I_3 - I_0$ = 0, Terminate with no Interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field ($r_0 r_1$), which determines the stepping motor rate as defined in Table 1

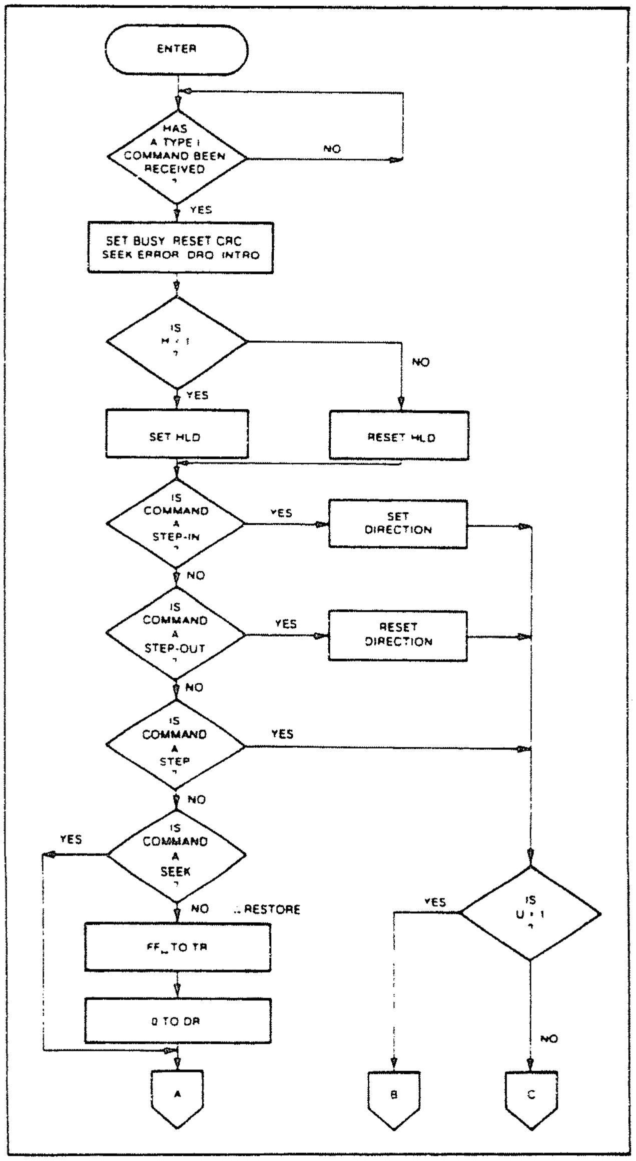
The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD179X receives a command that specifically disengages the head. If the FD179X is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

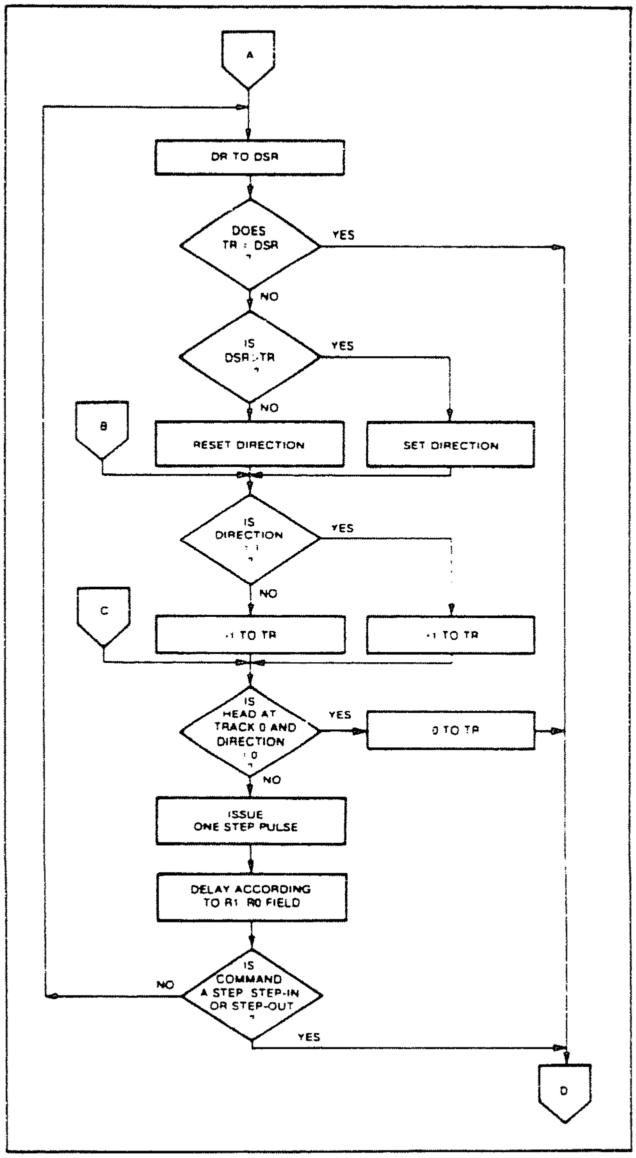
During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD179X terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.



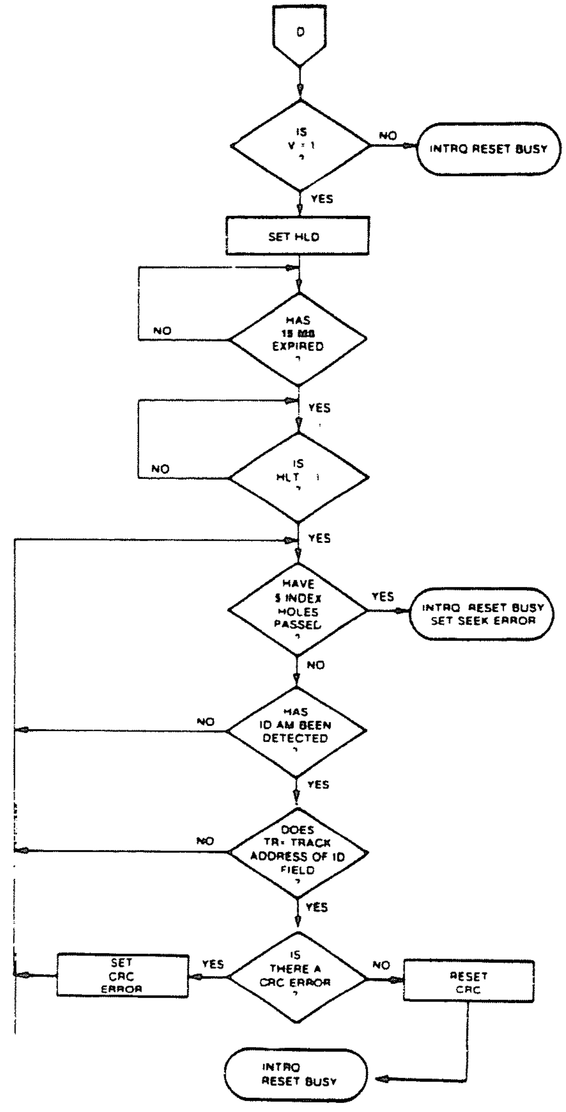
TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{\text{TROO}}$) input is sampled. If $\overline{\text{TROO}}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{\text{TROO}}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{\text{TROO}}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{\text{TROO}}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{\text{MR}}$ goes from an active to an inactive state.



NOTE: IF $\overline{\text{TEST}}$ = 0 THERE IS NO 15MS DELAY
IF $\overline{\text{TEST}}$ = 1 AND CLK = 1 MHz THERE IS A 30MS DELAY

TYPE I COMMAND FLOW

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

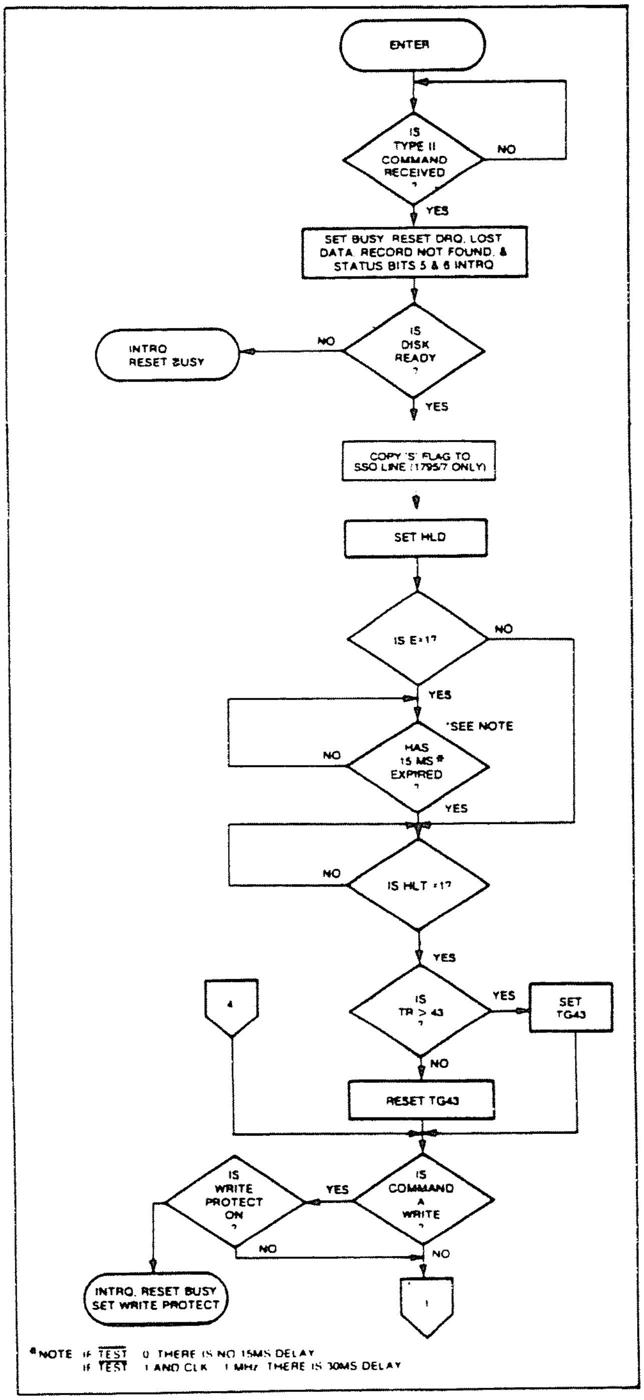
STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

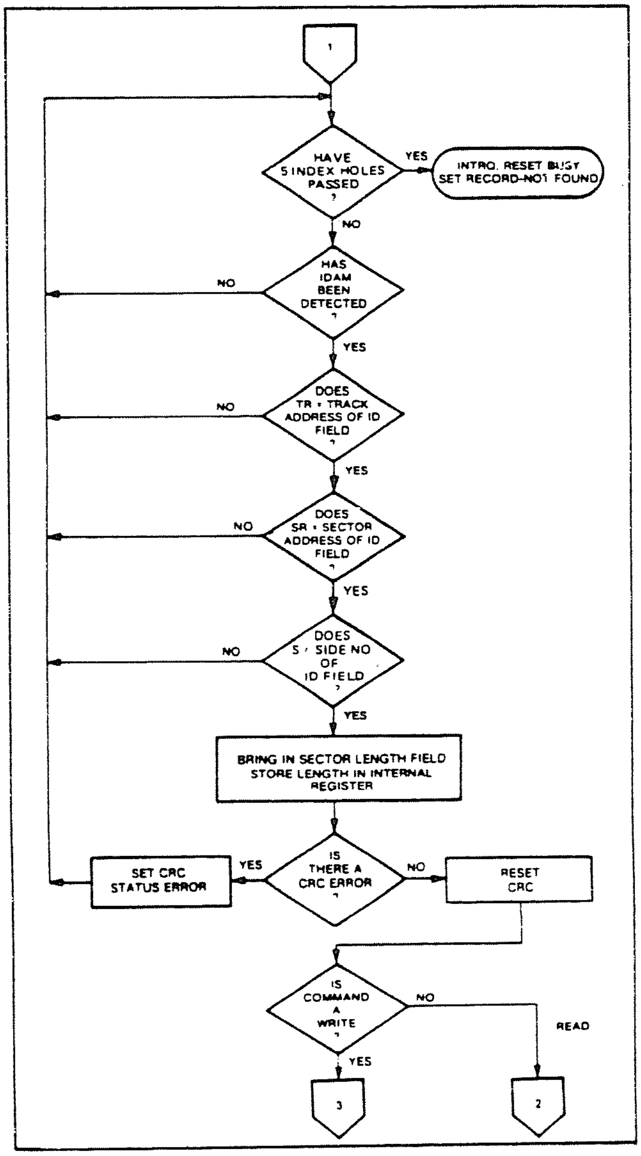
When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.



TYPE II COMMAND

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register until the sector regis-



TYPE II COMMAND

ter exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

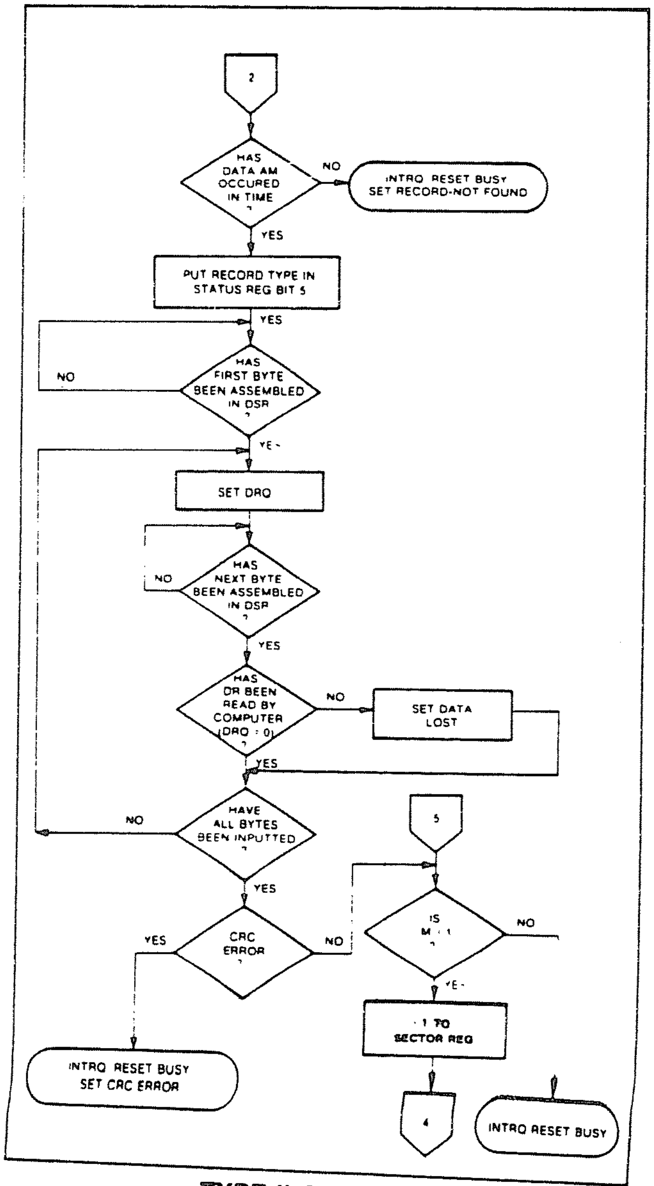
The Type II commands also contain side select compare flags. When C = 0, no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

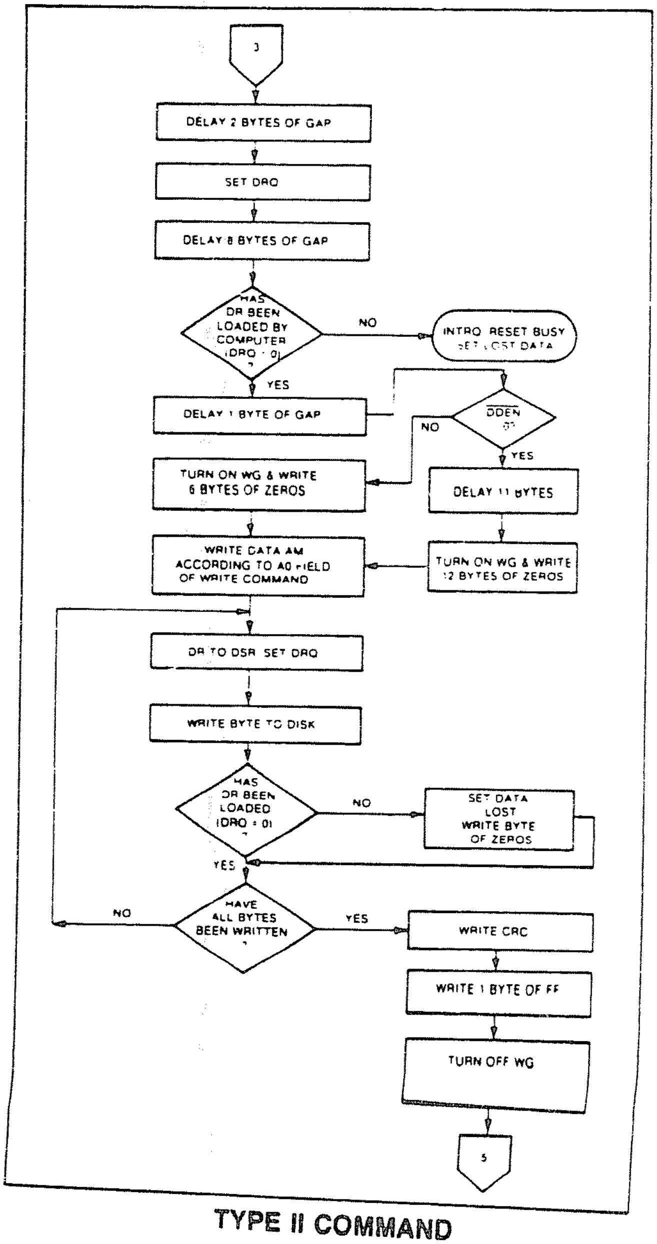
READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and



TYPE II COMMAND



TYPE II COMMAND

the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

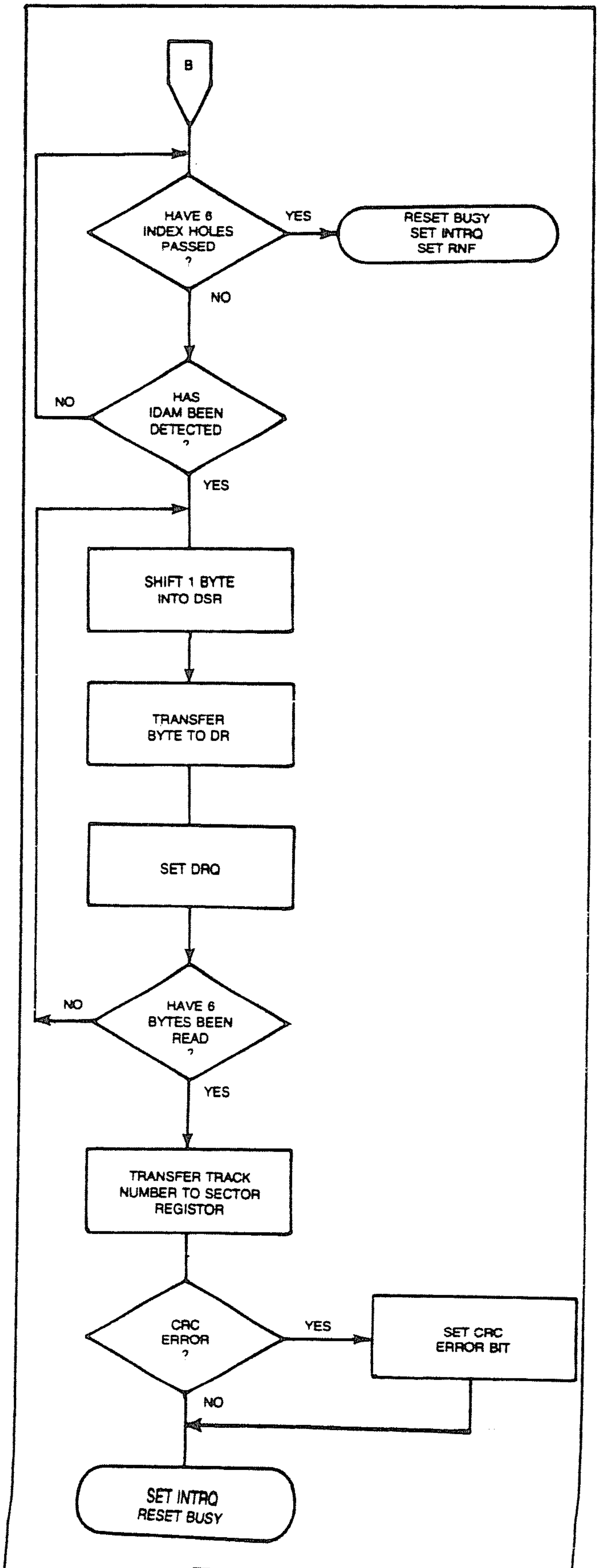
Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

<table>
<tr><td>GAP III</td><td>ID AM</td><td>TRACK NUMBER</td><td>SIDE NUMBER</td><td>SECTOR NUMBER</td><td>SECTOR LENGTH</td><td>CRC 1</td><td>CRC 2</td><td>GAP II</td><td>DATA AM</td><td>DATA FIELD</td><td>CRC 1</td><td>CRC 2</td></tr>
<tr><td colspan="10">ID FIELD</td><td colspan="3">DATA FIELD</td></tr>
</table>

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.



TYPE III COMMAND
Read Track/Address

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt (requires reset, see Note)

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. *This is the only command that will enable the immediate interrupt to clear on a subsequent Load Command Register or Read Status Register.*

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

Table 6. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

WESTERN DIGITAL
C O R P O R A T I O N

WD1691 FLOPPY SUPPORT LOGIC (F.S.L.)

October, 1980

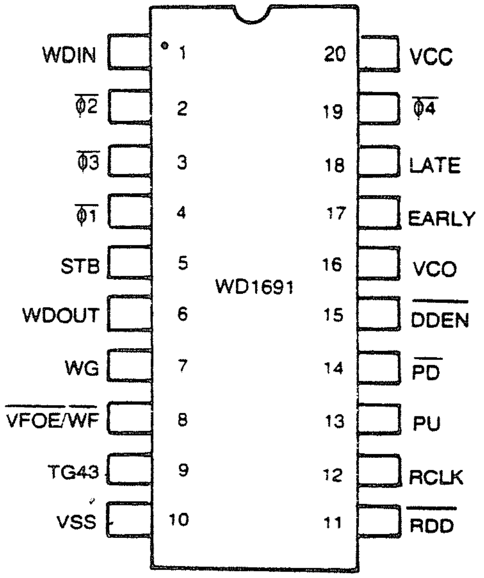
FEATURES

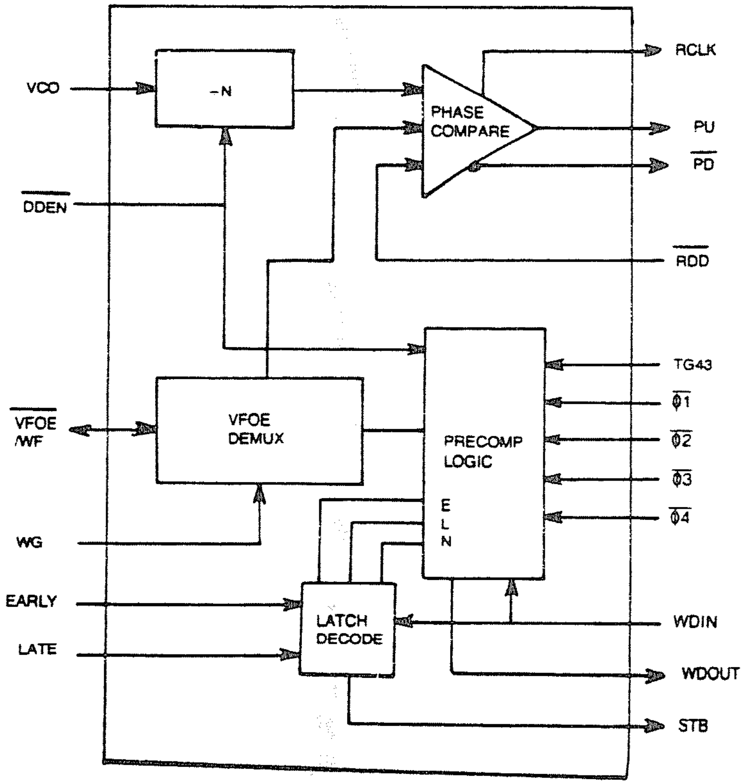
- Direct interface to the FD179X
- Eliminates external FDC Logic
- Data Separation/RCLK GENERATION
- Write Precompensation Signals
- VFOE/WF Demultiplexing
- Programmable Density
- 8" or 5.25" Drive Compatible
- All inputs and outputs TTL Compatible
- Single +5V Supply

GENERAL DESCRIPTION

The WD1691 F.S.L. has been designed to minimize the external logic required to interface the 179X Family of Floppy Disk Controllers to a drive. With the use of an external VCO, the WD 1691 will generate the RCLK signal for the WD179X, while providing an adjustment pulse (PUMP) to control the VCO frequency. VFOE/WF de-multiplexing is also accomplished and Write Precompensation signals have been included to interface directly with the WD2143 Clock Generator.

The WD1691 is implemented in N-MOS silicon gate technology and is available in a plastic or ceramic 20 pin dual-in-line package.





BLOCK DIAGRAM

PIN	NAME	SYMBOL	FUNCTION
1	WRITE DATA INPUT	WDIN	Ties directly to the FD179X WD pin.
2, 3, 4,19	PHASE 2, 3, 1, 4	$\overline{\phi 2}$ $\overline{\phi 3}$ $\overline{\phi 1}$ $\overline{\phi 4}$	4 Phase inputs to generate a desired Write Precompensation delay. These signals tie directly to the WD2143 Clock Generator.
5	STROBE	STB	Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of Ø4.
6	WRITE DATA OUTPUT	WDOUT	Serial, pre-compensated Write data stream to be sent to the disk drive's WD line.
7	WRITE GATE	WG	Ties directly to the FD179X WG pin.
8	VFO ENABLE/ WRITE FAULT	$\overline{\text{VFOE}}/\overline{\text{WF}}$	Ties directly to the FD179X $\overline{\text{VFOE}}/\overline{\text{WF}}$ pin.
9	TRACK 43	TG43	Ties directly to the FD179X TG43 pin, If Write Precompensation is required on TRACKS 44-76.
10	V_{ss}	V_{ss}	Ground
11	READ DATA	$\overline{\text{RDD}}$	Composite clock and data stream input from the drive.
12	READ CLOCK	RCLK	RCLK signal generated by the WD1691, to be tied to the FD179X RCLK pin.
13	PUMP UP	PU	Tri-state output that will be forced high when the WD1691 requires an increase in VCO frequency.
14	PUMP DOWN	$\overline{\text{PD}}$	Tri-state output that will be forced low when the WD1691 required a decrease in VCO frequency.
15	Double Density Enable	$\overline{\text{DDEN}}$	Double Density Select input. When Inactive (High), the VCO frequency is internally divided by two.
16	Voltage Controlled Oscillator	VCO	A nominal 4.0MHz (8" drive) or 2.0MHz (5.25" drive) master clock input.
17, 18	EARLY LATE	EARLY LATE	EARLY and LATE signals from the FD179X, used to determine Write Precompensation.
20	V_{cc}	V_{cc}	+ 5V ± 10% power supply

DEVICE DESCRIPTION

The WD1691 is divided into two sections:

1) Data Recovery Circuit
2) Write precompensation Circuit

The Data Separator or Recovery Circuit has four inputs: DDEN, VCO, RDD, and VFOE/WF; and three outputs: PU, PD and RCLK. The VFOE/WF input is used in conjunction with the Write Gate signal to enable the Data recovery circuit. When Write Gate is high, a write operation is taking place, and the data recovery circuits are disabled, regardless of the state on any other inputs.

When VFOE/WF and WRITE GATE are low, the data recovery circuit is enabled. When the RDD line goes Active Low, the PU or PD signals will become active. If the RDD line has made its transition in the beginning of the RCLK window, PU will go from a HI-Z state to a Logic I, requesting an *increase* in VCO frequency. If the RDD line has made its transition at the end of the RCLK window, PU will remain in a HI-Z state while PD will go to a logic zero, requesting a *decrease* in VCO frequency. When the leading edge of RDD occurs in the center of the RCLK window, both PU and PD will remain tri-stated, indicating that no adjustment of the VCO frequency is needed. The RCLK signal is a divide-by-16 (DDEN=1) or a divide-by-8 (DDEN=0) of the VCO frequency.

WG	VFOE/WF	RDD	PU+PD
1	X	X	HI-Z
0	1	X	HI-Z
0	0	1	HI-Z
0	0	0	Enable

The Write Precompensation circuit has been designed to be used with the WD2143-01 clock generator. When the WD1691 is operated in a "single density only" mode, write precompensation as well as the WD2143-01 is not needed. In this case, φ1, φ2, φ3, φ4, and STB should be tied together, DDEN left open, and TG43 tied to ground.

In the double-density mode (DDEN=0), the signals Early and Late are used to select a phase input (φ1 – φ4) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143-01 to start its pulse generation. φ2 is used as the write data pulse on nominal (Early=Late=φ), φ2 is used for early, and φ3 is used for late. The leading edge of φ4 resets the STB line in anticipation of the next write data pulse. When TG43=0 or DDEN=1, Precompensation is disabled and any transitions on the WDIN line will appear on the WDout line. If write precompensation is desired on all tracks, leave TG43 open (an internal pull-up will force a Logic I) while DDEN=0.

The signals, DDEN, TG43, and RDD have internal pull-up resistors and may be left open if a logic I is desired on any of these lines.

The minimum Voh level on PU is specified at 2.4V, sourcing 200ua. During PUMP UP time, this output will "drift" from a tri-state to .4V minimum. By tying PU and PD together, a PUMP signal is created that will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider can be used to set the tri-state level to approximately 1.4V. This yields a worst case swing of ± 1V; acceptable for most VCO chips with a linear voltage-to-frequencv characteristic.

Both PU and PD signals are affected by the width of the RAW READ (RDD) pulse. The wider the RAW READ pulse, the longer the PU or PD signal (depending upon the phase relationship to RCLK) will remain active. If the RAW READ pulse exceeds 250ns. (VCO = 4MHz, DDEN = 0) or 500ns. (VCO = 4MHz, DDEN = 1), then both a PU and PD will occur in the same window. This is undesirable and reduces the accuracy of the external integrator or low-pass filter to convert the PUMP signals into a slow moving D.C. correction voltage.

Eventually, the PUMP signals will have corrected the VCO input to exactly the same frequency multiple as the RAW READ signal. The leading edge of the RAW READ pulse will then occur in the exact center of the RCLK window, and ideal condition for the FD179X internal recovery circuits.

WESTERN DIGITAL

C O R P O R A T I O N

FD179X Application Notes

JUNE, 1980

INTRODUCTION

Over the past several years, the Floppy Disk Drive has become the most popular on-line storage device for mini and microcomputer systems. Its fast access time, reliability and low cost-per-bit ratio enables the Floppy Disk Drive to be *the* solution in mass storage for microprocessor systems. The drive interface to the Host system is standardized, allowing the OEM to substitute one drive for another with minimum hardware/ software modifications.

Since Floppy Disk Data is stored and retrieved as a self-clocking serial data stream, some means of separating the clock from the data and assembling this data in parallel form must be accomplished. Data is stored on individual Tracks of the media, requiring control of a stepper motor to move the Read/Write head to a predetermined Track. Byte sychronization must also be accomplished to insure that the parallel data is properly assembled. After all the design considerations are met, the final controller can consist of 40 or more TTL packages.

To alleviate the burden of Floppy Disk Controller design, Western Digital has developed a Family of LSI Floppy Disk controller devices. Through its own set of macro commands, the FD179X Controller Family will perform all the functions necessary to read and write data to the drive. Both the 8" standard and 5¼" mini-floppy are supported with single or double density recording techniques. The FD179X is compatible with the IBM 3740 (FM) data format, or the System 34 (MFM) standards. Provisions for non-standard formats and variable sector lengths have been included to provide more storage capability per track. Requiring standard +5, +12 power supplies the FD179X is available in a standard 40 pin dual-in-line package.

The FD179X Family consists of 6 devices. The differences between these devices is summarized in Figure 1. The 1792 and 1794 are "single density only" devices, with the Double Density Enable pin (DDEN) left open by the user. Both True and inverted Data bus devices are available. Since the 179X can only drive one TTL Load, a true data bus system may use the 1791 with external inverting buffers to arrive at a true bus scheme. The 1795 and 1797 are identical to the 1791 and 1793, except a side select output has been added that is controlled through the Command Register.

SYSTEM DESIGN

The first consideration in Floppy Disk Design is to determine which type of drive to use. The choice ranges from single-density single sided mini-floppy to the 8" double-density double-sided drive. Figure 2 illustrates the various drive and data capacities associated with each type. Although the 8" double-density drive offers twice as much storage, a more complex data separator and the addition of Write Precompensation circuits are mandatory for reliable data transfers. Whether to go with 8" double-density or not is dependent upon PC board space and the additional circuitry needed to accurately recover data with extreme bit shifts. The byte transfer time defines the nominal time required to transfer one byte of data from the drive. If the CPU used cannot service a byte in this time, then a DMA scheme will probably be required. The 179X also needs a few microseconds for overhead, which is subtracted from the transfer time. Figure 3 shows the actual service times that the CPU must provide on a byte-by-byte basis. If these times are not met, bytes of data will be lost during a read or write operation. For each byte transferred, the 179X generates a DRQ (Data Request) signal on Pin 38. A bit is provided in the status register which is also set upon receipt of a byte from the Disk. The user has the option of reading the status register through program control or using the DRQ Line with DMA or interrupt schemes. When the data register is read, both the status register DRQ bit and the DRQ Line are automatically reset. The next full byte will again set the DRQ and the process continues until the sector(s) are read. The Write operation works exactly the same way, except a WRITE to the Data Register causes a reset of both DRQ's.

RECORDING FORMATS

The FD179X accepts data from the disk in a Frequency-Modulated (FM) or Modified-Frequency-Modulated (MFM) Format. Shown in Figures 4A and 4B are both these Formats when writing a Hexidecimal byte of 'D2'. In the FM mode, the 8 bits of data are broken up into "bit cells." Each bit cell begins with a clock pulse and the center of the bit cell defines the data. If the data bit = 0, no pulse is written; if the data = 1, a pulse is written in the center of the cell. For the 8" drive, each clock is written 4 microseconds apart.

FIGURE 1. DEVICE CHARACTERISTICS

DEVICE	SNGL DENSITY	DBLE DENSITY	INVERTED BUS	TRUE BUS	DOUBLE-SIDED
1791	X	X	X		
1792	X		X		
1793	X	X		X	
1794	X			X	
1795	X	X	X		X
1797	X	X		X	X

FIGURE 2. STORAGE CAPACITIES

SIZE	DENSITY	SIDES	UNFORMATTED CAPACITY (NOMINAL)		BYTE TRANSFER TIME	FORMATTED CAPACITY	
			PER TRACK	PER DISK		PER TRACK	PER DISK
5¼″	SINGLE	1	3125	109,375*	64µs	2304**	80,640
5¼″	DOUBLE	1	6250	218,750	32µs	4608***	161,280
5¼″	SINGLE	2	3125	218,750	64µs	2304	161,280
5¼″	DOUBLE	2	6250	437,500	32µs	4608	322,560
8″	SINGLE	1	5208	401,016	32µs	3328	256,256
8″	DOUBLE	1	10,416	802,032	16µs	6656	512,512
8″	SINGLE	2	5208	802,032	32µs	3328	512,512
8″	DOUBLE	2	10,416	1,604,064	16µs	6656	1,025,024

*Based on 35 Tracks/Side
**Based on 18 Sectors/Track (128 byte/sec)
***Based on 18 Sectors/Track (256 bytes/sec)

In the MFM mode, clocks are decoded into the data stream. The byte is again broken up into bit cells, with the data bit written in the center of the bit cell if data = 1. Clocks are only written if both surrounding data bits are zero. Figure 4B shows that this occurs only once between Bit cell 4 and 5. Using this encoding scheme, pulses can occur 2, 3 or 4 microseconds apart. The bit cell time is now 2 microseconds; twice as much data can be recorded without increasing the Frequency rate due to this encoding scheme.

The 179X was designed to be compatible with the IBM 3740 (FM) and System 34 (MFM) Formats. Although most users do not have a need for data exchange with IBM mainframes, taking advantage of these well studied formats will insure a high degree of system performance. The 179X will allow a change in gap fields and sector lengths to increase usable storage capacity, but variations away from these standards is not recommended. Both IBM standards are soft-sector format. Because of the wide variation in address marks, the 179X can only support soft-sectored media. Hard sectored diskettes have continued to lose popularity, mainly due to the unavailability of a standard and the limitation of sector lengths imposed by the physical sector holes in the diskette.

PROCESSOR INTERFACE

The Interface of the 179X to the CPU consists of an 8-bit Bi-directional bus, read/write controls and optional interrupt lines. By selecting the device via the CHIP SELECT Line, each of the five internal registers can be accessed.

Shown below are the registers and their addresses:

PIN 3 CS	PIN 6 A_1	PIN 5 A_0	PIN 4 $\overline{RE}=0$	PIN 2 $\overline{WE}=0$
0	0	0	STATUS REG	COMMAND REG
0	0	1	TRACK REG	TRACK REG
0	1	0	SECTOR REG	SECTOR REG
0	1	1	DATA REG	DATA REG
1	X	X	H1-Z	H1-Z

Each time a command is issued to the 179X, the Busy bit is set and the INTRQ (Interrupt Request) Line is reset. The user has the option of checking the busy bit or use the INTRQ Line to denote command completion. The Busy bit will be reset whenever the 179X is idle and awaiting a new command. The INTRQ Line, once set, can only be reset by a READ of the status register or issuing a new command. The MR (Master Reset) Line does not affect INTRQ.

The A_0, A_1, Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU address lines, in which case the 179X will be memory-mapped and addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6820, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the 179X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

OPERATION	NEXT OPERATION	DELAY REQ'D
WRITE TO COMMAND REG	READ STATUS REGISTER	MFM = $14\mu s$* FM = $28\mu s$.
WRITE TO ANY REGISTER	READ FROM A DIFFERENT REG	NO DELAY

*NOTE: Times Double when CLK = 1MHz (5¼" drive)

Other CPU interface lines are CLK, $\overline{\text{MR}}$ and $\overline{\text{DDEN}}$. The CLK line should be 2MHz (8" drive) or 1MHz (5¼" drive) with a 50% duty cycle. Accuracy should be ±1% (crystal source) since all internal timing, including stepping rates, are based upon this clock.

The $\overline{\text{MR}}$ or Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a restore command (Hex '03') on the rising edge. A quicker stepping rate can be written to the command register after a $\overline{\text{MR}}$, in which case the remaining steps will occur at the faster programmed rate. The 179X will issue a maximum of 255 stepping pulses in an attempt to expect the $\overline{\text{TROO}}$ line to go active low. This line should be connected to the drive's $\overline{\text{TROO}}$ sensor.

The $\overline{\text{DDEN}}$ line causes selection of either single density ($\overline{\text{DDEN}}$ = 1) or double density operation. $\overline{\text{DDEN}}$ should not be switched during a read or write operation.

FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection to the drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs from the 179X. Inputs to the 179X may be buffered or tied to the Drives outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed −0.3 volts, while integrity of V_{IH} and V_{OH} levels should be kept within spec.

MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with a period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the $\overline{\text{IP}}$ or Index Pulse. This Line is tied to the drives' Index L.E.D. *sensor* and makes an active transition for each revolution of the diskette. The $\overline{\text{TR00}}$ Line is another L.E.D. sensor that informs the 179X that the stepper motor is at its furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open", Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The 179X will look at the ready signal prior to executing READ/WRITE commands. READY is *not* inspected during any Type I commands. All Type I commands will execute regardless of the Logic Level on this Line.

WRITE SIGNALS

Writing of data is accomplished by the use of the WD, WG, WF, TG43, EARLY and LATE Lines. The WG or Write Gate Line is used to enable write current at the drive's R/W head. It is made active prior to writing data on the disk. The WF or WRITE FAULT Line is used to inform the 179X of a failure in drive electronics. This signal is multiplexed with the VFOE Line and must be logically separated if required.

The TG43 or "TRACK GREATER than 43" Line is used to decrease the Write current on the inner tracks, where bit densities are the highest. If not required on the drive, TG43 may be left open.

WRITE PRECOMPENSATION

The 179X provides three signals for double density Write-Precompensation use. These signals are WRITE DATA, EARLY and LATE. When using single density drives (eighter 8" or 5¼"), Write Precompensation is not necessary and the WRITE DATA line is generally TTL Buffered and sent directly to the drive. In this mode, EARLY and LATE are left open.

For double density use, Write Precompensation is a function of the drive. Some manufacturers recommend Precompensating the 5¼" drive, while others do not. With the 8" drive, Precompensation may be specified from TRACK 43 on, or in most cases, all TRACKS. If the recommended Precompensation is not specified, check with the manufacturer for the proper configuration required.

The amount of Precompensation time also varies. A typical value will usually be specified from 100-300ns. Regardless of the parameters used, Write Precompensation must be done external to the 179X. When $\overline{\text{DDEN}}$ is tied low, EARLY or LATE will be activated at least 125ns. before and after the Write Data pulse. An Algorithm internal the 179X decides whether to raise EARLY or LATE, depending upon the previous bit pattern sent. As an example, suppose the recommended Precomp value has been specified at 150ns. The following action should be taken:

EARLY	LATE	ACTION TAKEN
0	0	delay WD by 150ns (nominal)
0	1	delay WD by 300ns (2X value)
1	0	do not delay WD

DATA SEPARATION

The 179X has two inputs (RAW READ & RCLK) and one output (VFOE) for use by an external data separator. The RAW READ input must present clock and data pulses to the 179X, while the RCLK input provides a "window" or strobe signal to clock each RAW READ pulse into the device. An ideal Data Separator would have the leading edge of the RAW READ pulse occur in the exact center of the RCLK strobe.

Motor Speed Variation, Bit shifts and read amplifier recovery circuits all cause the RAW READ pulses to drift away from their nominal positions. As this occurs, the RAW READ pulses will shift left or right with respect to RCLK. Eventually, a pulse will make its transition outside of its RCLK window, causing either a CRC error or a Record-not-Found error at the 179X.

A Phase-Lock-Loop circuit is one method of achieving synchronization between the RCLK and RAW READ signals. As RAW READ pulses are fed to the PLL, minor adjustments of the free-running RCLK frequency can be made. If pulses are occurring too far apart, the RCLK frequency is *decreased* to keep synchronization. If pulses begin to occur closer together, RCLK is *increased* until this new higher frequency is achieved. In normal read operations, RCLK will be constantly adjusted in an attempt to match the incoming RAW READ frequency.

Another method of Data Separation is the Counter-Separator technique. The RCLK signal is again free-running at a nominal rate, until a RAW READ pulse occurs. The Separator then denotes the position of the pulse with respect to RCLK (by the counter value), and counts down to increase or decrease the current RCLK window. The next RCLK window will occur at a nominal rate and will continue to run at this frequency until another RAW READ pulse adjusts RCLK, but only the present window is adjusted.

Both PPL and Counter/Separator are acceptable methods of Data Separation. The PPL has the highest reliability because of its "tracking" capability and is recommended for 8" double density designs.

Figure 12 illustrates a Counter/Separator utilizing a PROM as the count generator. Depending upon the RAW READ phase relationship to RCLK, the PROM is addressed and its data output is used as the counter value. A 16MHz clock is required for 8" double density, while an 8MHz clock can be used for single density.

745288 PROGRAMMING TABLE

ADDRESS	DATA	ACTION TAKEN
00	01	NONE
01	01	RETARD BY 1 COUNT
02	02	
03	03	
04	03	RETARD BY 2 COUNTS
05	04	
06	05	
07	06	
08	0B	ADVANCE BY 2 COUNTS
09	0D	
0A	0C	
0B	0E	
0C	0F	
0D	0F	ADVANCE BY 1 COUNT
0E	00	
0F	01	
10	01	FREE RUN
11	02	
12	03	
13	04	
14	05	
15	06	
16	07	
17	08	
18	09	
19	0A	
1A	0B	
1B	0C	
1C	0D	
1D	0E	
1E	0F	
1F	00	

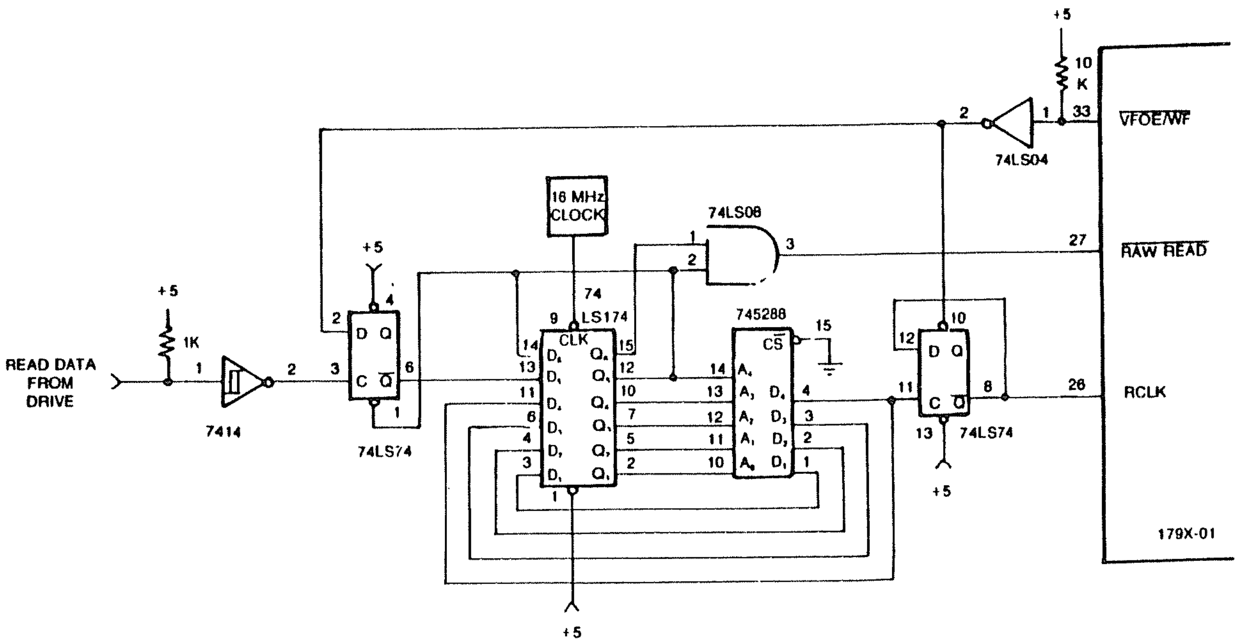
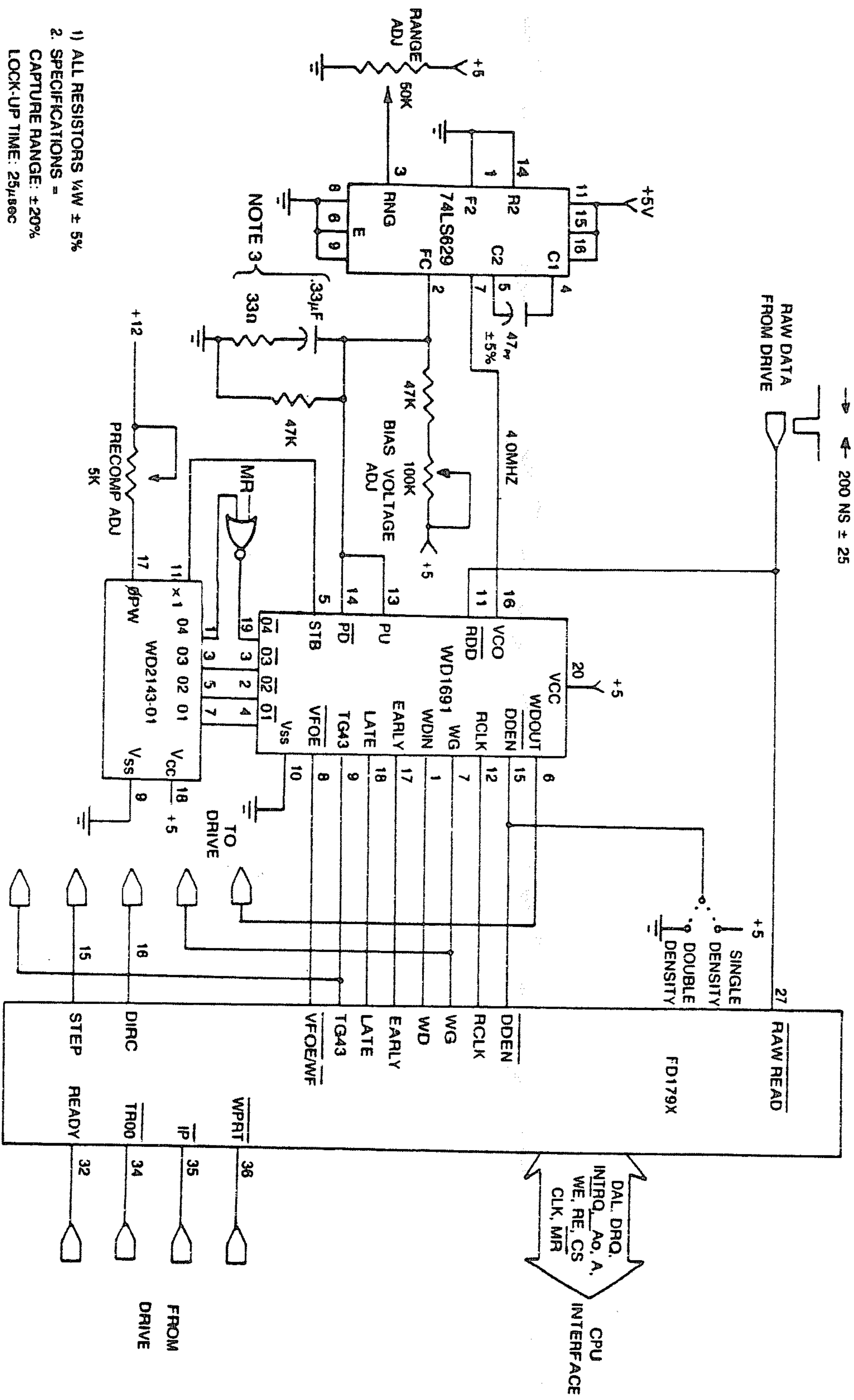


FIGURE 12. 179X DATA SEPARATOR

(PROVIDED COURTESY OF ANDROMEDA SYSTEMS, PANORAMA CITY, CA 91402)

Figure 14 illustrates a PPL data recovery circuit using the Western Digital 1691 Floppy Support device. Both data recovery and Write Precomp Logic is contained within the 1691, allowing low chip count and PLL reliability. The 74S124 supplies the free-running VCO output. The PUMP UP and PUMP DOWN signals from the 1691 are used to control the 74S124's frequency.



1) ALL RESISTORS ¼W ± 5%
2. SPECIFICATIONS =
CAPTURE RANGE: ±20%
LOCK-UP TIME: 25µsec
(ALL ONE'S PATTERN, MFM)
3) FOR

5 1/4"	8
68µf	.33µf
68Ω	33Ω

FIGURE 14. 8" SINGLE/DOUBLE DENSITY SYSTEM

ADVANCE INFORMATION

WESTERN DIGITAL
CORPORATION

WD2143-01 Four Phase Clock Generator

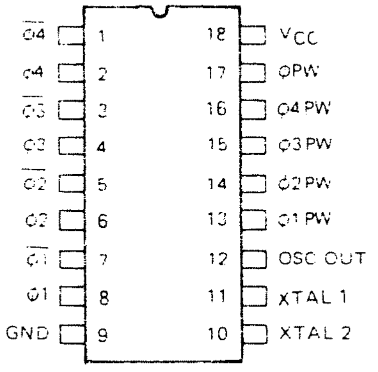
September 1980

FEATURES

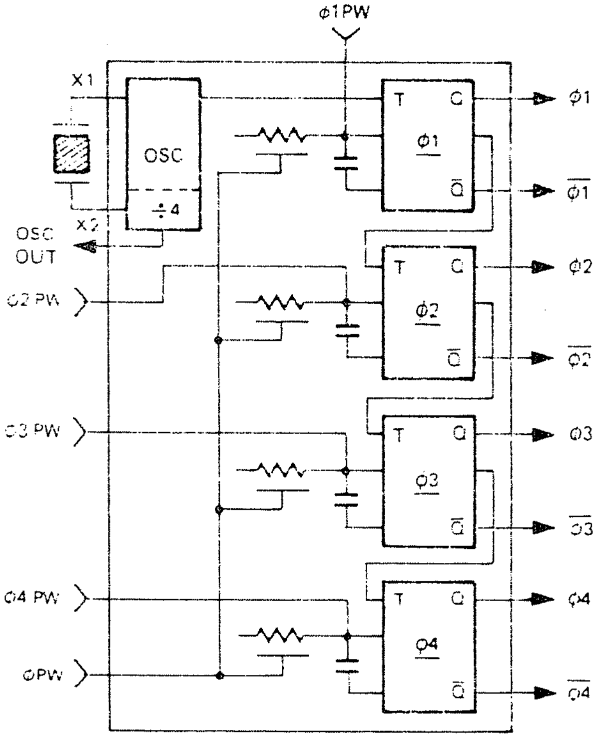
- TRUE AND INVERTED OUTPUTS
- SINGLE 5 VOLT SUPPLY
- TTL COMPATABLE
- ON CHIP OSCILLATOR
- XTAL OR TTL CLOCK INPUTS
- 3 MHz OPERATION
- TTL CLOCK OUTPUT
- PROGRAMMABLE PULSE WIDTHS
- PROGRAMMABLE PHASE WIDTHS
- NO EXTERNAL CAPACITOR
- NON-OVERLAPPING OUTPUTS

GENERAL DESCRIPTION

The WD2143-01 Four-Phase Clock Generator is a MOS/LSI device capable of generating four non-overlapping clocks. The output pulse widths are controlled by tying an external resistor to the proper control inputs. All pulse widths may be set to the same width by tying the ØPW line through an external resistor. Each pulse width can also be individually programmed by tying a resistor through the appropriate Ø1PW — Ø4PW control inputs. In addition, the OSC OUT line provides a TTL square wave output at a divide-by-four of the crystal frequency.



PIN CONNECTIONS



WD2143-01 BLOCK DIAGRAM

TTL
MSI

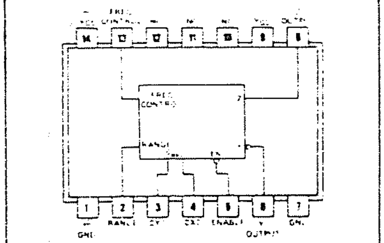
TYPES SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

D2501, JANUARY 1980 – REVISED OCTOBER 1980

- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Output Circuitry
- Highly Stable Operation over Specified Temperature and/or Supply Voltage Ranges

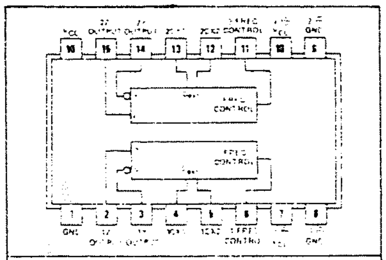
DEVICE TYPE	SIMILAR TO	NUMBER VCO's	COMP'L Z OUT	ENABLE	RANGE INPUT	R_{ext}
'LS624	'LS324	single	yes	yes	yes	no
'LS625	'LS325	dual	yes	no	no	no
'LS626	'LS326	dual	yes	yes	no	no
'LS627	'LS327	dual	no	no	no	no
'LS628	'LS324	single	yes	yes	yes	yes
'LS629	'LS124	dual	no	yes	yes	no

SN54LS' . . . J OR W PACKAGE
SN74LS' . . . J OR N PACKAGE
'LS624 (TOP VIEW)



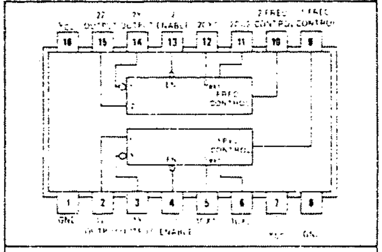
logic: see description

'LS625 (TOP VIEW)



logic: see description

'LS626 (TOP VIEW)



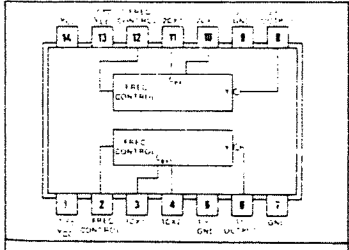
logic: see description

description

These voltage-controlled oscillators (VCO's) are improved versions of the original VCO family: SN54LS124, SN54LS324 thru SN54LS327, SN74LS124, and SN74LS324 thru SN74LS327. These new devices feature improved voltage-to-frequency linearity, range, and compensation. With the exception of the 'LS624 and 'LS628, all of these devices feature two independent VCO's in a single monolithic chip. The 'LS624, 'LS625, 'LS626 and 'LS628 have complementary Z outputs. The output frequency for each VCO is established by a single external component (either a capacitor or a crystal), in combination with voltage-sensitive inputs used for frequency control and frequency range. Each device has a voltage-sensitive input for frequency control; however, the 'LS624, 'LS628, and 'LS629 devices also have one for frequency range. (See Figures 1 thru 6).

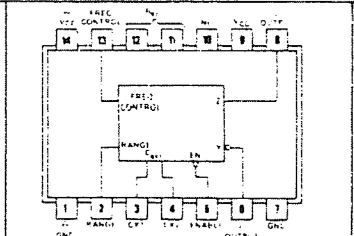
The 'LS628 features two $R_{external}$ pins that can offer more precise temperature compensation than its 'LS624 counterpart.

'LS627 (TOP VIEW)



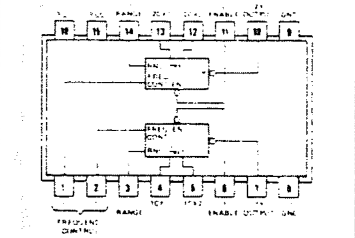
logic: see description

'LS628 (TOP VIEW)



logic: see description

'LS629 (TOP VIEW)



logic: see description

NC—No internal connection

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Figure 3 and Figure 6 contain the necessary information to choose the proper capacitor value to obtain the desired operating frequency.

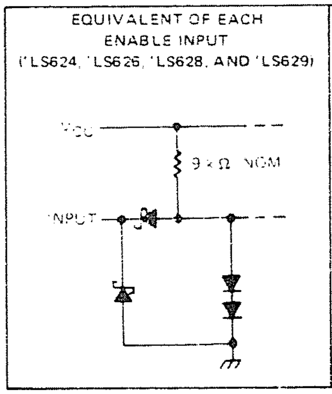
The devices can also be operated from a crystal by connecting a fundamental series resonant crystal across the C_{ext} pins. (Fundamental frequency ≤ 20 MHz.) The frequency control should be connected to 5 volts and, where applicable, the range control should also be connected to 5 volts.

A single 5-volt supply can be used; however, one set of supply voltage and ground pins (V_{CC} and Gnd) is provided for the enable, synchronization-gating, and output sections, and a separate set (⊝V_{CC} and ⊝Gnd) is provided for the oscillator and associated frequency-control circuits so that effective isolation can be accomplished in the system. For operation of frequencies greater than 10 MHz, it is recommended that two independent supplies be used. Disabling either VCO of the 'LS625 and 'LS627 can be achieved by removing the appropriate ⊝V_{CC}. An enable input is provided on the 'LS624, 'LS626, 'LS628 and 'LS629. When the enable input is low the output is enabled; when the enable input is high, the internal oscillator is disabled, Y is high, and Z is low. Caution! Crosstalk may occur in the dual devices ('LS625, 'LS626, 'LS627, and 'LS629) when both VCO's are operated simultaneously.

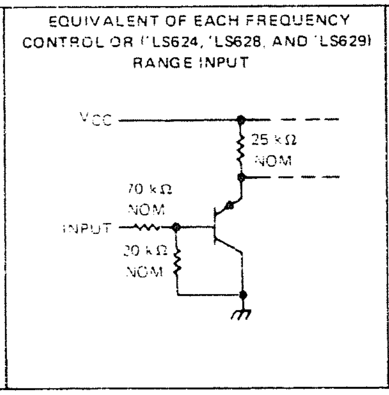
The pulse-synchronization-gating section ensures that the first output pulse is neither clipped nor extended. The duty cycle of the square-wave output is fixed at approximately 50 percent.

The SN54LS624 thru SN54LS629 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS624 thru SN74LS629 are characterized for operation from 0°C to 70°C.

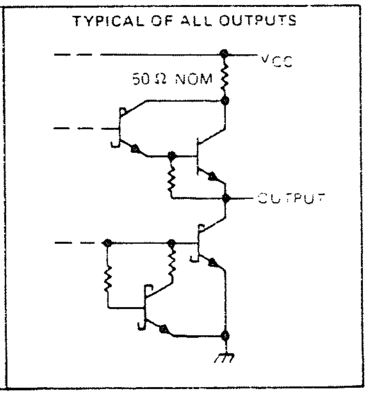
schematics of inputs and outputs



EQUIVALENT OF EACH ENABLE INPUT ('LS624, 'LS626, 'LS628, AND 'LS629)



EQUIVALENT OF EACH FREQUENCY CONTROL OR ('LS624, 'LS628, AND 'LS629) RANGE INPUT



TYPICAL OF ALL OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2)		7 V
Input voltage:	Enable input♦	7 V
	Frequency control or range input▲	V_{CC}
Operating free-air temperature range:	SN54LS' Circuits	−55°C to 125°C
	SN74LS' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

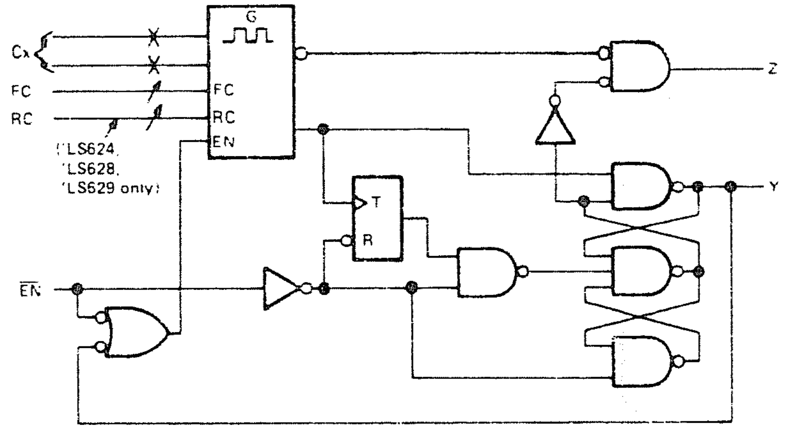
♦The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

▲The range input is provided only on 'LS624, 'LS628, and 'LS629.

NOTES: 1. Voltage values are with respect to the appropriate ground terminal.

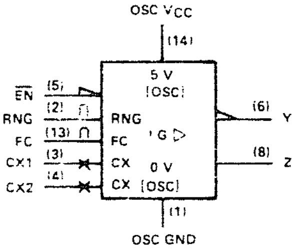
2. Throughout this data sheet, the symbol V_{CC} is used for the voltage applied to both the V_{CC} and ⊝ V_{CC} terminals, unless otherwise noted.

functional block diagram (positive logic)

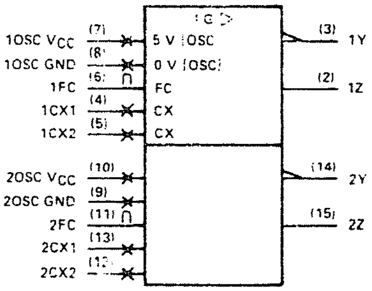


logic symbols†

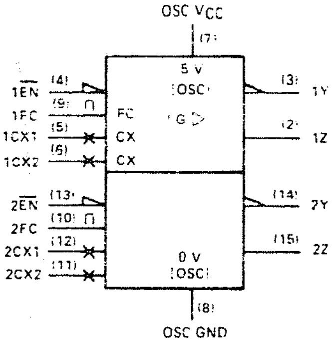
'LS624



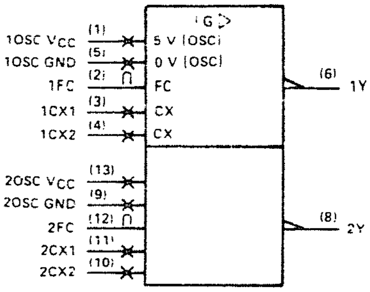
'LS625



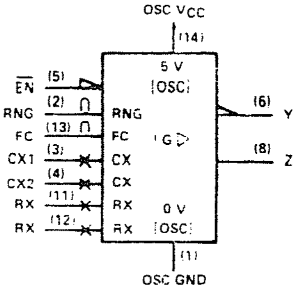
'LS626



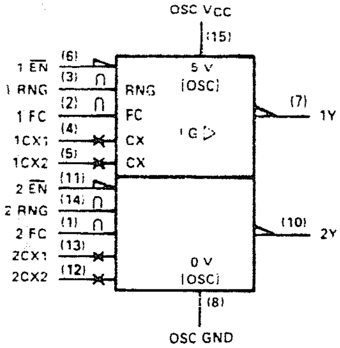
'LS627



'LS628



'LS629



MOTOROLA

MCM4116

MOS

(N-CHANNEL)

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4116 is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

By multiplexing row and column address inputs, the MCM4116 requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116 is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes.

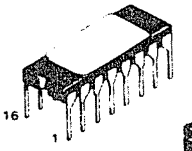
The MCM4116 incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses requiring a refresh cycle every 2 milliseconds.

- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 16,384 × 1 Organization
- ±10% Tolerance on All Power Supplies
- All Inputs are Fully TTL Compatible
- Three-State Fully TTL-Compatible Output
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation – 462 mW Active, 20 mW Standby (Max)
- Fast Access Time Options: 150 ns – MCM4116L-15, C-15
  200 ns – MCM4116L-20, C-20
  250 ns – MCM4116L-25, C-25
  300 ns – MCM4116L-30, C-30
- Easy Upgrade from 16-Pin 4K RAMs
- Pin Compatible with 2117, 2116, 6616, μPD416, and 4116

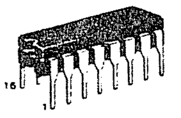
ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	-0.5 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

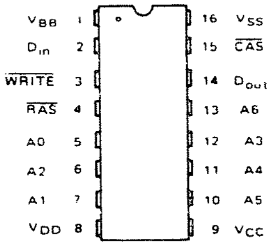


L SUFFIX
CERAMIC PACKAGE
CASE 690



C SUFFIX
FRIT-SEAL PACKAGE
CASE 620

PIN ASSIGNMENT



PIN NAMES

A0–A6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{in}	Data In
D_{out}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{BB}	Power (–5 V)
V_{CC}	Power (+5 V)
V_{DD}	Power (+12 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	Vdc	1
	V_{CC}	4.5	5.0	5.5	Vdc	1, 2
	V_{SS}	0	0	0	Vdc	1
	V_{BB}	-4.5	-5.0	-5.5	Vdc	1
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7	–	7.0	Vdc	1
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4	–	7.0	Vdc	1
Logic 0 Voltage, all inputs	V_{IL}	-1.0	–	0.8	Vdc	1

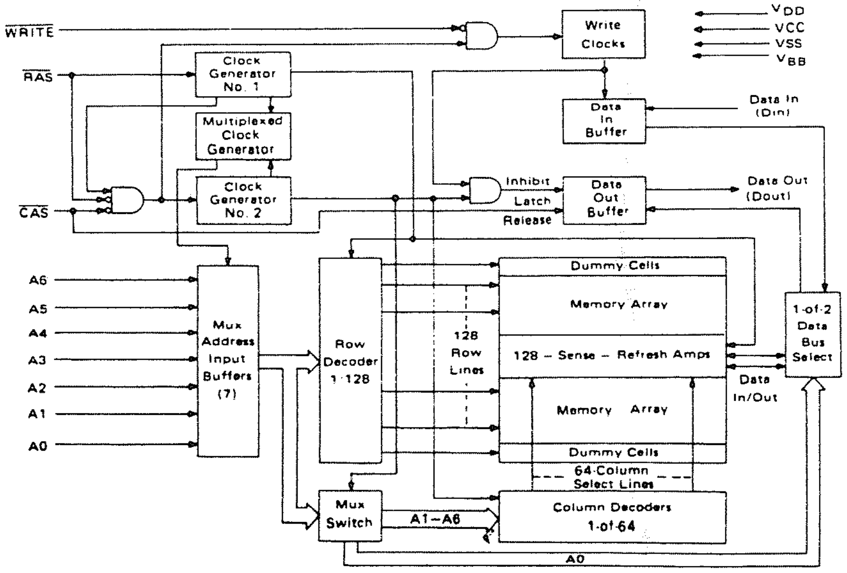
DC CHARACTERISTICS (V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}	–	35	mA	4
V_{CC} Power Supply Current	I_{CC}	–	–	mA	5
Average V_{BB} Power Supply Current	$I_{BB1,3}$	–	200	μA	
Standby V_{BB} Power Supply Current	I_{BB2}	–	100	μA	
Standby V_{DD} Power Supply Current	I_{DD2}	–	1.5	mA	6
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}	–	27	mA	4
Input Leakage Current (any input)	$I_{I(L)}$	–	10	μA	
Output Leakage Current	$I_{O(L)}$	–	10	μA	6, 7
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4	–	Vdc	2
Output Logic 0 Voltage @ I_{out} = 4.2 mA	V_{OL}	–	0.4	Vdc	

NOTES:

1. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
2. Output voltage will swing from V_{SS} to V_{CC} under open circuit conditions. For purposes of maintaining data in power down mode V_{CC} may be reduced to V_{SS} without affecting refresh operations. V_{OH}(min) specification is not guaranteed in this mode.
3. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate.
4. Current is proportional to cycle rate, maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
7. $0\ V \leq V_{out} \leq +5.5\ V$
8. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$

BLOCK DIAGRAM



AC OPERATING CONDITIONS AND CHARACTERISTICS (See Notes 3, 9, 14)

(Read, Write, and Read-Modify-Write Cycles)

RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = −5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

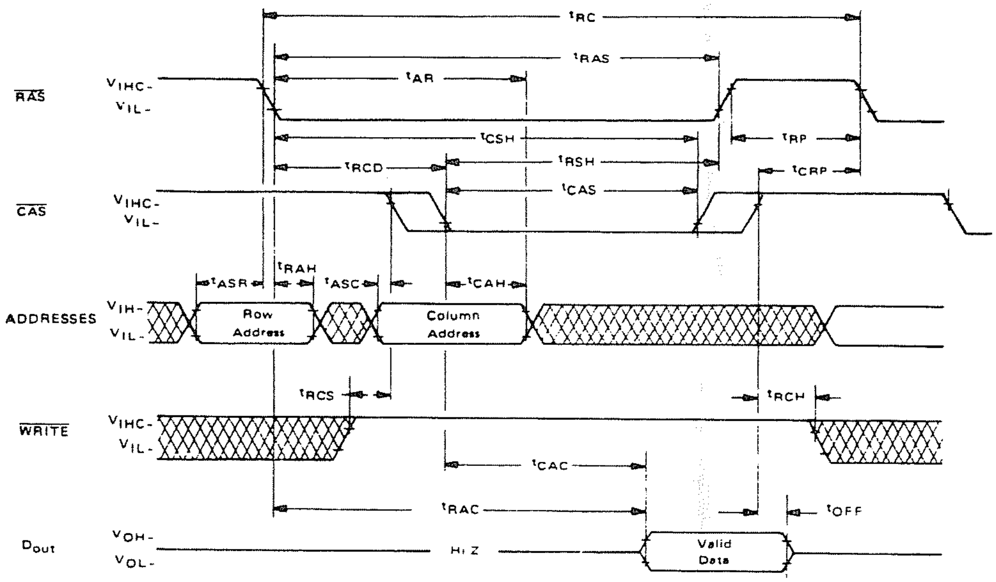
Parameter	Symbol	MCM4116-15		MCM4116-20		MCM4116-25		MCM4116-30		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	375	–	375	–	410	–	480	–	ns	
Read Write Cycle Time	t_{RWC}	375	–	375	–	515	–	660	–	ns	
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	–	250	–	300	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	90	–	135	–	165	–	200	ns	11, 12
Output Buffer and Turn-off Delay	t_{OFF}	0	40	0	50	0	60	0	60	ns	
Row Address Strobe Precharge Time	t_{RP}	100	–	120	–	150	–	180	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	150	10,000	200	10,000	250	10,000	300	10,000	ns	
Column Address Strobe Pulse Width	t_{CAS}	90	10,000	135	10,000	165	10,000	200	10,000	ns	
Row to Column Strobe Lead Time	t_{RCD}	20	60	25	65	35	85	60	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	20	–	25	–	35	–	60	–	ns	
Column Address Setup Time	t_{ASC}	−10	–	−10	–	−10	–	−10	–	ns	
Column Address Hold Time	t_{CAH}	45	–	55	–	75	–	100	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	105	–	120	–	160	–	200	–	ns	
Transition Time (Rise and Fall)	t_T	3.0	35	3.0	50	3.0	50	3.0	50	ns	14
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Write Command Hold Time	t_{WCH}	45	–	55	–	75	–	100	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	105	–	120	–	160	–	200	–	ns	
Write Command Pulse Width	t_{WP}	45	–	55	–	75	–	100	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	60	–	80	–	100	–	180	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	60	–	80	–	100	–	180	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	45	–	55	–	75	–	100	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	105	–	120	–	160	–	200	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100	–	135	–	165	–	200	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
$\overline{WRITE}$ Command Setup Time	t_{WCS}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	70	–	95	–	125	–	180	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	120	–	160	–	210	–	280	–	ns	16
$\overline{CAS}$ Precharge Time (Page mode cycle only)	t_{CP}	60	–	80	–	100	–	100	–	ns	
Page Mode Cycle Time	t_{PC}	170	–	225	–	275	–	325	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	150	–	200	–	250	–	300	–	ns	

Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A5), D_{in}	C_{I1}	4.0	5.0	pF	9
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8.0	10	pF	9
Output Capacitance (D_{out})	C_o	5.0	7.0	pF	7, 9

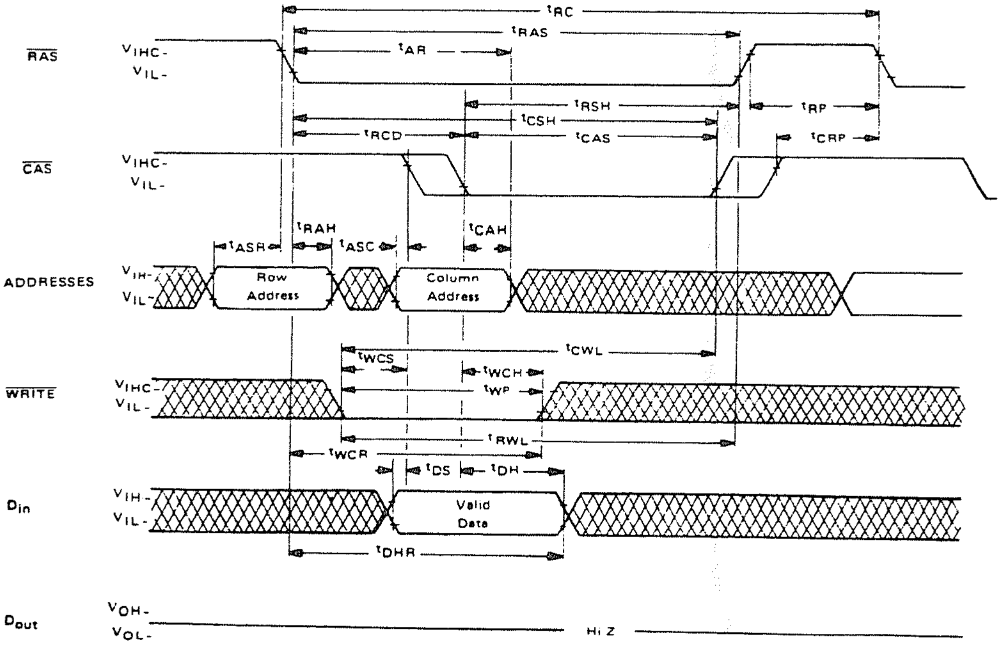
NOTES (continued)

9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} + t_T \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} + t_T \geq t_{RCD}$ (max).
12. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}
14. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transistion times are measured between V_{IHC} or V_{IH} and V_{IL}
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

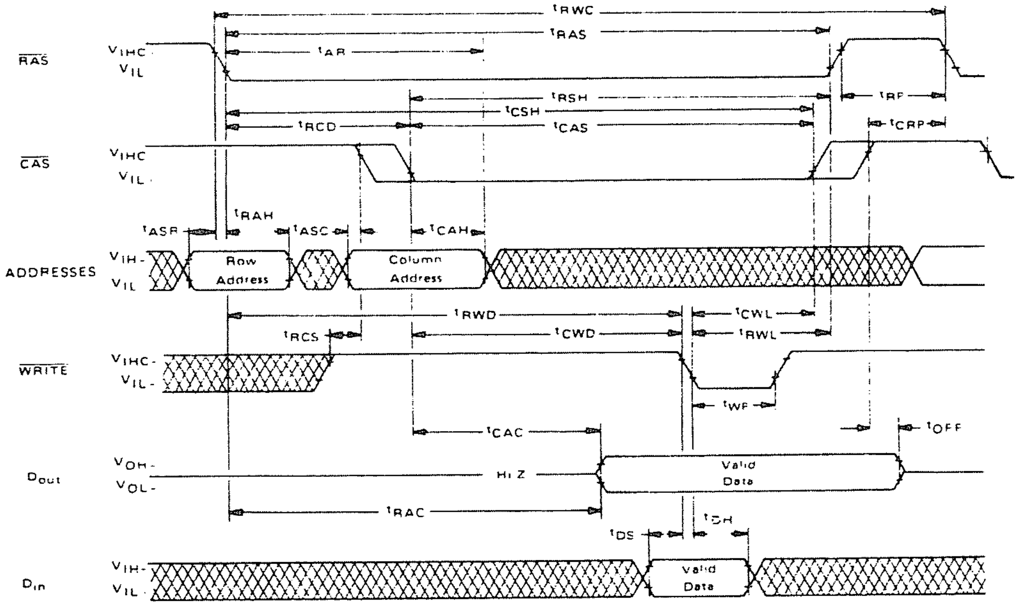
READ CYCLE TIMING



WRITE CYCLE TIMING

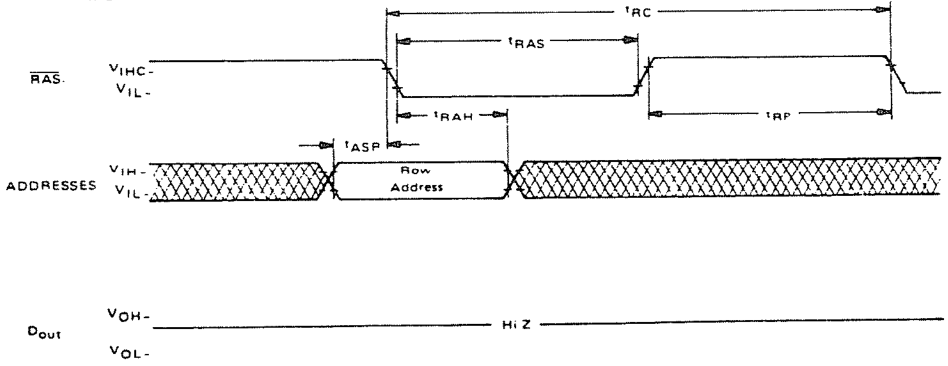


READ-WRITE/READ-MODIFY-WRITE CYCLE

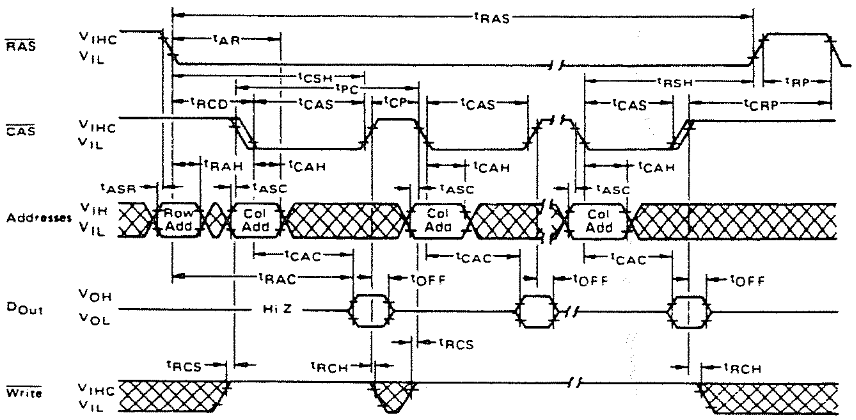


$\overline{RAS}$ ONLY REFRESH TIMING

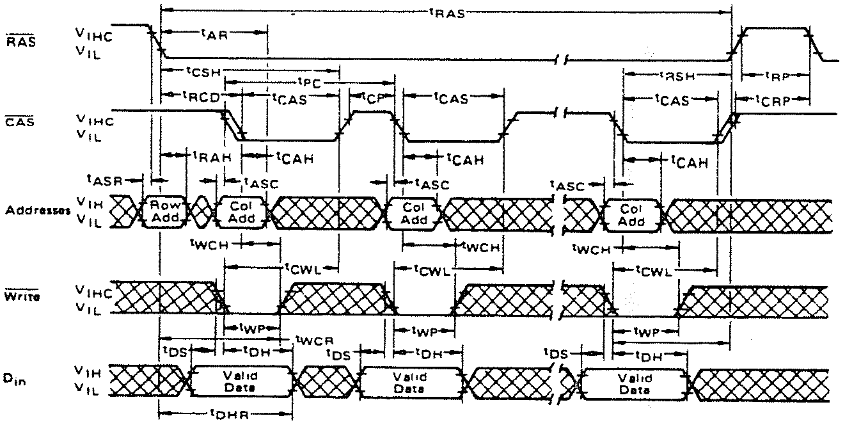
Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care



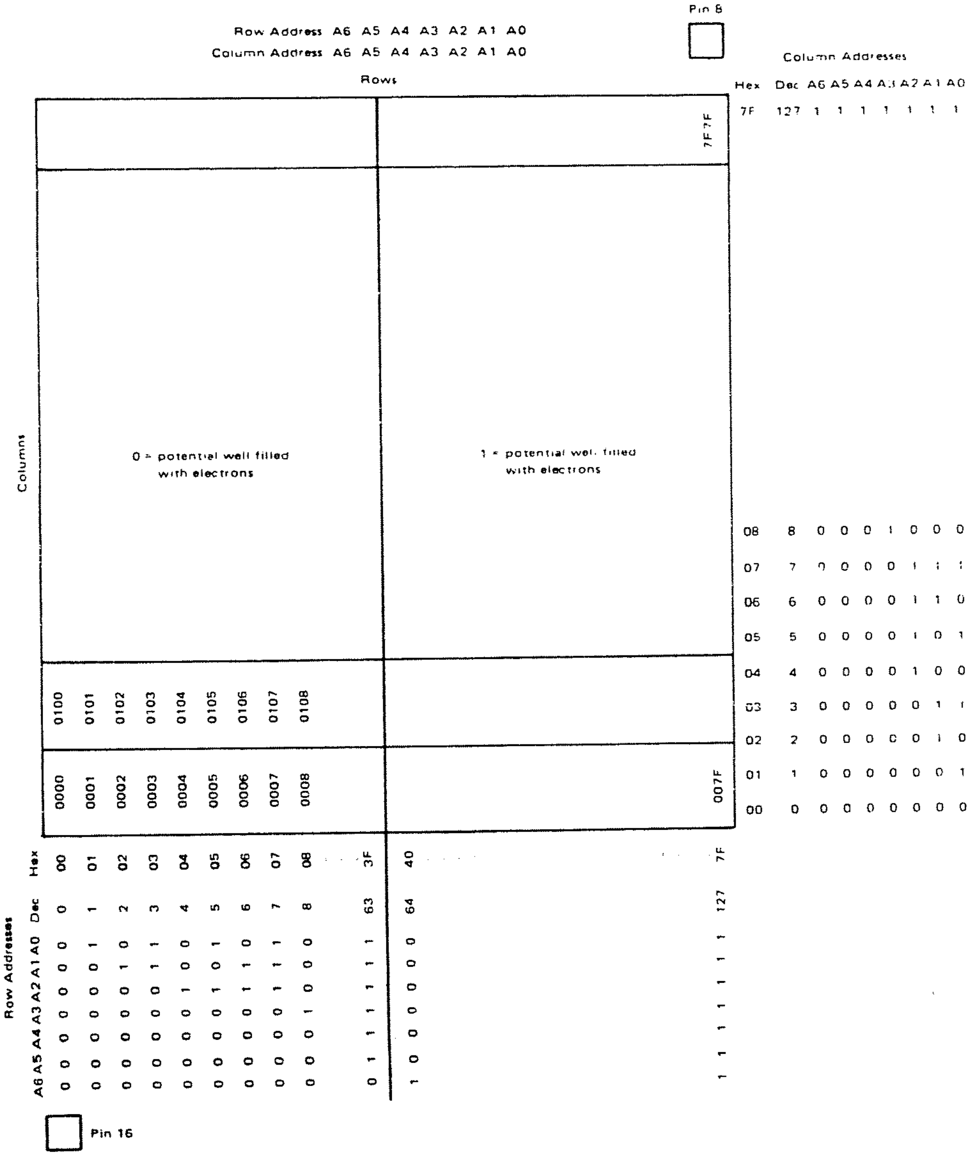
PAGE MODE READ CYCLE



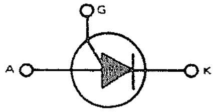
PAGE MODE WRITE CYCLE



MCM4116 BIT ADDRESS MAP



MPU131 (SILICON)
thru
MPU133



SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-trigger, oscillator, pulse and timing circuits. The MPU131, MPU132 and MPU133 may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO-92 plastic package for high-volume requirements, this package is readily adaptable for use in automatic insertion equipment.

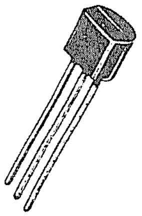
- Programmable – R_{BB}, η, I_V and I_P.
- Low On-State Voltage – 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current – 5.0 nA Maximum
- High Peak Output Voltage – 11 Volts Typical
- Low Offset Voltage – 0.35 Volt Typical (R_G = 10 k ohms)

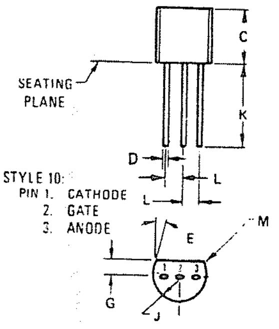
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation Derate Above 25°C	P_F $1/\theta_{JA}$	375 5.0	mW mW/°C
DC Forward Anode Current Derate Above 25°C	I_T	200 2.67	mA mA/°C
DC Gate Current	I_G	±20	mA
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle 20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
Gate to Cathode Reverse Voltage	V_{GKR}	5.0	Volt
Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
Anode to Cathode Voltage	V_{AK}	±40	Volt
Operating Junction Temperature Range	T_J	-50 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

SILICON
PROGRAMMABLE UNIJUNCTION
TRANSISTORS

40 VOLTS
375 mW





STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
C	4.450	4.700	0.175	0.185
D	0.407	0.482	0.016	0.019
E	5° NOM		5° NOM	
G	1.150	1.390	0.045	0.055
J	2.160	2.420	0.085	0.095
K	12.700	-	0.500	-
L	1.270 TP		0.050 TP	
M	0.076	0.330	0.003	0.013

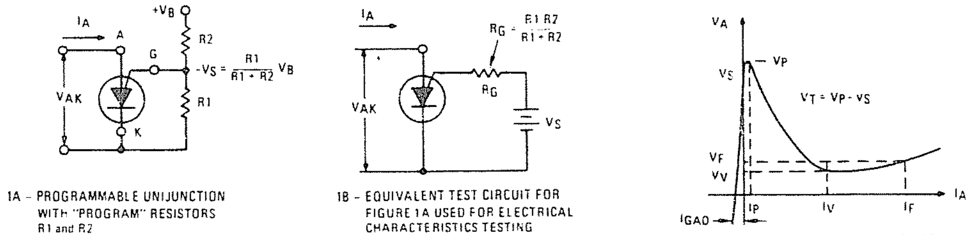
CASE 29-01

MPU131, MPU132, MPU133 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Peak Current	MPU131	2,9-14	I_P	–	1.25	2.0	μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU132			–	0.19	0.30	
	MPU133			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU131			–	4.0	5.0	
	MPU132			–	1.20	2.0	
	MPU133				0.70	1.0	
Offset Voltage	MPU131	1	V_T	0.2	0.70	1.6	Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU132			0.2	0.50	0.6	
	MPU133			0.2	0.40	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms) (All Types)				0.2	0.35	0.6	
Valley Current		1,4,5,	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU131, 132			–	18	50	
	MPU133			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU131			70	270	–	
	MPU132, 133			50	270	–	
Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	5.0	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	30	75	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	–	0.8	1.5	Volts
Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	11	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – PROGRAMMABLE UNIJUNCTION WITH "PROGRAM" RESISTORS R1 and R2

1B – EQUIVALENT TEST CIRCUIT FOR FIGURE 1A USED FOR ELECTRICAL CHARACTERISTICS TESTING (ALSO SEE FIGURE 2)

1C – ELECTRICAL CHARACTERISTICS

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

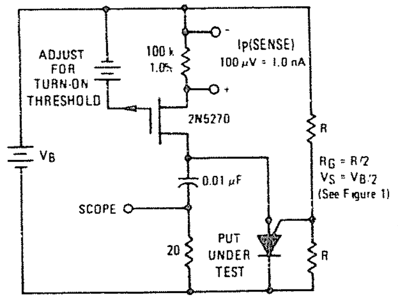
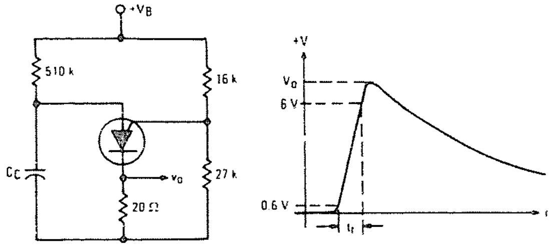


FIGURE 3 – V_o AND t_r TEST CIRCUIT



MOTOROLA

MC1488

QUAD MDTL LINE DRIVER
RS-232C

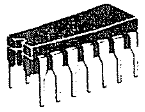
SILICON MONOLITHIC
INTEGRATED CIRCUIT

QUAD LINE DRIVER

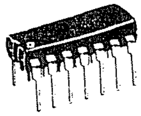
The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

Features:

- Current Limited Output
  ±10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

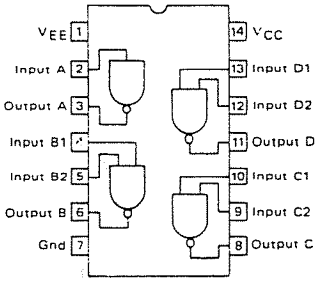


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

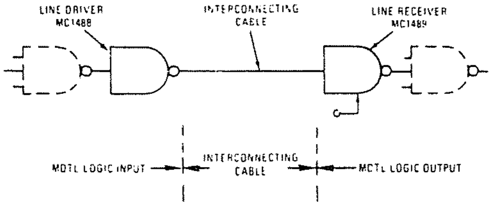


P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS

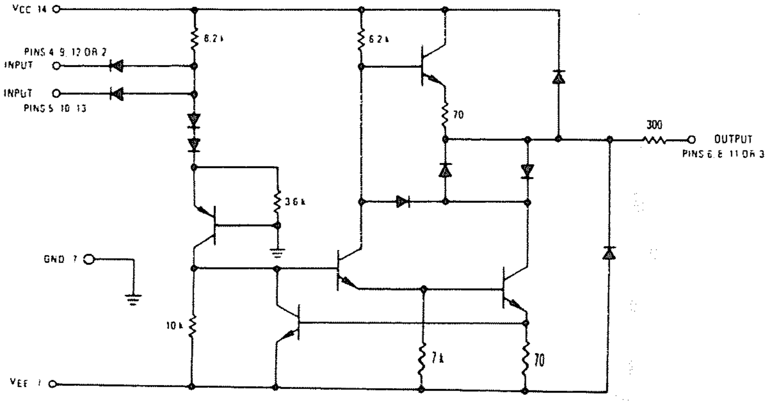


TYPICAL APPLICATION



CIRCUIT SCHEMATIC

(1/4 OF CIRCUIT SHOWN)



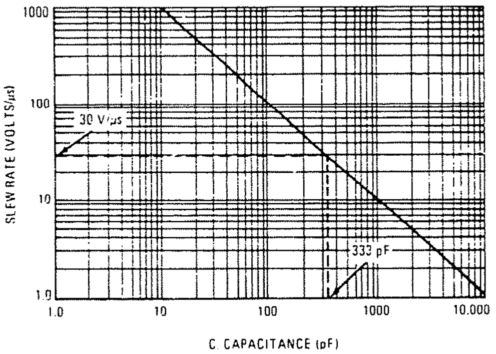
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

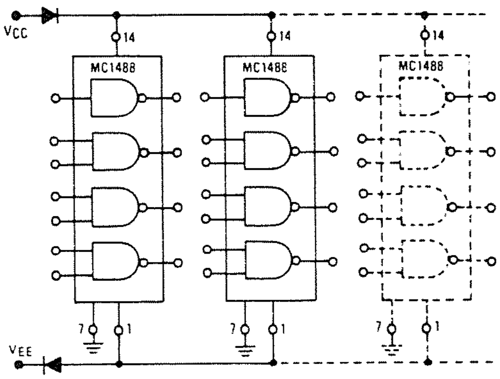
The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

FIGURE 12 – SLEW RATE versus CAPACITANCE FOR I_{SC} = 10 mA



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geqslant 9.0$ V; $V_{EE} \leqslant -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility.

1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power-Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488 will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

MOTOROLA

MC1489L
MC1489AL

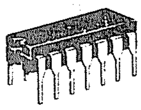
QUAD LINE RECEIVERS

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

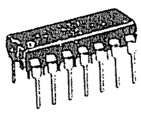
- Input Resistance – 3.0 k to 7.0 kilohms
- Input Signal Range – ± 30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering

QUAD MDTL
LINE RECEIVERS
RS-232C

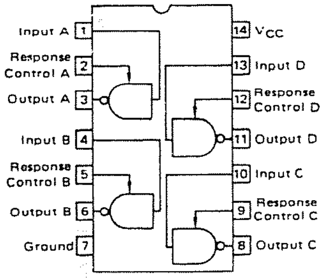
SILICON MONOLITHIC
INTEGRATED CIRCUIT



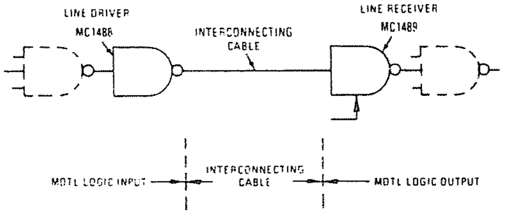
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



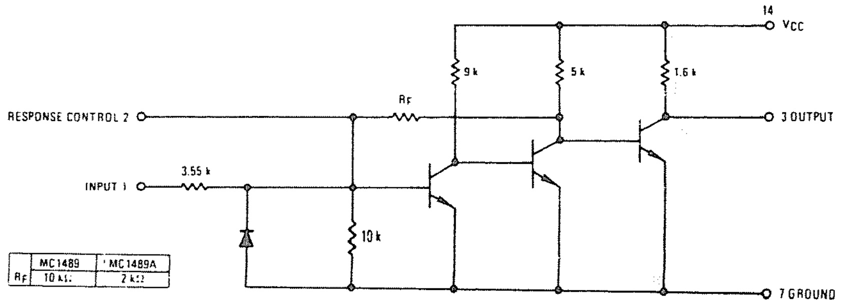
P SUFFIX
PLASTIC PACKAGE
CASE 646



TYPICAL APPLICATION



CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



	MC1489	MC1489A
RF	10 kΩ	2 kΩ

APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE} (Ref. Sect. 2.4).

The receiver shall detect a voltage between -3.0 and -25 volts as a logic "1" and inputs between +3.0 and +25 volts as a logic "0" (Ref. Sect. 2.3). On some interchange leads, an open circuit or power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or logic "1" (Ref. Sect. 2.5). For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 6, 8 and 9 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 12 and 13 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 14.)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 15 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

FIGURE 12 – TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

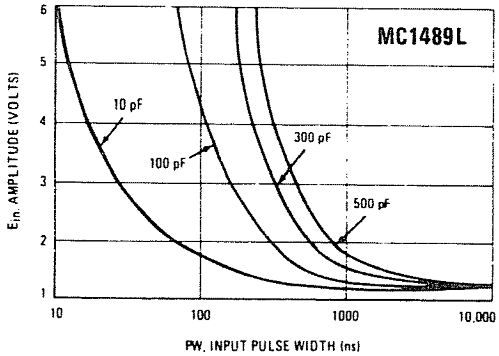
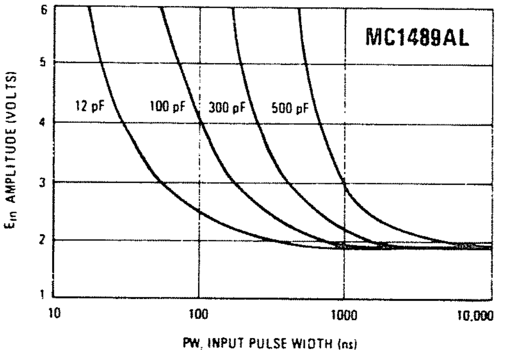


FIGURE 13 – TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



p-channel JFETs designed for . . .

Siliconix

- Analog Switches
- Choppers
- Commutators

Performance Curves PS
See Section 5

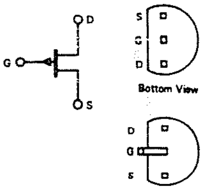
BENEFITS

- Low Cost
- Simplifies Series-Shunt Switching when when Combined with J113, its N-Channel Complement
- Low Insertion Loss
  $R_{DS(on)} < 85\ \Omega$ (J174)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
  $C_{sg(off)} < 5.5$ pF
  $C_{dg(off)} < 5.5$ pF
- Fast Switching
  $t_{d(on)} + t_r = 7$ ns Typical

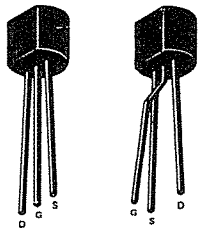
ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . −55 to 135°C
Storage Temperature Range . . . . −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

TO-92
See Section 7



(-18)



ELECTRICAL CHARACTERISTICS (25°C uniess otherwise noted)

		Characteristics		J174			J175			J176			J177			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			1			1			1			1	nA	$V_{DS} = 0, V_{GS} = 20$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	$V_{DS} = -15$ V, $I_D = -10$ nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30			30			30			30				$V_{DS} = 0, I_G - 1\ \mu A$	
4		I_{DSS}	Saturation Drain Current (Note 3)	-20		-100	-7		-60	-2		-25	-1.5		-20	mA	$V_{DS} = -15$ V, $V_{GS} = 0$	
5		$I_{D(off)}$	Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	$V_{DS} = -15$ V, $V_{GS} = 10$ V	
6		$r_{DS(on)}$	Drain-Source ON Resistance			85			125			250			300	Ω	$V_{GS} = 0, V_{DS} = -0.1$ V	
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	$V_{DS} = 0, V_{GS} = 10$ V	f = 1 MHz
8		$C_{sg(off)}$	Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5				
9		$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance		32			32			32			32			$V_{DS} = V_{GS} = 0$	
10		$t_{d(on)}$	Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions	
11		t_r	Rise Time		5			10			20			25				
12		$t_{d(off)}$	Turn Off Delay Time		5			10			15			20				
13		t_f	Fall Time		10			20			20			25				

Switching Time Test Conditions

	J174	J175	J176	J177
V_{DD}	-10 V	-6 V	-6 V	-6 V
$V_{GS(off)}$	12 V	8 V	6 V	3 V
R_L	560 Ω	1.2 KΩ	5.6 KΩ	10 KΩ
$V_{GS(on)}$	0 V	0 V	0 V	0 V

NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300 μs; duty cycle ≤ 3%.

PS

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MC1372

COLOR TV VIDEO MODULATOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

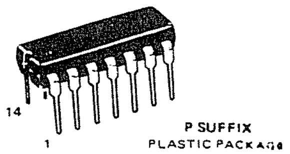
COLOR TV VIDEO MODULATOR

. . . an integrated circuit used to generate an RF TV signal from baseband color-difference and luminance signals.

The MC1372 contains a chroma subcarrier oscillator, lead and lag network, a quasi-quadrature suppressed carrier DSB chroma modulator, an RF oscillator and modulator, and a TTL compatible clock driver with adjustable duty cycle.

The MC1372 is a companion part to the MC6847 Video Display Generator, providing and accepting the correct dc interconnection levels. This device may also be used as a general-purpose modulator with a variety of video signal generating devices such as video games, test equipment, video tape recorders, etc.

- Single 5.0 Vdc Supply Operation for NMOS and TTL Compatibility
- Minimal External Components
- Compatible with MC6847 Video Display Generator
- Sound Carrier Addition Capability
- Modulates Channel 3 or 4 Carrier with Encoded Video Signal
- Low Power Dissipation
- Linear Chroma Modulators for High Versatility
- Composite Video Signal Generation Capability
- Ground-Referenced Video Prevents Overmodulation



P SUFFIX
PLASTIC PACKAGE
CASE 646

Pin Connections

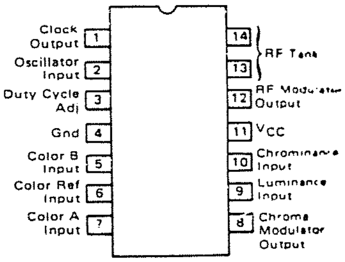
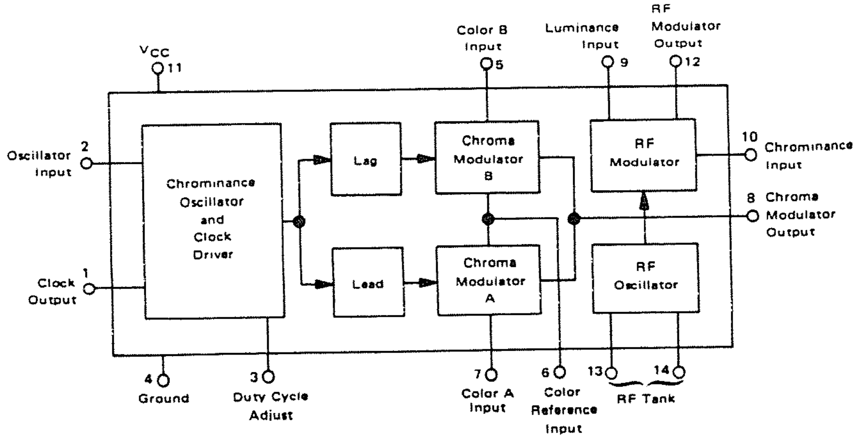


FIGURE 1 – BLOCK DIAGRAM



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Value	Unit
Supply Voltage	8.0	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C
Junction Temperature	150	°C
Power Dissipation, Package Derate above 25°C	1.25 13	Watts mW/°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	5.0	Vdc
Luma Input Voltage – Sync Tip Peak White	1.0 0.35	Vdc
Color Reference Voltage	1.5	Vdc
Color A, B Input Voltage Range	1.0 to 2.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 Vdc, T_A = 25°C, Test Circuit 1 unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Operating Supply Voltage	4.75	5.0	5.25	Volts
Supply Current	–	25	–	mA
CHROMA OSCILLATOR/CLOCK DRIVER (Measured at Pin 1 unless otherwise noted)				
Output Voltage (V_{OL}) (V_{OH})	– 2.4	– –	0.4 –	Vdc
Rise Time (V1 = 0.4 to 2.4 Vdc)	–	–	50	ns
Fall Time (V1 = 2.4 to 0.4 Vdc)	–		50	ns
Duty Cycle Adjustment Range (V3 = 5.0 Vdc) (Measured at V1 = 1.4 V)	70	–	30	%
Inherent Duty Cycle (No connection to Pin 3)	–	50	–	%
CHROMA MODULATOR (V5 = V6 = V7 = 1.5 Vdc unless otherwise noted)				
Input Common Mode Voltage Range (Pins 5, 6, 7)	0.8	–	2.3	Vdc
Oscillator Feedthrough (Measured at Pin 8)	–	15	31	mV(p-p)
Modulation Angle [θ8(V7 = 2.0 Vdc) – θ8(V5 = 2.0 Vdc)]	85	100	115	degrees
Conversion Gain [V8/(V7 – V6); V8/(V5 – V6)]	–	0.6	–	V(p-p)/Vdc
Input Current (Pins 5, 6, 7)	–	–	−20	µA
Input Resistance (Pins 5, 6, 7)	100	–	–	kΩ
Input Capacitance (Pins 5, 6, 7)	–	–	5.0	pF
Chroma Modulator Linearity (V5 = 1.0 to 2.0 V; V7 = 1.0 to 2.0 V)	–	4.0	–	%
RF MODULATOR				
Luma Input Dynamic Range (Pin 9, Test Circuit 2)	0	–	1.5	Volts
RF Output Voltage (f = 67.25 MHz, V9 = 1.0 V)	–	15	–	mVrms
Luma Conversion Gain (ΔV12/ΔV9; V9 = 0.1 to 1.0 Vdc) Test Circuit 2	–	0.8	–	V/V
Chroma Conversion Gain (ΔV12/ΔV10; V10 = 1.5 Vp-p, V9 = 1.0 Vdc) Test Circuit 2	–	0.95	–	V/V
Chroma Linearity (Pin 12, V10 = 1.5 Vp-p) Test Circuit 2	–	1.0	–	%
Luma Linearity (Pin 12, V9 = 0 to 1.5 Vdc) Test Circuit 2	–	2.0	–	%
Input Current (Pin 9)	–	–	−20	µA
Input Resistance (Pin 10)	–	800	–	Ω
Input Resistance (Pin 9)	100	–	–	kΩ
Input Capacitance (Pins 9, 10)	–	–	5.0	pF
Residual 920 kHz (Measured at Pin 12) See Note 1	–	50	–	dB
Output Current (Pin 12, V9 = 0 V) Test Circuit 2	–	1.0	–	mA

TEMPERATURE CHARACTERISTICS (V_{CC} = 5 Vdc, T_A = 0 to 70°C, IC only)

Chroma Oscillator Deviation (f_o = 3.579545 MHz)	–	±50	–	Hz
RF Oscillator Deviation (f_o = 67.25 MHz)	–	±250	–	kHz
Clock Drive Duty Cycle Stability	±5.0	–	–	%

NOTE 1. V9 = 1.0 Vdc, V_C = 300 mV(p-p) @ 3.58 MHz,
V_S = 250 mV(p-p) @ 4.5 MHz, Source Impedance = 75 Ω.

FIGURE 2 – TEST CIRCUIT 1

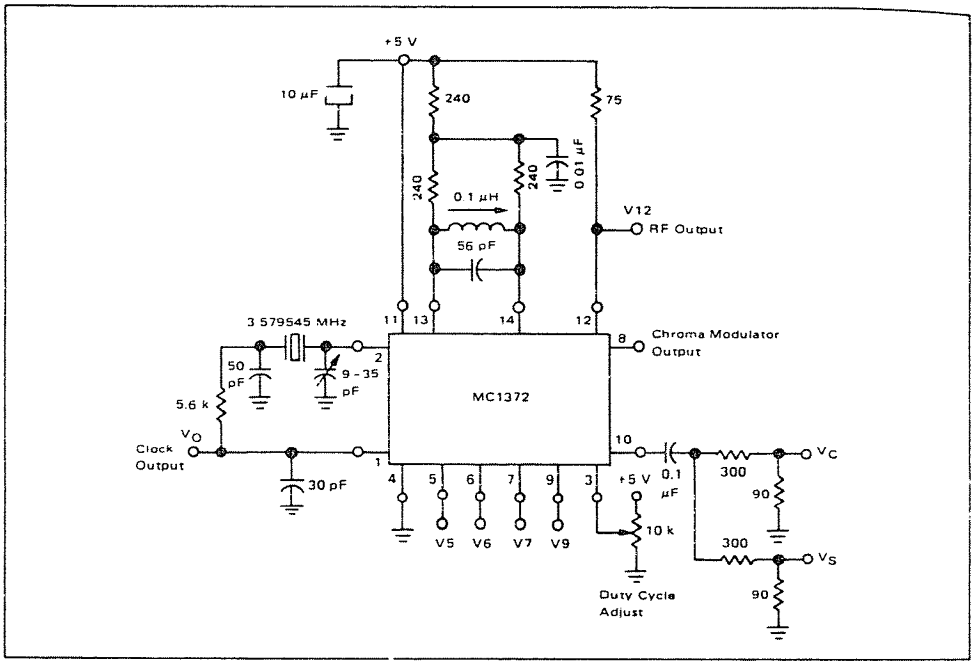
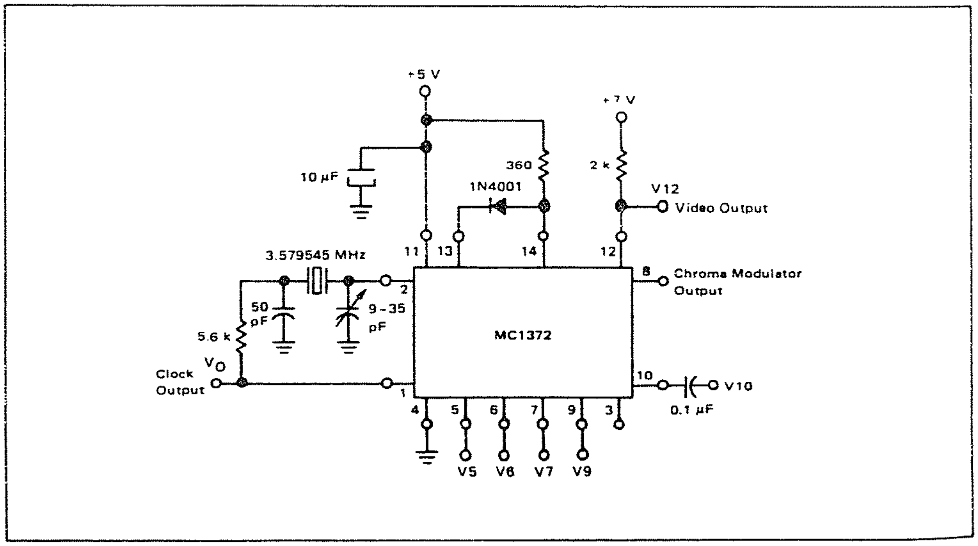


FIGURE 3 – TEST CIRCUIT 2



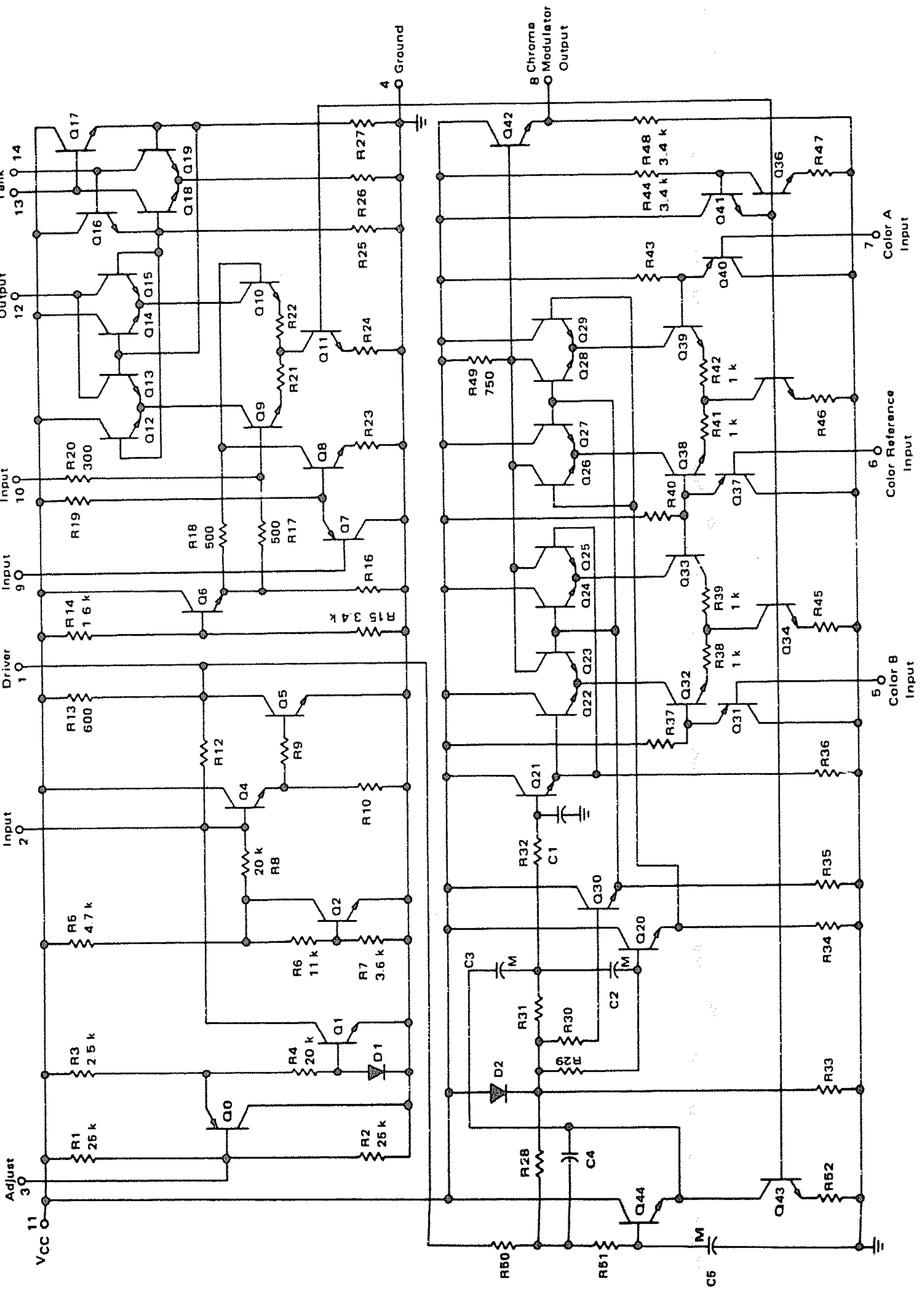


FIGURE 4 – SCHEMATIC DIAGRAM

OPERATIONAL DESCRIPTION

Pin 1 – Clock Output

Provides a rectangular pulse output waveform with frequency equal to the chrominance subcarrier oscillator. This output is capable of driving one LS-TTL load.

Pin 2 – Oscillator Input

Color subcarrier oscillator feedback input. Signal from the clock output is externally phase shifted and ac coupled to this pin.

Pin 3 – Duty Cycle Adjust

A dc voltage applied to this pin adjusts the duty cycle of the clock output signal. If the pin is left unconnected, the duty cycle is approximately 50%.

Pin 4 – Ground

Pin 5 – Color B Input

Dc coupled input to Chroma Modulator B, whose phase leads modulator A by approximately 100°. The modulator output amplitude and polarity correspond to the voltage difference between this pin and the Color Reference Voltage at Pin 6.

Pin 6 – Color Reference Input

The dc voltage applied to this pin establishes the reference voltage to which Color A and Color B inputs are compared.

Pin 7 – Color A Input

Dc coupled input to Chroma Modulator A, whose phase lags modulator B by approximately 100°. The modulator output amplitude and polarity correspond to the voltage difference between this pin and the Color Reference Voltage at Pin 6.

Pin 8 – Chroma Modulator Output

Low impedance (emitter follower) output which provides the vectorial sum of chroma modulators A and B.

Pin 9 – Luminance Input

Input to RF modulator. This pin accepts a dc coupled luminance and sync signal. The amplitude of the RF signal output increases with positive voltage applied to the pin, and ground potential results in zero output (i.e., 100% modulation). A signal with positive-going sync should be used.

Pin 10 – Chrominance Input

Input to the RF modulator. This pin accepts ac coupled chrominance provided by the Chroma Modulator Output (pin 8). The signal is reduced by an internal resistor divider before being applied to the RF modulator. The resistor divider consists of a 300 ohm series resistor and a 500 ohm shunt resistor. Additional gain reduction may be obtained by the addition of external series resistance to pin 10.

Pin 11 – V_{CC}

Positive supply voltage

Pin 12 – RF Modulator Output

Common collector of output modulator stage. Output impedance and stage gain may be selected by choice of resistor connected between this pin and dc supply.

Pins 13 and 14 – RF Tank

A tuned circuit connected between these pins determines the RF oscillator frequency. The tuned circuit must provide a low dc resistance shunt. Applying a dc offset voltage between these pins results in baseband composite video at the RF Modulator Output.

MC1372 CIRCUIT DESCRIPTION

The chrominance oscillator and clock driver consist of emitter follower Q4 and inverting amplifier Q5. Signal presented at clock driver output pin 1 is coupled to oscillator input pin 2 through an external RC and crystal network, which provides 180° phase shift at the resonant frequency. The duty cycle of the output waveform is determined by the dc component at pin 1 internally coupled through R12 to the base of Q4. As pin 1 dc voltage increases, a smaller portion of the sinusoidal feedback signal at pin 2 exceeds the Q4 base voltage of two times V_{BE} required for conduction. As the dc level is reduced, device Q4 and thus Q5 is turned on for a longer percentage of the cycle. Transistors Q0, Q1, Q2 and diode D1 provide the biasing network which determines the dc operating level of the oscillator. The transistor Q2 and resistors R5, R6, and R7 form a voltage reference of four times V_{BE} at the collector of Q2. The dc voltage at pin 1 is determined by the values of R4, R8, and R12 and the applied duty cycle adjust voltage at pin 3. Since these resistors are nominally equal, the voltage at pin 1 will always approximate the dc voltage at pin 3.

The oscillator signal at pin 1 is internally coupled to active filter Q44. This filter reduces the frequency content above 4 MHz. The output of the filter at the emitter of Q44 is ac coupled through C3 to the input of the lead/lag network. R32 and C1 provide approximately 50° of phase lag, while C2 and R29 provide approximately 50° of phase lead. These two quasi-quadrature waveforms are used to switch chroma modulators B and A, respectively. The transistors Q22 through Q25 and Q32–Q33 form a doubly balanced modulator. The input signal applied at pin 5 is compared to the color dc reference voltage applied at pin 6 in differential amplifier Q32–Q33. The source current provided by transistor Q34 is partitioned in transistors Q32 and Q33 according to the differential input signal. The bases of transistors Q23 and Q24 are connected to the dc reference voltage at the emitter of Q30. The bases of transistors Q22 and Q25 are connected to the phase delayed oscillator signal at the emitter of buffer transistor Q21. The differential signal currents provided by Q32 and Q33 are switched in transistors Q22 through Q25 and the resultant signal voltage is developed across R49. This signal has the phase and frequency of the oscillator signal at the emitter of Q21. The amplitude is proportional to the differential input signal applied between pins 5 and 6. Transistors Q26 through Q29 and Q38–Q39 form chroma modulator B. This modulator develops a signal voltage which is proportional to the differential voltage applied between pins 7 and 6. The phase and frequency of the output is equal to the phase advanced chroma oscillator at the emitter of buffer transistor Q20. Both chroma modulators A and B share the same output resistor, R49, so the output signal presented at the emitter of Q42 (pin 8) is the algebraic sum of modulators A and B.

The RF oscillator consists of differential amplifier Q18 and Q19 cross-coupled through emitter followers Q16 and Q17. The oscillator will operate at the parallel resonant frequency of the network connected between pins 13 and 14. The oscillator output is used to switch the doubly balanced RF modulator, Q9 through Q15. Transistors Q7 and Q9 provide level shifting and a high input impedance to the luminance input pin 9. The bases of transistors Q9 and Q10 are both biased through resistors R17 and R18, respectively, to the same dc reference voltage at Q6 emitter. The base voltage at Q10 may only be offset in a negative direction by luminance signal current source Q8. This design insures that overmodulation due to the luminance signal will never occur. The chrominance signal developed at pin 8 is externally ac coupled to pin 10 where it is reduced by resistor dividers R20 and R17, and added to the luminance signal in Q9. The resultant differential composite video currents are switched at the appropriate RF frequency in Q12 through Q15. The output signal current is presented at pin 12.

Transistors Q36, Q41 and resistors R44, R47 provide a highly stable voltage reference for biasing current sources Q43, Q34, Q35, and Q11.

MC1372 APPLICATION INFORMATION

Chrominance Oscillator

The oscillator is used as a clock signal for driving associated external circuitry, in addition to providing a switching signal for the chroma modulators. The IC uses an external crystal in a Colpitts configuration, as shown in Figure 5. Resistor R1 provides current limiting to reduce the signal swing. Capacitor C2 is adjusted for the exact frequency desired (3.579545 MHz).

In some applications, the duty cycle of the clock signal at pin 1 must be modified to overcome gate delays in associated equipment. The duty cycle may be adjusted by varying the dc voltage applied to pin 3. This adjustment may be made with the use of a potentiometer (10 kΩ) between supply and ground. With no connection to pin 3, the duty cycle is approximately 50%.

Chroma Modulator

The chrominance oscillator is internally phase shifted and applied to chroma modulators A and B. No external lead/lag networks are necessary. The phase relationship between the modulators is approximately 100°, which was chosen to provide the best rendition of colors using equal amplitude color-difference signals. The voltage applied to pin 5, 6, or 7 must always be within the Input Common Mode Voltage Range. Since the amplitude of chrominance output is proportional to the voltage difference between pins 5 and 6 or 7 and 6, it is desirable to select the Color Reference Voltage applied to pin 6 to be midway between $V5_{max}$ and $V5_{min}$ (which should be $V7_{max}$ and $V7_{min}$). The Chroma B Modulator will be defined as a (B-Y) modulator if a burst flag signal is applied to the Color B Input (pin 5) at the appropriate time. This voltage should be negative with respect to the Color Reference Voltage, and typically has an amplitude equal to $1/2[V6-V5_{min}]$. Since the phase of burst is always defined as −(B-Y), the Chroma A Modulator approximates an (R-Y) modulator; however, the phase is offset by 10° from the nominal 90°, to provide the 100° phase shift as discussed previously.

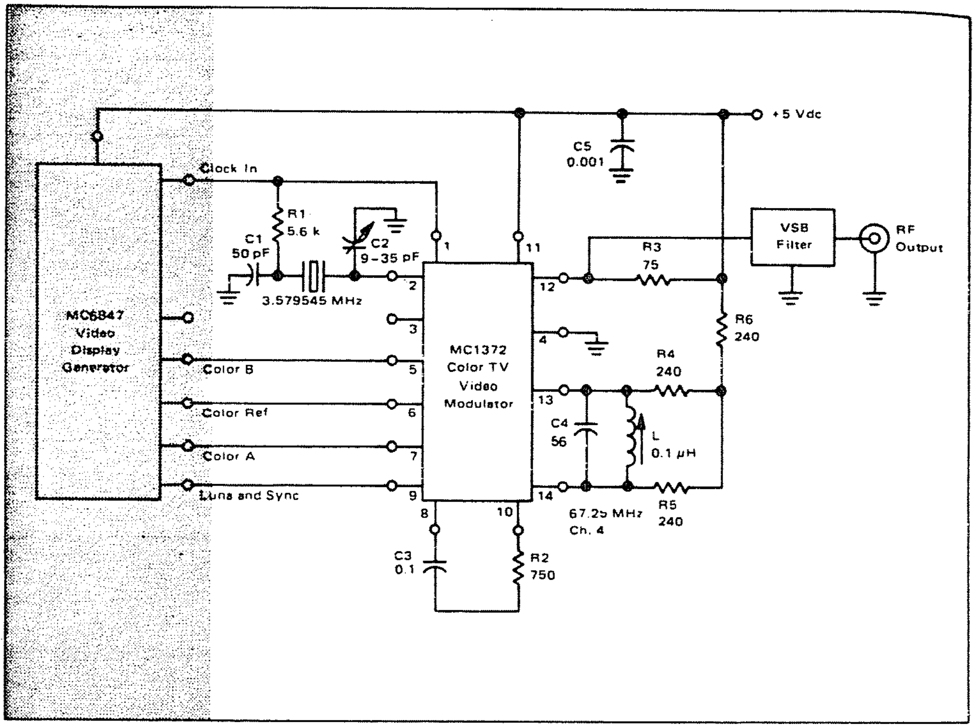
RF Modulator and Oscillator

The coil and capacitor connected between pins 13 and 14 should be selected to have a parallel resonance at the carrier frequency of the desired TV channel. The values of 56 pF and 0.1 µH shown in Figure 5 were chosen for a Channel 4 carrier frequency of 67.25 MHz. For Channel 3 operation, the resonant frequency should be 61.25 MHz (C = 75 pF, L = 0.1 µH). Resistors R4 and R5 are chosen to provide an adequate amplitude of switching voltage, whereas R6 is used to lower the maximum dc level of switching voltage below V_{CC}, thus preventing saturation within the IC.

Composite Luminance and Sync should be dc coupled to Luminance Input, pin 9. This signal must be within the Luma Input Dynamic Range to insure linearity. Since an increase in dc voltage applied to pin 9 results in an increase in RF output, the input signal should have positive-going sync to generate an NTSC compatible signal. As long as the input signal is positive, overmodulation is prevented by the integrated circuit.

Chrominance information should be ac coupled to Chrominance Input, pin 10. This pin is internally connected to a resistor divider consisting of a series 300 ohms and a shunt 500 ohms resistor. The input impedance is thus 800 ohms, and a coupling capacitor should be appropriately chosen.

FIGURE 5 – TYPICAL APPLICATION CIRCUIT



The Luminance to Chrominance ratio (L:C) may be modified with the addition of an external resistor in series with pin 10 (as shown in Figure 5). The unmodified L:C (A_0) is determined by the ratio of the respective Conversion Gain for equal amplitude signals (typically, 0.883 = −1.6 dB). The modified L:C will be governed by the equation $A_0(1 + R_{ext}/800)$ for equal amplitude input signals.

The internal chrominance modulators are not internally connected to the RF modulator; therefore, the user has the option of connecting an externally generated chrominance signal to the RF modulator. In addition, the RF modulator is wideband, and a 4.5 MHz FM audio signal may be added to the chrominance input at pin 10. This may be accomplished by selecting an appropriate series input resistor to provide the correct Luminance:Sound ratio.

The modulated RF signal is presented as a current at RF Modulator Output, pin 12. Since this pin represents a current source, any load impedance may be selected for matching purposes and gain selection, as long as the voltage at pin 12 is high enough to prevent the output devices from reaching saturation (approximately 4.5 V with components in Figure 5). The peak current out of pin 12 is typically 2 mA. Hence, a load resistance of up to 250 ohms may be safely used with a 5 V supply.

Composite Video Signal Generation

The RF modualtor may be easily used as a composite video generator by replacing the RF oscillator tank circuit with a diode as shown in Figure 3. This results in the output modulator being biased so the summation of luminance and chrominance appears unswitched at pin 12. The polarity of the output waveform is controlled by the direction of the diode. *Inverted video:* Anode to pin 14, cathode to pin 13. *Non-inverted video:* Anode to pin 13, cathode to pin 14. Note that the supply resistor must always be connected to the anode of the diode.

The amplitude of signal may be increased by increasing the load resistor on pin 12 and returning it to a higher supply voltage. Any voltage up to the Absolute Maximum Rating may be used.

Applications with MC6847 Video Display Generator

The MC1372 may be easily interfaced to the MC6847 as shown in Figure 5. The dc levels generated and required by the VDG are compatible with the MC1372, so that pins 1, 5, 6, 7, and 9 may be directly coupled to the appropriate MC6847 pins. Both integrated circuits as well as any associated NMOS MPU may be driven from a common 5 Vdc supply.

Recommended Chroma-Luma Signals

A chroma modulation angle of 100° was chosen to facilitate a desirable selection of colors with a minimum number of input signal levels. The following table demonstrates applicable signal levels for a variety of colors.

RECOMMENDED CHROMA-LUMA SIGNALS

	Pin #9 Luminance Input (Vdc)	Pin #7 Color A (Vdc)	Pin #6 Color Ref. (Vdc)	Pin #5 Color B (Vdc)
Sync	1.0	1.5	1.5	1.5
Blanking	0.75	1.5	1.5	1.5
Burst	0.75	1.5	1.5	1.25
Black	0.70	1.5	1.5	1.5
Green	0.50	1.0	1.5	1.0
Yellow	0.38	1.5	1.5	1.0
Blue	0.62	1.5	1.5	2.0
Red	0.62	2.0	1.5	1.5
Cyan	0.50	1.0	1.5	1.5
Magenta	0.50	2.0	1.5	2.0
Orange	0.50	2.0	1.5	1.0
Buff	0.38	1.5	1.5	1.5

MOTOROLA

MCM2716
MCM27A16

Advance Information

2048 X 8-BIT UV ERASABLE PROM

The MCM2716/27A16 is a 16,384-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

For ease of use, the device operates from a single power supply and has a static power-down mode. Pin-for-pin mask programmable ROMS are available for large volume production runs of systems initially using the MCM2716/27A16.

- Single ± 10% 5 V Power Supply
- Automatic Power-down Mode (Standby)
- Organized as 2048 Bytes of 8 Bits
- Low Power Dissipation
- TTL Compatible During Read and Program
- Maximum Access Time = 450 ns MCM2716
  350 ns MCM27A16
- Pin Equivalent to Intel's 2716
- Pin Compatible to MCM68A316E Mask Programmable ROMs

Mode	PIN NUMBER					
	9–11, 13–17 DQ	12 V_{SS}	18 $\overline{E}$/Progr	20 $\overline{G}$	21 V_{PP}	24 V_{CC}
Read	Data out	V_{SS}	V_{IL}	V_{IL}	V_{CC}	V_{CC}
Output Disable	Hi Z	V_{SS}	Don't Care	V_{IH}	V_{CC}	V_{CC}
Standby	Hi Z	V_{SS}	V_{IH}	Don't Care	V_{CC}	V_{CC}
Program	Data in	V_{SS}	Pulsed V_{IL} to V_{IH}	V_{IH}	V_{IHP}	V_{CC}
Program Verify	Data out	V_{SS}	V_{IL}	V_{IL}	V_{IHP}	V_{CC}
Program Inhibit	Hi Z	V_{SS}	V_{IL}	V_{IH}	V_{IHP}	V_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Storage Temperature	−65 to +125	°C
All Input or Output Voltages with Respect to V_{SS} during Read	+ 6 to −0.3	Vdc
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.3	Vdc

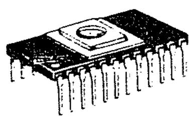
NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is advance information and specifications are subject to change without notice.

MOS

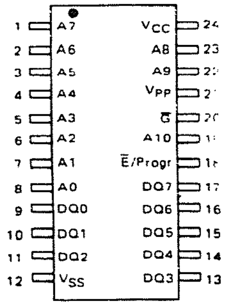
(N-CHANNEL, SILICON-GATE)

2048 X 8-BIT
UV ERASABLE PROM



CERAMIC PACKAGE
CASE 716-03

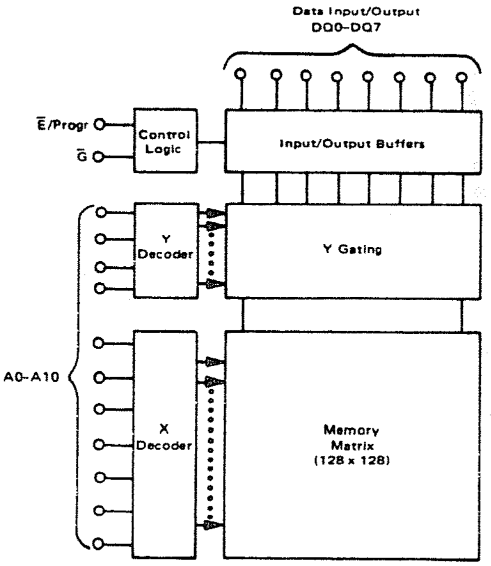
PIN ASSIGNMENT



*PIN NAMES	
A	Address
DQ	Data Input/Output
$\overline{E}$/Progr	Chip Enable/Program
$\overline{G}$	Output Enable

*New industry standard nomenclature

BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC READ OPERATING CONDITIONS ($T_A = 0^\circ$ to $+70^\circ C$)

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage*	MCM2716	V_{CC}	4.75	5.0	5.25	Vdc
	MCM27A16		4.5	5.0	5.5	
		V_{PP}	$V_{CC} - 0.6$	5.0	$V_{CC} + 0.6$	
Input High Voltage		V_{IH}	2.0	–	$V_{CC} + 1.0$	Vdc
Input Low Voltage		V_{IL}	−0.1	–	0.8	Vdc

READ OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	$V_{in} = 5.25$ V	I_{in}	–	–	10	µA
Output Leakage Current	$V_{out} = 5.25$ V, $\overline{G} = 5.0$ V	I_{LO}	–	–	10	µA
V_{CC} Supply Current* (Standby)	$\overline{E}$/Progr $= V_{IH}$, $\overline{G} = V_{IL}$	I_{CC1}	–	10	25	mA
V_{CC} Supply Current* (Active)	$\overline{G} = \overline{E}$/Progr $= V_{IL}$	I_{CC2}	–	57	100	mA
V_{PP} Supply Current*	$V_{PP} = 5.85$ V	I_{PP1}	–	–	5.0	mA
Output Low Voltage	$I_{OL} = 2.1$ mA	V_{OL}	–	–	0.45	V
Output High Voltage	$I_{OH} = -400$ µA	V_{OH}	2.4	–	–	V

*V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. With V_{PP} connected directly to V_{CC} during the read operation, the supply current would be the sum of I_{PP1} and I_{CC}. The additional 0.6 V tolerance on V_{PP} makes it possible to use a driver circuit for switching the V_{PP} supply pin from V_{CC} in Read mode to +25 V for programming. Typical values are for $T_A = 25^\circ C$ and nominal supply voltages.

CAPACITANCE

($f = 1.0$ MHz, $T_A = 25^\circ C$, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance ($V_{in} = 0$ V)	C_{in}	4.0	6.0	pF
Output Capacitance ($V_{out} = 0$ V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

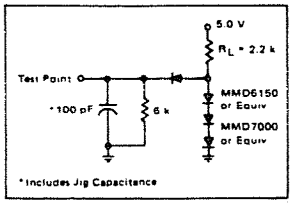
AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10% unless otherwise noted.)

Input Pulse Levels	0.8 Volt to 2.2 Volts	Input and Output Timing Levels	2.0 Volts
Input Rise and Fall Times	20 ns	Output Load	See Figure 1

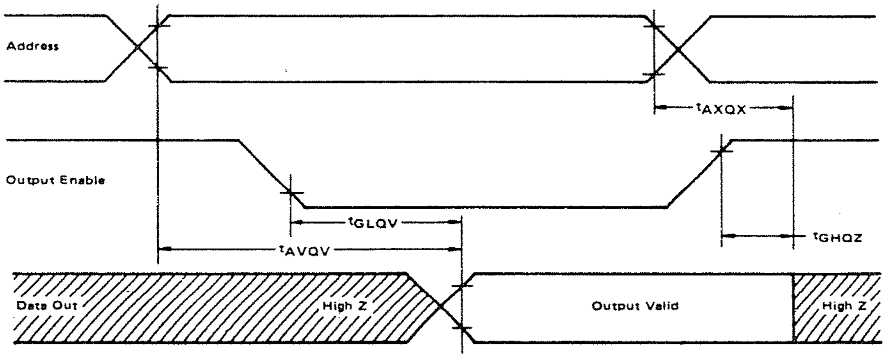
Characteristic	Condition	Symbol	MCM27A16		MCM2716		Units
			Min	Max	Min	Max	
Address Valid to Output Valid	$\overline{E}$/Progr = G = V_{IL}	t_{AVQV}	–	350	–	450	ns
$\overline{E}$/Progr to Output Valid	(Note 2)	t_{ELQV}	–	350	–	450	
Output Enable to Output Valid	$\overline{E}$/Progr = V_{IL}	t_{GLQV}	–	120	–	120	
$\overline{E}$/Progr to Hi Z Output		t_{EHQZ}	0	100	0	100	
Output Disable to Hi Z Output	E/Progr = V_{IL}	t_{GHQZ}	0	100	0	100	
Data Hold from Address	$\overline{E}$/Progr = G = V_{IL}	t_{AXDX}	0	–	0	–	

FIGURE 1 — AC TEST LOAD



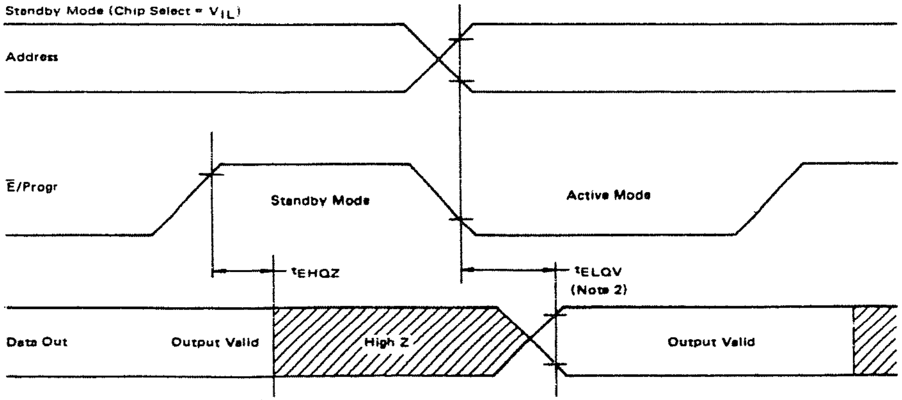
*Includes Jig Capacitance

READ MODE TIMING DIAGRAMS
(Chip Enable = V_{IL})



STANDBY MODE
(Output Enable = V_{IL})

Standby Mode (Chip Select = V_{IL})



NOTE 2: t_{ELQV} is referenced to $\overline{E}$/Progr or stable address, whichever occurs last.

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC} V_{PP}	4.75 24	5.0 25	5.25 26	Vdc Vdc
Input High Voltage for Data	V_{IH}	2.2	–	V_{CC} + 1	Vdc
Input Low Voltage for Data	V_{IL}	-0.1	–	0.8	Vdc

*V_{CC} must be applied simulataneously or prior to Vpp. V_{CC} must also be switched off simultaneously with or after Vpp. The device must not be inserted into or removed from a board with Vpp at +25 V. Vpp must not exceed the +26 V maximum specifications.

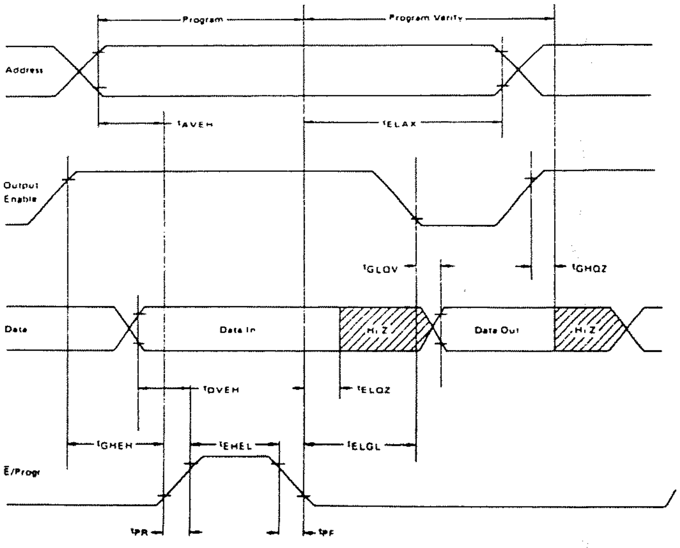
PROGRAMMING OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	V_{in} = 5.25 V/0.45	I_{LI}	–	–	10	μAdc
Vpp Supply Current	$\overline{E}$/Progr = V_{IL}	I_{PP1}	–	–	5.0	mAdc
Vpp Programming Pulse Supply Current	$\overline{E}$/Progr = V_{IH}	I_{PP2}	–	–	30	mAdc
V_{CC} Supply Current		I_{CC}	–	–	100	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVEH}	2.0	–	μs
Output Enable High to Program Pulse	t_{GHEH}	2.0	–	μs
Data Setup Time	t_{DVEH}	2.0	–	μs
Address Hold Time	t_{ELAX}	2.0	–	μs
Output Enable Hold Time	t_{ELGL}	2.0	–	μs
Data Hold Time	t_{ELQZ}	2.0	–	μs
Output Disable to Hi Z Output	t_{GHQZ}	0	120	ns
Output Enable to Valid Data ($\overline{E}$/Progr = V_{IL})	t_{GLQV}	–	120	ns
Program Pulse Width	t_{EHEL}	45	55	ms
Program Pulse Rise Time	t_{PR}	5	–	ns
Program Pulse Fall Time	t_{PF}	5	–	ns

PROGRAMMING OPERATION TIMING DIAGRAM



Z80®-CPU
Z80A-CPU

Product Specification

MARCH 1978

The Zilog Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

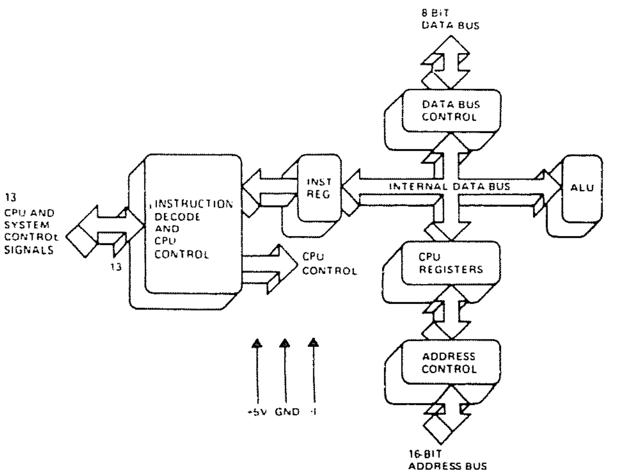
The Z80 and Z80A CPU's are third generation single chip microprocessors with unrivaled computational power. This increased computational power results in higher system through-put and more efficient memory utilization when compared to second generation microprocessors. In addition, the Z80 and Z80A CPU's are very easy to implement into a system because of their single voltage requirement plus all output signals are fully decoded and timed to control standard memory or peripheral circuits. The circuit is implemented using an N-channel, ion implanted, silicon gate MOS process.

Figure 1 is a block diagram of the CPU, Figure 2 details the internal register configuration which contains 208 bits of Read/Write memory that are accessible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or as 16-bit register pairs. There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast Interrupt response. Each CPU also contains a 16-bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

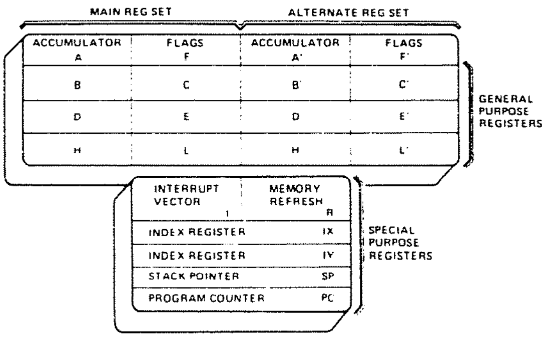
The two 16-bit index registers allow tabular data manipulation and easy implementation of relocatable code. The Refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to a interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

FEATURES

- Single chip, N-channel Silicon Gate CPU.
- 158 instructions—includes all 78 of the 8080A instructions with total software compatibility. New instructions include 4-, 8- and 16-bit operations with more useful addressing modes such as indexed, bit and relative.
- 17 internal registers.
- Three modes of fast interrupt response plus a non-maskable interrupt.
- Directly interfaces standard speed static or dynamic memories with virtually no external logic.
- 1.0 μs instruction execution speed.
- Single 5 VDC supply and single-phase 5 volt Clock.
- Out-performs any other single chip microcomputer in 4-, 8-, or 16-bit applications.
- All pins TTL Compatible
- Built-in dynamic RAM refresh circuitry.

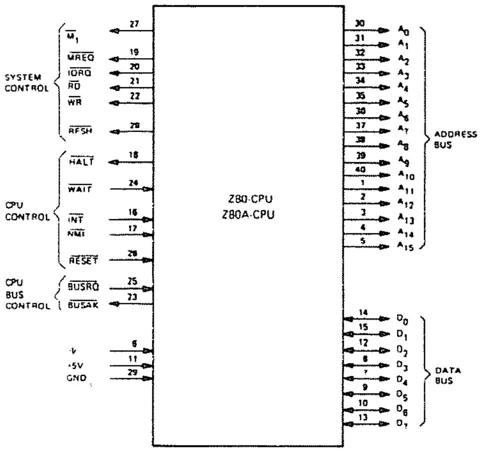


Z80, Z80A CPU BLOCK DIAGRAM



Z80, Z80A CPU REGISTERS

Z80, Z80A-CPU Pin Description



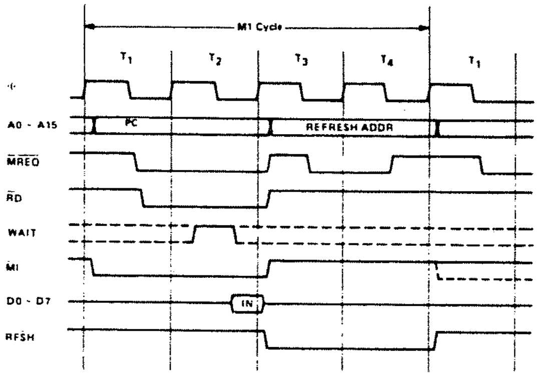
Z80, Z80A CPU PIN CONFIGURATION

A_0-A_{15} (Address Bus)	Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.
D_0-D_7 (Data Bus)	Tri-state input/output, active high. D_0 - D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.
$\overline{M_1}$ (Machine Cycle one)	Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.
$\overline{\text{MREQ}}$ (Memory Request)	Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.
$\overline{\text{IORQ}}$ (Input/ Output Request)	Tri-state output, active low. The $\overline{\text{IORQ}}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{\text{IORQ}}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.
$\overline{\text{RD}}$ (Memory Read)	Tri-state output, active low. $\overline{\text{RD}}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
$\overline{\text{WR}}$ (Memory Write)	Tri-state output, active low. $\overline{\text{WR}}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
$\overline{\text{RFSH}}$ (Refresh)	Output, active low. $\overline{\text{RFSH}}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{\text{MREQ}}$ signal should be used to do a refresh read to all dynamic memories.
$\overline{\text{HALT}}$ (Halt state)	Output, active low. $\overline{\text{HALT}}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.
$\overline{\text{WAIT}}$ (Wait)	Input, active low. $\overline{\text{WAIT}}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.
$\overline{\text{INT}}$ (Interrupt Request)	Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.
$\overline{\text{NMI}}$ (Non Maskable Interrupt)	Input, active low. The non-maskable nterrupt request line has a higher priority than $\overline{\text{INT}}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{\text{NMI}}$ automatically forces the Z-80 CPU to restart to location 0066_H.
$\overline{\text{RESET}}$	Input, active low. $\overline{\text{RESET}}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.
$\overline{\text{BUSRQ}}$ (Bus Request)	Input, active low. The bus request signal has a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.
$\overline{\text{BUSAK}}$ (Bus Acknowledge)	Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signal

Timing Waveforms

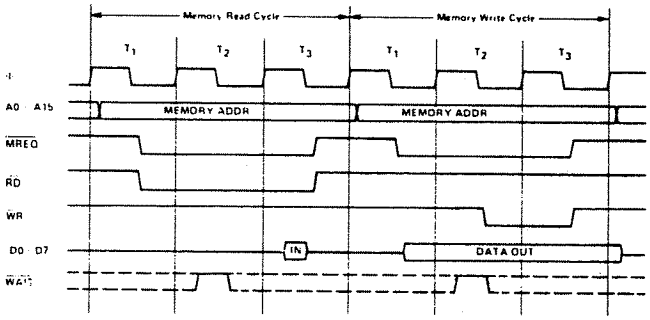
INSTRUCTION OP CODE FETCH

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later MREQ goes active. The falling edge of MREQ can be used directly as a chip enable to dynamic memories. RD when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T_3. Clock states T_3 and T_4 of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The refresh control signal RFSH indicates that a refresh read of all dynamic memories should be accomplished.



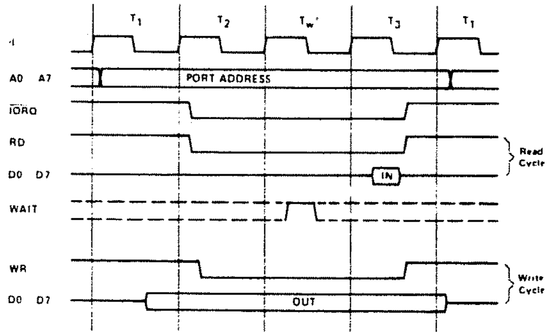
MEMORY READ OR WRITE CYCLES

Illustrated here is the timing of memory read or write cycles other than an OP code fetch (M_1 cycle). The MREQ and RD signals are used exactly as in the fetch cycle. In the case of a memory write cycle, the MREQ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The WR line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory.



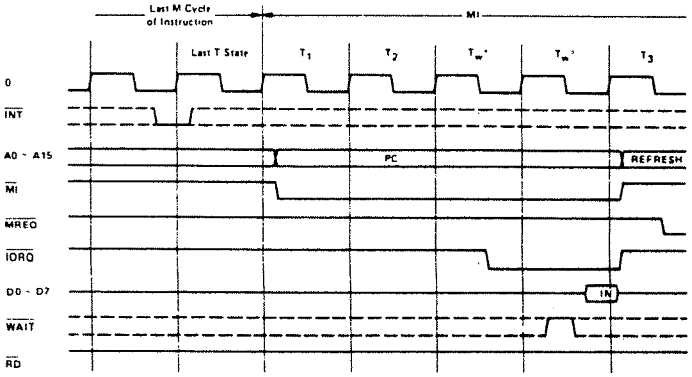
INPUT OR OUTPUT CYCLES

Illustrated here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (Tw*). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and activate the WAIT line if a wait is required.



INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special M_1 cycle is generated. During this M_1 cycle, the IORQ signal becomes active (instead of MREQ) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the Z80 peripheral controllers, can be easily implemented.



Z80, Z80A Instruction Set

The following is a summary of the Z80, Z80A instruction set showing the assembly language mnemonic and the symbolic operation performed by the instruction. A more detailed listing appears in the Z80-CPU technical manual, and assembly language programming manual. The instructions are divided into the following categories:

- 8-bit loads
- 16-bit loads
- Exchanges
- Memory Block Moves
- Memory Block Searches
- 8-bit arithmetic and logic
- 16-bit arithmetic
- General purpose Accumulator & Flag Operations
- Miscellaneous Group
- Rotates and Shifts
- Bit Set, Reset and Test
- Input and Output
- Jumps
- Calls
- Restarts
- Returns

In the table the following terminology is used.

b ≡ a bit number in any 8-bit register or memory location
cc ≡ flag condition code
  NZ ≡ non zero
  Z ≡ zero
  NC ≡ non carry
  C ≡ carry
  PO ≡ Parity odd or no over flow
  PE ≡ Parity even or over flow
  P ≡ Positive
  M ≡ Negative (minus)
d ≡ any 8-bit destination register or memory location
dd ≡ any 16-bit destination register or memory location
e ≡ 8-bit signed 2's complement displacement used in relative jumps and indexed addressing
L ≡ 8 special call locations in page zero. In decimal notation these are 0, 8, 16, 24, 32, 40, 48 and 56
n ≡ any 8-bit binary number
nn ≡ any 16-bit binary number
r ≡ any 8-bit general purpose register (A, B, C, D, E, H, or L)
s ≡ any 8-bit source register or memory location
s_b ≡ a bit in a specific 8-bit register or memory location
ss ≡ any 16-bit source register or memory location
subscript "L" ≡ the low order 8 bits of a 16-bit register
subscript "H" ≡ the high order 8 bits of a 16-bit register
( ) ≡ the contents within the ( ) are to be used as a pointer to a memory location or I/O port number

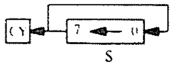
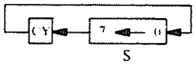
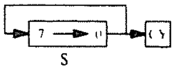
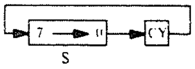
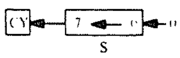
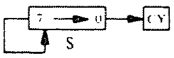
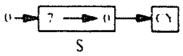
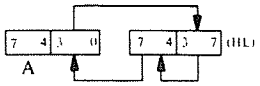
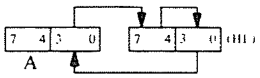
8-bit registers are A, B, C, D, E, H, L, I and R
16-bit register pairs are AF, BC, DE and HL
16-bit registers are SP, PC, IX and IY

Addressing Modes implemented include combinations of the following:

- Immediate
- Immediate extended
- Modified Page Zero
- Relative
- Extended
- Indexed
- Register
- Implied
- Register Indirect
- Bit

	Mnemonic	Symbolic Operation	Comments
8-BIT LOADS	LD r, s	r ← s	s ≡ r, n, (HL), (IX+e), (IY+e)
	LD d, r	d ← r	d ≡ (HL), r (IX+e), (IY+e)
	LD d, n	d ← n	d ≡ (HL), (IX+e), (IY+e)
	LD A, s	A ← s	s ≡ (BC), (DE), (nn), I, R
	LD d, A	d ← A	d ≡ (BC), (DE), (nn), I, R
16-BIT LOADS	LD dd, nn	dd ← nn	dd ≡ BC, DE, HL, SP, IX, IY
	LD dd, (nn)	dd ← (nn)	dd ≡ BC, DE, HL, SP, IX, IY
	LD (nn), ss	(nn) ← ss	ss ≡ BC, DE, HL, SP, IX, IY
	LD SP, ss	SP ← ss	ss = HL, IX, IY
	PUSH ss	$(SP-1) \leftarrow ss_H, (SP-2) \leftarrow ss_L$	ss = BC, DE, HL, AF, IX, IY
	POP dd	$dd_L \leftarrow (SP); dd_H \leftarrow (SP+1)$	dd = BC, DE, HL, AF, IX, IY
EXCHANGES	EX DE, HL	DE → HL	
	EX AF, AF′	AF → AF′	
	EXX	$\begin{pmatrix}BC\\DE\\HL\end{pmatrix} \leftarrow \begin{pmatrix}BC'\\DE'\\HL'\end{pmatrix}$	
	EX (SP), ss	$(SP) \leftrightarrow ss_L, (SP+1) \leftrightarrow ss_H$	ss ≡ HL, IX, IY

	Mnemonic	Symbolic Operation	Comments
MEMORY BLOCK MOVES	LDI	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1	
	LDIR	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1 Repeat until BC = 0	
	LDD	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1	
	LDDR	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1 Repeat until BC = 0	
MEMORY BLOCK SEARCHES	CPI	A-(HL), HL ← HL+1 BC ← BC-1	
	CPIR	A-(HL), HL ← HL+1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	A-(HL) sets the flags only, A is not affected
	CPD	A-(HL), HL ← HL-1 BC ← BC-1	
	CPDR	A-(HL), HL ← HL-1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	
8-BIT ALU	ADD s	A ← A + s	
	ADC s	A ← A + s + CY	CY is the carry flag
	SUB s	A ← A - s	
	SBC s	A ← A - s - CY	s ≡ r, n, (HL) (IX+e), (IY+e)
	AND s	$A \leftarrow A \wedge s$	
	OR s	$A \leftarrow A \vee s$	
	XOR s	$A \leftarrow A \oplus s$	

	Mnemonic	Symbolic Operation	Comments
8-BIT ALU	CP s	A - s	s = r, n (HL) (IX+e), (IY+e)
	INC d	d ← d + 1	d = r, (HL) (IX+e), (IY+e)
	DEC d	d ← d - 1	
16-BIT ARITHMETIC	ADD HL, ss	HL ← HL + ss	ss ≡ BC, DE HL, SP
	ADC HL, ss	HL ← HL + ss + CY	
	SBC HL, ss	HL ← HL - ss - CY	
	ADD IX, ss	IX ← IX + ss	ss ≡ BC, DE, IX, SP
	ADD IY, ss	IY ← IY + ss	ss ≡ BC, DE, IY, SP
	INC dd	dd ← dd + 1	dd ≡ BC, DE, HL, SP, IX, IY
	DEC dd	dd ← dd - 1	dd ≡ BC, DE, HL, SP, IX, IY
GP ACC. & FLAG	DAA	Converts A contents into packed BCD following add or subtract.	Operands must be in packed BCD format
	CPL	A ← $\overline{A}$	
	NEG	A ← 00 − A	
	CCF	CY ← $\overline{CY}$	
	SCF	CY ← 1	
MISCELLANEOUS	NOP	No operation	
	HALT	Halt CPU	
	DI	Disable Interrupts	
	EI	Enable Interrupts	
	IM 0	Set interrupt mode 0	8080A mode
	IM 1	Set interrupt mode 1	Call to 0038_H
	IM 2	Set interrupt mode 2	Indirect Call
ROTATES AND SHIFTS	RLC s		s ≡ r, (HL) (IX+e), (IY+e)
	RL s		
	RRC s		
	RR s		
	SLA s		
	SRA s		
	SRL s		
	RLD		
	RRD		

	Mnemonic	Symbolic Operation	Comments
BIT S, R, & T	BIT b, s	Z ← $\overline{s_b}$	Z is zero flag
	SET b, s	s_b ← 1	s ≡ r, (HL) (IX+e), (IY+e)
	RES b, s	s_b ← 0	
INPUT AND OUTPUT	IN A, (n)	A ← (n)	
	IN r, (C)	r ← (C)	Set flags
	INI	(HL) ← (C), HL ← HL + 1 B ← B - 1	
	INIR	(HL) ← (C), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	IND	(HL) ← (C), HL ← HL - 1 B ← B - 1	
	INDR	(HL) ← (C), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
	OUT(n), A	(n) ← A	
	OUT(C), r	(C) ← r	
	OUTI	(C) ← (HL), HL ← HL + 1 B ← B - 1	
	OTIR	(C) ← (HL), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	OUTD	(C) ← (HL), HL ← HL - 1 B ← B - 1	
	OTDR	(C) ← (HL), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
JUMPS	JP nn	PC ← nn	cc { NZ PO Z PE NC P C M
	JP cc, nn	If condition cc is true PC ← nn, else continue	
	JR e	PC ← PC + e	
	JR kk, e	If condition kk is true PC ← PC + e, else continue	kk { NZ NC Z C
	JP (ss)	PC ← ss	ss = HL, IX, IY
	DJNZ e	B ← B - 1, if B = 0 continue, else PC ← PC + e	
CALLS	CALL nn	(SP-1) ← PC_H (SP-2) ← PC_L, PC ← nn	cc { NZ PO Z PE NC P C M
	CALL cc, nn	If condition cc is false continue, else same as CALL nn	
RESTARTS	RST L	(SP-1) ← PC_H (SP-2) ← PC_L, PC_H ← 0 PC_L ← L	
RETURNS	RET	PC_L ← (SP), PC_H ← (SP+1)	
	RET cc	If condition cc is false continue, else same as RET	cc { NZ PO Z PE NC P C M
	RETI	Return from interrupt, same as RET	
	RETN	Return from non- maskable interrupt	

A.C. Characteristics Z80-CPU

$T_A = 0°C$ to $70°C$, $Vcc = +5V \pm 5\%$, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	.4	[12]	μsec	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	180	[E]	nsec	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	180	2000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		145	nsec	$C_L = 50pF$
	$t_{F(AD)}$	Delay to Float		110	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		230	nsec	$C_L = 50pF$
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	60		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]			
	t_H	Any Hold Time for Setup Time	0		nsec	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		100	nsec	$C_L = 50pF$
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		90	nsec	$C_L = 50pF$
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		110	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		100	nsec	
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		110	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		100	nsec	$C_L = 50pF$
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		130	nsec	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		100	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		110	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80	nsec	$C_L = 50pF$
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		90	nsec	
	$t_{DH\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		100	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		130	nsec	$C_L = 50pF$
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		130	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		180	nsec	$C_L = 50pF$
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		150	nsec	
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	$C_L = 50pF$
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		120	nsec	$C_L = 50pF$
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		110	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	90		nsec	
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		100	nsec	
	t_{mr}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		nsec	

[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

[1] $t_{acm} = t_{w(\Phi H)} + t_f - 75$

[2] $t_{aci} = t_c - 80$

[3] $t_{ca} = t_{w(\Phi L)} + t_r - 40$

[4] $t_{caf} = t_{w(\Phi L)} + t_r - 60$

[5] $t_{dcm} = t_c - 210$

[6] $t_{dci} = t_{w(\Phi L)} + t_r - 210$

[7] $t_{cdf} = t_{w(\Phi L)} + t_r - 80$

[8] $t_{w(MRL)} = t_c - 40$

[9] $t_{w(MRH)} = t_{w(\Phi H)} + t_f - 30$

[10] $t_{w(\overline{WRL})} = t_c - 40$

[11] $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 80$

NOTES

A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

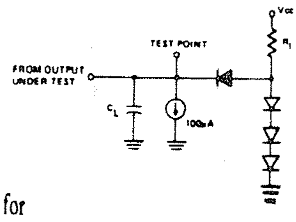
B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

C. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

D. Output Delay vs. Loaded Capacitance
TA = 70°C Vcc = +5V ±5%

Add 10nsec delay for each 50pf increase in load up to a maximum of 200pf for the data bus & 100pf for address & control lines

E. Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum

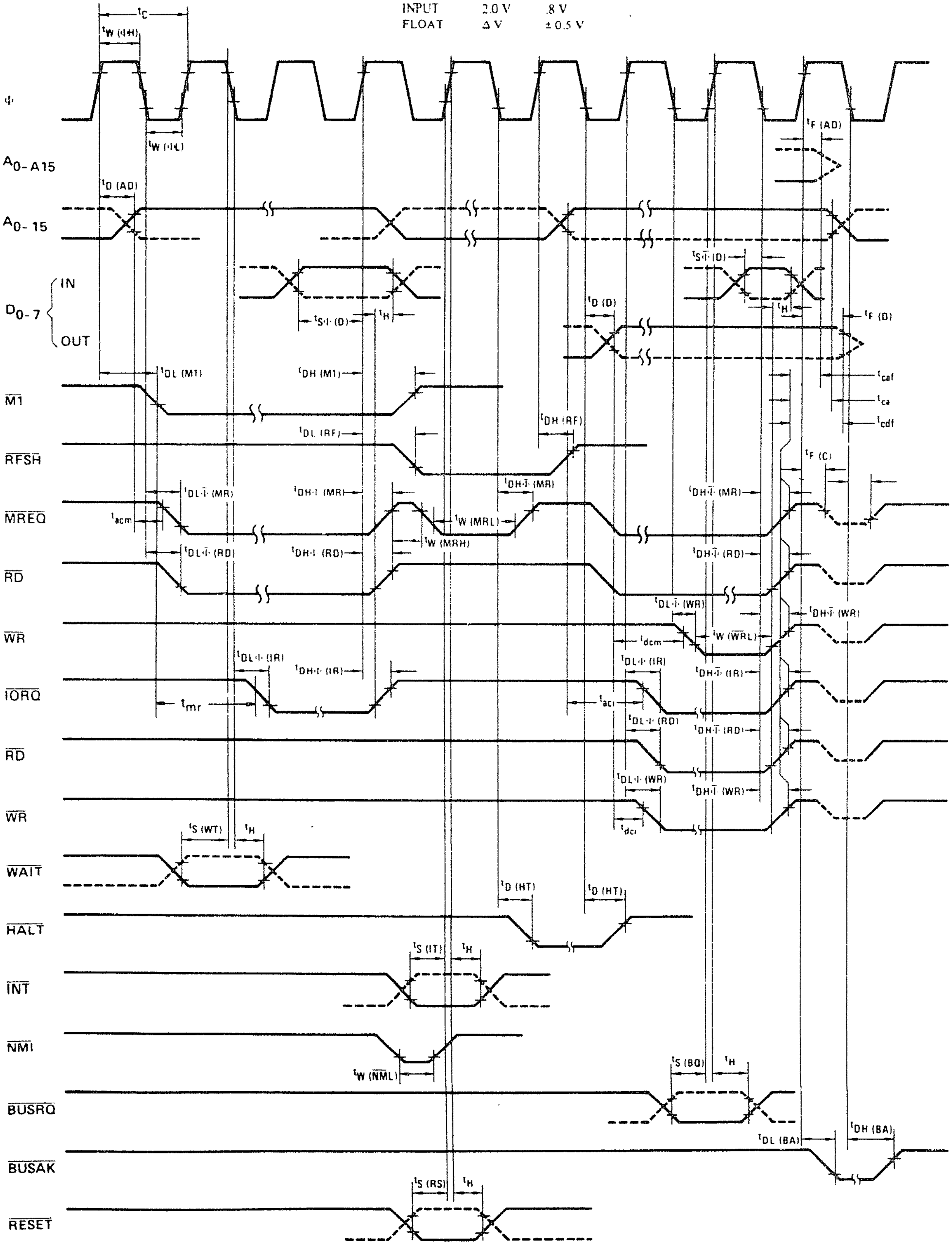


Load circuit for Output

A.C. Timing Diagram

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	V_{cc} -.6V	.45V
OUTPUT	2.0 V	.8 V
INPUT	2.0 V	.8 V
FLOAT	Δ V	± 0.5 V



Absolute Maximum Ratings

Temperature Under Bias	Specified operating range
Storage Temperature	-65°C to +150°C
Voltage On Any Pin with Respect to Ground	-0.3V to +7V
Power Dissipation	1.5W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: For Z80-CPU all AC and DC characteristics remain the same for the military grade parts except I_{cc}

I_{cc} = 200 mA

Z80-CPU D.C. Characteristics

T_A = 0°C to 70°C V_{cc} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	$V_{cc}-.6$		$V_{cc}+.3$	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current			150	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80-CPU
Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C
E – Extended 5V ±5% -40° to 85°C
M – Military 5V ±10% -55° to 125°C

Z80A-CPU D.C. Characteristics

T_A = 0°C to 70°C V_{cc} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	$V_{cc}-.6$		$V_{cc}+.3$	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current		90	200	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80A-CPU
Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C

A.C. Characteristics Z80A-CPU

$T_A = 0°C$ to $70°C$, $V_{cc} = +5V \pm 5\%$, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	.25	[12]	μsec	
	$t_w(\Phi H)$	Clock Pulse Width, Clock High	110	[E]	nsec	
	$t_w(\Phi L)$	Clock Pulse Width, Clock Low	110	2000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		110	nsec	$C_L = 50pF$
	$t_{F(AD)}$	Delay to Float		90	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		150	nsec	$C_L = 50pF$
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	35		nsec	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	50		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]			
	t_H	Any Hold Time for Setup Time		0	nsec	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		85	nsec	$C_L = 50pF$
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		75	nsec	$C_L = 50pF$
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		85	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		85	nsec	
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		85	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		85	nsec	$C_L = 50pF$
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		95	nsec	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		85	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		85	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		65	nsec	$C_L = 50pF$
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		80	nsec	
	$t_{DH\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		80	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		100	nsec	$C_L = 50pF$
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		100	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		130	nsec	$C_L = 50pF$
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		120	nsec	
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	$C_L = 50pF$
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	50		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		100	nsec	$C_L = 50pF$
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		100	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	60		nsec	
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80	nsec	
	t_{mr}	M1 Stable Prior to IORQ (Interrupt Ack.)	[11]		nsec	

[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

[1] $t_{acm} = t_{w(\Phi H)} + t_f - 65$

[2] $t_{aci} = t_c - 70$

[3] $t_{ca} = t_{w(\Phi L)} + t_r - 50$

[4] $t_{caf} = t_{w(\Phi L)} + t_r - 45$

[5] $t_{dcm} = t_c - 170$

[6] $t_{dci} = t_{w(\Phi L)} + t_r - 170$

[7] $t_{cdf} = t_{w(\Phi L)} + t_r - 70$

[8] $t_{w(\overline{MRL})} = t_c - 30$

[9] $t_{w(\overline{MRH})} = t_{w(\Phi H)} + t_f - 20$

[10] $t_{w(\overline{WRL})} = t_c - 30$

[11] $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 65$

NOTES:

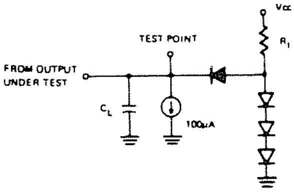
A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

C. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

D. Output Delay vs. Loaded Capacitance
$TA = 70°C$ $V_{cc} = +5V \pm 5\%$
Add 10nsec delay for each 50pf increase in load up to maximum of 200pf for data bus and 100pf for address & control lines.

E. Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum



Load circuit for Output

TYPES TL080 THRU TL085, TL080A THRU TL084A, TL081B, TL082B, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 12484, FEBRUARY 1977—REVISED OCTOBER 1979

24 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

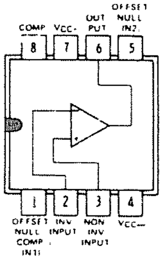
- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL080, TL080A)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ

description

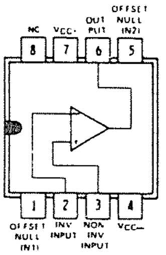
The TL081 JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL081 Family.

Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

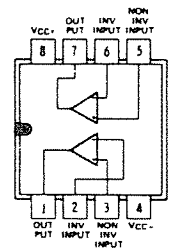
TL080, TL080A
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



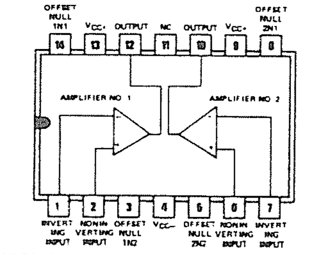
TL081, TL081A, TL081B
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



TL082, TL082A, TL082B
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)

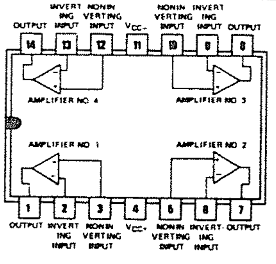


TL083, TL083A
J OR N DUAL-IN-LINE
PACKAGE (TOP VIEW)

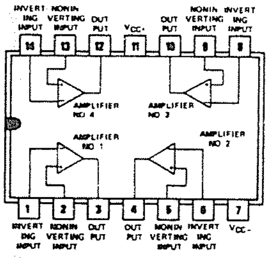


PINS 8 AND 13 ARE INTERNALLY INTERCONNECTED

TL084, TL084A, TL084B
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE
(TOP VIEW)



TL085
N DUAL-IN-LINE
PACKAGE (TOP VIEW)



NC—No internal connection

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TEXAS INSTRUMENTS
INCORPORATED
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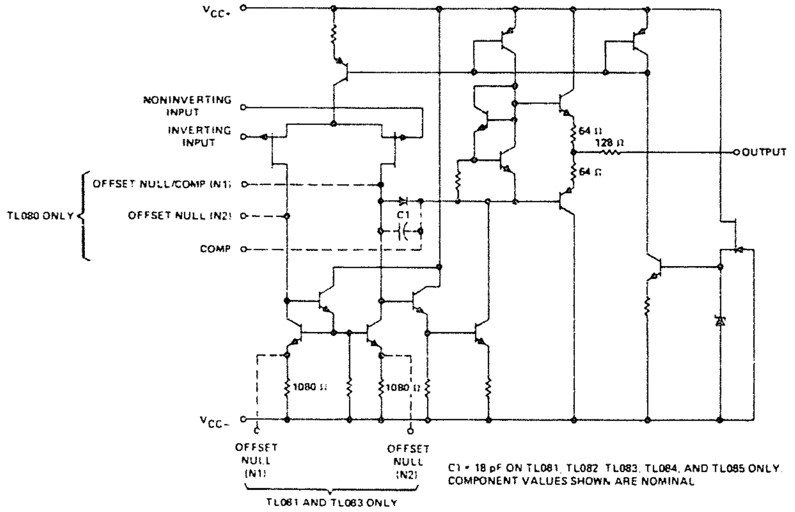
TYPES TL080 THRU TL085, TL080A THRU TL084A, TL081B, TL082B, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

schematic (each amplifier)



C1 = 18 pF ON TL081, TL082, TL083, TL084, AND TL085 ONLY.
COMPONENT VALUES SHOWN ARE NOMINAL

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL08_M	TL08_I	TL08_C TL08_AC TL08_BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (See Note 5)		680	680	680	mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds	J, JG, or W package	300	300	300	°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	N or P package		260	260	°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Table. In the J and JG packages, TL08_M chips are alloy-mounted; TL08_I, TL08_C, TL08_AC, and TL08_BC chips are glass-mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-Mounted Chip)	680 mW	11.0 mW/°C	88°C
J (Glass-Mounted Chip)	680 mW	8.2 mW/°C	67°C
JG (Alloy-Mounted Chip)	680 mW	8.4 mW/°C	69°C
JG (Glass-Mounted Chip)	680 mW	6.6 mW/°C	47°C
N	680 mW	9.2 mW/°C	76°C
P	680 mW	8.0 mW/°C	65°C
W	680 mW	8.0 mW/°C	65°C

Also see Dissipation Derating Curves, Section 2.

DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

	TL080	TL081	TL082	TL083	TL084	TL085
TL08_M	JG	JG	JG	J	J, W	•
TL08_I	JG, P	JG, P	JG, P	J, N	J, N	•
TL08_C	JG, P	JG, P	JG, P	J, N	J, N	N
TL08_AC	JG, P	JG, P	JG, P	J, N	J, N	•
TL08_BC	•	JG, P	JG, P	•	J, N	•

•These combinations are not defined by this data sheet.

electrical characteristics, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†		TL08_M			TL08_I			TL08_C TL08_AC TL08_BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω, T_A = 25°C	'80,'81,'82,'83,'85‡		3	6		3	6		5	15	mV
			TL084		3	9		3	6		5	15	
			TL08_A								3	6	
			'81B,'82B,'84B								2	3	
		R_S = 50 Ω, T_A = full range	'80,'81,'82,'83,'85‡			9			9			20	
			TL084			15			9			20	
			TL08_A									7.5	
			'81B,'82B,'84B									5	
α_{VIO}	Temperature coefficient of input offset voltage	R_S = 50 Ω,	T_A = full range		10			10			10		μV/°C
I_{IO}	Input offset current§	T_A = 25°C	TL08_‡		5	100		5	100		5	200	pA
			TL08_A								5	100	
			'81B,'82B,'84B								5	100	
		T_A = full range	TL08_‡			20			10			5	nA
			TL08_A									3	
			'81B,'82B,'84B									3	
I_{IB}	Input bias current§	T_A = 25°C	TL08_‡		30	200		30	200		30	400	pA
			TL08_A								30	200	
			'81B,'82B,'84B								30	200	
		T_A = full range	TL08_‡			50			20			10	nA
			TL08_A									7	
			'81B,'82B,'84B									7	
V_{ICR}	Common-mode input voltage range	T_A = 25°C	TL08_‡	±11	±12		±11	±12		±10	±11		V
			TL08_A							±11	±12		
			'81B,'82B,'84B							±11	±12		
V_{OPP}	Maximum peak-to-peak output voltage swing	T_A = 25°C	R_L = 10 kΩ	24	27		24	27		24	27		V
		T_A = full range	R_L ≥ 10 kΩ	24			24			24			
			R_L ≥ 2 kΩ	20	24		20	24		20	24		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V, T_A = 25°C	TL08_‡	25	200		50	200		25	200		V/mV
			TL08_A							50	200		
			'81B,'82B,'84B							50	200		
		R_L ≥ 2 kΩ, V_O = ±10 V, T_A = full range	TL08_‡	15			25			15			
			TL08_A							25			
			'81B,'82B,'84B							25			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S ≥ 10 kΩ, T_A = 25°C	TL08_‡	80	86		80	86		70	76		dB
			TL08_A							80	86		
			'81B,'82B,'84B							80	86		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	R_S ≥ 10 kΩ, T_A = 25°C	TL08_‡	80	86		80	86		70	76		dB
			TL08_A							80	86		
			'81B,'82B,'84B							80	86		
I_{CC}	Supply current (per amplifier)	No load, T_A = 25°C	No signal,		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{o1}/V_{o2}	Channel separation	A_{VD} = 100,	T_A = 25°C		120			120			120		dB

---

† All characteristics are specified under open-loop conditions unless otherwise noted. Full range for T_A is −55°C to 125°C for TL08_M; −25°C to 85°C for TL08_I; and 0°C to 70°C for TL08_C, TL08_AC, and TL08_BC.

‡ Types TL085I and TL085M are not defined by this data sheet.

§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°$ C

PARAMETER		TEST CONDITIONS		TL08_M			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1	8	13			13		V/μs
t_r	Rise time	$V_I = 20$ mV, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1		0.1			0.1		μs
	Overshoot factor				10%			10%		
V_n	Equivalent input noise voltage	$R_S = 100$ Ω,	f = 1 kHz		25			25		nV/$\sqrt{Hz}$

PARAMETER MEASUREMENT INFORMATION

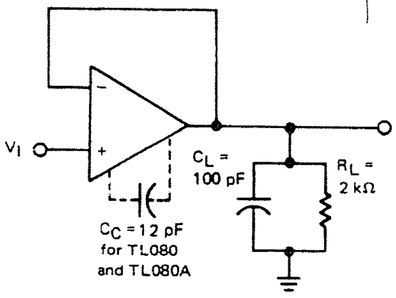


FIGURE 1—UNITY-GAIN AMPLIFIER

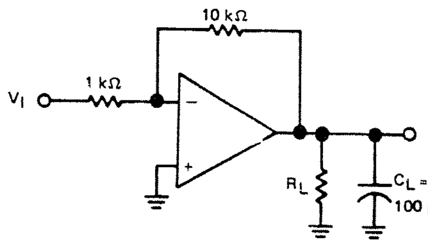


FIGURE 2—GAIN-OF-10 INVERTING AMPLIFIER

INPUT OFFSET VOLTAGE NULL CIRCUITS

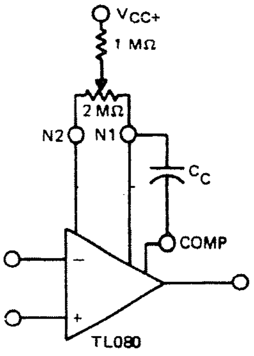


FIGURE 3

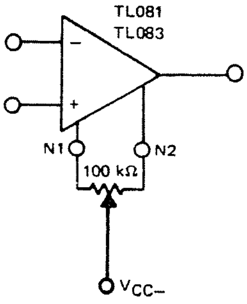
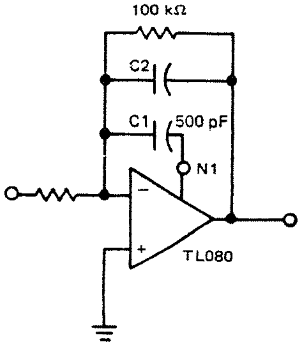


FIGURE 4



FEED-FORWARD COMPENSATION

FIGURE 5

TYPICAL APPLICATION DATA

0.5-Hz SQUARE-WAVE OSCILLATOR

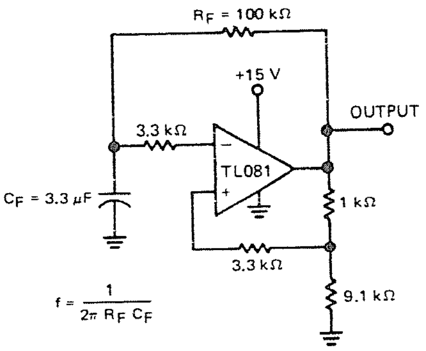


FIGURE 24—0.5-Hz SQUARE-WAVE OSCILLATOR

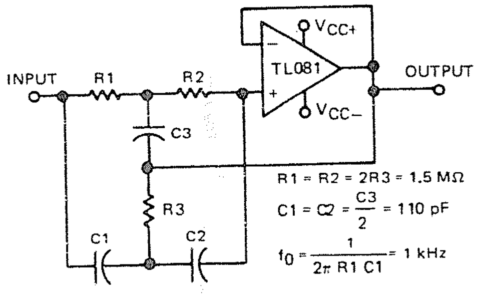
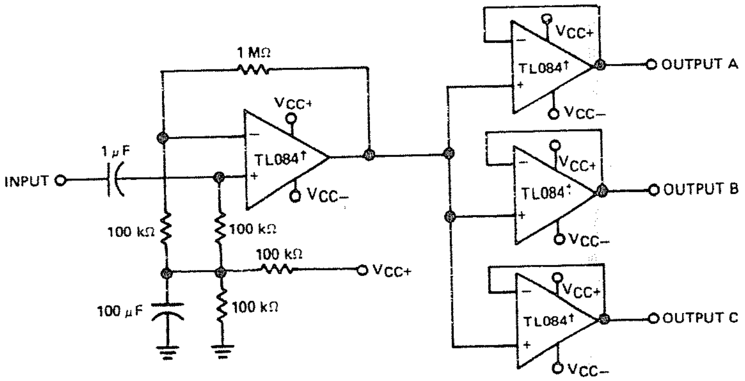
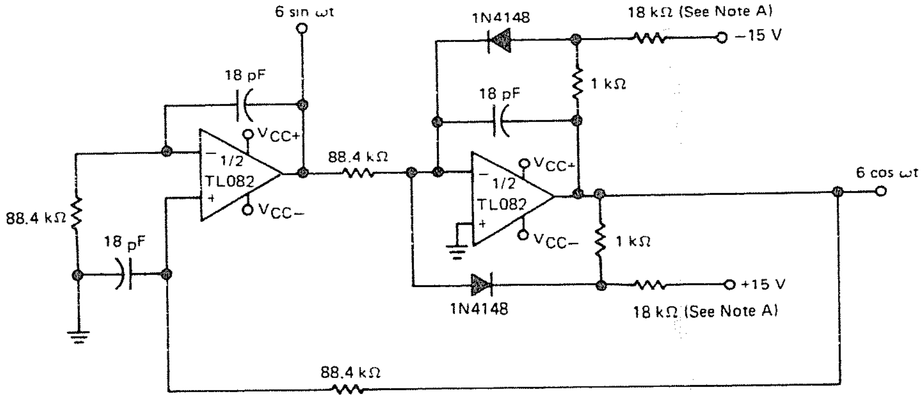


FIGURE 25—HIGH-Q NOTCH FILTER



† or TL085

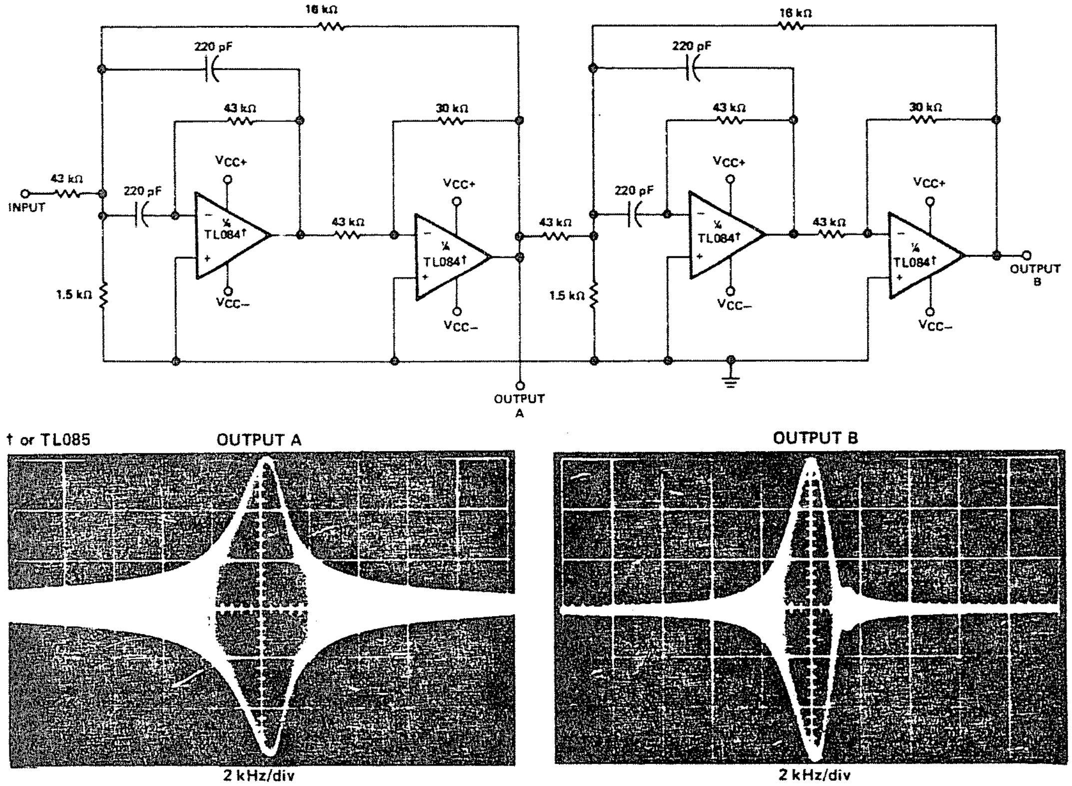
FIGURE 26—AUDIO DISTRIBUTION AMPLIFIER



Note A: These resistor values may be adjusted for a symmetrical output.

FIGURE 27—100-kHz QUADRATURE OSCILLATOR

TYPICAL APPLICATION DATA



† or TL085

2 kHz/div
SECOND-ORDER BANDPASS FILTER
f_o = 100 kHz, Q = 30, GAIN = 4

2 kHz/div
CASCADED BANDPASS FILTER
f_o = 100 kHz, Q = 69, GAIN = 16

FIGURE 28—POSITIVE-FEEDBACK BANDPASS FILTER

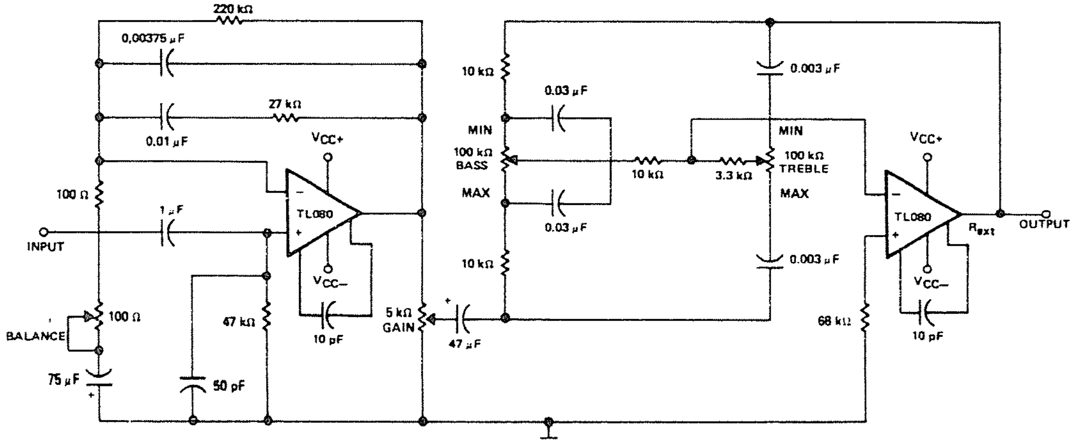


FIGURE 29—IC PREAMPLIFIER

SCHOTTKY† PROMS

SERIES 14 AND 18 PROGRAMMABLE READ-ONLY MEMORIES

JUNE 1981

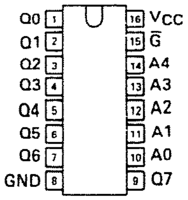
- Titanium-Tungsten (Ti-W) Fuse Link For Reliable Low-Voltage Full Family Compatible Programming
- Full Decoding And Fast Chip Select Simplify System Design
- P-N-P Inputs For Reduced Loading On System Buffers/Drivers
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

NEW TYPE NUMBER 0°C to 70°C	OLD TYPE NUMBER 0°C to 70°C	BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION†	TYPICAL PERFORMANCE	
				ADDRESS ACCESS TIME	POWER DISSIPATION
TBP18SA030 (J, N)▲	SN74S188 (J, N)	256 Bits (32W X 8B)	◇	25 ns	400 mW
TBP18S030 (J, N)▲	SN74S288 (J, N)		▽		
TBP14S10 (J, N)▲	SN74S287 (J, N)	1024 Bits (256W X 4B)	▽	42 ns	500 mW
TBP14SA10 (J, N)▲	SN74S387 (J, N)		◇		
TBP18SA22 (J, N)▲	SN74S470 (J, N)	2048 Bits (256W X 8B)	◇	50 ns	550 mW
TBP18S22 (J, N)▲	SN74S471 (J, N)		▽		
TBP18S42 (J, N)▲	SN74S472 (J, N)	4096 Bits (512W X 8B)	▽	55 ns	600 mW
TBP18SA42 (J, N)▲	SN74S473 (J, N)		◇		
TBP18S46 (J, N)▲	SN74S474 (J, N)	4096 Bits (512W X 8B)	▽	55 ns	600 mW
TBP18SA46 (J, N)▲	SN74S475 (J, N)		◇		

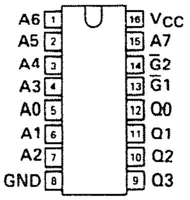
▲ For full temperature parts (−55°C to +125°C) use suffix MJ. For devices with MIL-STD 883B processing (−55°C to +125°C) see page 2-3.

† ◇ = open collector, ▽ = three state.

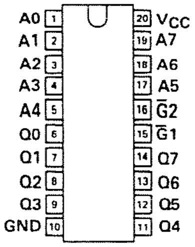
TBP18SA030, TBP18S030
256 BITS
(32 WORDS BY 8 BITS)
(TOP VIEW)



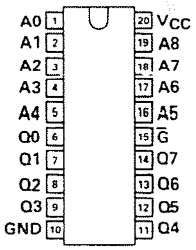
TBP14S10, TBP14SA10
1024 BITS
(256 WORDS BY 4 BITS)
(TOP VIEW)



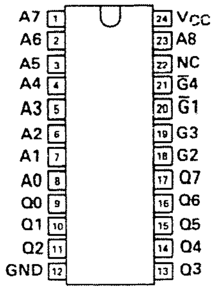
TBP18SA22, TBP18S22
2048 BITS
(256 WORDS BY 8 BITS)
(TOP VIEW)



TBP18S42, TBP18SA42
4096 BITS
(512 WORDS BY 8 BITS)
(TOP VIEW)



TBP18S46, TBP18SA46
4096 BITS
(512 WORDS BY 8 BITS)
(TOP VIEW)



Pin assignments for all of these memories are the same for the J and N packages. See Product Guide, Section 7, for chip carrier pin assignments.

description

These monolithic TTL programmable read-only memories (PROMs) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in 100 microseconds. The Schottky-clamped versions of these PROMs offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit PROMs can be used to significantly improve system density for fixed memories as all are offered in the 20-pin dual-in-line package having pin-row spacings of 0.300 inch (7,62 mm).

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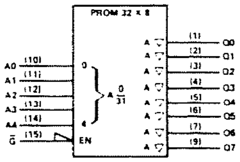
† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

logic symbols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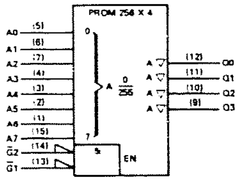
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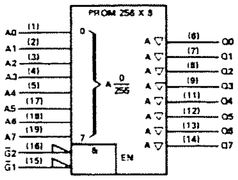
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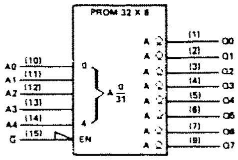
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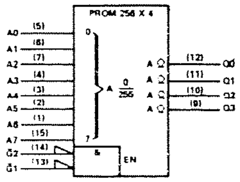
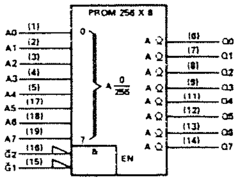

TBP14SA10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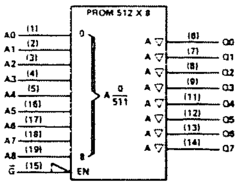
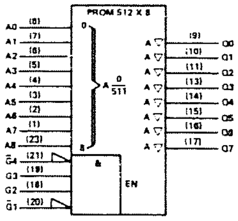
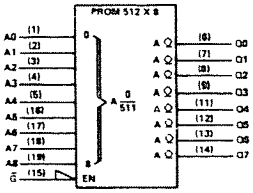
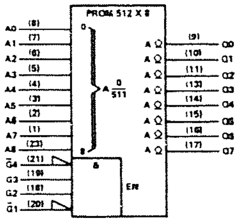

TBP18S42


TBP18S46


TBP18SA42


TBP18SA46

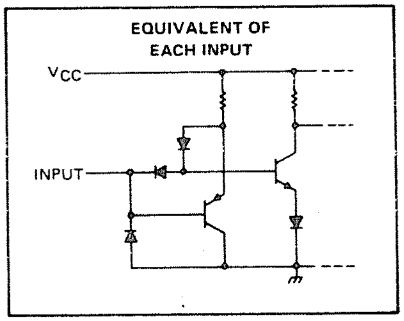
description (continued)

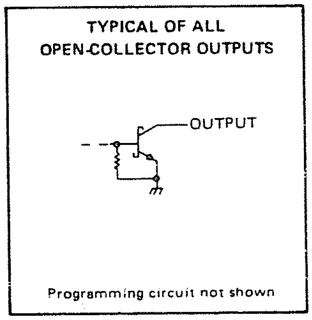
Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROMs, except the TBP14S10 and TBP14SA10 are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs that have never been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

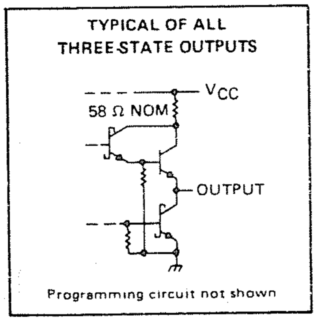
A low level at the chip-select input(s) enables each PROM. The opposite level at any chip-select input causes the outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		7V
Input voltage		5.5V
Off-state output voltage		5.5V
Operating free-air temperature range:	Full-temperature-range circuits	−55°C to 125°C
	Commercial-temperature-range circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

recommended conditions for programming the TBP18S', TBP18SA', TBP14S', and TBP14SA' PROMs

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.25	V
	Program pulse	9	9.25	9.5	
Input voltage	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed			See load circuit (Figure 1)		
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse X (see Figure 2 and Note 3)		15	25	100	µs
Programming duty cycle for Y pulse			25	35	%
Free-air temperature		20	25	30	°C

† Absolute maximum ratings.

NOTES: 1. Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.

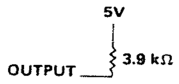
2. The TBP18S030, TBP18SA030, TBP18SA22, TBP18S22, TBP18S42, TBP18SA42, TBP18S46 and TBP18SA46 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The TBP14S10, TBP14SA10 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.

3. Programming is guaranteed if the pulse applied as 98 µs in duration.

step-by-step programming procedure for the TBP18SA030, TBP18S030, TBP14S10, TBP14SA10, TBP18SA22, TBP18S22, TBP18SA42, TBP18S42, TBP18S46, TBP18SA46

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9 kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current into the programmer output is 150 mA.
5. Step V_{CC} to 9.25 nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 1 µs and 1 ms after V_{CC} has reached its 9.25 level. See programming sequence of Figure 2.
7. After the X pulse time is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within the range of 1 µs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 1 µs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.
11. Verify accurate programming of every word after all words have been programmed using V_{CC} values of 4.5 and 5.5 volts.

NOTE: Only one programming attempt per bit is recommended.



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION

FIGURE 1 – LOAD CIRCUIT

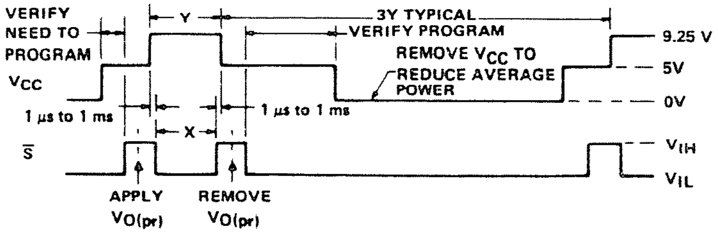


FIGURE 2 – VOLTAGE WAVEFORMS FOR PROGRAMMING

recommended operating conditions

PARAMETER		TBP14S10, TBP18S22			TBP18S030			TBP18S42, TBP18S46			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−6.5			−6.5			−6.5	
Low-level output current, I_{OL}				16			20			12	mA
Operating free-air temperature, T_A	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		FULL TEMP (MJ)			COMM. TEMP (J, N)			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	$I_I = -18$ mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50			50	µA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50			−50	µA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	µA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	TBP14S10		100	135		100	135	mA
			TBP18S030		80	110		80	110	
			TBP18S22		110	155		110	155	
			TBP18S42, TBP18S46		120	155		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(A)}$ (ns) Access time from address			$t_{a(S)}$ (ns) Access time from chip select (enable time)			t_{PXZ} (ns) Disable time from high or low level			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
TBP14S10MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, 5 pF for t_{PXZ}, See Page 1-12		42	75		15	40		12	40	ns
TBP14S10			42	65		15	35		12	35	ns
TBP18S030MJ			25	50		12	30		8	30	ns
TBP18S030			25	40		12	25		8	20	ns
TBP18S22MJ			50	80		20	40		15	35	ns
TBP18S22			50	70		20	35		15	30	ns
TBP18S42MJ, TBP18S46MJ			55	85		20	45		15	40	ns
TBP18S42, TBP18S46			55	75		20	40		15	35	ns

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 4: The typical values of I_{CC} are with all outputs low.

SERIES 14 AND 18
PROGRAMMABLE READ-ONLY MEMORIES
WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

PARAMETER		TBP14SA10, TBP18SA22 MIN	NOM	MAX	TBP18SA030 MIN	NOM	MAX	TBP18SA42, TBP18SA46 MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}				16			20			16	mA
Operating free-air temperature, T_A	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	$I_I = -18$ mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50	μA
			V_{OH} = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250	μA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	TBP18SA030		80	110	mA
			TBP14SA10		100	135	
			TBP18SA22		110	155	
			TBP18SA42, TBP18SA46		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(A)}$ Access time from address MIN	TYP‡	MAX	$t_{a(S)}$ Access time from chip select (enable time) MIN	TYP‡	MAX	t_{PLH} Propagation delay time, low-to-high-level output from chip select (disable time) MIN	TYP‡	MAX	UNIT
TBP18SA030MJ	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Page 1-12		25	50		12	30		12	30	ns
TBP18SA030			25	40		12	25		12	25	ns
TBP14SA10MJ			42	75		15	40		15	40	ns
TBP14SA10			42	65		15	35		15	35	ns
TBP18SA22MJ			50	80		20	40		15	35	ns
TBPSA22			50	70		20	35		15	30	ns
TBP18SA42MJ, TBP18SA46MJ			55	85		20	45		15	40	ns
TBP18SA42, TBP18SA46			55	75		20	40		15	35	ns

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

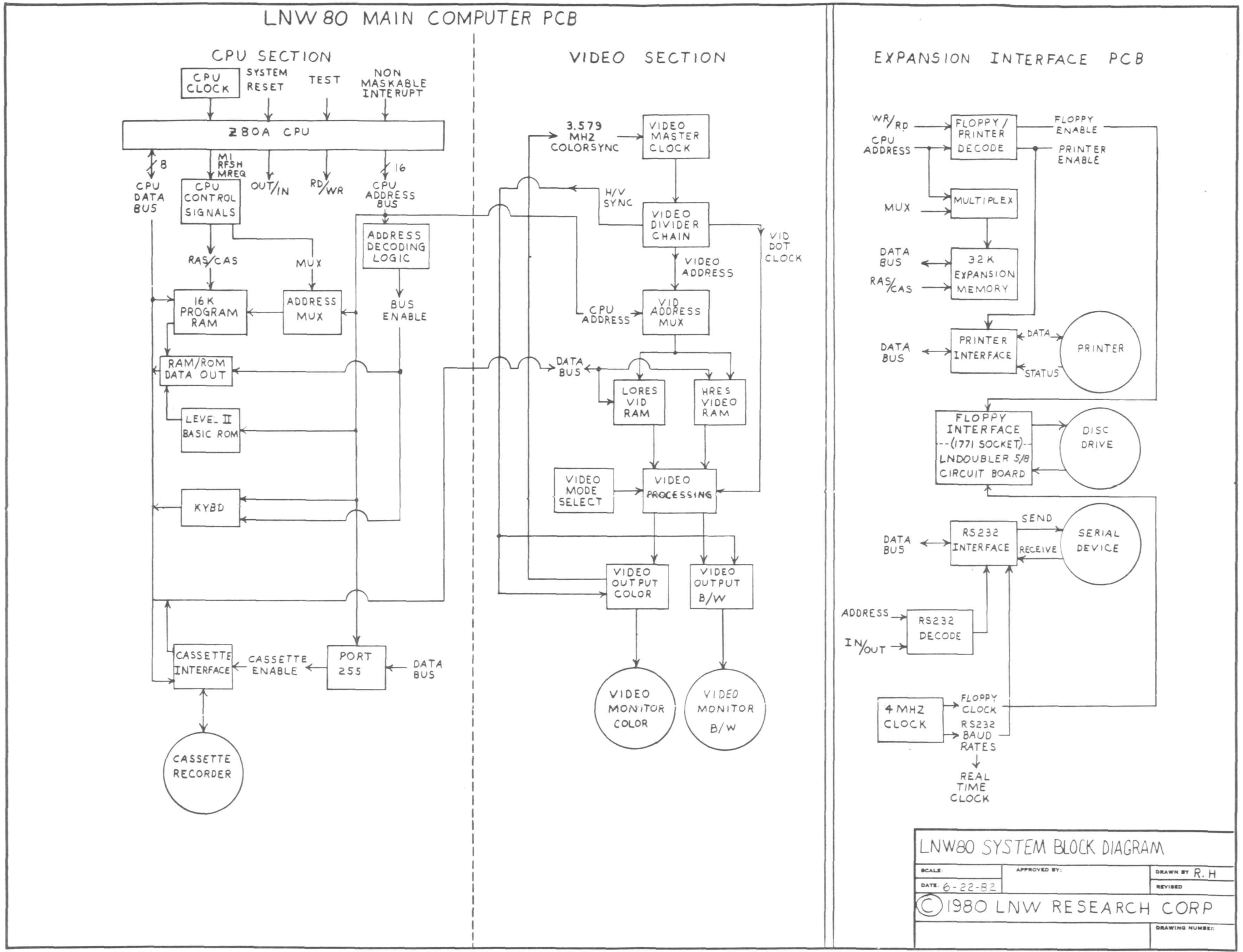
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 4: The typical values of I_{CC} are with all output low.

APPENDIX 2 ENGINEERING DRAWINGS

1. BLOCK DIAGRAM
2. LNW80 PRINTED CIRCUIT BOARD SCHEMATIC PAGE 1 OF 4
3. LNW80 PRINTED CIRCUIT BOARD SCHEMATIC PAGE 2 OF 4
4. LNW80 PRINTED CIRCUIT BOARD SCHEMATIC PAGE 3 OF 4
5. LNW80 PRINTED CIRCUIT BOARD SCHEMATIC PAGE 4 OF 4
6. KEYBOARD SCHEMATIC
7. EXPANSION BOARD SCHEMATIC PAGE 1 OF 2
8. EXPANSION BOARD SCHEMATIC PAGE 2 OF 2
9. LNDOUBLER 5/8 SCHEMATICS
10. TOP ASSEMBLY LNW80
11. LNW80 PRINTED CIRCUIT BOARD COMPONENT SIDE
12. LNW80 PRINTED CIRCUIT BOARD SOLDER SIDE
13. LNW80 PRINTED CIRCUIT BOARD ASSEMBLY DRAWING
14. LNW80 PRINTED CIRCUIT BOARD ASSEMBLY DRAWING
15. SYSTEM EXPANSION PRINTED CIRCUIT BOARD COMPONENT SIDE
16. SYSTEM EXPANSION PRINTED CIRCUIT BOARD SOLDER SIDE
17. EXPANSION FINAL ASSEMBLY DRAWING
18. LNDOUBLER 5/8 PRINTED CIRCUIT BOARD



LNW80 SYSTEM BLOCK DIAGRAM

SCALE:
APPROVED BY:
DRAWN BY R. H
DATE: 6-22-82
REVISED

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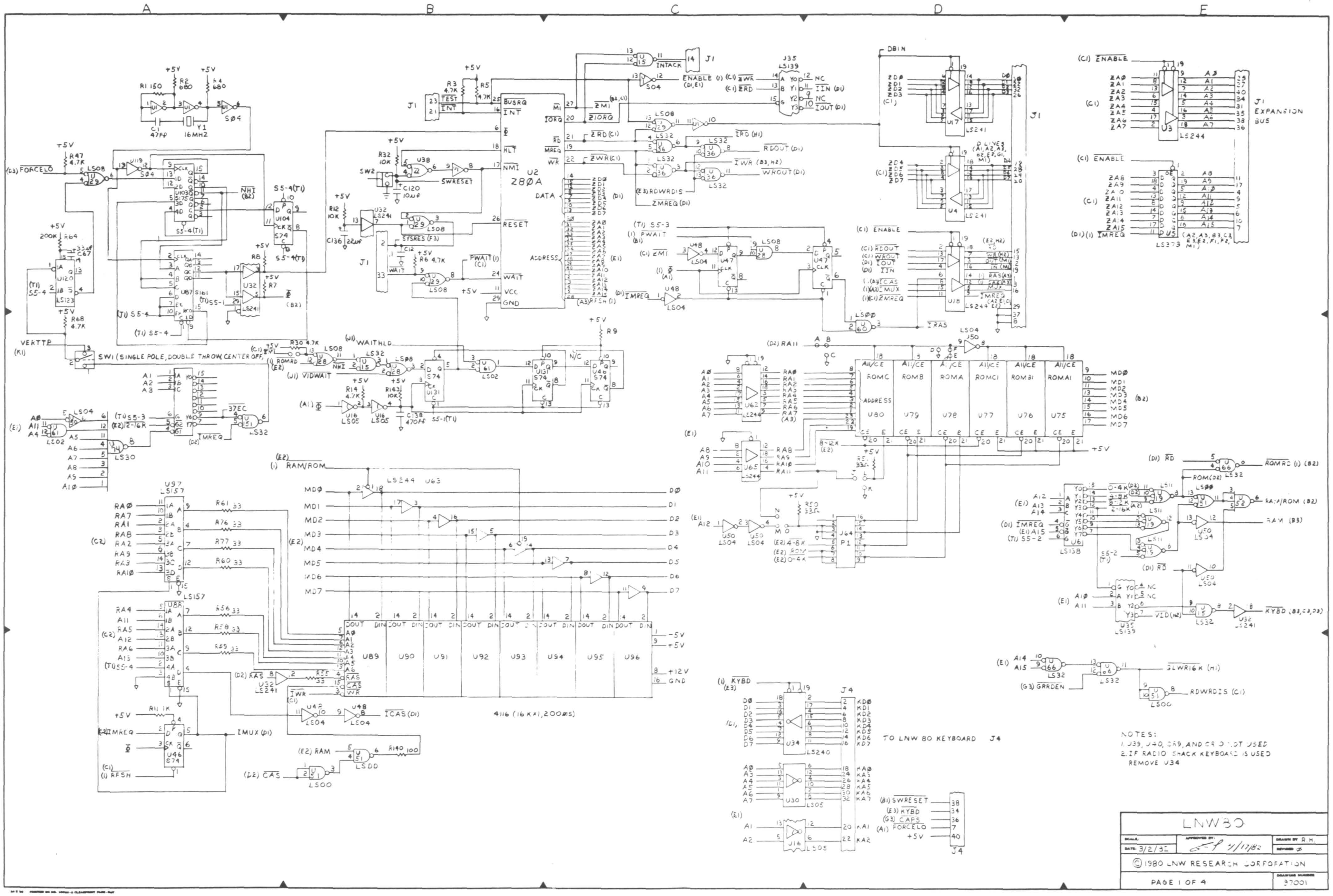
DRAWING NUMBER:

17236 PRINTED ON NO. 1000H-8 CLEARPRINT FADE-OUT



NOTES:
1. U39, U40, CR9, AND CR10 NOT USED
2. IF RADIO SHACK KEYBOARD IS USED
REMOVE U34

LNW80

SCALE:
DATE: 3/2/81
APPROVED BY: 4/17/82
DRAWN BY R.H.
REVISED 0

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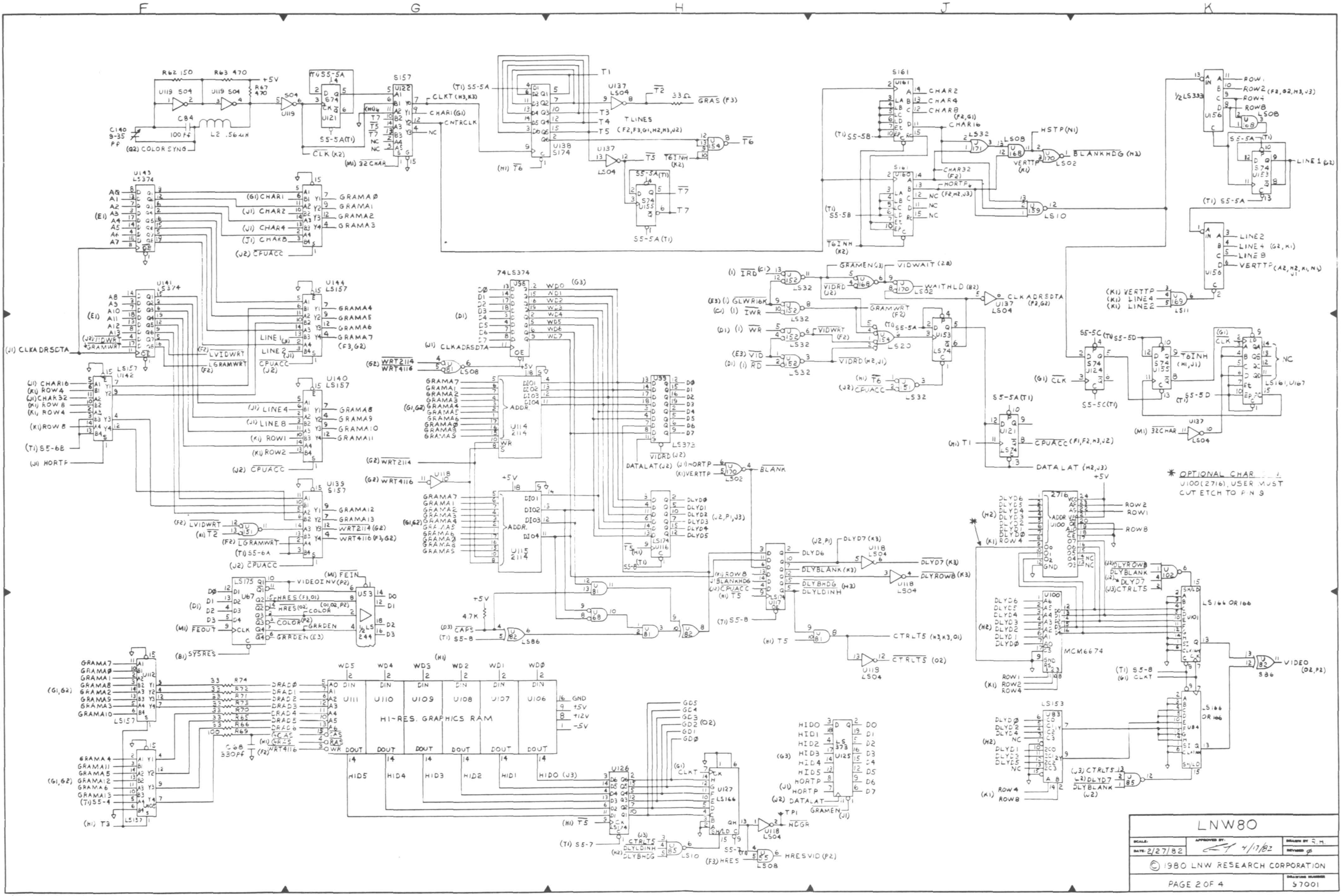
PAGE 1 OF 4
DRAWING NUMBER 37001



* OPTIONAL CHAR
U100 (2716), USER MUST
CUT ETCH TO PIN 9

LNW80

SCALE:

APPROVED BY: 4/17/82

DRAWN BY R.H.

DATE: 2/27/82

REVISED 0

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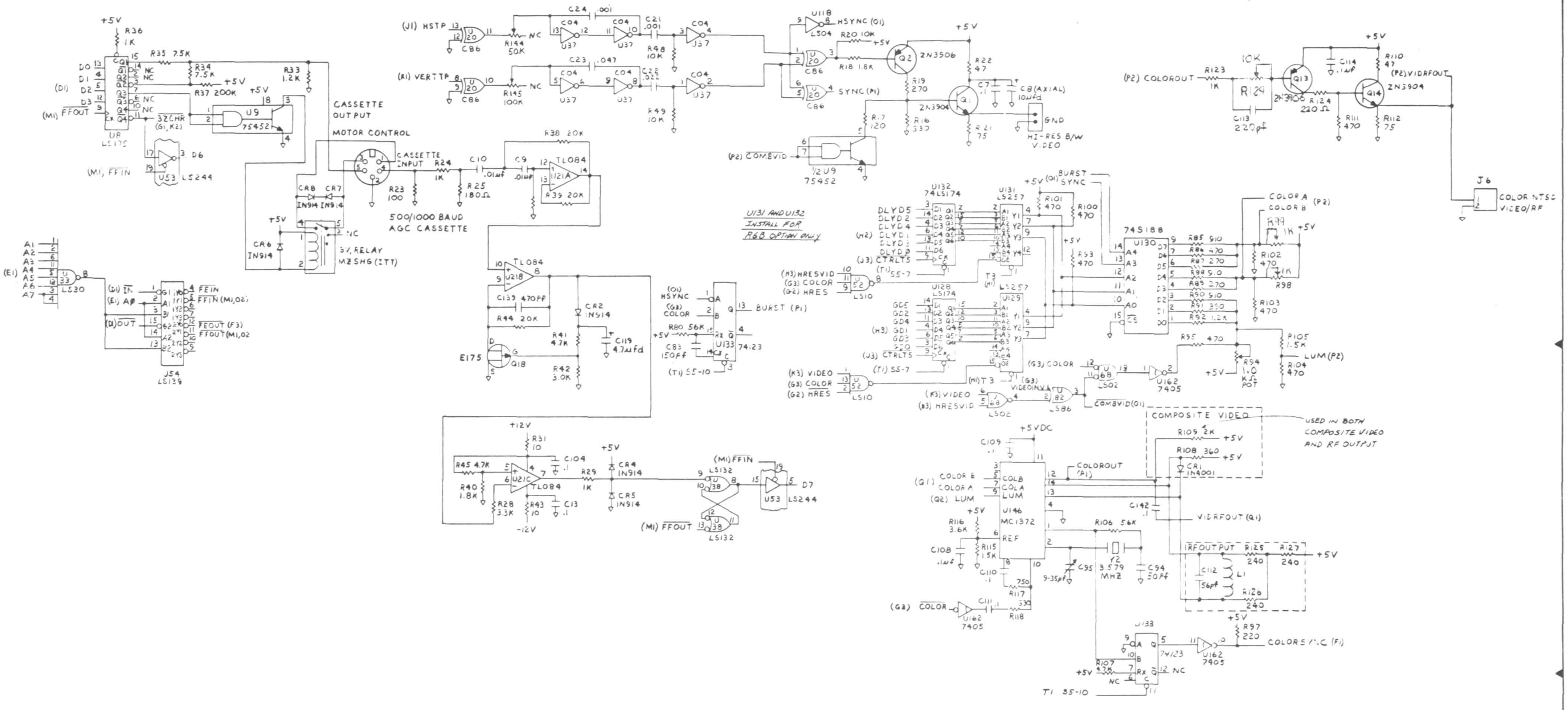
PAGE 2 OF 4

DRAWING NUMBER 57001



LNW80

SCALE:

DATE: 3/3/82

APPROVED BY: 4/17/82

DRAWN BY R.H.

REVISED

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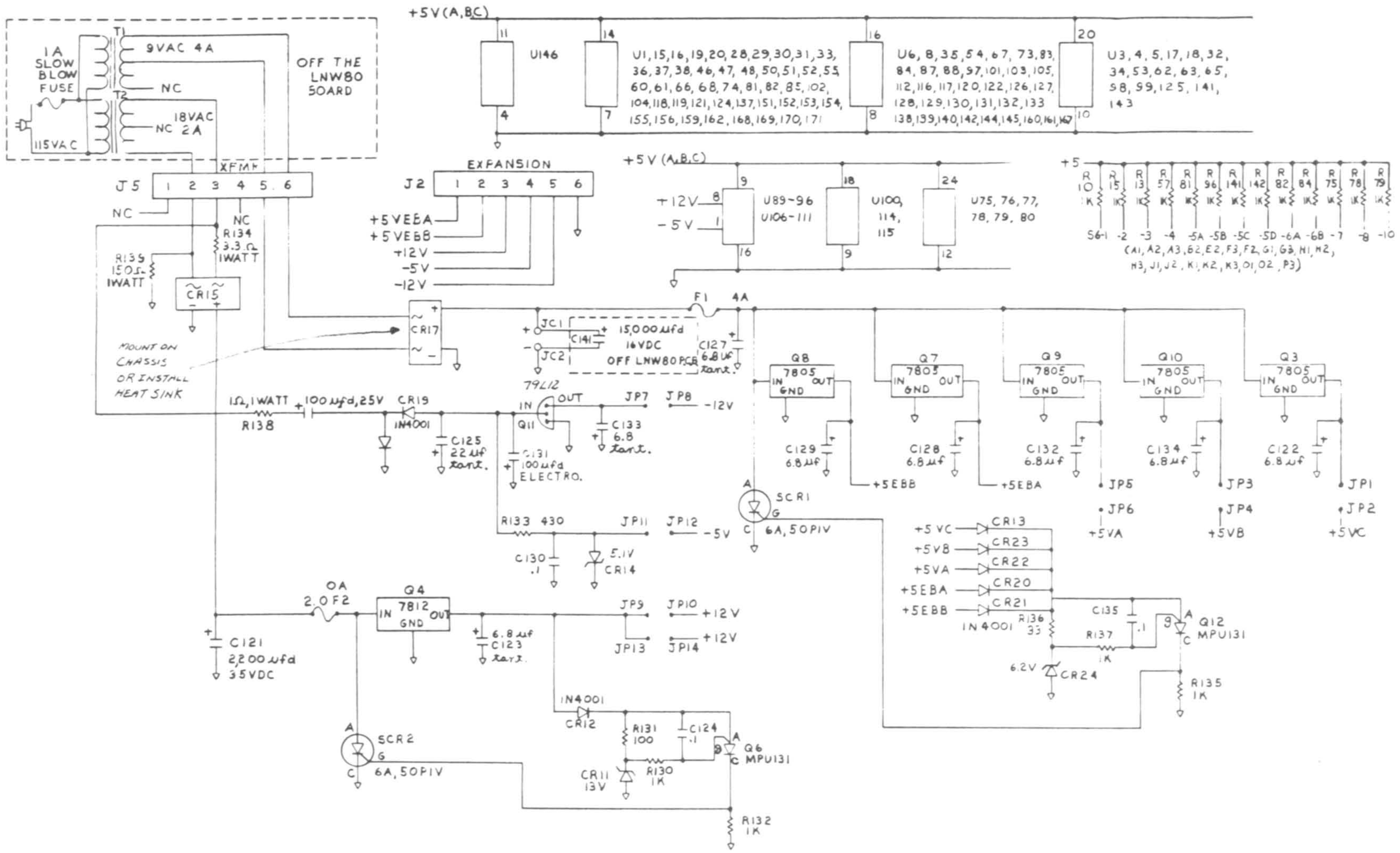
PAGE 3 OF 4

DRAWING NUMBER 97001



LNW80

SCALE:

APPROVED BY: -/17/82

DRAWN BY R.H.

DATE: 2/26/82

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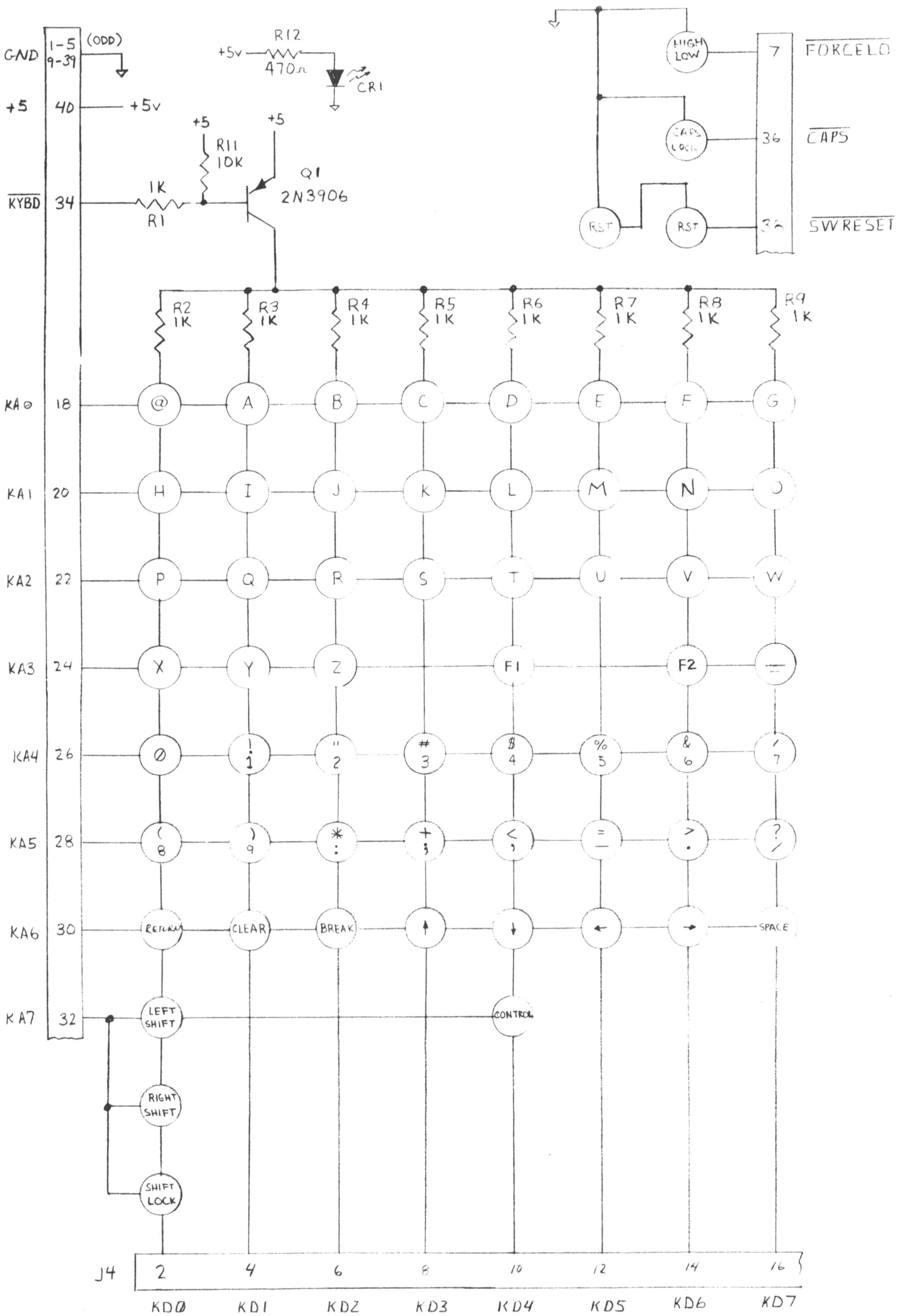
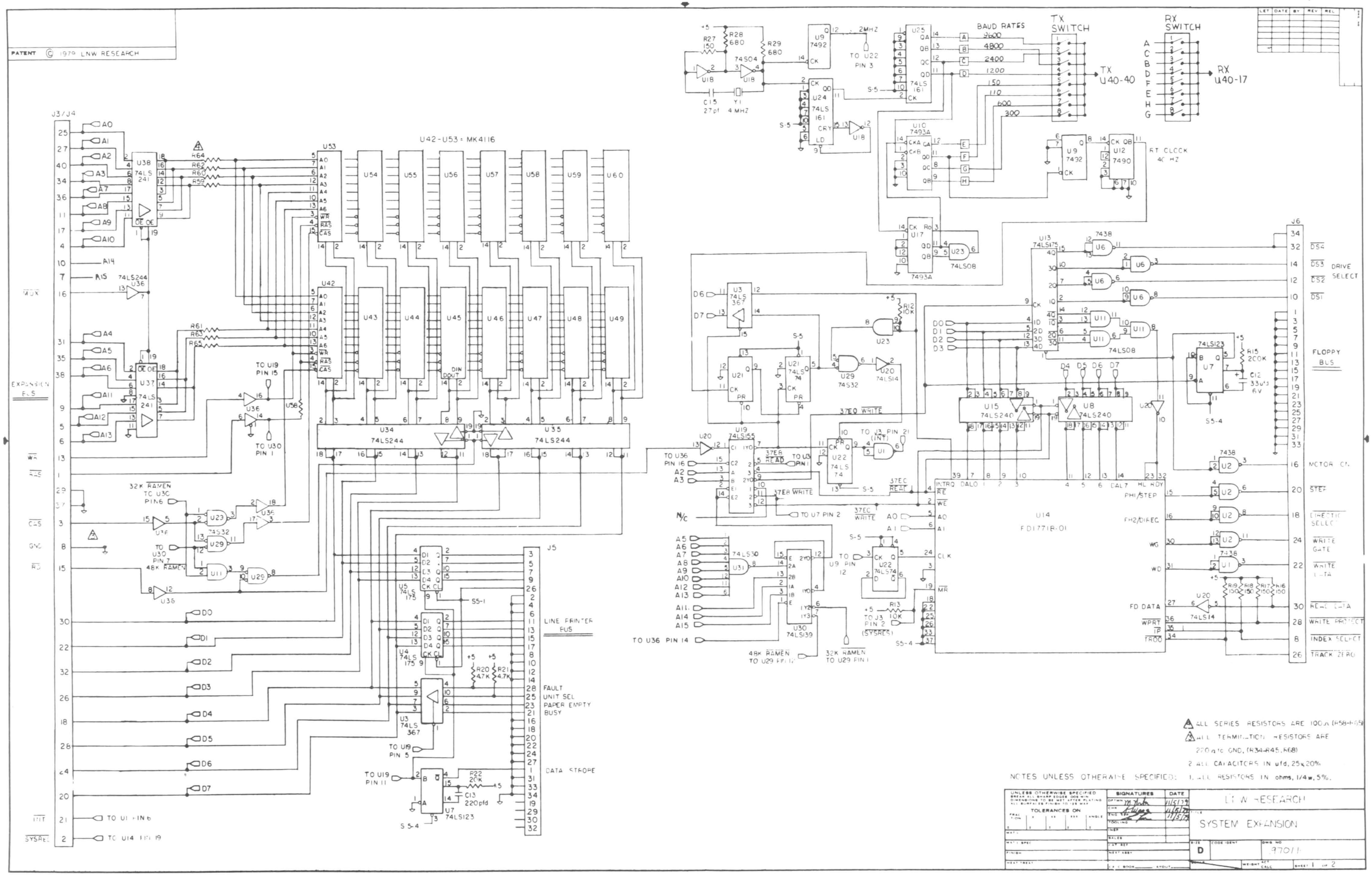
PAGE 4 OF 4

DRAWING NUMBER 97001



© 1980	LNW RESEARCH CORPORATION LNW80 KEYBOARD
2-3-81 A	
7-21-82 B	

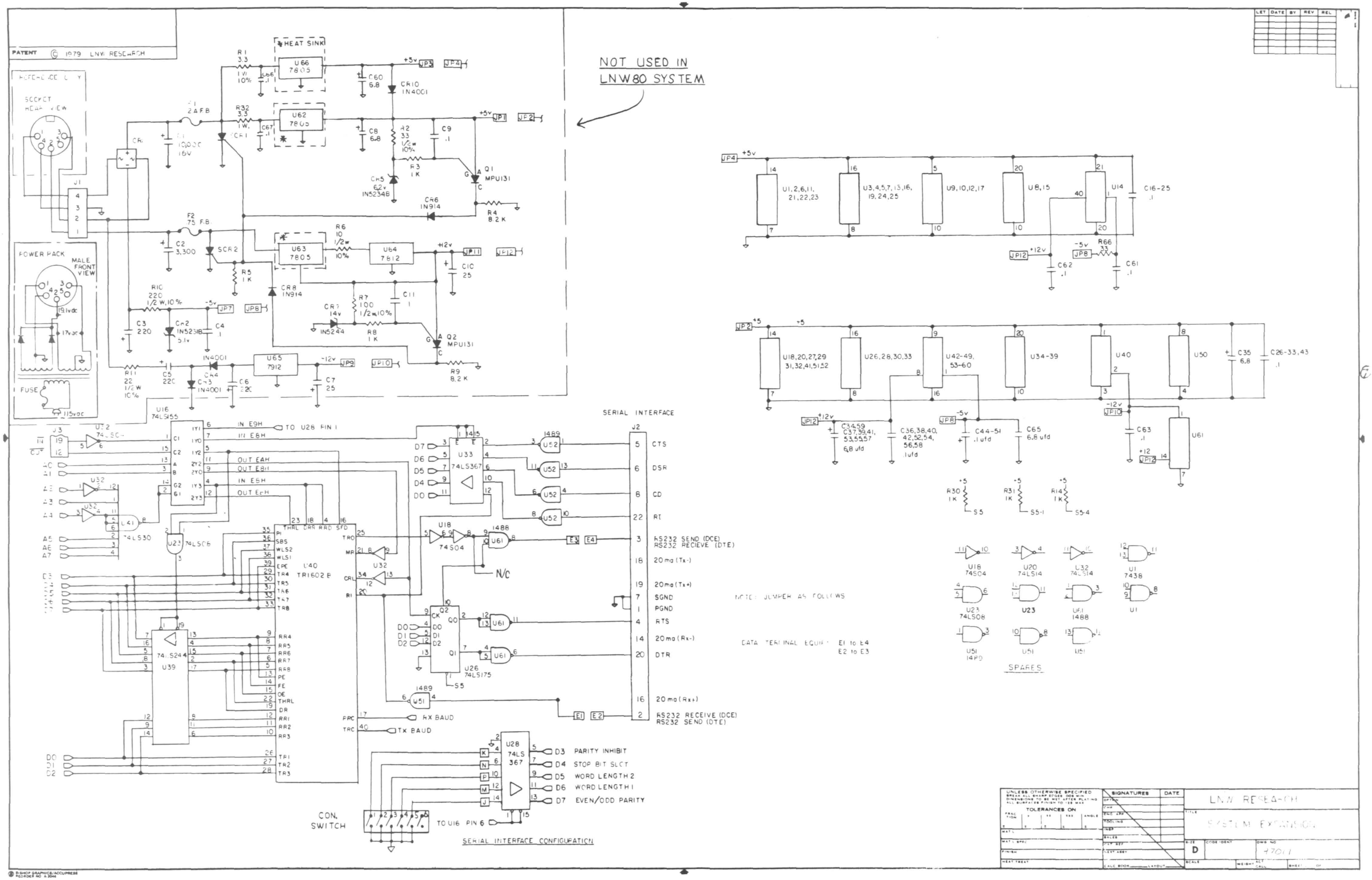
PATENT © 1979 LNW RESEARCH



NOTES UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS IN ohms, 1/4 w, 5%.
2. ALL CAPACITORS IN ufd, 25v 20%
3. ALL TERMINATION RESISTORS ARE 220 Ω to GND, (R34-R45, R68)
4. ALL SERIES RESISTORS ARE 100Ω (R58-R65)

UNLESS OTHERWISE SPECIFIED BREAK ALL SHARP EDGES .005 MIN DIMENSIONS TO BE MET AFTER PLATING ALL SURFACES FINISH TO 125 MAX	SIGNATURES	DATE	LNW RESEARCH
TOLERANCES ON	DFTMN M. Horton	11/5/79	TITLE SYSTEM EXPANSION
	CHK	11/5/79	
	ENG	11/5/79	
	SIZE D	CODE IDENT	DWG NO 97011
			SHEET 1 OF 2

PATENT © 1979 LNW RESEARCH



NOT USED IN
LNW80 SYSTEM

NOTE: JUMPER AS FOLLOWS

DATA TERMINAL EQUIP: E1 to E4
E2 to E3

LET	DATE	BY	REV	REL

UNLESS OTHERWISE SPECIFIED
BREAK ALL SHARP EDGES .005 MIN
DIMENSIONS TO BE MET AFTER PLATING
ALL SURFACES FINISH TO 125 MAX

TOLERANCES ON
FRACTION ± | X ± | XX ± | XXX ± | ANGLE ±

MAT'L
MAT'L SPEC
FINISH
HEAT TREAT

SIGNATURES	DATE
DFTSMN	
CHK	
ENG APP	
TOOLING	
INSP	
SALES	

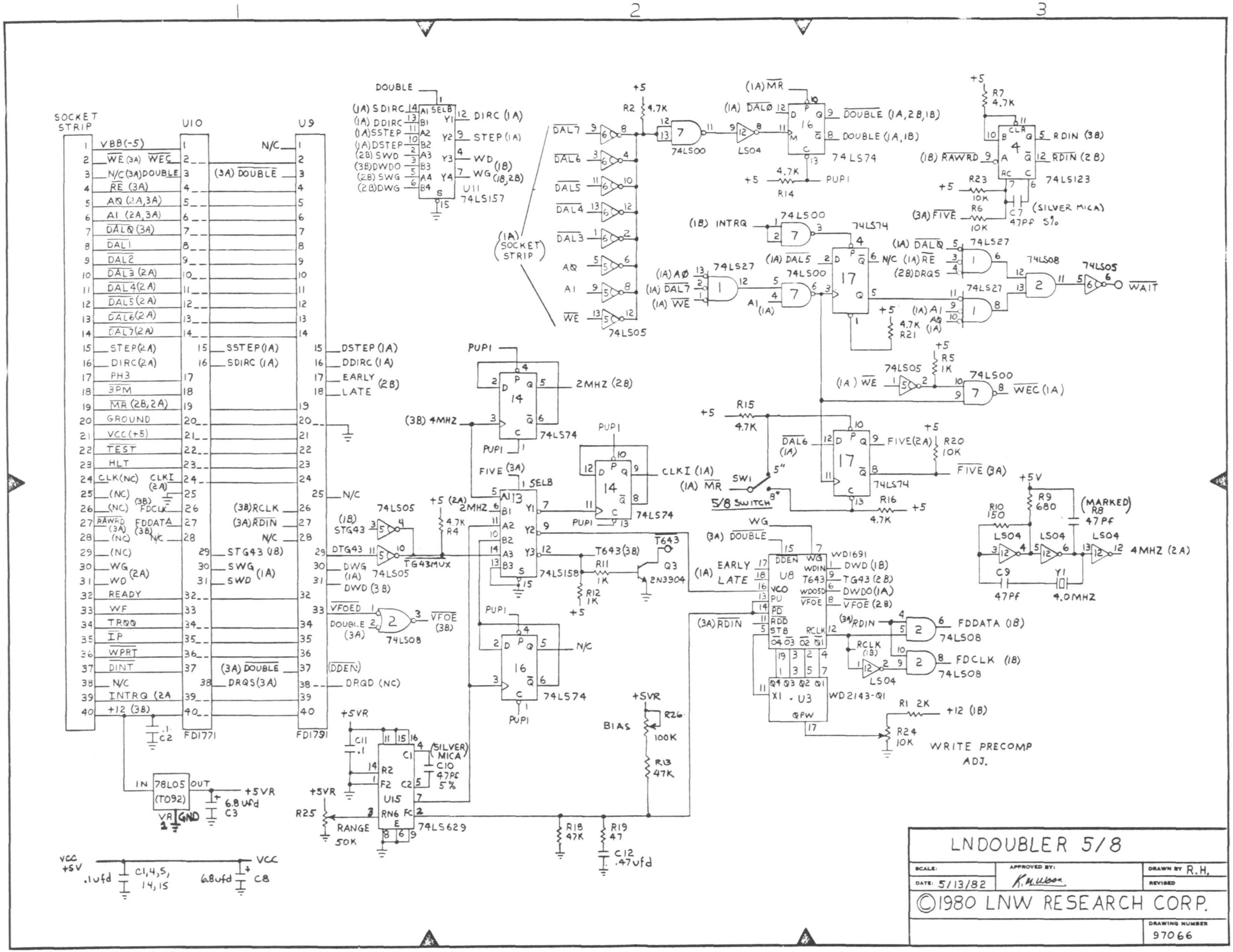
CAT REF
NEXT ASSY
CALC BOOK ____ LAYOUT ____

LNW RESEARCH

TITLE
SYSTEM EXPANSION

SIZE D
CODE IDENT
DWG NO 47011
SCALE
WEIGHT ACT CALC
SHEET OF

BISHOP GRAPHICS/ACCUPRESS REORDER NO A 2046



LNDOUBLER 5/8

SCALE:
APPROVED BY: K. Mullen
DRAWN BY R.H.
DATE: 5/13/82
REVISED

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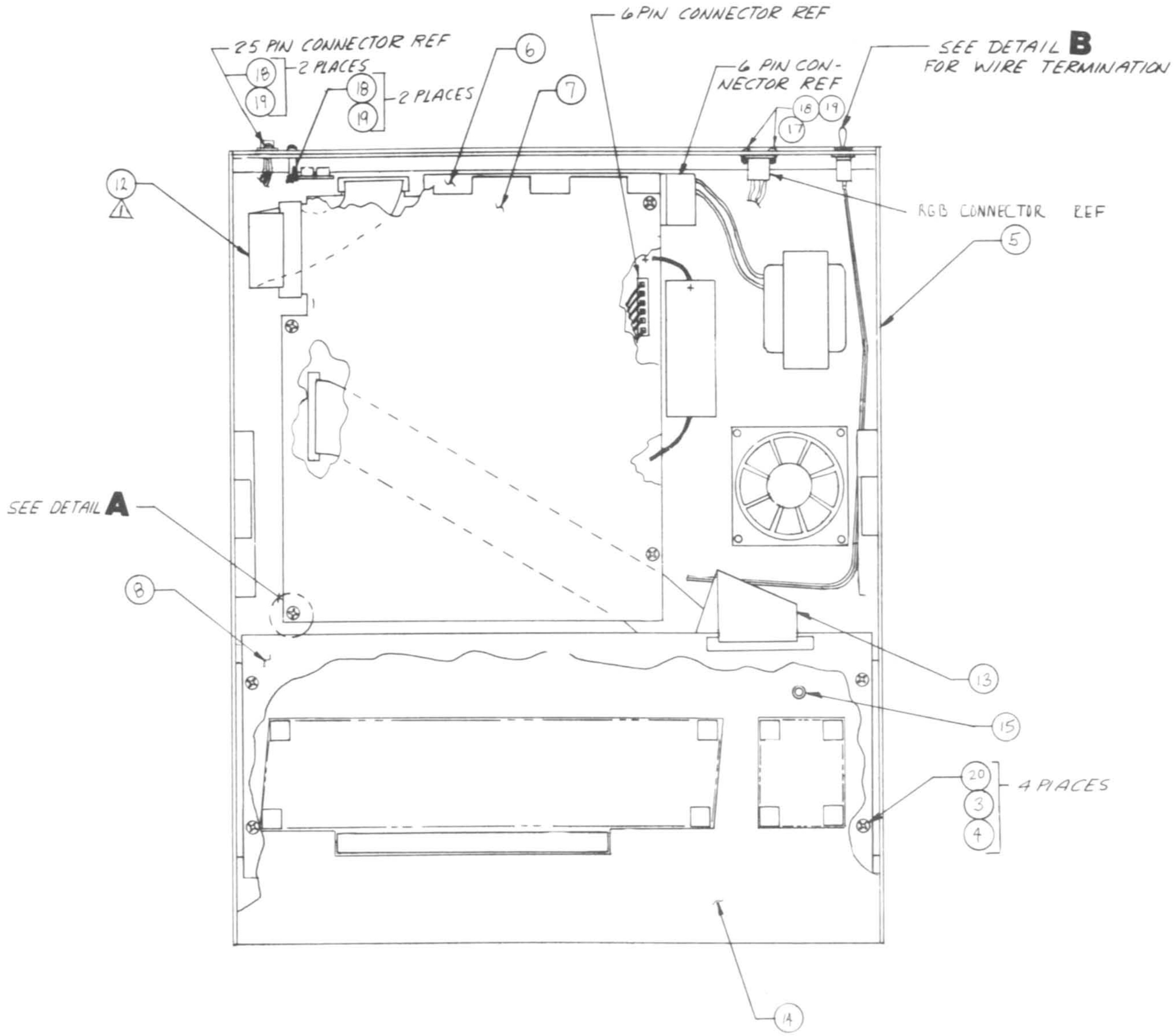
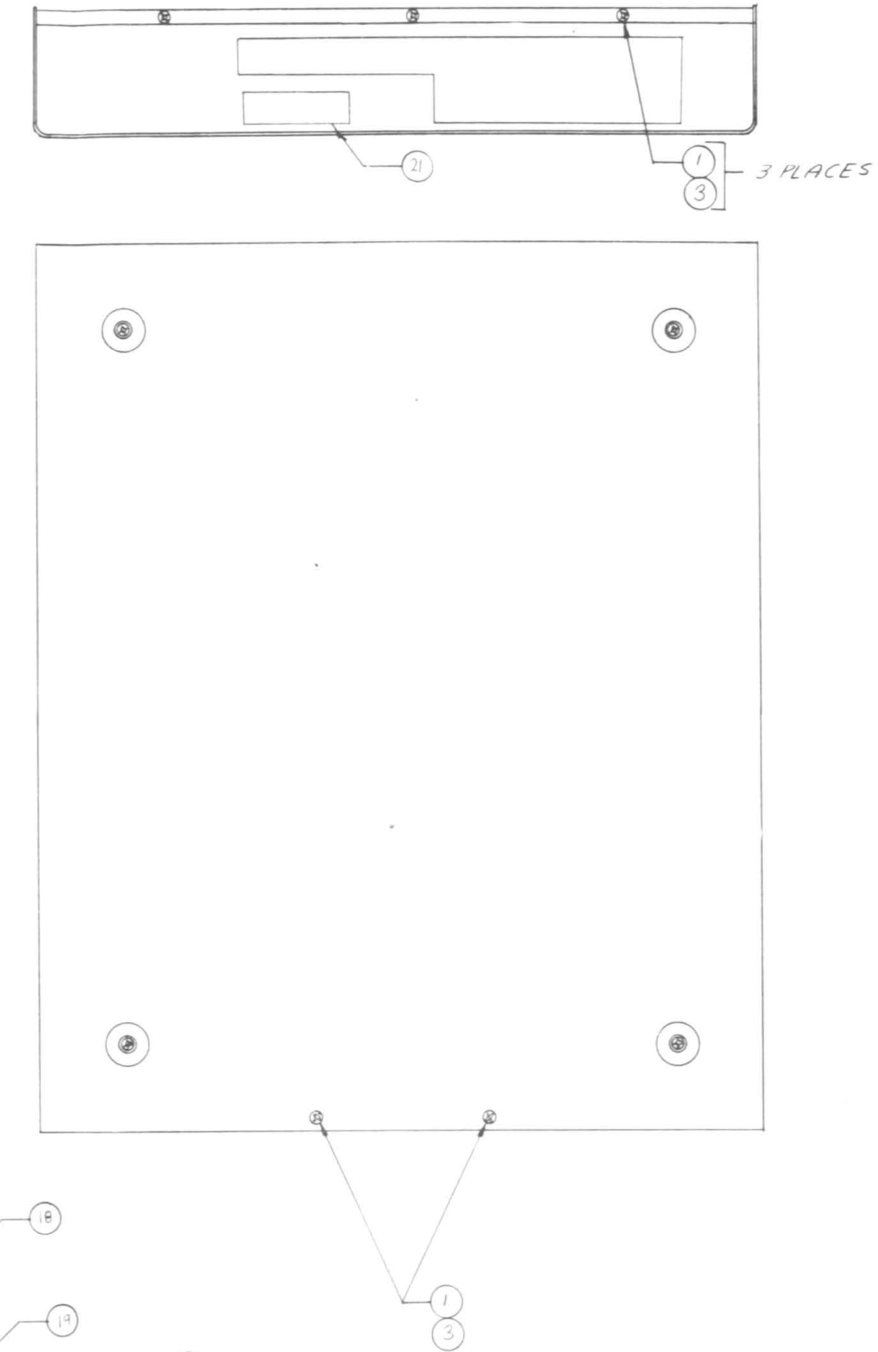
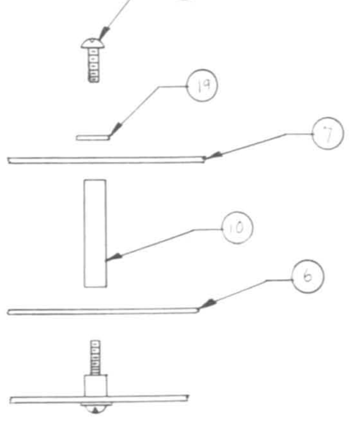
DRAWING NUMBER 97066

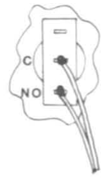
17322 PRINTED ON NO. 1000H-5 CLEARPRINT FADE-OUT







DETAIL **A** (4 PLACES)
SCALE: NONE



DETAIL **B**
SCALE: NONE

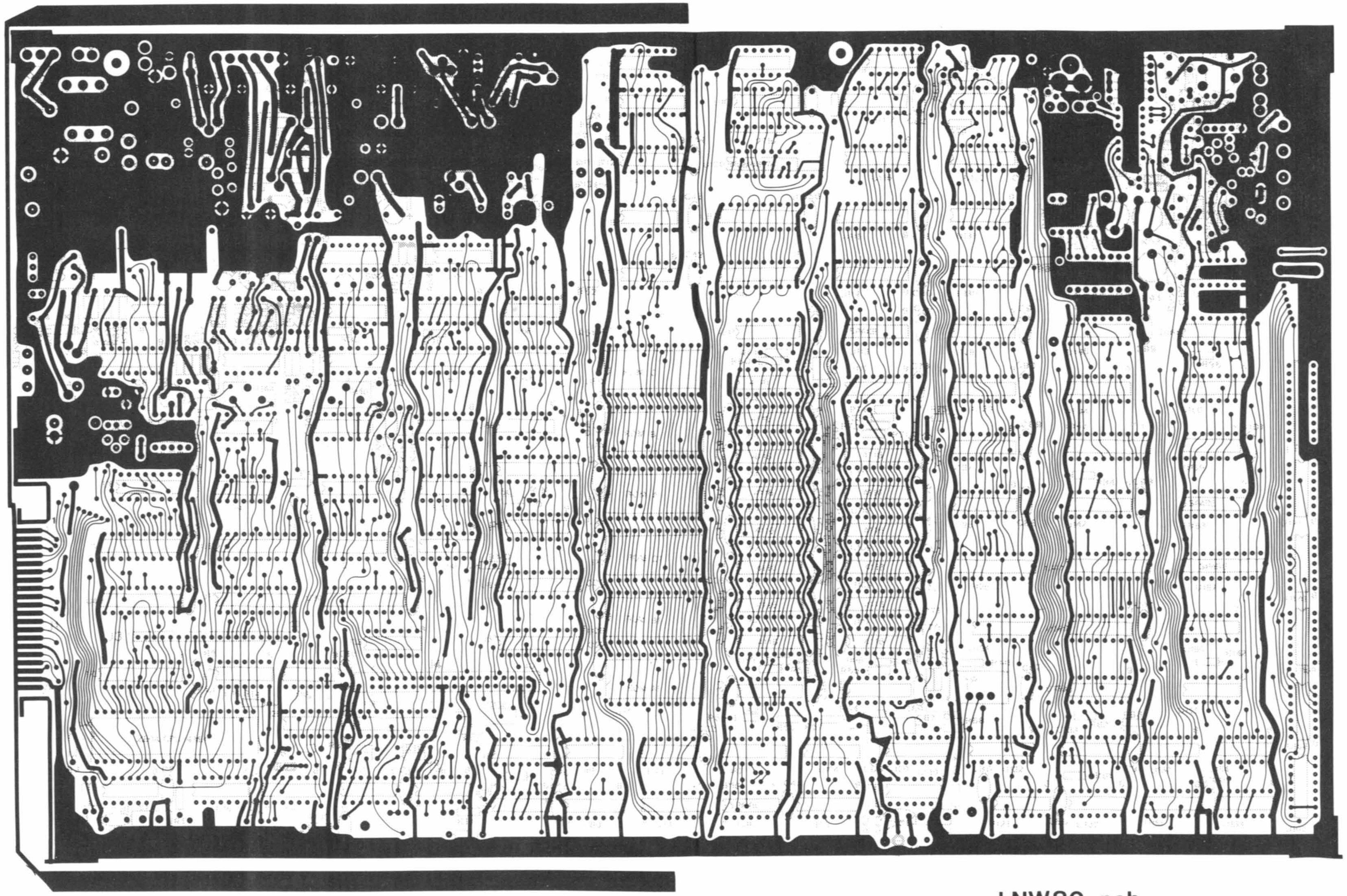
2 PAINT ALL EXTERIOR SCREWS PAINT #27122

⚠1 SHIELD ON CABLE SUCH THAT
BLUE LINE INDICATES PIN 39

NOTES UNLESS OTHERWISE SPECIFIED

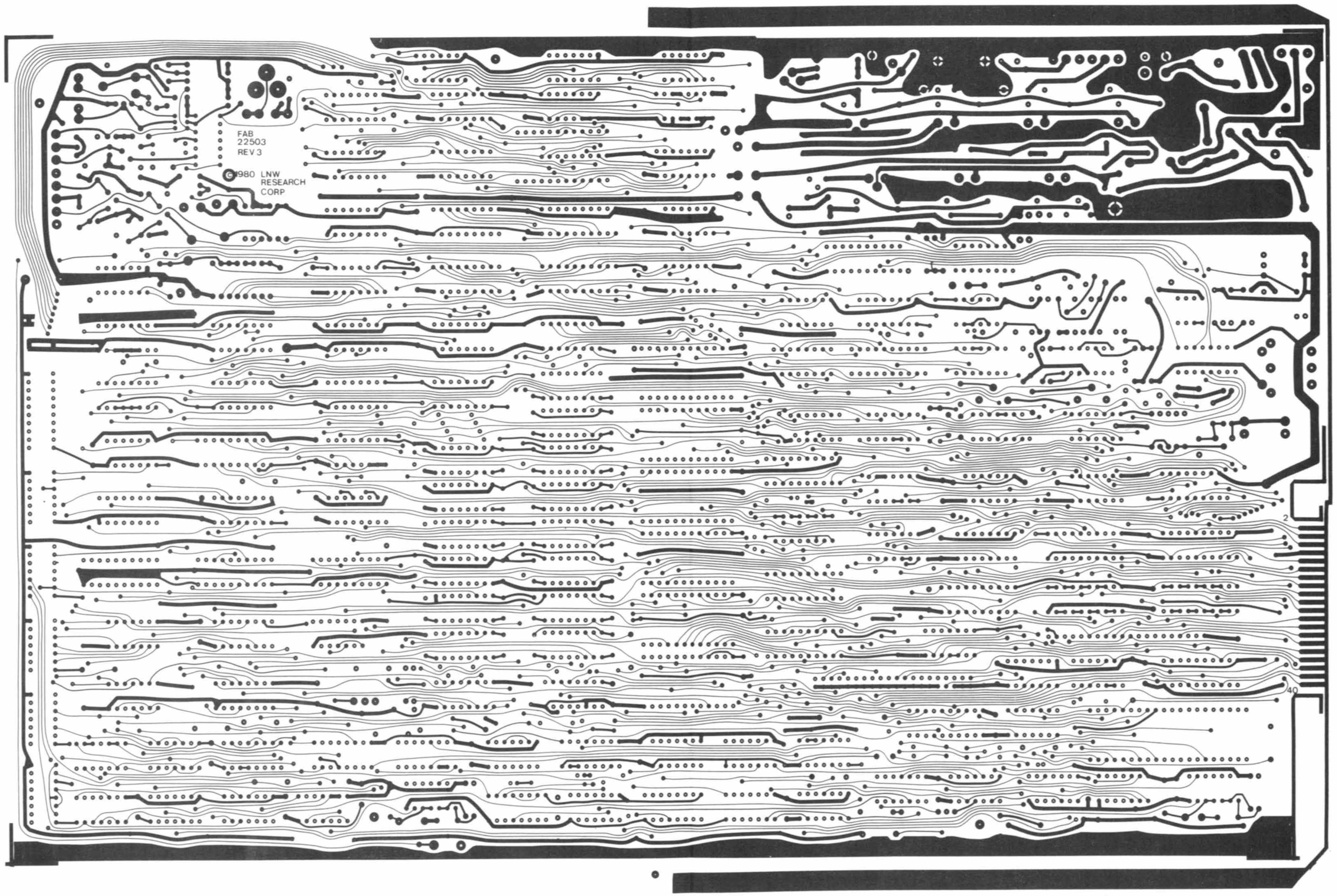
LNW RESEARCH CORP.		
SCALE: 1/2	APPROVED BY M. Nichols 6/3/82	DRAWN BY A Gordon
DATE: 4/25/82		REVISED
TOP ASSEMBLY LNW 80		
	DRAWING NUMBER 95000	REV C

33534 PRINTED ON NO. 1000H-8 CLEARPRINT FADE-OUT



COMPONENT SIDE

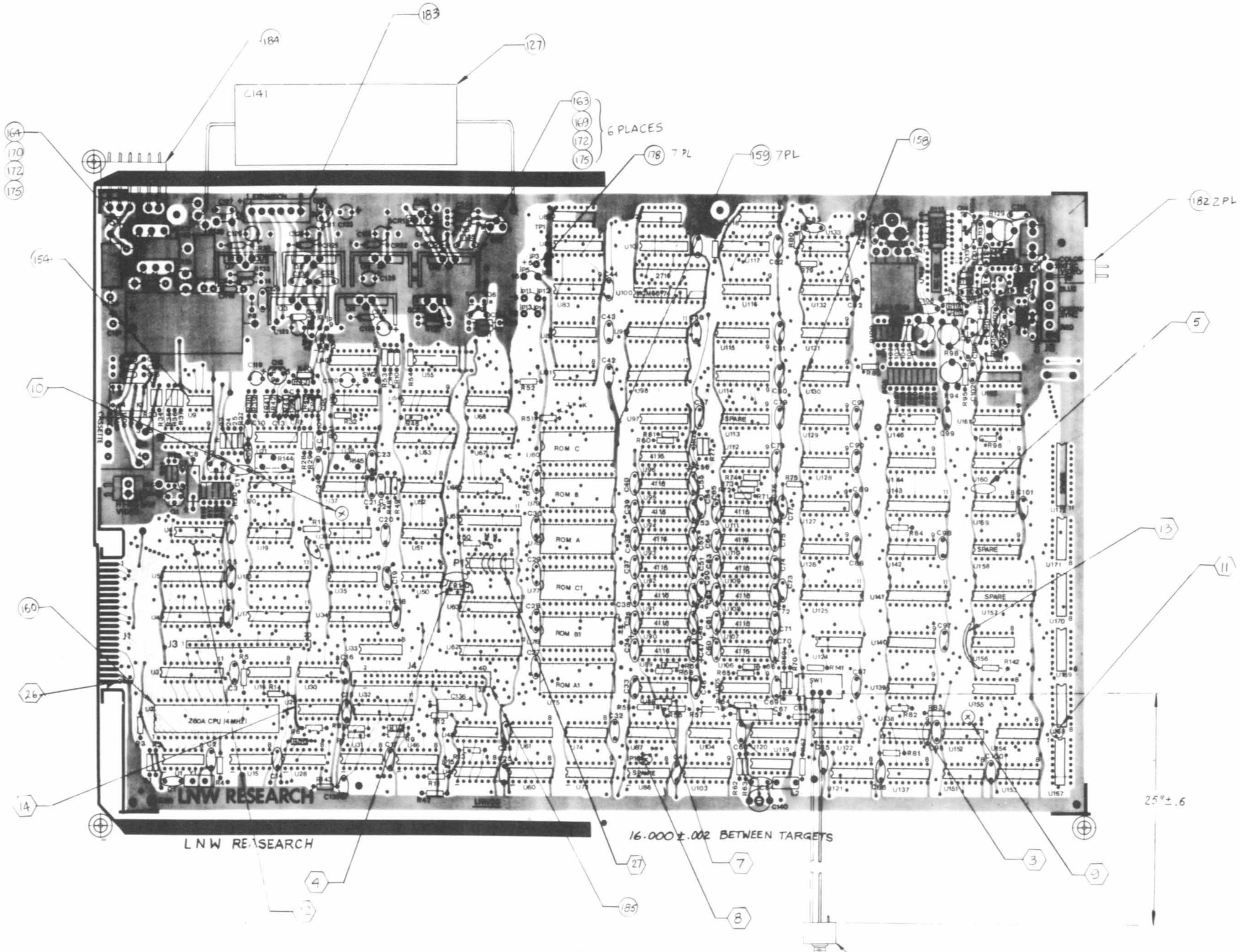
LNW80 pcb



SOLDER SIDE

LNW80 pcb

REVISIONS				
PART REV.	DOC REV.	DESCRIPTIONS	DATE	APPROVED



⑫ CUT TRACE AT U153 PIN 5 (CKT SIDE, SH2
⑪ CUT TRACE AT U168 PIN 6 (BELOW U168)
⑩ CUT TRACE AT U36 PIN 12.
⑨ CUT TRACE AT U152 PIN 10.
⑧ CUT TRACE BETWEEN U46 PIN 5 TO U88 PIN 1
⑦ ADDED RESISTOR 330Ω FROM U88 PIN 1 TO U87 PIN 8. (R124)
⑥ ADDED CAPACITOR 330pF FROM U37 PIN 6 TO U37 PIN 7 (CKT SIDE, SH2)(C146)
⑤ ADDED CAPACITOR 220pF FROM U159 PIN 12 TO U159 PIN 14. (C143)
④ ADDED CAPACITOR 100pF FROM R140 TO U70 PIN 7. (C144)
③ ADDED CAPACITOR 47pF FROM U138 PIN 9 TO U138 PIN 8. (C145)
2. U2, 75-80, 100 130, C141, SW1 SHALL BE INSTALL AT FINAL ASSEMBLY.

1. ASSEMBLE PER LNW RESEARCH WORKMANSHIP STANDARD.
NOTES: UNLESS OTHERWISE SPECIFIED

㉗ JUMPER P1: 2-15, 4-13, 5-12, 7-10
㉖ JUMPER FROM J1-39 TO J1-37
㉕ JUMPER FROM U28-13 TO SW1-1
㉔ JUMPER FROM U18-5 TO U97-1
㉓ U18-7 U89-3
㉒ U6-4 U6-5 (U6-4 lifted)
㉑ U36-3 U152-10
⑳ JP15 PAD ABOVE SILK SCREEN JP16
⑲ U153-6 U170-11
⑱ U170-8 U170-9
⑰ U170-12 U170-1
⑯ U170-13 U121-12
⑮
⑭ R6 R14 (USE LEAD OF R14. DO NOT PLACE R14 LEAD IN FED-THRU)
⑬ JUMPER FROM R142 TO U156 PIN 14

UN-028 R_a in micron/micro-inch
GEN. ROUGHNESS
UNIT
SCALE FULL
PROJECTION USA
UN-0803
TOL. UNLESS STATED OTHERWISE
TREATMENT/FINISH
MATERIAL

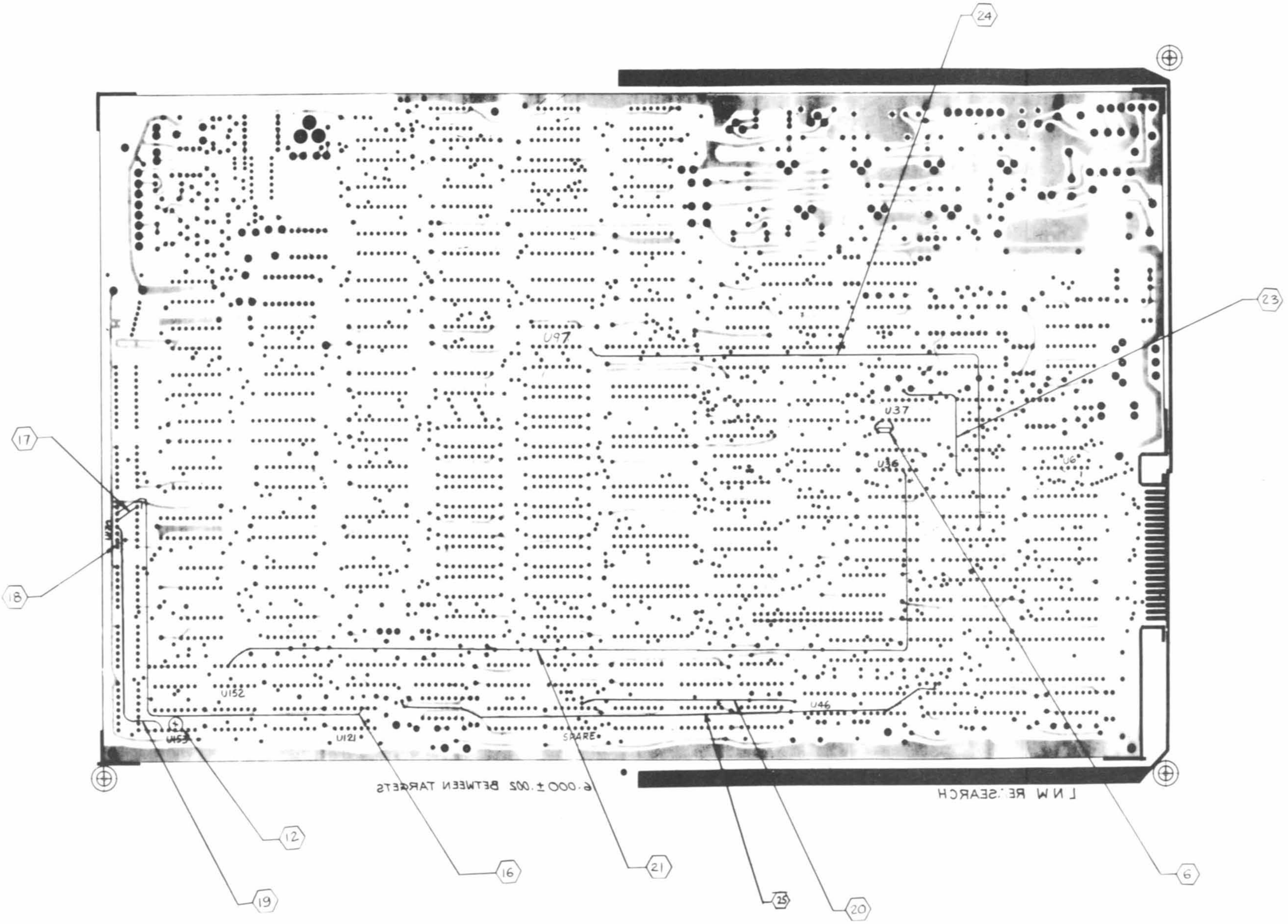
APPROVALS	DATE
PROG. ENG. M Natur	10/20
ENG. MGR.	
MFG. ENG.	
QA MGR.	

NEXT ASSEMBLIES

TITLE LNW80
NO. 97000
A 10/27/81
DFTMN. H. NGUYEN
CHK.
SIZE 2
GR
SH 1/2
PROPERTY OF LNW RESEARCH CORP TUSTIN CA
FORM A

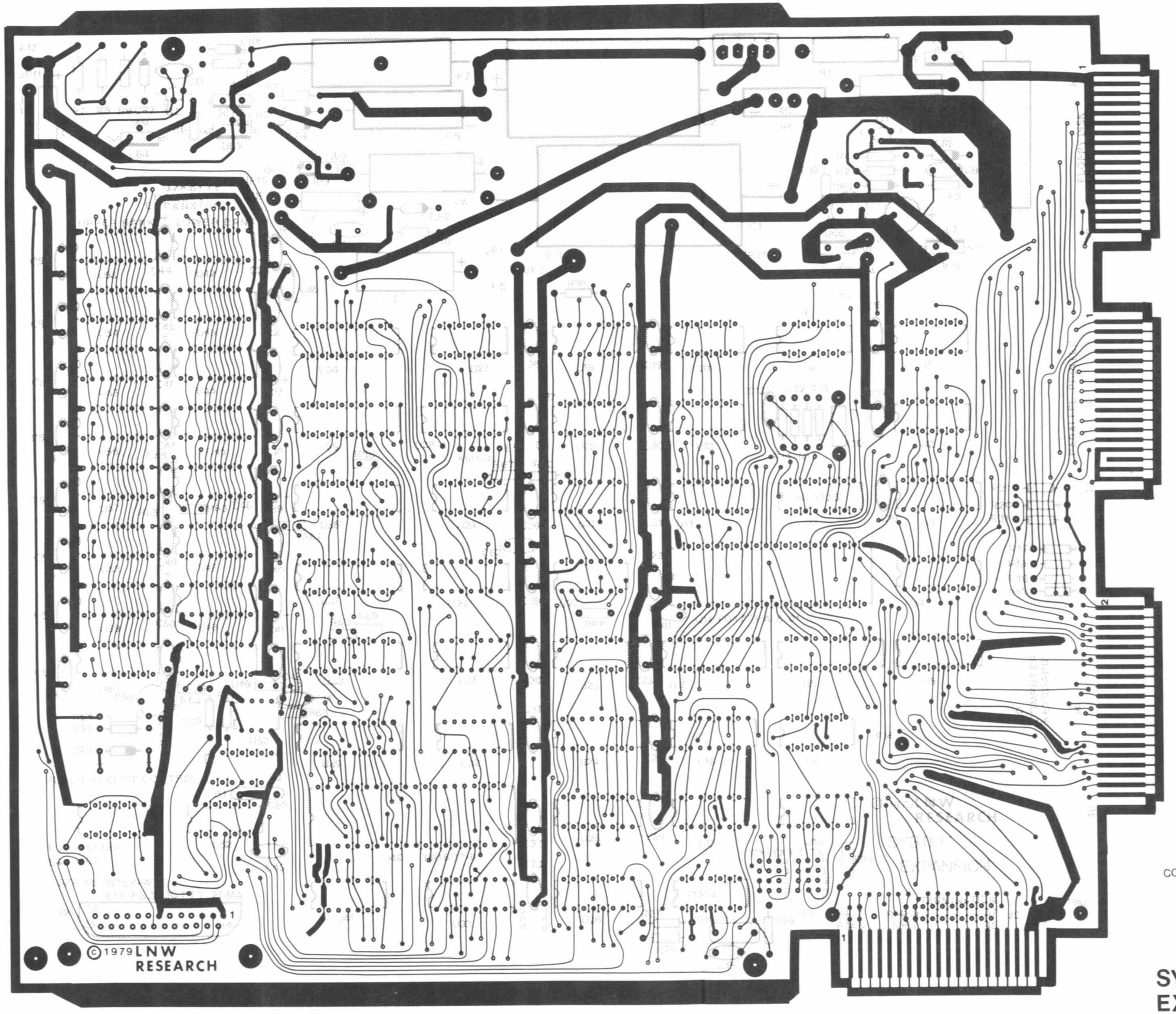
REVISIONS

PART REV.	DOC REV.	DESCRIPTIONS	DATE	APPROVED



NOTES: UNLESS OTHERWISE SPECIFIED

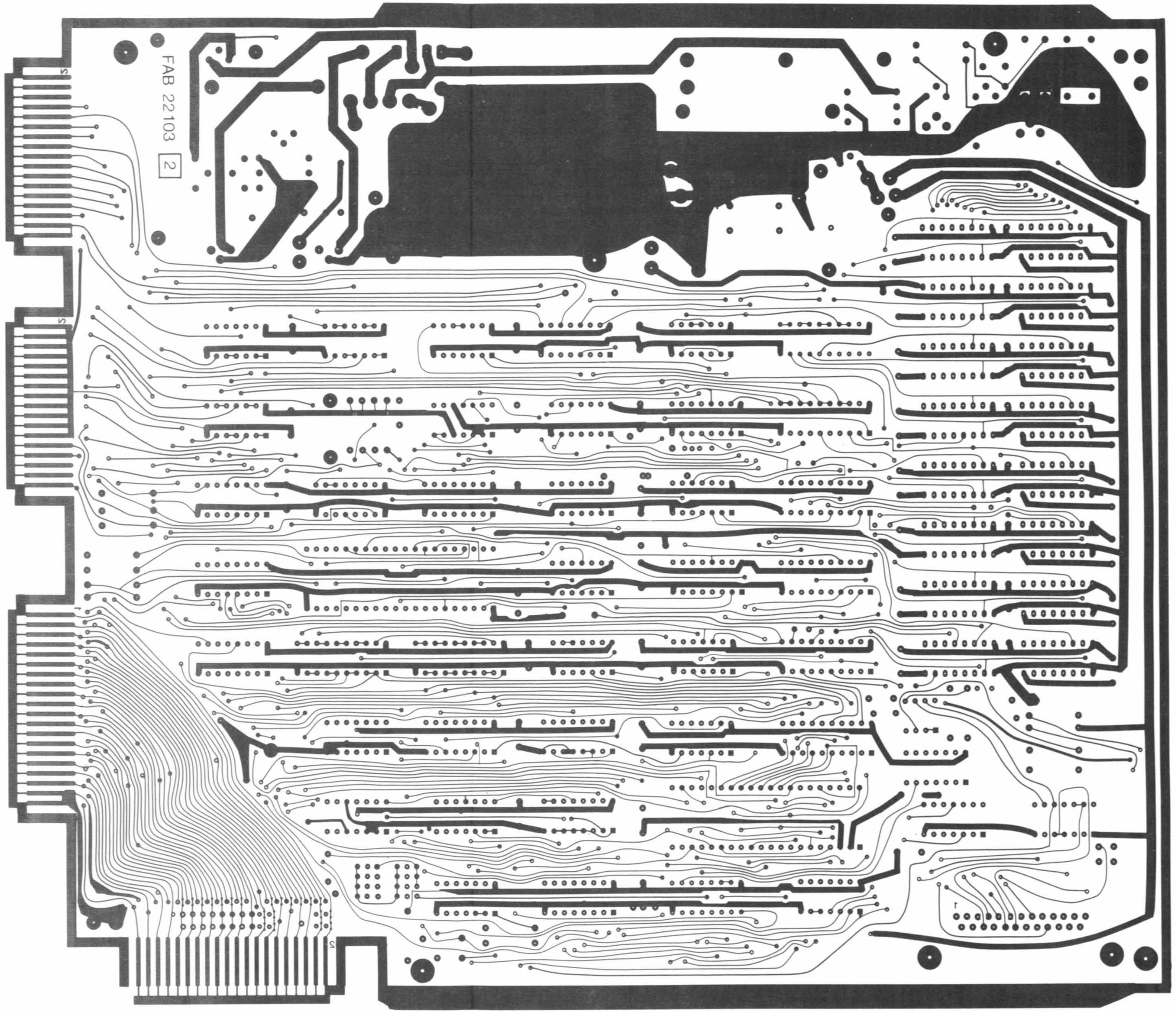
SIZE	NEXT ASSEMBLY	DRAWING NO.	REV
D	LNW80	97000	L
SCALE FULL	DO NOT SCALE DRAWING	SHEET 2 OF 2	



COMPONENT SIDE

SYSTEM
EXPANSION PCB

SYSTEM EXPANSION PCB



SOLDER SIDE

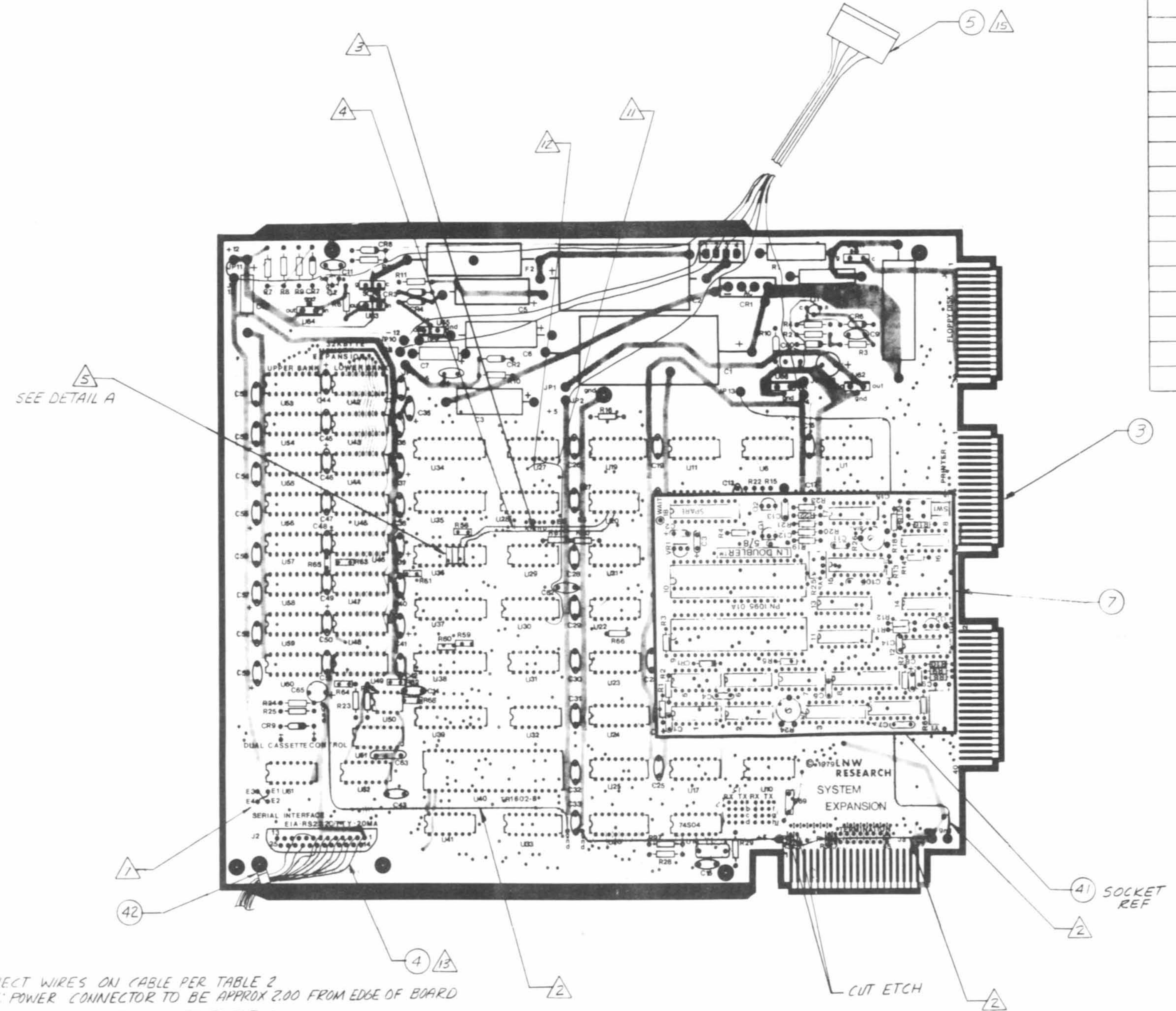
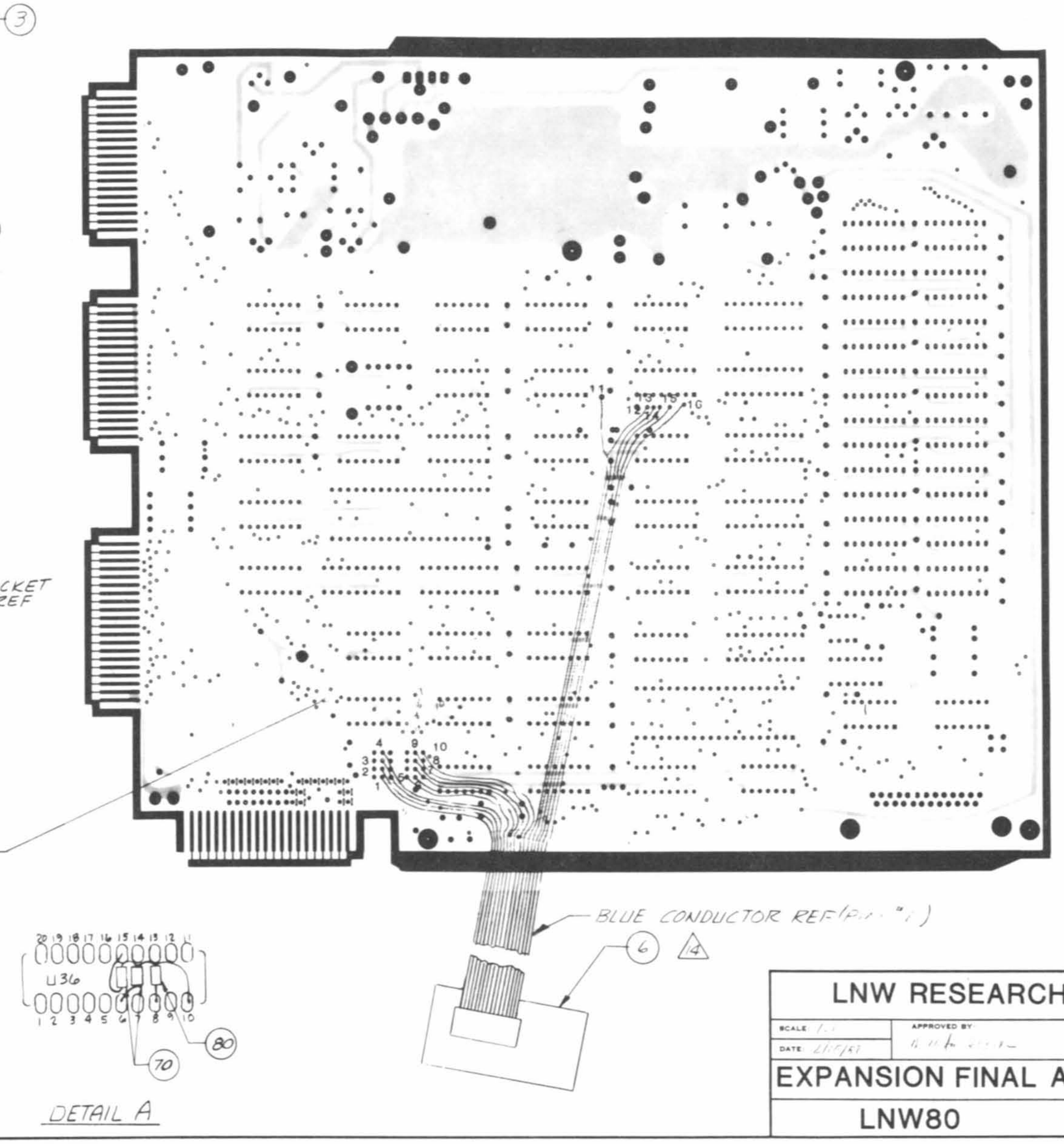


TABLE 1	
FROM RS232 P.C. BD ASSY	TO REAR SIDE OF EXP P.C. BD
1	8
2	9
3	7
4	10
5	11
6	6
7	5
8	12
9	13
10	4
11	14
12	3
13	2
14	15
15	1
16	16

TABLE 2	
FROM POWER CONNECTOR	TO [illegible]
1	J12
2	JP10
3	[illegible]
4	JP12
5	[illegible]
6	[illegible]



DETAIL A

15 CONNECT WIRES ON CABLE PER TABLE 2
NOTE: POWER CONNECTOR TO BE APPROX 2.00 FROM EDGE OF BOARD

14 CONNECT WIRES ON CABLE PER TABLE 1
NOTE: RS232 PCB ASSEMBLY TO BE APPROX 8.00 FROM EDGE OF BOARD

13 SOLDER WIRES PIN TO PIN AND SECURE IN PLACE
NOTE: CONNECTOR TO BE APPROX 12.00 FROM EDGE OF BOARD

12 JUMPER FROM U27 PIN6 TO PAD SHOWN

11 JUMPER FROM U30 PIN 7 TO U27 PIN 5

10

9

8

7 JUMPER FROM E1 TO E4 AND E2 TO E3

6 CUT ETCH BETWEEN J6-32 & J6-34 (FARSIDE)

5 ADD ITEM 78 QTY 2 & ITEM 79 QTY 1

4 JUMPER FROM U36 PIN PIN 14 TO U20 PIN 3

3 JUMPER FROM U36 PIN 13 TO U20 PIN 4

2 ADD JUMPERS FOR GROUND AS SHOWN

1. ASSEMBLE PER LNW RESEARCH WORKMANSHIP STANDARD

LNW RESEARCH CORP.

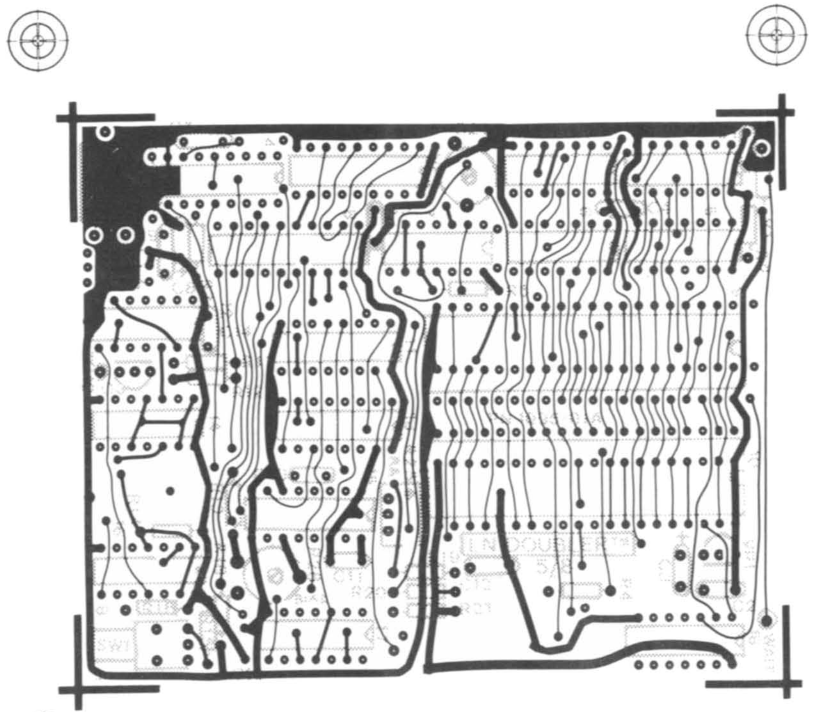
SCALE: [illegible]	APPROVED BY: [illegible]	DRAWN BY: [illegible]
DATE: [illegible]		REVISED

EXPANSION FINAL ASSEMBLY

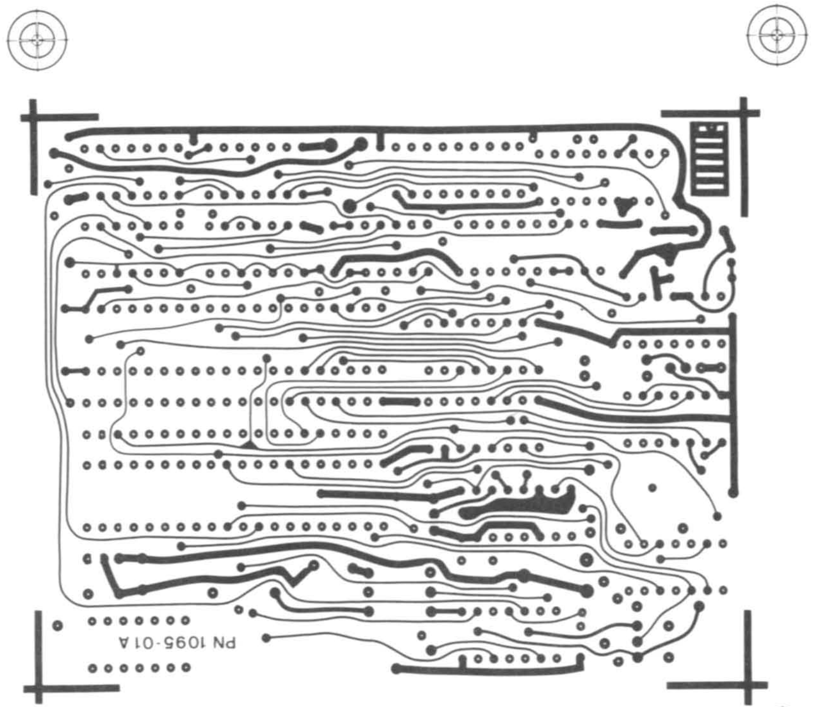
LNW80

DRAWING NUMBER [illegible] B

PRINTED ON NO. 1000H-8 CLEARPRINT FADE-OUT



COMPONENT SIDE



SOLDER SIDE

LNDOUBLER 5/8 PCB

USER'S RESPONSE SHEET

Manual Title: LNW80 TECHNICAL REFERENCE MANUAL

Manual Date: JULY 8, 1982 Date of This Letter: ________

User's Name: ____________________ Telephone: ____________________

Company: ________________________ Office/Dept.: ________________

Street Address: ____

City/State/Zip Code: ____

Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

Location in Manual Comment/Suggestion

FOLD ON TWO LINES (LOCATED ON REVERSE SIDE) STAPLE AND MAIL

FOLD

PLACE
POSTAGE
HERE

LNW RESEARCH CORP.
2620 WALNUT AVE. STE A
TUSTIN, CA. 92680

FOLD

LNW Research Corp.
2620 WALNUT Tustin, CA. 92680
(714) 641-8850 (714) 544-5744

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