APPENDIX

1. Basic Information on Circuitry

1.1 Table of Binary code

	DECIMAL							
A 15	8	3	2	7	6	8	32 K	
A 14	4	1	6	3	8	4	16 K	
A 13	2		8	1	9	2	8 K	1000 ~ F000
A 12	1		4	0	9	6	4 K	
A 11	8		2	0	4	8	2 K	
A 10	4		1	0	2	4	1 K	100 ~ F00
A 9	2			5	1	2		
A 8	1			2	5	6		
A 7	8			1	2	8		
A 6	4				6	4		10 ~ F0
A 5	2				3	2		
A 4	1				1	6		
A 3	8					8		
A 2	4					4		0 ~ F
A 1	2					2		
A 0	1					1		

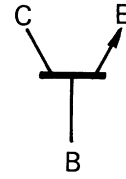| Decimal	HEX	(Bit) Binary	Decimal	HEX	(Bit) Binary	Decimal	HEX	(Bit) binary
0	0	0000	6	6	0110	12	C	1100
1	1	0001	7	7	0111	13	D	1101
2	2	0010	8	8	1000	14	E	1110
3	3	0011	9	9	1001	15	F	1111
4	4	0100	10	A	1010	16	10	10000
5	5	0101	11	B	1011	17	11	10001

1.2 Transistors and Color Code
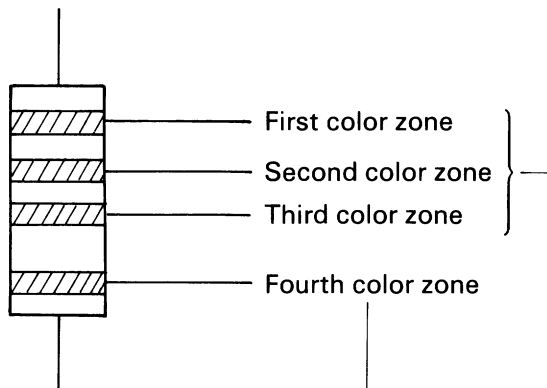
(1) Transistors
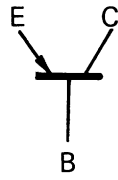
PNP Transistor

Turned on when the base (B) is at low level.

NPN Transistor

Turned on when the base (B) is at high level.

### (2) Color markings of resistors and capacitors

First color zone

Second color zone

Third color zone

Fourth color zone

Color	Error
Gold	±5%
Silver	±10%
Non-colored	±20%

Color	First color zone	Second color zone	Third color zone
Black	0	0	10^0
Brown	1	1	10^1
Red	2	2	10^2
Orange	3	3	10^3
Yellow	4	4	10^4
Green	5	5	10^5
Blue	6	6	10^6
Purple	7	7	10^7
Grey	8	8	10^8
White	9	9	10^9
Gold	–	–	10^{-1}
Silver	–	–	10^{-2}

1.3 Circuit Symbols

(1) AND circuit (H: High level, L: Low level)
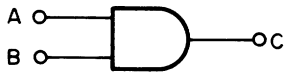
Truth Table

Input		Output
A	B	C
L	L	L
H	L	L
L	H	L
H	H	H
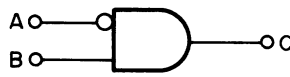
Truth Table

Input		Output
A	B	C
L	L	L
H	L	L
L	H	H
H	H	L

Truth Table

Input		Output
A	B	C
L	L	H
H	L	L
L	H	H
H	H	H

(Concept of AND Circuit)
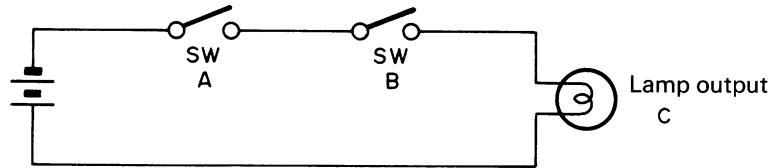
(2) OR circuit
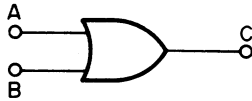
Truth Table

Input		Output
A	B	C
L	L	L
H	L	H
L	H	H
H	H	H
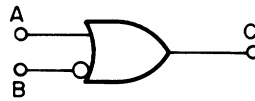
Truth Table

Input		Output
A	B	C
L	L	H
H	L	H
L	H	L
H	H	H
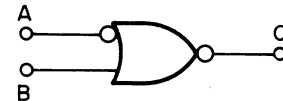
Truth Table

Input		Output
A	B	C
L	L	H
H	L	L
L	H	H
H	H	H

(Concept of OR Circuit)
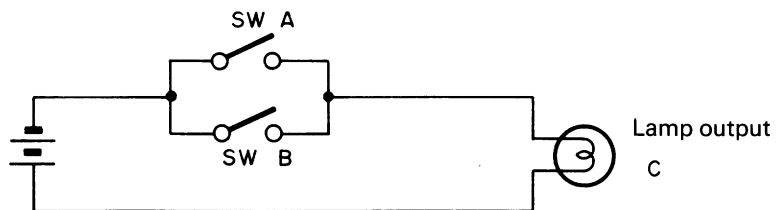
(3) Logics of AND circuit and OR circuit
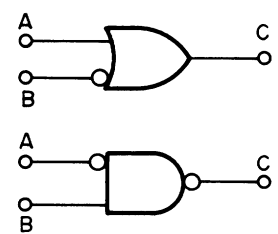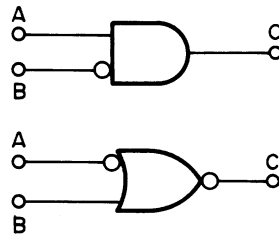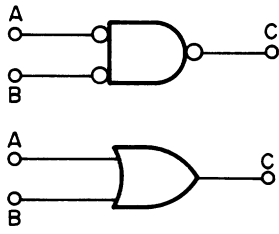
Truth Table

Input		Output
A	B	C
L	L	L
H	L	H
L	H	H
H	H	H

Truth Table

Input		Output
A	B	C
L	L	L
H	L	H
L	H	L
H	H	L

Truth Table

Input		Output
A	B	C
L	L	H
H	L	H
L	H	L
H	H	H

(4) Inverter circuit
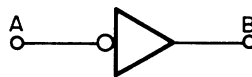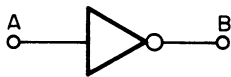
Input	Output
A	B
L	H
H	L

Input	Output
A	B
L	H
H	L

Input	Output
A	B
L	L
H	H

Note: The circle in the symbol indicates the open collector type.

(5) Flip-flop

A PRESET
B CLEAR
C CLOCK
D DATA
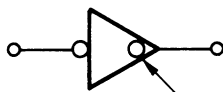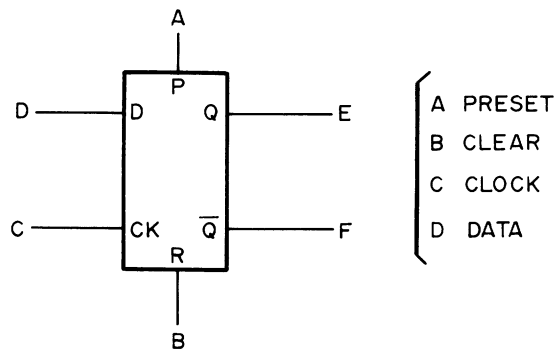
Truth Table

	Input				Output	
	A	B	C	D	Q	$\overline{Q}$
1	L	H	×	×	H	L
2	H	L	×	×	L	H
3	L	L	×	×	H*	H*
4	H	H	L→H	H	H	L
5	H	H	L→H	L	L	H
6	H	H	L	H	H	L
7	H	H	L	L	L	H

* Temporary state

(6) Decoder
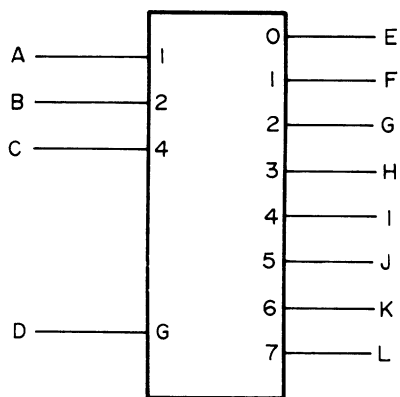
	Input				Output							
	A	B	C	D	E	F	G	H	I	J	K	L
1	−	−	−	L	L	L	L	L	L	L	L	L
2	L	L	L	H	H	L	L	L	L	L	L	L
3	H	L	L	H	L	H	L	L	L	L	L	L
4	L	H	L	H	L	L	H	L	L	L	L	L
5	H	H	L	H	L	L	L	H	L	L	L	L
6	L	L	H	H	L	L	L	L	H	L	L	L
7	H	L	H	H	L	L	L	L	L	H	L	L
8	L	H	H	H	L	L	L	L	L	L	H	L
9	H	H	H	H	L	L	L	L	L	L	L	H

2. IC

2.1 Table of Main ICs

Name	Part Code	Type	Location of Use
6301	X40006310	CPU (Main CPU)	8G
6301 (MASK)	Y201800301	CPU (Slave CPU)	6D
M16010C'	X400004491	RAM (2K byte)	13C ~ 16C, 12G ~ 15G
MB3761	X440167610	OP AMP	2B
TL497	X440034970	Switching voltage regulator	3A
TD62504	X440045040	Driver (Transistor array)	7E
HD75188	X440751880	Line driver (for RS-232C)	6B
HD75189	X440751890	Line receiver (for RS-232C)	7B
TC4016BP	X460401600	Two-way switch	2F, 4D
TC4049BP	X460404900	Converter	2C, 7C, 11H
TC4068BP	X460406800	8-input NAND	1G
TC4093BP	X460409300	2-input NAND	6C
TC4011UBP	X460401101	2-input NAND	5F
TC4049UBP	X460404902	Converter	7C, 8D
TC40H000	X460400004	2-input NAND	1E, 5D, 8E
TC40H002	X460400204	2-input NOR	1F, 3E, 4F
TC40H004	X460400404	HEX INVERTER	3F, 4E, 5E, 11G
TC40H010	X460401004	3-input NAND	2E
TC40H074	X460407404	Flip-flop	10H
TC40H138	X460413804	Decoder	9E, 15D, 16D, 16G
TC40H166	X460416604	Shift register	10G
TC40H273	X460427304	Flip-flop	5G, 9G
TC40H367	X460436704	3-input buffer	3G, 4G
TC40H373	X460437304	Latch	16E
TD6303F	X440043030	Motor control	Microcassette IC1

2.2 ICs

(1) 6301
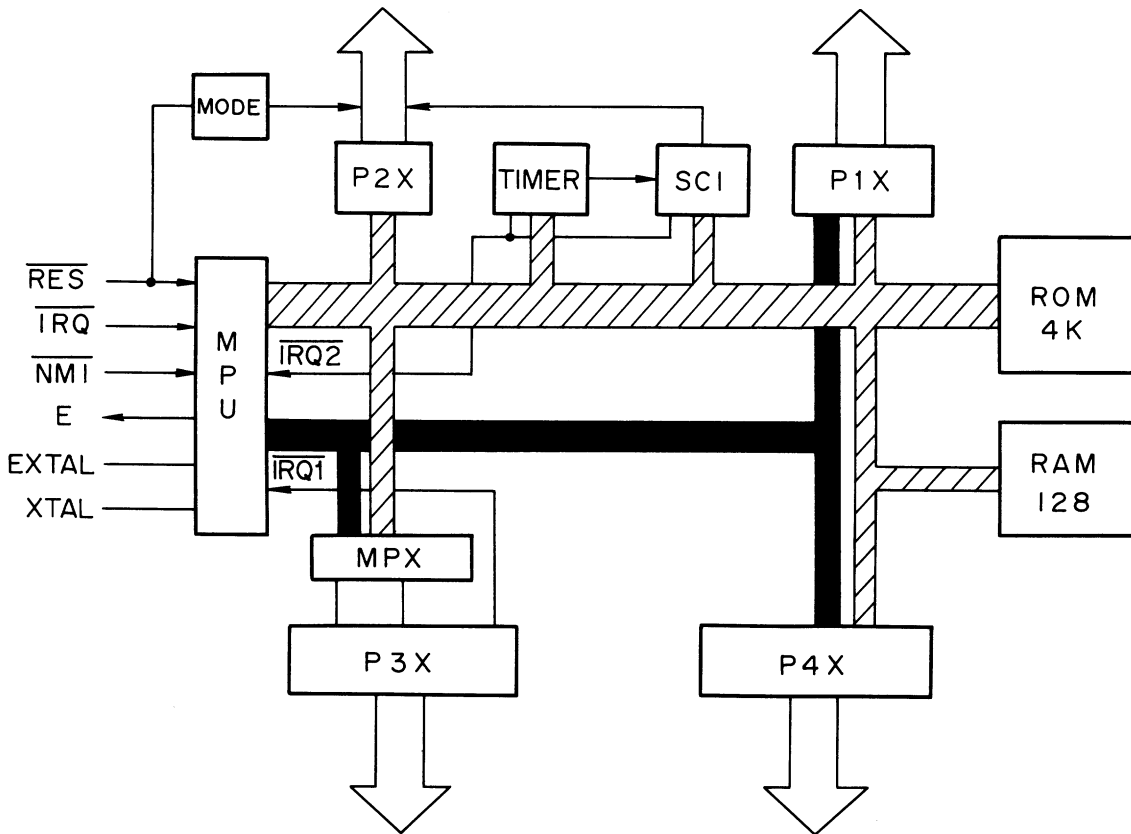
The HX-20 employs a 2.4576 MHz crystal oscillator, whose output frequency is divided into one quarter by an internal circuit, i.e., 614.4 kHz (about every 1.63 μsec.), which drives the HX-20.

The main CPU operates in the expanded multiplex mode, while the slave CPU operates in the single chip mode. Thus, the ports are used as shown below.

Port	Main CPU	Slave CPU
Port 1	Parallel I/O terminal	I/O terminal
Port 2	Serial I/O terminal	I/O terminal
Port 3	Address/data terminal	I/O terminal
Port 4	Address terminal	I/O terminal

Main CPU 6301 (8G)

Pin No.	Port	Direction	Meaning	
1	G	————	GND	
2	X TAL	In	Oscillator input 2.4576 MHz	
3	EX TAL	In	Oscillator input 2.4576 MHz	
4	NMI	In	Non-mask interrupt	Low: Interrupt
5	IRQ	In	I/O request	Low: On
6	RS	In	Reset signal	
7	S.T.B.	–	Unused	
8	20	In	Bar code reader data line	
9	21	Out	RS232C TX (transmitting data)	
10	22	Out	Serial select	Low: Peripheral High: Slave 63d
11	23	In	Slave 6301 serial (RX)	
12	24	Out	Slave 6301 serial (TX)	
13	10	In	Data set ready (DSR)	Low: On
14	11	In	Clear to send (CTS)	Low: On
15	12	Out	Slave CPU R/W control	
16	13	In	External port interrupt	Low: Interrupt
17	14	In	Power abnormal (PWA) (IRQ1)	Low: Interrupt
18	15	In	Keyboard interrupt (IRQ1)	Low: Interrupt
19	16	In	Peripheral status (Serial option)	Low: On
20	17	In	Cartridge option flag	Low: ROM High: μCASSETTE

Main CPU 6301 (8G)

Pin No.	Port	Direction	Meaning
21	Vcc		+5V
22	A15	Out	Address bus
23	A14	Out	
24	A13	Out	
25	A12	Out	
26	A11	Out	
27	A10	Out	
28	A9	Out	
29	A8	Out	
30	DA7	In/Out	Data address bus
31	DA6	In/Out	
32	DA5	In/Out	
33	DA4	In/Out	
34	DA3	In/Out	
35	DA2	In/Out	
36	DA1	In/Out	
37	DA0	In/Out	
38	R/$\overline{\text{W}}$	Out	Read/write
39	AS	Out	Address strobe
40	E	Out	ENABLE

Slave CPU 6301 (6D)

Pin No.	Port	Direction	Meaning		
1	G	–	GND		
2	X TAL	In	Oscillator input 2.4576 (MHz)		
3	EX TAL	In	Oscillator input 2.4576 (MHz)		
4	NM1	In	Non-mask interrupt		Low: ON
5	IRQ	–	Unused		
6	R̄	In	Request signal		
7	STB	–	Unused		
8	20	In	RS-232C (RX) receiving data	Microcassette	LOW: READ DATA HIGH: WRITE ENABLE
9	21	Out	Microcassette internal clock	Write data	
10	22	In	Serial select		LOW: BRAKE HIGH: NORMAL
11	23	In	Serial data (RX)		
12	24	Out	Serial data (TX)		
13	10	Out	Printer head 1		LOW: OFF HIGH: ON
14	11	Out	Printer head 2		
15	12	Out	Printer head 3		
16	13	Out	Printer head 4		↓
17	14	Out	Printer Motor		LOW: ON HIGH: OFF
18	15	Out	Speaker		LOW: OFF HIGH: ON
19	16	In	Printer reset pulse		
20	17	In	Printer timing pulse		

Slave CPU 6301 (6D)

| Pin No.	Port	Direction	Meaning		
21	Vcc	–	+5V		
22	47	In	Carrier detect		Low: Carrier detected High: Not detected
23	46	Out	Rom cartridge select	Microcassette clock Low: Counter High: Head switch	
24	45	Out	Cassette/RS-232C select		Low: RS232-C High: Microcassette
25	44	Out	ROM address counter clear		Clock
26	43	Out	ROM cartridge power switch Low: Off High: On		Microcassette command
27	42		Clear shift register	Microcassette power switch Low: Off High: On	
28	41	Out	Port enable always on	Printer motor control Low: Open High: Brake	
29	40	In	PLUG 2		
30	37	Out	Program power on/off		LOW: Off High: On
31	36	Out	RS-232 power on		Low: Off High: On
32	35	Out	Bar code on/off		Low: On High: Off
33	34	Out	Slave status flag		
34	33	Out	External cassette write data		
35	32	In	External cassette read data		
36	31	Out	Request to send (RTS)		
37	30	Out	External cassette remote on/off		Low: On High: Off
38	–	–	Unused		
39	SC1	–	Unused		
40	–	–	Unused		

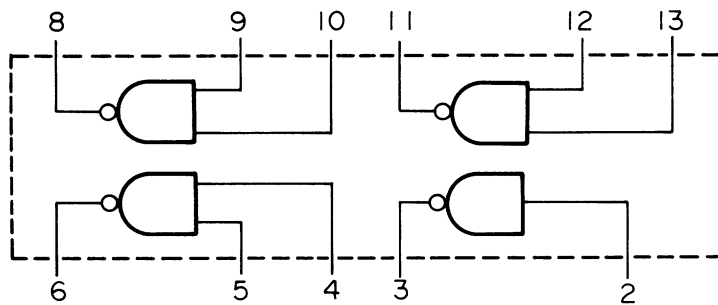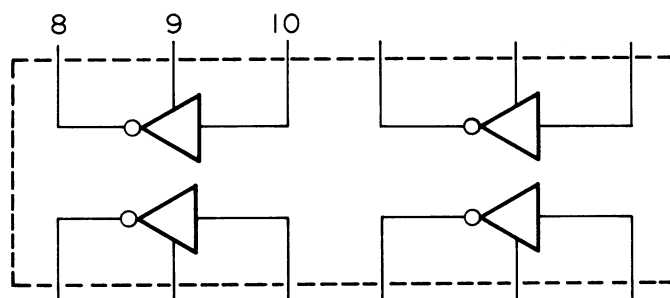## (2) MB 3761
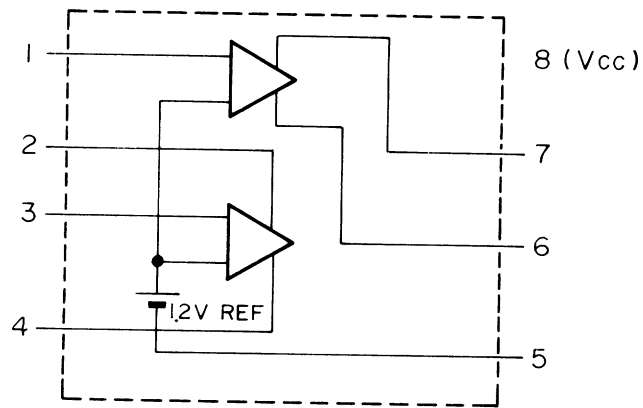
(3) TL 497
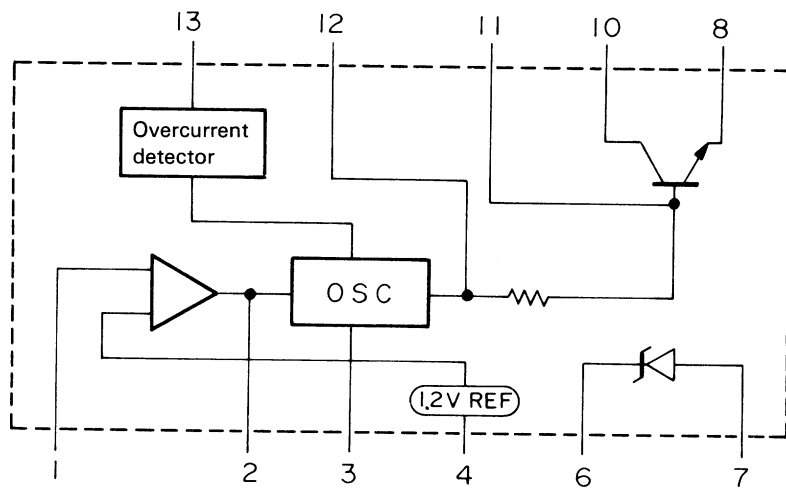
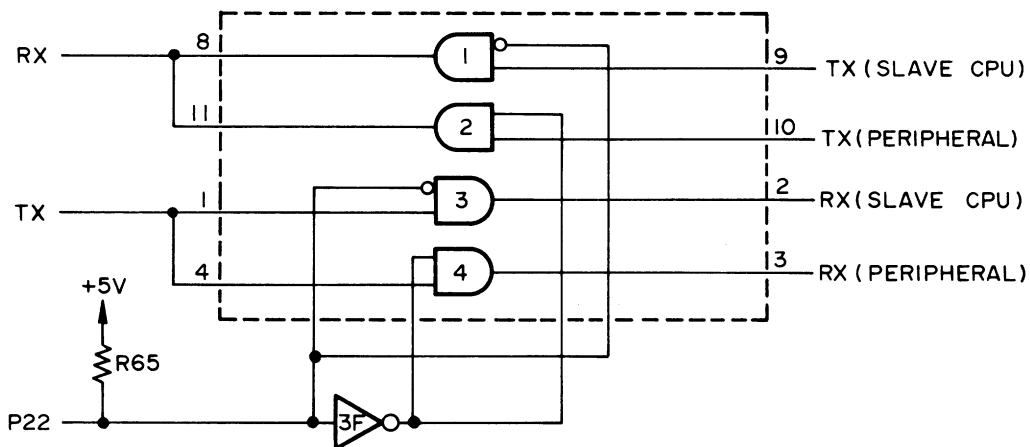## (4) TD 62504
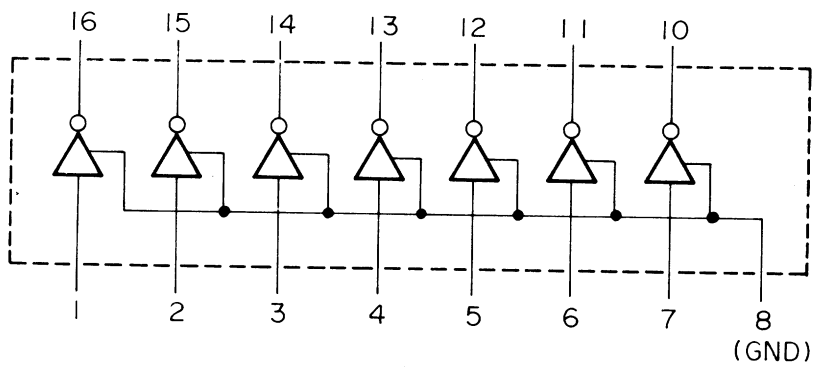
(Pin 9: Not used)

(5) 75188
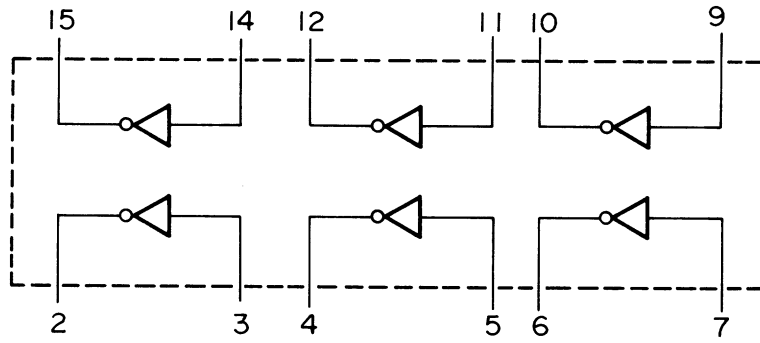

(Pin 1: Vcc, 7: GND)

(6) 75189

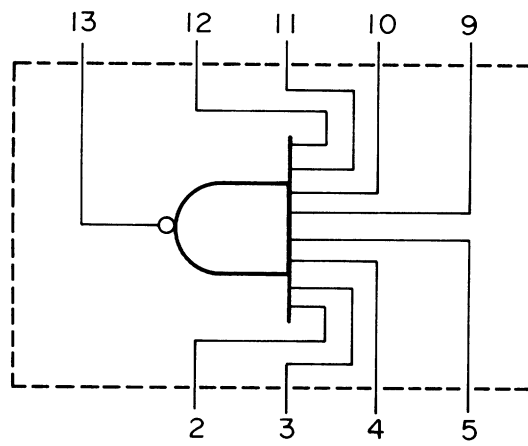
(Pin 7: GND, 14: Vcc)
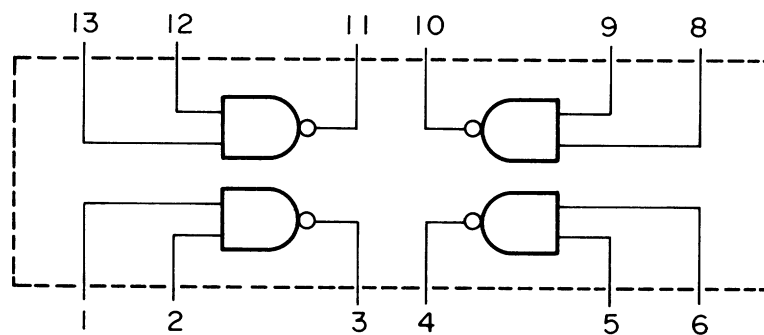
(7) TC 4016

(8) 4049

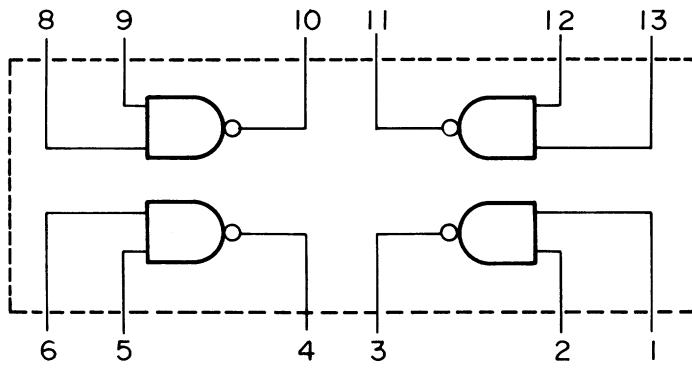(Pin 8: GND, 1 : Vcc, 13/16 Unused)

(9) 4068

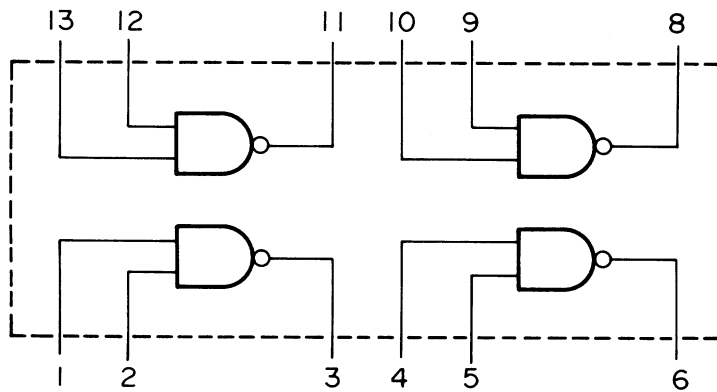(Pin 7: GND, 14: Vcc, 1/6/8: Unused)
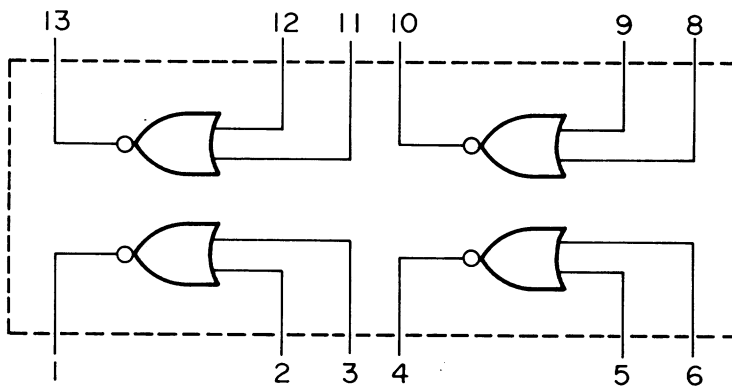
(10) 4093

(11) TC 4011BP

(Pin 7: Vss, 14: V_{DD})

(12) 40H000P

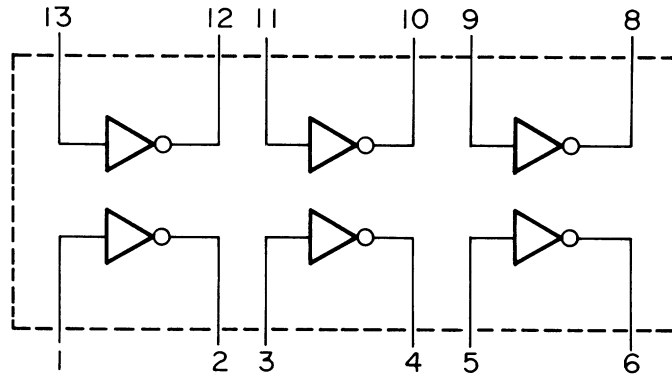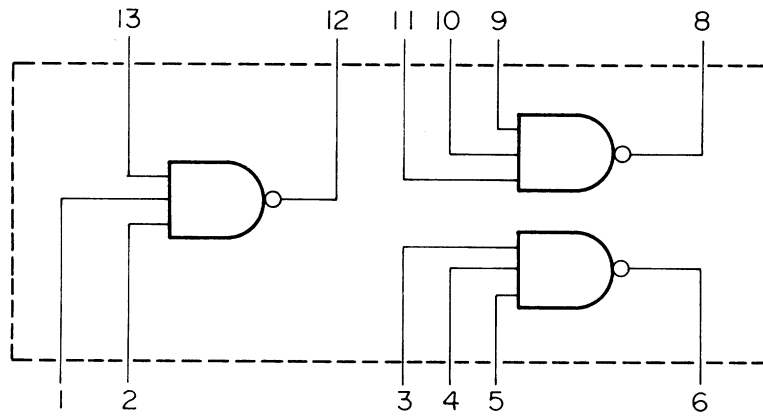(Pin 7: GND, 14: V_{DD})

(13) 40H002P

(Pin 7: GND, 14: V_{DD})

(14) 40H004P

(Pin 7: GND, 14: V_{DD})

(15) 40H010P

(Pin 7: GND, 14 : V_{DD})

(16) 40H074P
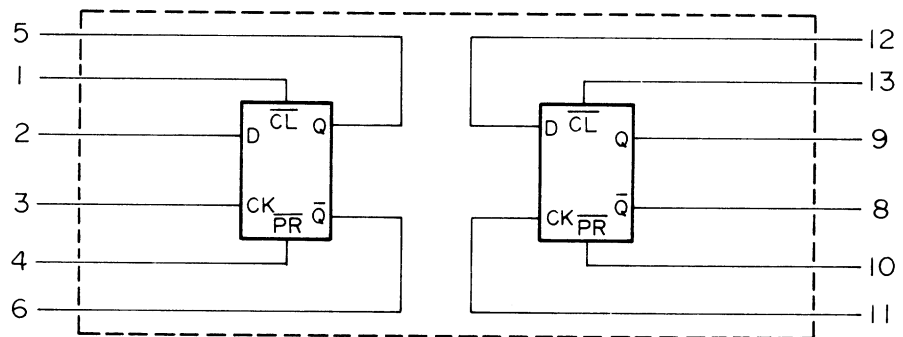
(D MODE) . . . . $\overline{CL}$ and $\overline{PR}$ at high level
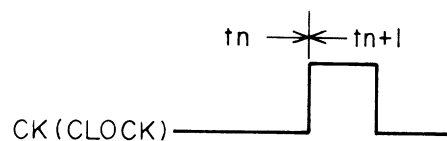
t_n	t_{n+1}	Output
D	$\overline{Q}$	Q
H	L	H
L	H	L
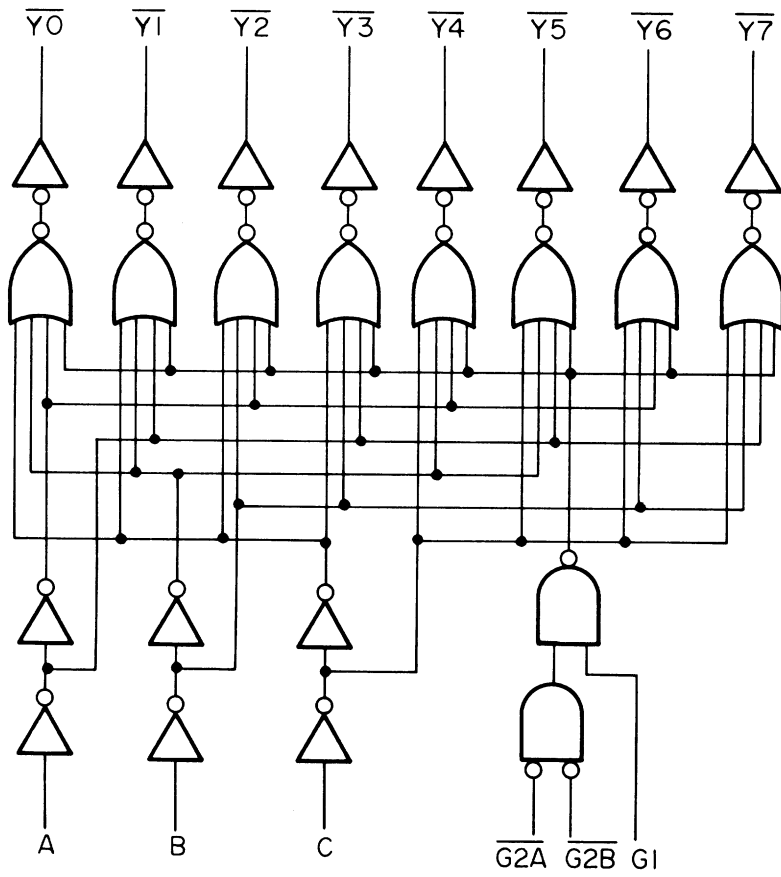
Input						Output							
Gate													
G I	$\overline{G2A}$	$\overline{G2B}$	A	B	C	Y0	Y I	Y 2	Y 3	Y 4	Y 5	Y 6	Y 7
L	—	—	—	—	—	H	H	H	H	H	H	H	H
—	H	—	—	—	—	H	H	H	H	H	H	H	H
—	—	H	—	—	—	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

(18) 40H166

SERIAL INPUT (1)

SHIFT / LOAD (15)

PARALLEL INPUT A (2)

$\overline{Q}A$

PARALLEL INPUT B (3)

$\overline{Q}B$

PARALLEL INPUT C (4)

$\overline{Q}C$

PARALLEL INPUT D (5)

$\overline{Q}D$

PARALLEL INPUT E (10)

$\overline{Q}E$

PARALLEL INPUT F (11)

$\overline{Q}F$

PARALLEL INPUT G (12)

$\overline{Q}G$

PARALLEL INPUT H (14)

CLOCK (7)

CLOCK INHIBIT (6)

$\overline{CLEAR}$ (9)

(13) OUTPUT QH
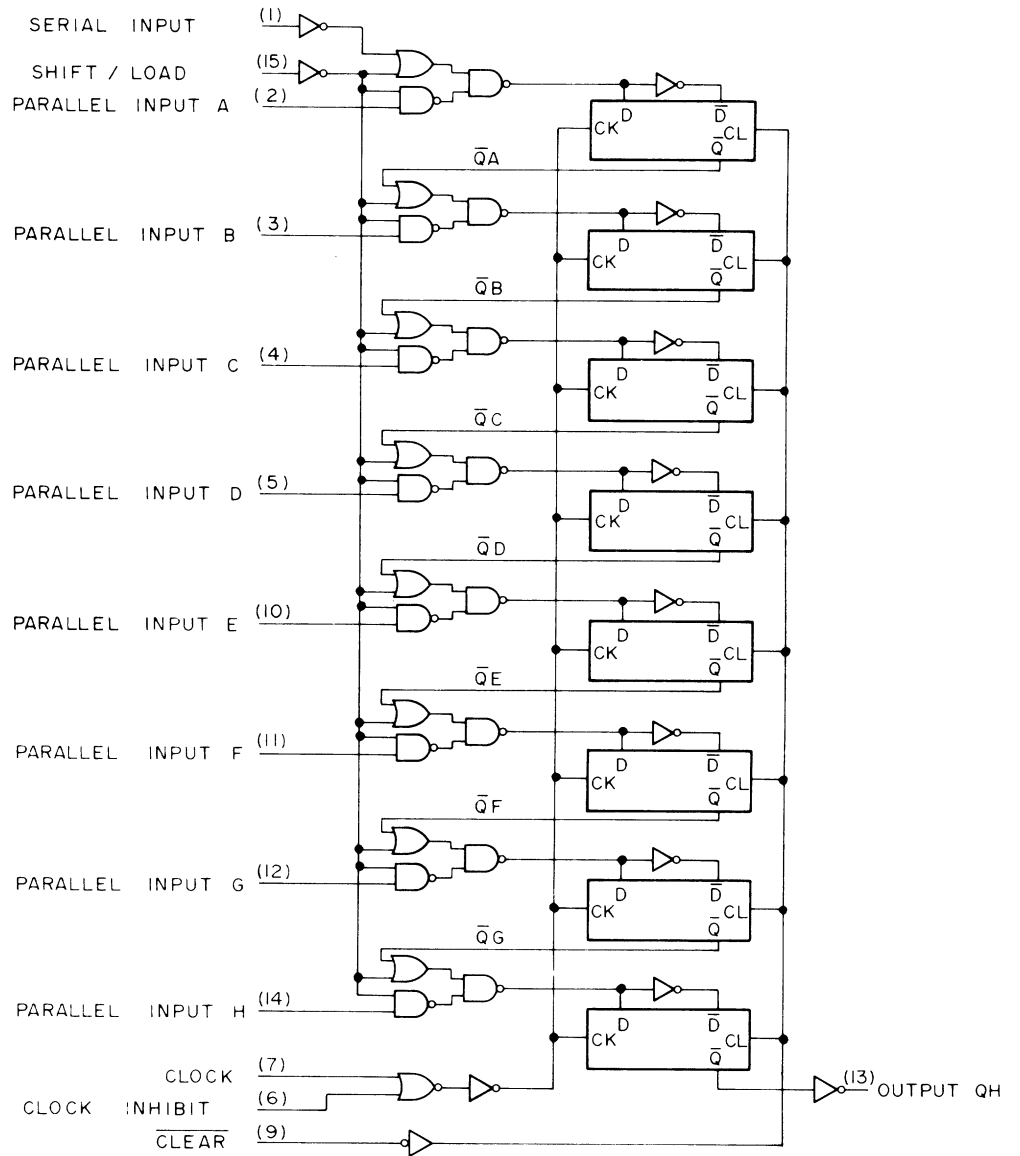
INPUTS							OUTPUTS			FUNCTION
$\overline{CLEAR}$	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL INPUT	PARALLEL INPUT		INTERNAL		Q H	MODE
					A	H	Q A	Q B		
L	※	※	※	※	※	※	L	L	L	Clear
H	H	L	↑	L	※	※	L	Q_{An}	Q_{Gn}	Shift
H	H	L	↑	H	※	※	H	Q_{An}	Q_{Gn}	
H	L	L	↑	※	L	L	L	P_{INB}	L	
H	L	L	↑	※	L	H	L	P_{INB}	H	Parallel
H	L	L	↑	※	H	L	H	P_{INB}	L	Load
H	L	L	↑	※	H	H	H	P_{INB}	H	
H	※	H	※	※	※	※	Q_{AO}	Q_{BO}	Q_{HO}	Hold
H	※	※	↓	※	※	※	Q_{AO}	Q_{BO}	Q_{HO}	No change

(19) 40H166
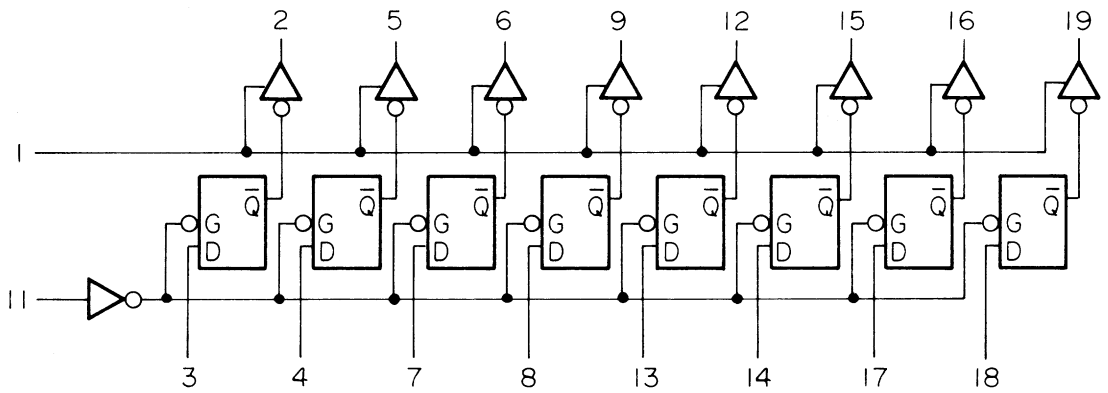

H273

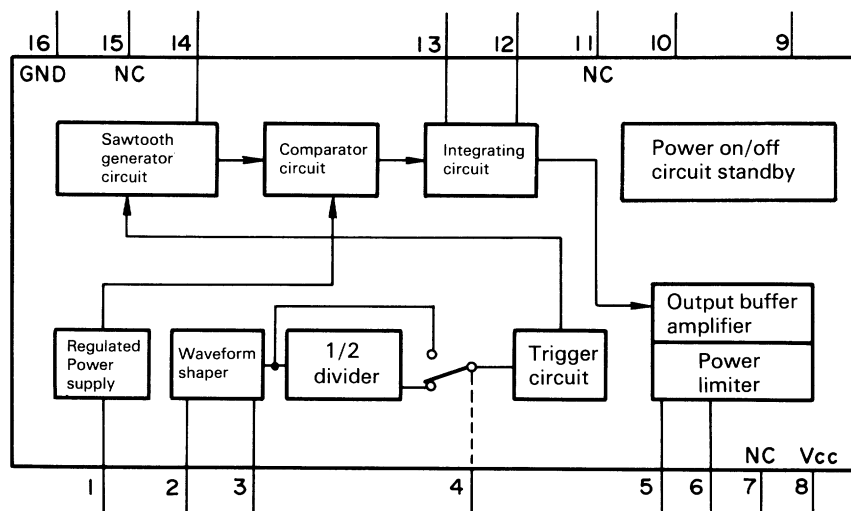(Pin 10: V$_{SS}$, 20: V$_{DD}$)
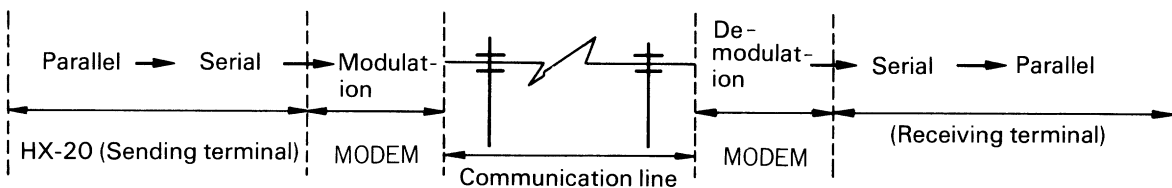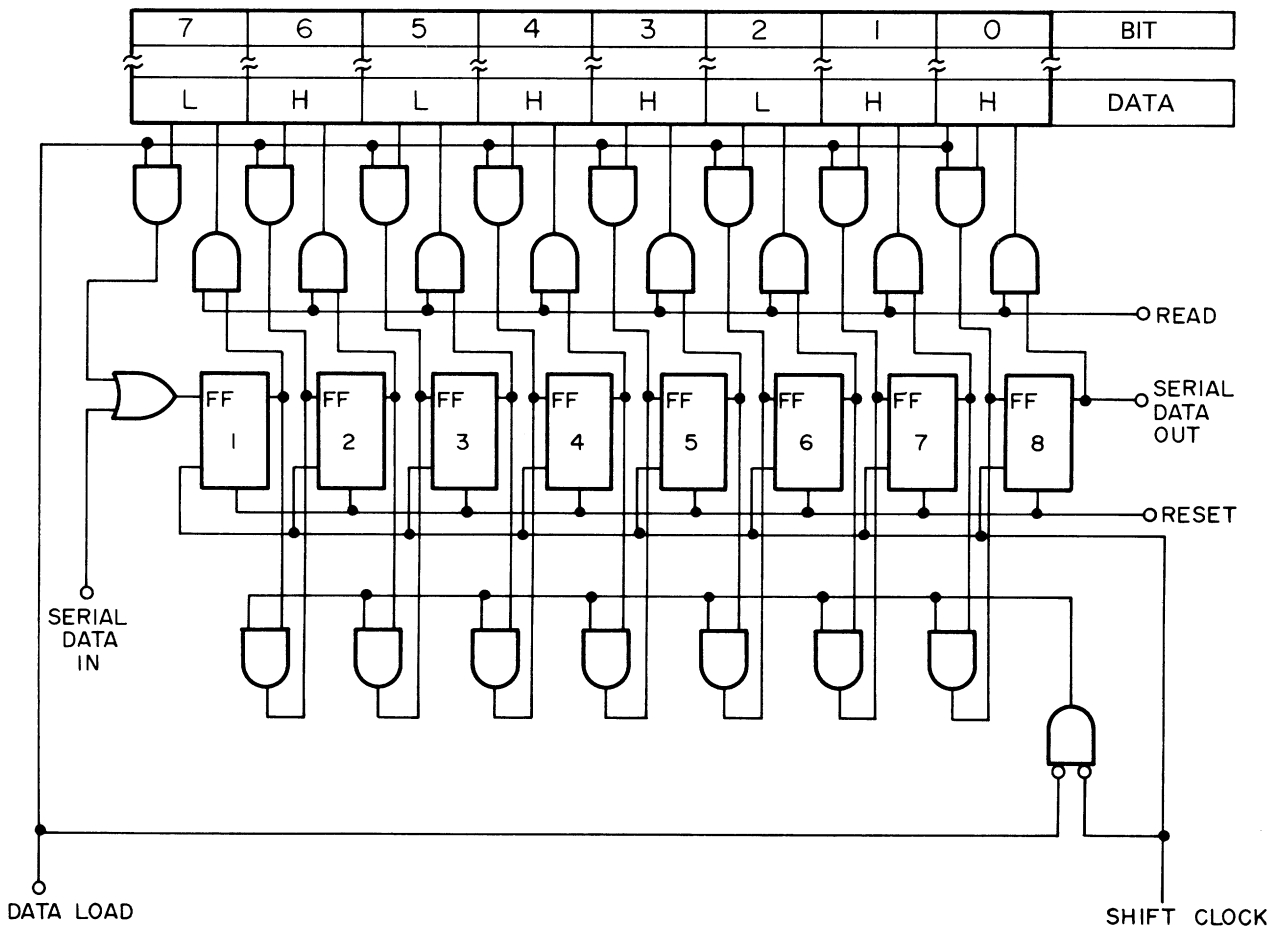
(20) 40H367

(Pin 8: GND, 16: V$_{DD}$)

H373

(Pin 10: V$_{SS}$, 20: V$_{DD}$)

(21) TD6303F

3. Serial – Parallel Conversion

The HX-20 converts data program-wise. The concept of serial ↔ parallel conversion using the hardware shown below is explained.

7	6	5	4	3	2	1	O	BIT
L	H	L	H	H	L	H	H	DATA

Parallel ⟶ Serial ⟶ Modulation → Communication line ← De-modulation → Serial ⟶ Parallel

HX-20 (Sending terminal) | MODEM | Communication line | MODEM | (Receiving terminal)

Data conversion from serial to parallel and vice versa is necessary for reducing the number of communication lines in data transfer.

Serial-parallel conversion performed by the above circuit is briefly explained on the next page. page.

## 3.1   Parallel to Serial Conversion (Add start and stop bits.)

After the flip-flop circuit is reset by a reset signal, parallel data is read into FF '1' to FF '8' by a data load signal.

Then, the data is shifted bit by bit at the timing of NOT DATA LOAD and SHIFT CLOCK, and these bits are output to SERIAL DATA OUT. In performing this operation, it is necessary to add a start bit and a stop bit to the data.

3.2   Serial to Parallel Conversion

After resetting the flip-flop with a reset signal, the serial data bits coming from SERIAL DATA IN are set into FF '1', and are shifted bit by bit at the SHIFT CLOCK timing.

After shifting 1 byte of data bits, the bits are read out to the parallel data line by a read signal. In this conversion operation, the start bit and stop bit are separated from the data.
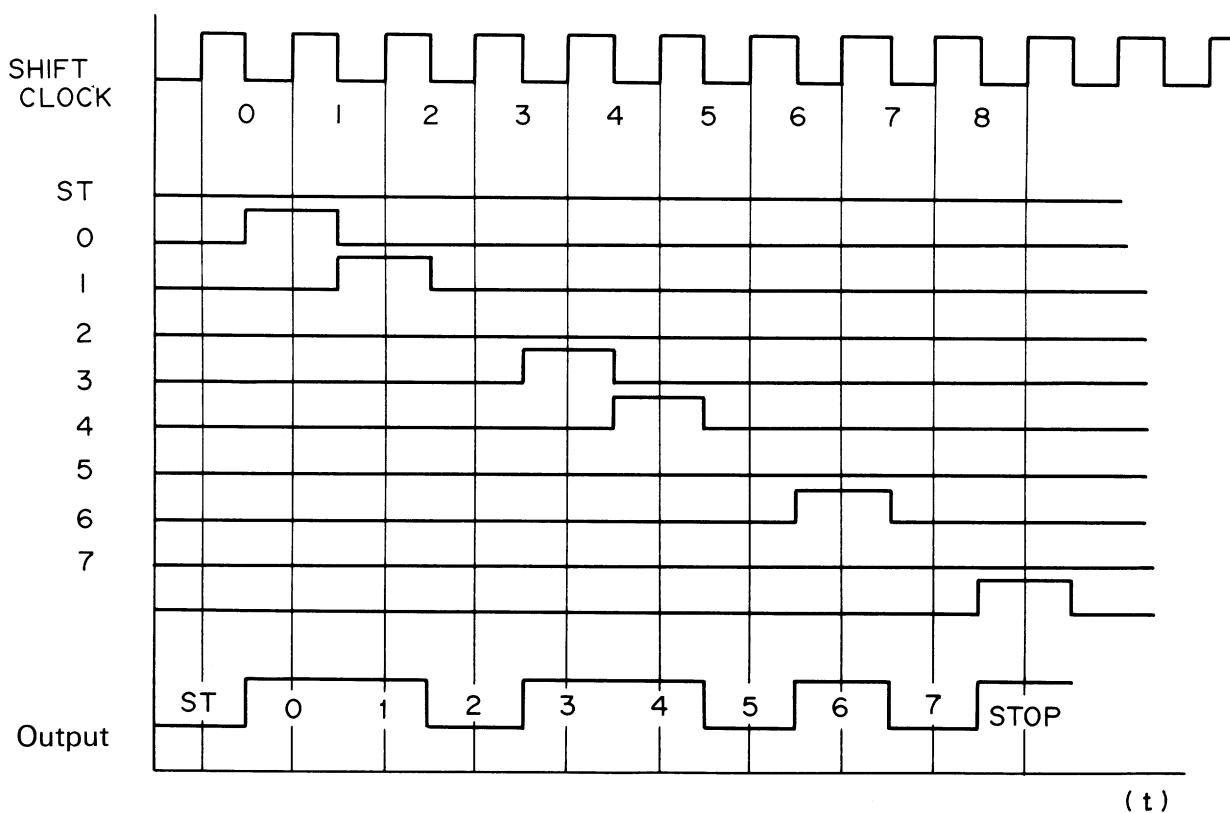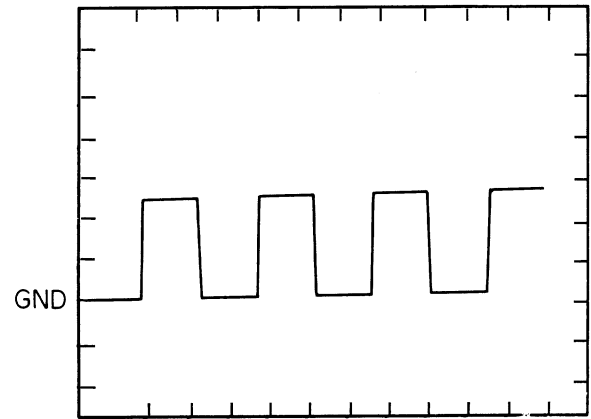

(Serial conversion)

4. Main Circuit Signals

4.1 Enable Signal (E)

POINT   IC 8G PIN 40

VOLTAGE   2.0V DC/DIV

SWEEP   0.5 μsec.

A system clock with a period of 1.6 μsec

*A pulse waveform is always output if power is on.

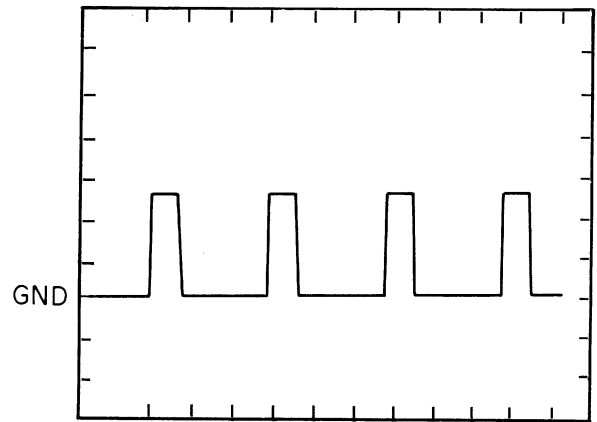## 4.2 Address Strobe Signal (AS)

POINT IC   8G PIN39

VOLTAGE   2.0V DC/DIV

SWEEP   0.5 μsec.

This signal is output every 1.6 μsec.

*A pulse waveform is always output if power is on.

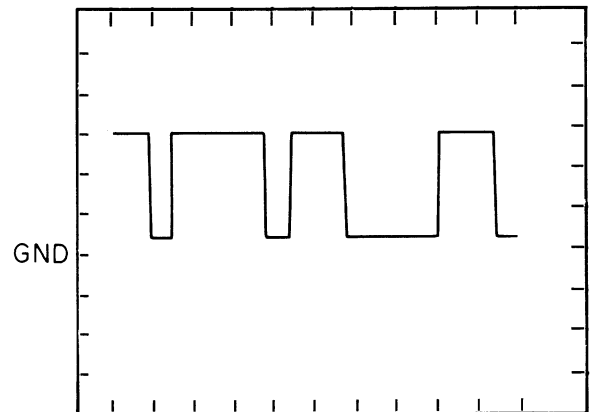## 4.3 Address/Data Bus Signal

POINT   IC 8G PIN37

VOLTAGE   2.0V DC/DIV

SWEEP   1.0 μsec.

Address/data buses are not constant depending on the program command and data being executed.

* Normally high level

4.4 LCD Chip Select Signal (CS)

POINT   IC 16G PIN 14

VOLTAGE   2.0V DC/DIV

SWEEP   2.0 μsec
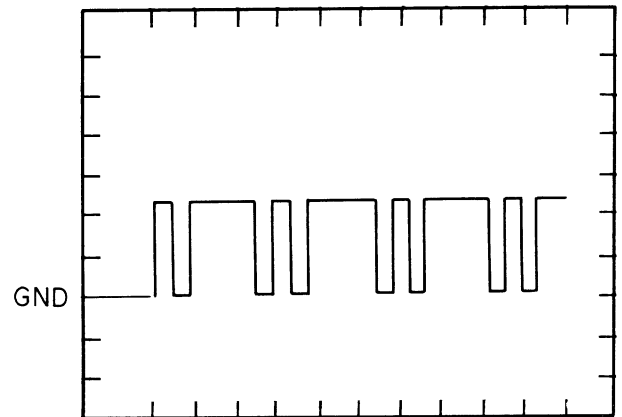
*Normally high level
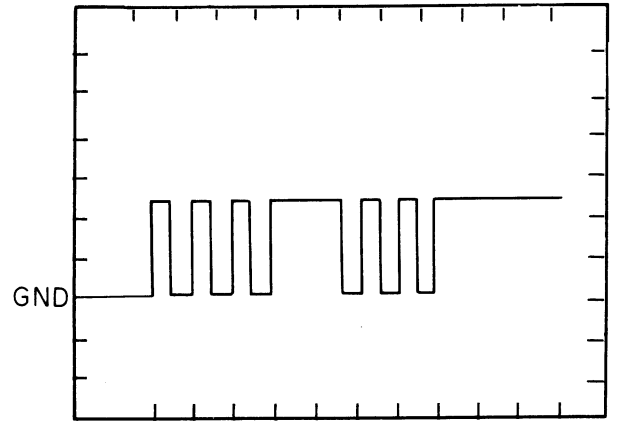
4.5 LCD Shift Clock Signal (SCK)

POINT   IC 11H PIN2

VOLTAGE   2.0V DC/DIV

SWEEP   2.0 μsec.

*Normally high level

4.6 Clock Pulse for Clock

POINT   IC 6G PIN2

VOLTAGE   2.0V DC/DIV

SWEEP   10 μsec.

*Normally a pulse waveform
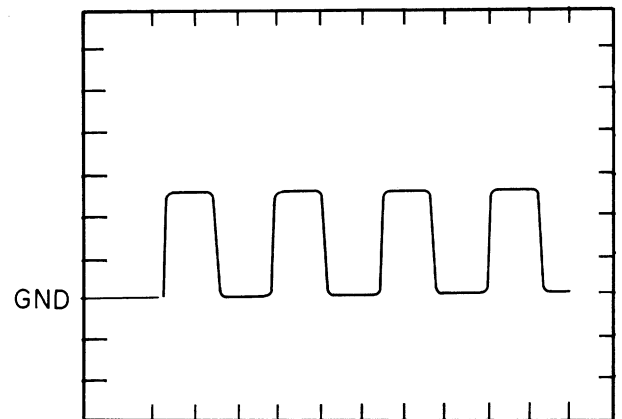
4.7 KSC Signal

POINT   IC 5G PIN5
VOLTAGE   2.0V DC/DIV
SWEEP   0.2 msec

   * Normally low level

4.8 Key Input Control Signal

POINT   IC 6C PIN13
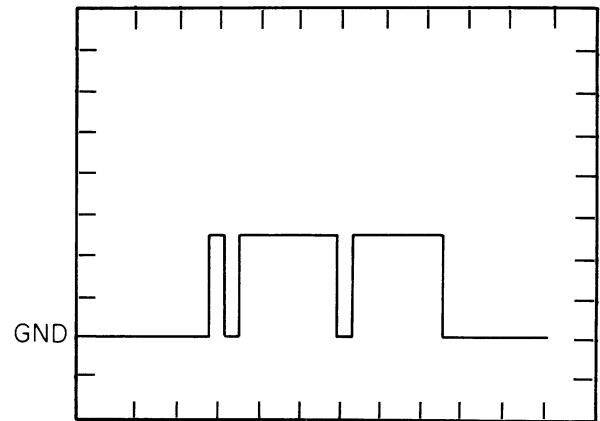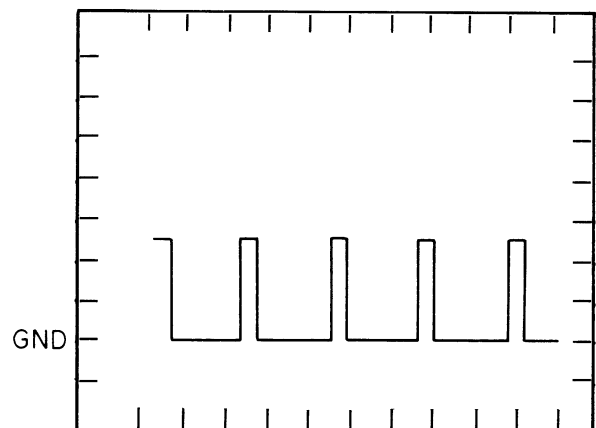VOLTAGE   2.0V DC/DIV
SWEEP   50 μsec.

* Normally low level

4.9 KB REQUEST Signal

POINT   IC 8G PIN18
VOLTAGE   2.0V DC/DIV
SWEEP   50 μsec.

   * Normally high level

A-25
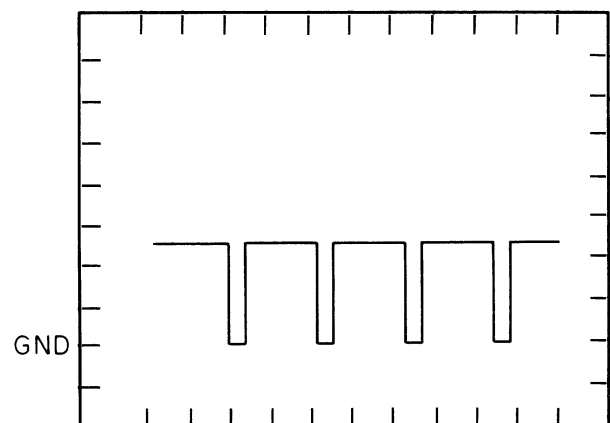
4.10 Cassette Write Waveform Slave Output

POINT   IC 6D PIN 33

VOLTAGE   2.0V DC/DIV

SWEEP   0.5 msec

Bit on where pulse is wide; bit off where pulse is narrow

*Normally low level
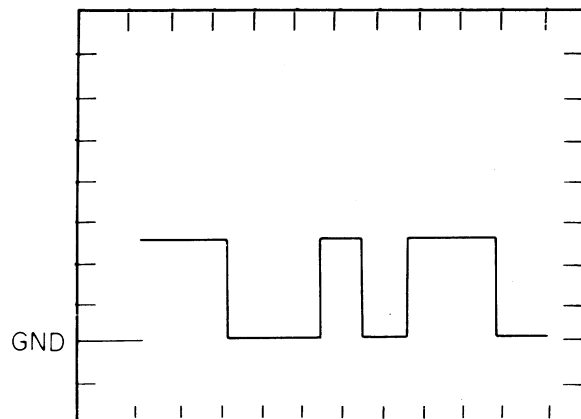
4.11 Cassette Read Waveform

POINT   IC 8D PIN7

VOLTAGE   2.0V AC/DIV

SWEEP   0.5 msec.

All bits are off. When bit is on, pulse width is twice as large.

*Normally high level
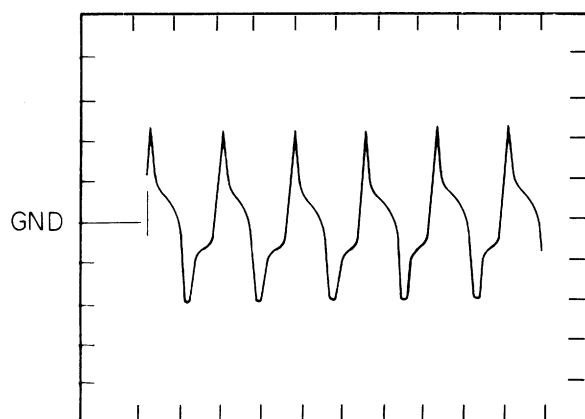
4.12 Cassette Read Waveform

POINT   IC 8D PIN6

VOLTAGE   2.0V DC/DIV

SWEEP   0.5 msec.

This is a shaped version of the above input to IC 8D Pin 7.

*Normally low level
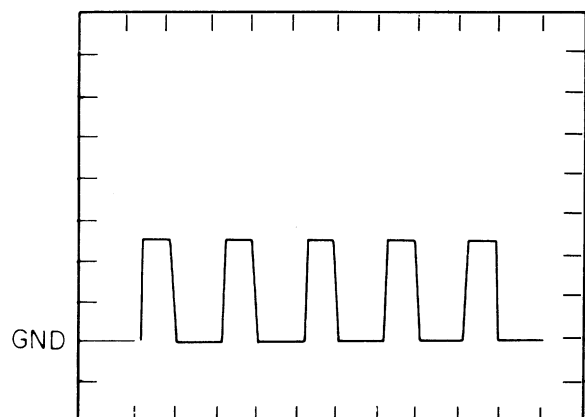
4.13 Microcassette Read Waveform

	CH1	CH2
POINT	IC4 PIN1	IC4 PIN2
VOLTAGE	2.0V DC/DIV	0.5V DC/DIV
SWEEP	0.1 msec	0.1 msec
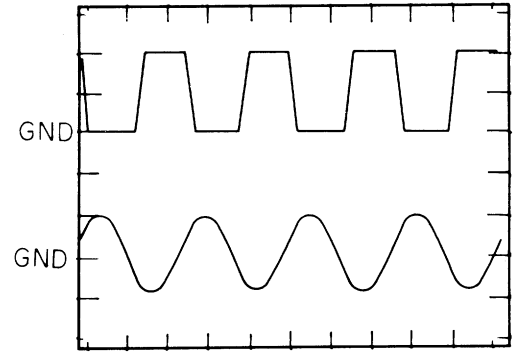
4.14 Microcassette Read Waveform

	CH1	CH2
POINT	IC4 PIN1	IC4 PIN2
VOLTAGE	2.0V DC/DIV	2.0V DC/DIV
SWEEP	0.1 msec.	0.1 msec.
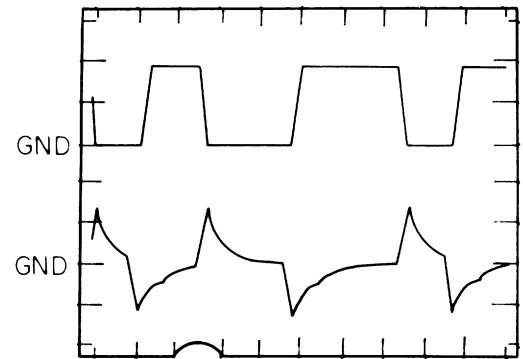
4.15 Tachogenerator Output

POINT	R16
VOLTAGE	0.2V AC/DIV
SWEEP	1.0 msec.

This signal has a period of 400 Hz. In case of no speed control (REW/FF), the period increases to more than 400 Hz and the waveform to about 1.5 Vp-p.
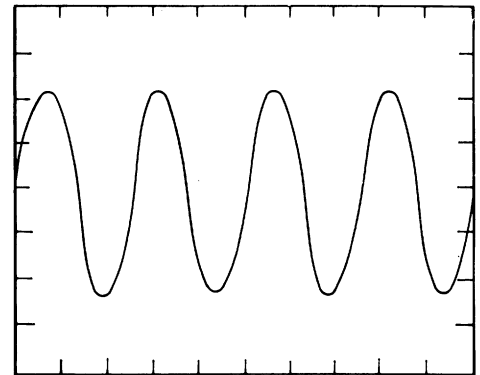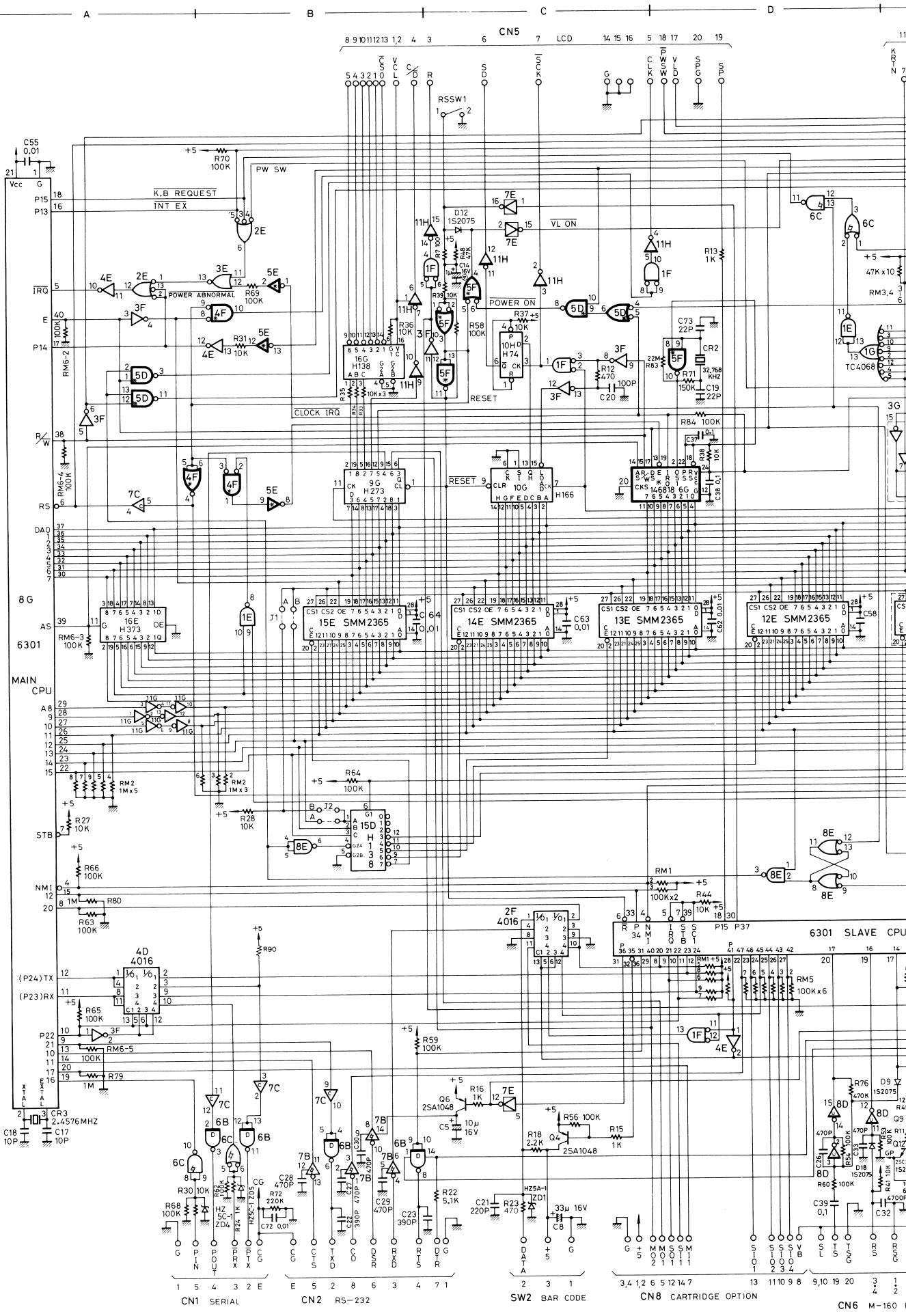
HC(X)-20 MOSU BOARD
UNIT No. Y201202000

A-28
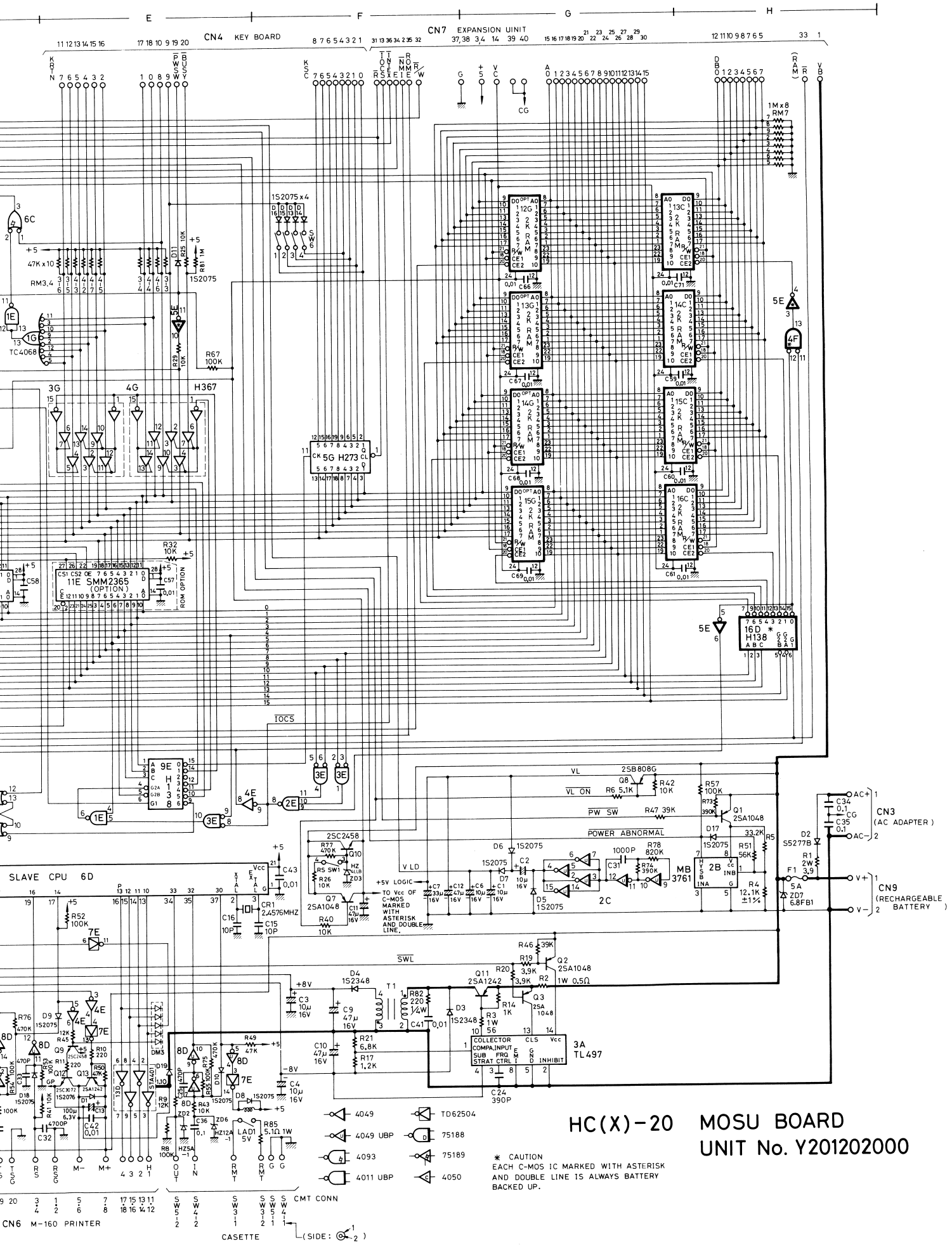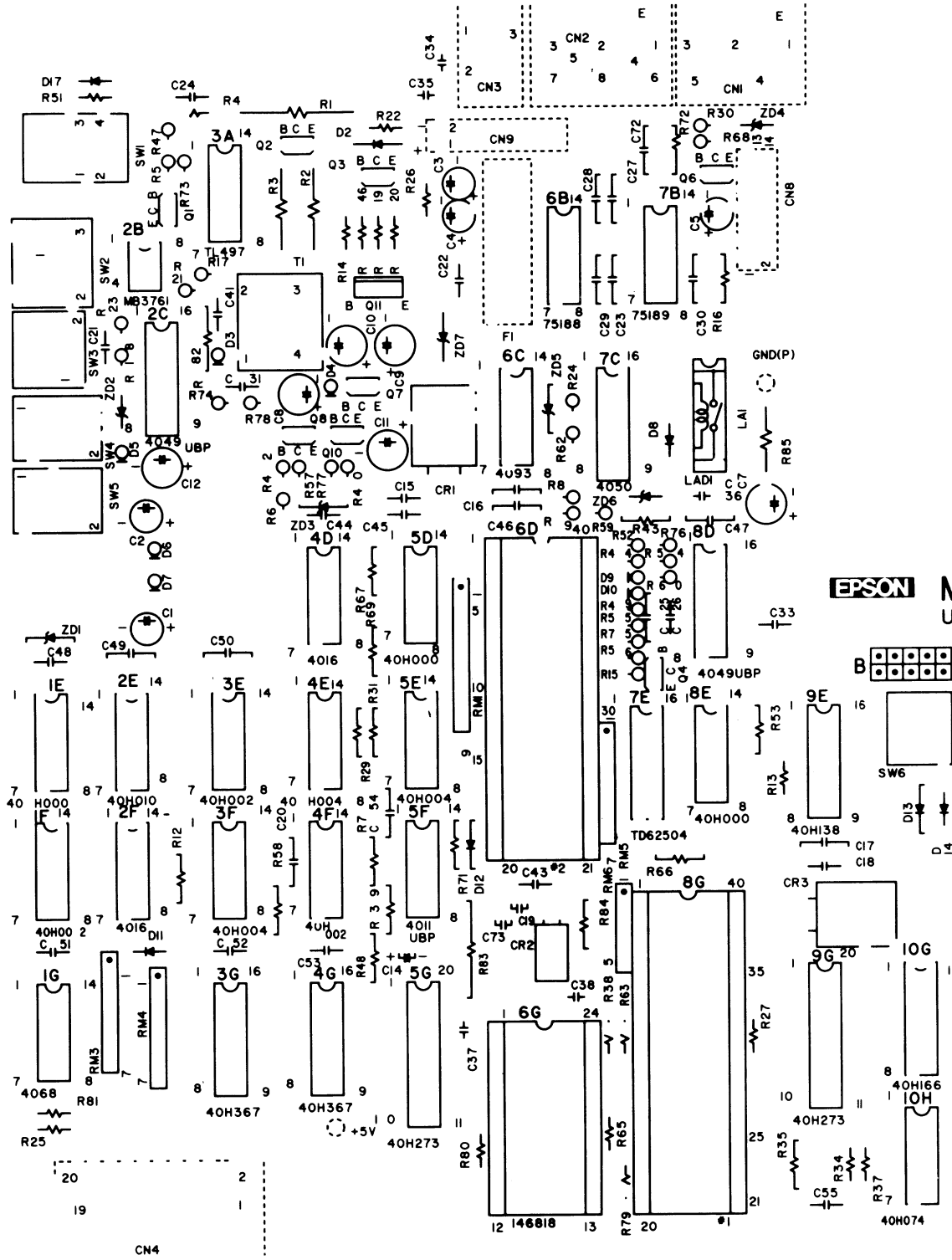
(MOSU BOARD COMPORNENT SIDE V

EPSON MOSU BOARD
UNIT Y20120200000

(COMPORNENT SIDE VIEW)

C61 16C RM2 C60 15C C59 14C C71 13C RM7
24 24 24 24
R10
20 20
R50
R28
RAM4 RAM5 RAM6 RAM7
16D 15D 13D
R64 E 12 B 10 STA401
Q12 E B E C B
DI8 Q13 DI Q9 RM8
R45 C13 5 C39
J2 R41 VP
B A C32 10 C42 20 R32
9 8 9 8
40H138 40H138
C64 5 CN6 15

39 C65 28 15E 1 28 14E 1 28 13E 1 28 12E 1 28 11E 4
16E 3
31 20 1 2
25 DI6 DI5 SW
21 20 DI3
11 10 JI D
40H B
373 A
C70
15 ROM0 14 15 ROM1 14 15 ROM2 14 15 ROM3 14 15 ROM4
16 16G C69 15G C68 14G C67 13G C66 12G VC 14 11G 16 10G
R33
CN7 R36 5 40H 004
9 40H138 8 40HI66
16 11H 14 10H
10
10
RAM0 12 RAM1 12 13 RAM2 12 13 RAM3 12
20 13 C6 R70 9 8 8
1 5 15 C56 4049 40H0
CN5

(MOSU BOARD REAR SI

This is a circuit board layout diagram (PCB component placement view). The text and labels are positioned according to their location on the board.

E CN2 3 1

E 2 CN2 5 3
1 4 6 8 7 CN3
4 CN1 5 2

ZD4 R30 C34 C35

R68 R72 C72 C27 CN9 2 C3 R26 R22 D2 R1 R4 C24 D17 R51

E C B Q6 147B C5 C29 146B R R R C4 C22 E C B Q3 Q2 143A SW1

CN8 R16 C30 75189 8 C29 C23 75188 7 F1 ZD7 C10 QII B TL497 MB376 R17 R21 2B 2C 4049 UBP

GND(P) R85 LA1 LAD1 C7 36 C47 8D R76 R43 R52 6D C46 ZD5 R24 R62 6C 4093 C16 R8 40 R9 CRI C15 C45 C44 ZD3 Q7 Q8 R78 R74 R82 D3 C41 T1 Q10 R40 R57 R77 R42 R6 C12 C2 CI

B 11E 3H ROM4 9E R53 R13 8E 7E 4050 ZD6 RI5 4049UBP TD62504 RM6 145D R67 R69 144D 4016 C50 C49 ZDI C48 IE 40H0 00

SW6 40H138 C17 C18 CR3 40H000 RM5 C43 D12 R71 145E R31 R29 C54 R7 144E 04 C20 40H002 3E 2E 40H010 1F 40H0

II G 10G 20 9G 8G R66 R84 CI9 CR2 C73 R83 205G C14 R48 C53 4G R58 40H004 3F 2F1 4016 IG RM4 RM3

II H 10H 40H166 40H273 35 R27 6G 24 C37 40H367 40H 002 C 52 3G 40H367 R81 4068

4049 40H074 C55 R34 R37 25 R35 21 *1 20 R79 146818 13 12 R65 R80 *2 C43 +5V 0 20 19 2 1 CN4

A-31

#1

V₁ V₂ V₃ V₄ Vss   SO C CS
                   BUSY D SYNC
34 SYNC
29 SI
32 SCK
27 CLK
28 RESET

37 36 35 25   31 30 33

COL0 ————— COL39

~57 59~64 2~ 24

#2

58 26 38 37 36 35 25   31 30 33
VDD VDD V₁ V₂ V₃ V₄ Vss SO C CS
                        BUSY D ROW0
34 SYNC
29 SI
32 SCK
27 CLK
28 RESET
ROW7

39

46

COL0 ————— COL39

47 ~57 59~64 2~ 24

COL40 ————— COL79   COL80 ————— COL119   16A — 9A

LCD PANEL

COL160 ——— COL199   COL200 ————— COL239   9B — 16B

~57 59~64 2~ 24   47 ~57 59~64 2~ 24

#4

COL0 ————— COL39
34 SYNC
29 SI
32 SCK
27 CLK
28
SO C RESET
BUSY D CS
V₁ V₂ V₃ V₄ Vss
37 36 35 25   31 30 33

#5

COL0 ————— COL39
34 SYNC
29 SI
32 SCK
27 CLK
28 RESET
SO C ROW0
ROW7
VDD VDD V₁ V₂ V₃ V₄ Vss BUSY D CS
58 26 38 37 36 35 25   31 30 33

RM1   RM2   1MΩ x 12

2 5 2 6 7 4 3 5

CLK SCK SI CS5 CS4 CS3 CS2 CS1 CS0

8 13 10 7 3 6 4 5 2

TO KEY BOARD CONNECTOR CN3)

HC(X)-20   LCD
UNIT No. Y201502000

CN 2 (TO MOSU BOARD CN4)

NOT USED

5 x 8

C2458
Q2

R4 10K   R3 10K   R1 20K

Q1
C2458

VR1
10K VR

D1

D2

R2
10K

C1
0.01

PW SW
W 3

14	Vcc	
1	G	
12	$\overline{BUSY}$(SO)	
11	C/$\overline{D}$	
9	R	
8	$\overline{CLK}$	
13	SCK	
10	SD	
7	$\overline{CS5}$	
3	$\overline{CS4}$	
6	$\overline{CS3}$	
4	$\overline{CS2}$	
5	$\overline{CS1}$	
2	$\overline{CS0}$	

CN3

S_{PG}]2
SP]1   CN4

HC(X)-20 KEY BOARD
UNIT No. Y201501000

$\overline{P}$ G V C/ R C $\overline{S}$ S $\overline{C}$ $\overline{C}$ $\overline{C}$ $\overline{C}$ $\overline{C}$ V S S
W   L $\overline{D}$ L C S D S S S S S C P P
S   D   K K K   5 4 3 2 1 0 L G
W

18 14 17   4   3   5   7   6   8   9 10 11 12 13   1   20 19
    15   2
    16

CN1   (TO MOSU BOARD CN5)

1

2

3

R17
3.3K

R1
100Ω
1W

1Ω
1W
R2

T1
3   4

RGP15G
D1

Q1
A1244

C8
0.01μ

R16
220

R20
27K

R18
2.7K

A1048
Q2

14   13   10

C10
39p

TL497
3A

8

Q4
C3074

SR1   7805
1   2
IN   OUT
COMMON
3

1   2   3   4   5

R15
100

R13
6.8K

R19
10K

Q3
C1472

R14
1.2K

C9
330P

C1   10V
100μ

C3
12V
0.1μ

C6
12V
0.1μ

J

R21
100K

4

5

6

7

8

A-33

HC(X)-20 ROM CAT
UNIT No. Y202201000

RLD +

RLD −

E + (ORANGE)

E − (BLUE)

R8 390   Q4 A1204   D1 1S2348   D2 1S 2348   Q5 A1204   R9 390   R29 15K

R26 15K   Q15 C2712

R27 15K   Q9 C2532

Q16 C2712   Q10 C2532   R28 15K

R30 15K   R4 220   Q13 C2532

Q6 A1204

R5 220

R31 15K   Q11 C2532   R32 680   Q12 2SD1048

HPM + (RED)

C18 0.68μ

HPM − (BLACK)

M+ (RED)

M− (BLACK)

C20 0.01μ   C19 0.01μ

C5 2.2μ 10V   C13 0.22μ   VR1 200K   2.2μ 10V C6   10K R45   C14 0.01μ   TP2

R34 15K   R42 300K   R10 1K   FG I (ORANGE)

C7 0.0033μ   FG II (ORANGE)

R39 27K

TP1

2712 Q18

16 4   12   13   14   1   3   2

6   Vcc

TD6303F   IC1

G

R33 15K   Q19 C2712   9   10   5   8   R1 2.2M   R2 100

HSW I (BROWN)

HSW II (BROWN)

WE I

WE II

TP3

(IC4)   2   2904   3   C10 0.047μ   (IC4)   8 V+   2904   7   4 V−   6   5   C9 0.022μ   (IC5)   5   2904   7   6   C8 0.1μ

RPH+ (PINK)

C16 47P   C12 33P   C15 0.015μ

R22 1M

R43 10K   R21 39K   R40 330K   R20 5.1K   R19 10K   R24 6.8K   R41 390K   R17 5.1K   R16 5.1K

RPH− (WHITE)

C17 4.7μ 10V

R18 330Ω

R13 680Ω   C4 2.2μ 10V

R23 10K   Q20 A1162
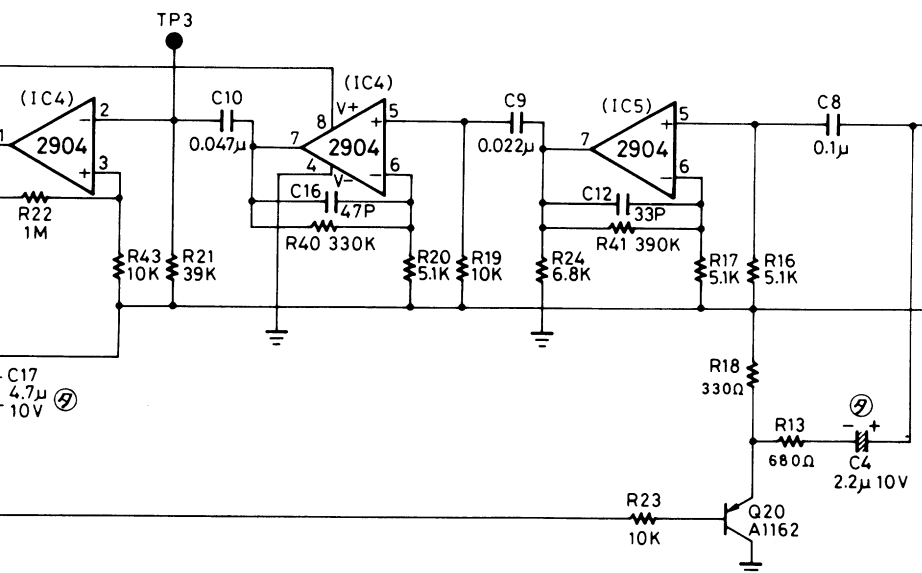
HC(X)−20 μMCT
UNIT No. Y202210000
(Y202209000)

A-34

M5C 6847 P-1

2C
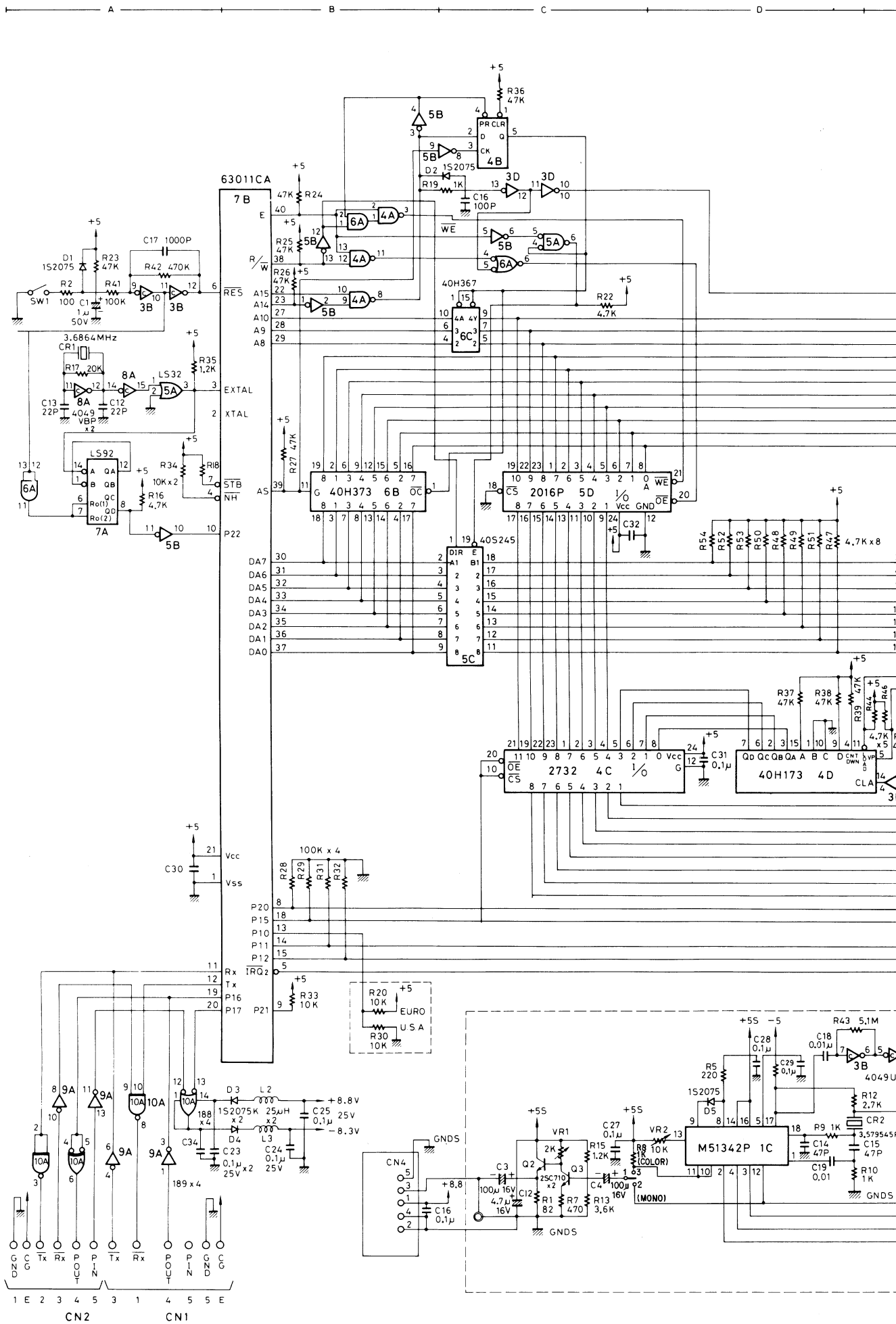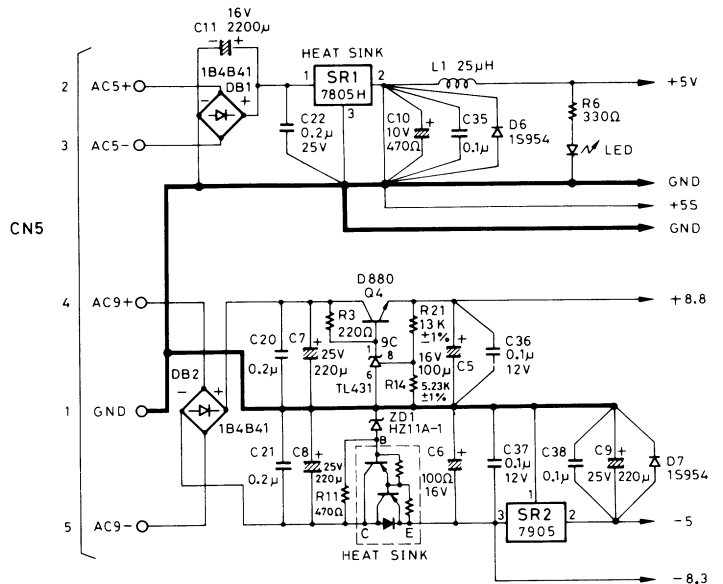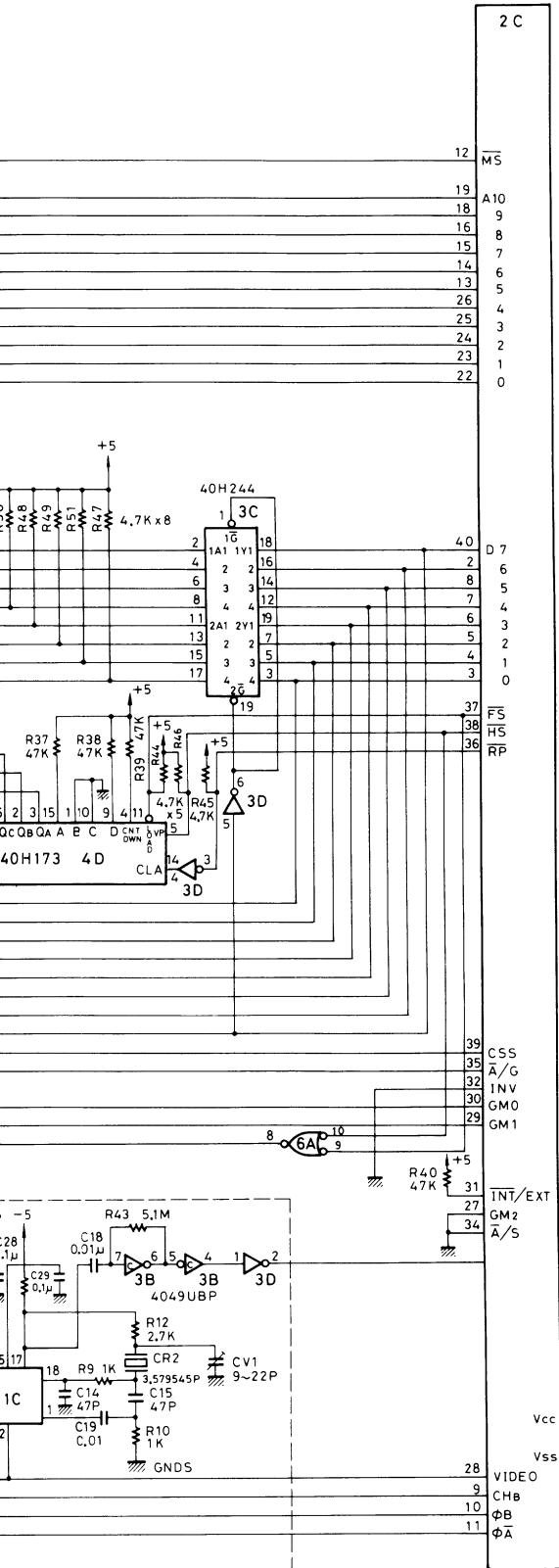
USAGE LOCATION	IC TYPE	USAGE LOCATION	IC TYPE
1C	M51342P	5C	40H245P
2C	M506847P	5D	2016P
3B 8A	4049UBP	6A	40H008P
3C	40H244P	6B	40H373P
3D 5B	40H004P	6C	40H367P
4A	40H000P	7A	74LS92P
4B	40H074P	7B	63011CA
4C	D2732D	9A	SN75189
4D	40H193P	10A	SN75188
5A	74LS32		

HC(X)-20 TVA BOARD
UNIT NO. Y202203200

IC TYPE	USAGE LOCATION
40H000	1A 5A
40H002	3A 6A
40H004	7A
40H010	4A
40H138	2A 8A
40H367	9A 10A 11A
40H245	12A

✱ CAUTION
IC 'IA' MARKED WITH ASTARISK
AND DOUBLE LINE IS ALWAYS
BATTERY BACKED UP.

HC(X)-20 EXP BOARD
UNIT No. Y202204000