CHAPTER 4
OPTIONS

4.1 Microcassette

The microcassette is controlled by the main and slave CPUs. Its operation is controlled by storing the commands sent from the slave CPU as serial data into an instruction register. A counter circuit employing a photo-reflector is provided so it is possible to feed the tape fast to the required area by using this counter.

4.1.1 Hardware Composition

The microcassette consists of a power supply, motor drive circuit block, read/write control block, and motor speed control block, etc. and is designed to turn power on only when it is used.

The tape is fed at a speed of 2.4 cm/sec by a 2400 rpm capstan motor. Data is read or written at about 1300 BPS, and about 50 KB of data can be input to a 30-minute cassette.

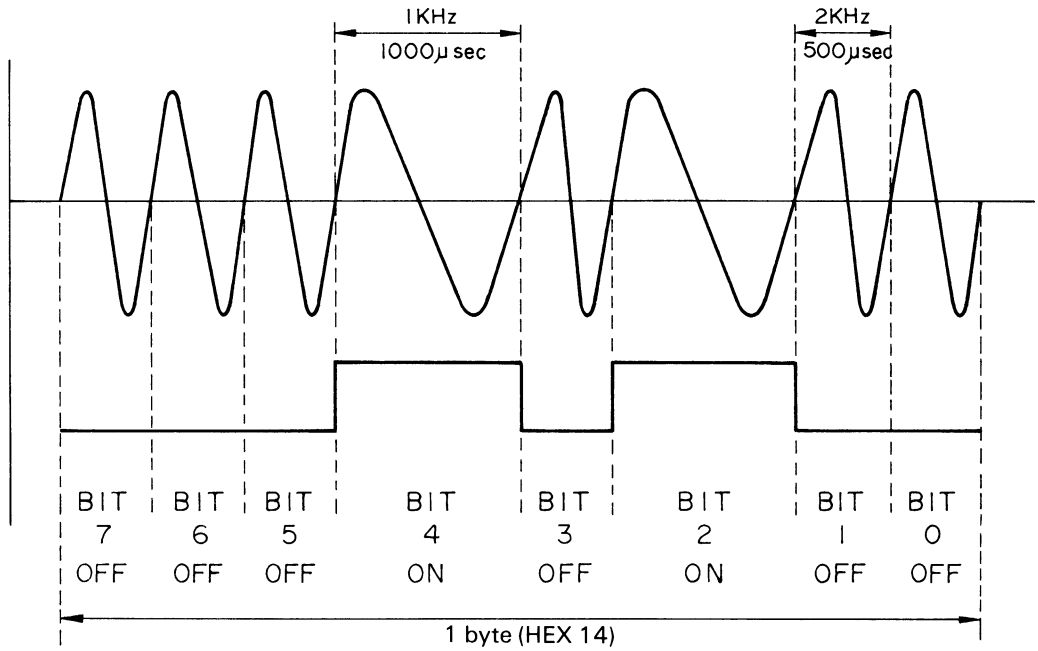


Fig. 4-1

Data is written onto a tape by FSK (frequency modulation) for a period of 2 kHz at bit 0 (off) or of 1 kHz at bit 1 (on).

● Hardware Block Diagram

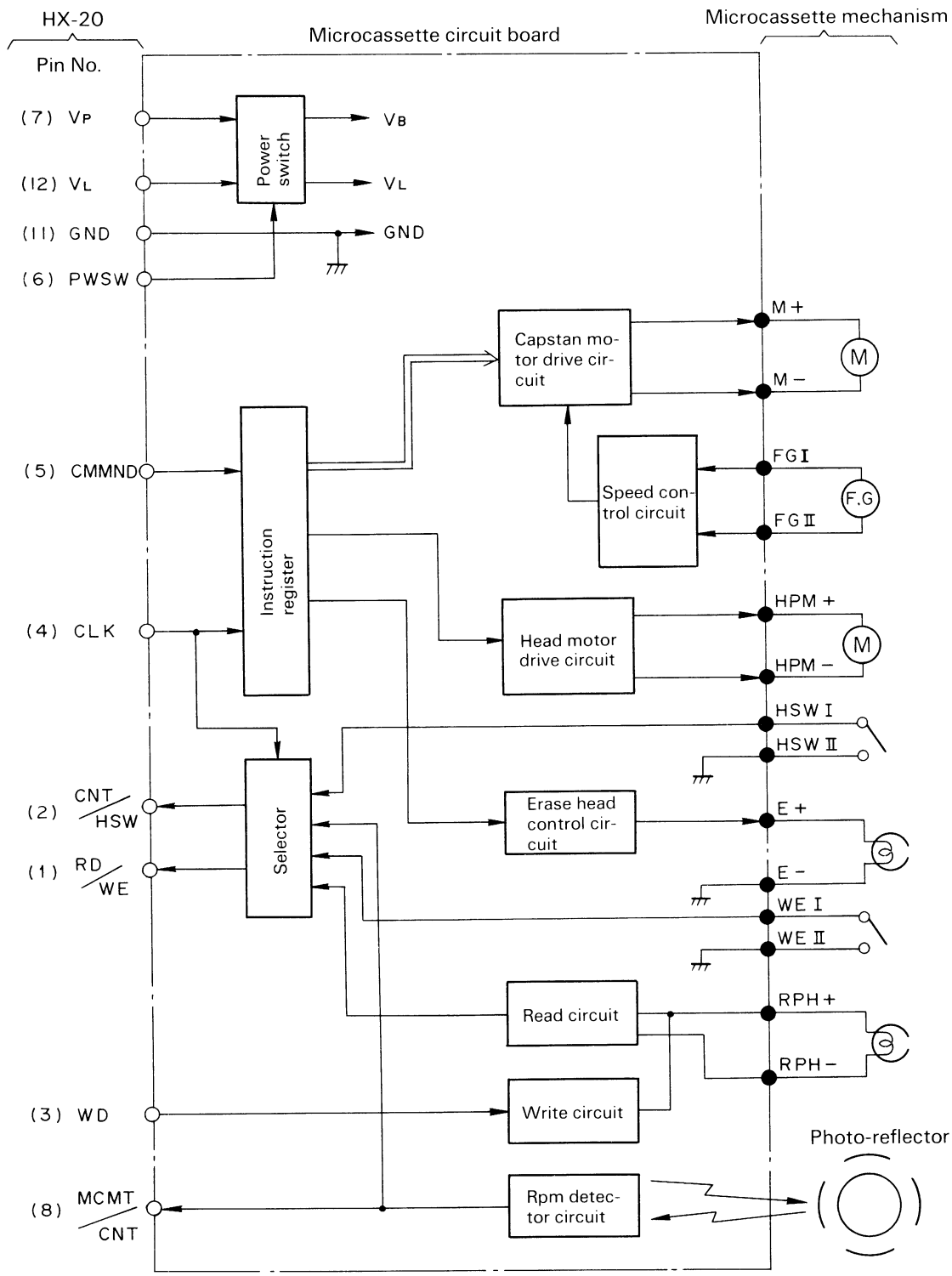


Fig. 4-2

4.1.2 Interface with HX-20

(1) The microcassette is connected to the MOSU circuit board with the cable set No. 701. The interface signals for the MOSU circuit board apply where the ROM cartridge is connected so their names are different from those for the microcassette.

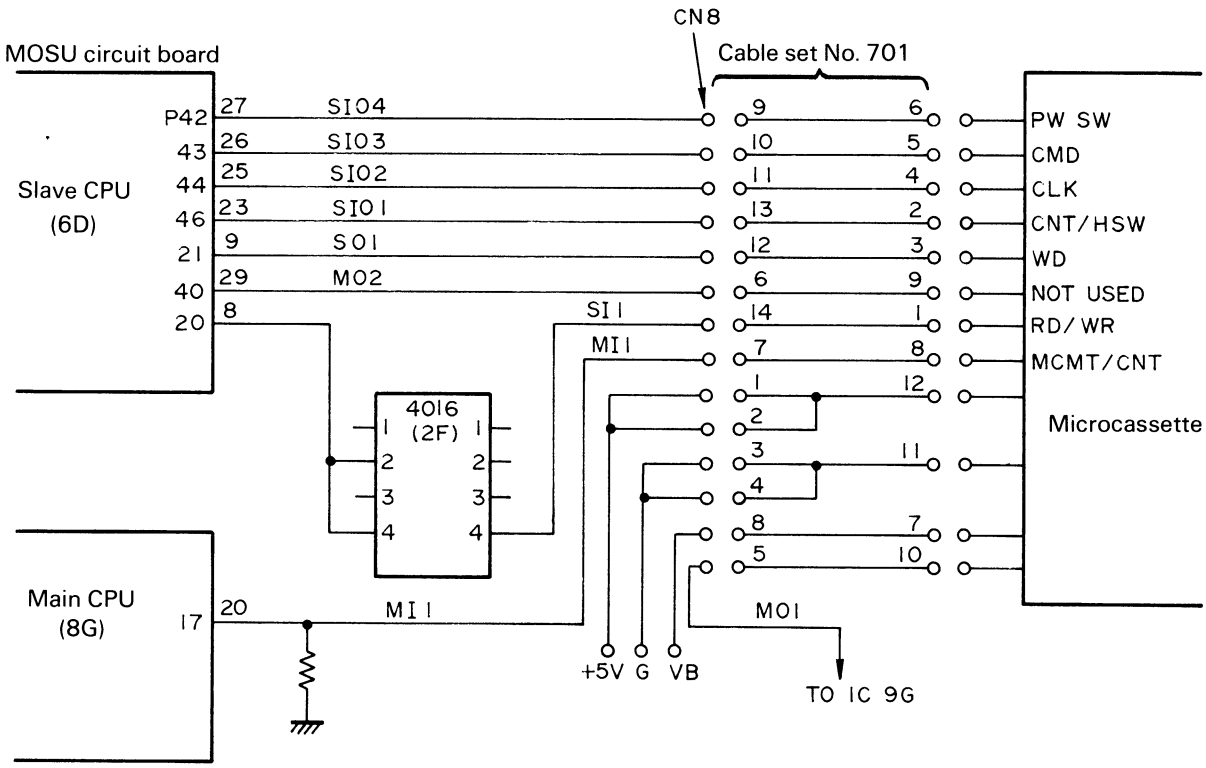


Fig. 4-3

(2) Interface signals

Pin No.	Signal direction I/O	Signal name			Description
		Special Name	Common Name	Port	
1 (14)	In	RD/WE	Si1	Slave Port 2 Bit 0	Selected depending on CLK (Pin No. 4) value. CLK = 0 : RD Microcassette read data CLK = 1 : WE Accidental erasure prevention signal WE = 0 (prevention of writing to)
2 (13)	In	CNT/HSW	Sio1	Slave Port 4 Bit 6	Selected depending on LCK (Pin No. 4) value. CLK = 0 : CNT rpm detect signal CLK = 1 : HSW Head switch HSW=0 (Head off)
3 (12)	Out	WD	So 1	Slave Port2 Bit 1	Microcassette write data
4 (11)	Out	CLK	Sio 2	Slave Port4 Bit 1	Command set clock and RD/WE, CNT/HSW select signal
5 (10)	Out	CMMND	Sio 3	Slave Port 4 Bit 3	Command serial data output
6 (9)	Out	PWSW	Sio 4	Slave Port 4 Bit 2	Power on-off switch
7 (8)	–	VB			+5V (Microcassette mechanism drive voltage)
8 (7)	In	MCMT/ CNT	Mi 1	Main Port 1 Bit	Power off: Microcassette in or out = 1 (in) = 0 (out) Power on: Rpm detect signal is input.
9 (6)	Out		Mo 2	Main Address 26 Bit 7	Unused
10 (5)	Out		Mo1	Main Address 26 Bit 6	Unused
11 (4.3)		GND			Ground
12 (2.1)		V_L			+5V (for write/read circuit, selector instruction register)

Figures in parentheses indicate pin numbers of CN8 on the MOSU circuit board.

Fig. 4-4

4.1.3 Power Supply

The power supply consists of a circuit which constantly supplies the voltage by V_L and a motor circuit which supplies the voltage VB only when the microcassette is in use. V_L is always supplied to instruction register (IC2) and selector (IC3) to permit reception of commands and status check of the HSW and WE switches at any time. When a power on signal (PW SW) goes high, transistor Q8 in the motor drive circuit is turned on so the base of transistor Q2 goes low, and the voltage VB is supplied to the collector of Q2. Transistor Q1 is turned on simultaneously so the voltage VB is supplied to the collector of Q1 to supply it to the LED lamp for the microcassette.

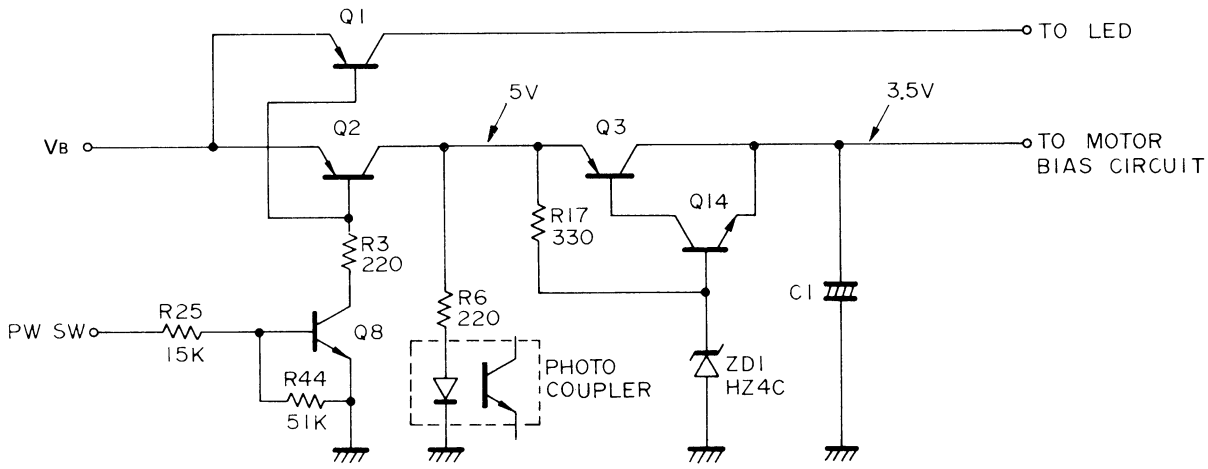


Fig. 4-5

A motor drive voltage of +3V is generated by stepping down the voltage VB (about 5V) to about 3.5V by means of transistors Q3 and Q14 and zener diode ZD1 (4V). The 3.5V is output to the collector of transistor Q3. In the circuit that generate the motor voltage from VB, first the output voltage of Q2 is applied to ZD1 via R7. If the applied voltage is higher than 4V, ZD1 occurs zener breakdown so a current flows via R7. As a result, the base of Q14 goes low to turn off the transistor; and the collector output of transistor Q3 is also turned off. As the zener yield of ZD1 causes a large current to flow via R7, the voltage drop across R7 lower the cathode voltage of ZD1 to 4V or less. Thus, the zener yield stops and transistors Q14 and Q3 are turned on again to supply a voltage to the collector of Q3. This process is repeated to generate a voltage of +4V minus the internal voltage drop in the transistors, that is, about 3.5V.

4.1.4 Capstan Motor Drive Circuit

Motor condition is controlled by commands in the instruction register. There are 5 modes as follows:

1) Stop
2) Play/Rec (Read or write)
3) REW (Rewind)
4) FF (Fast Feed)
5) Brake

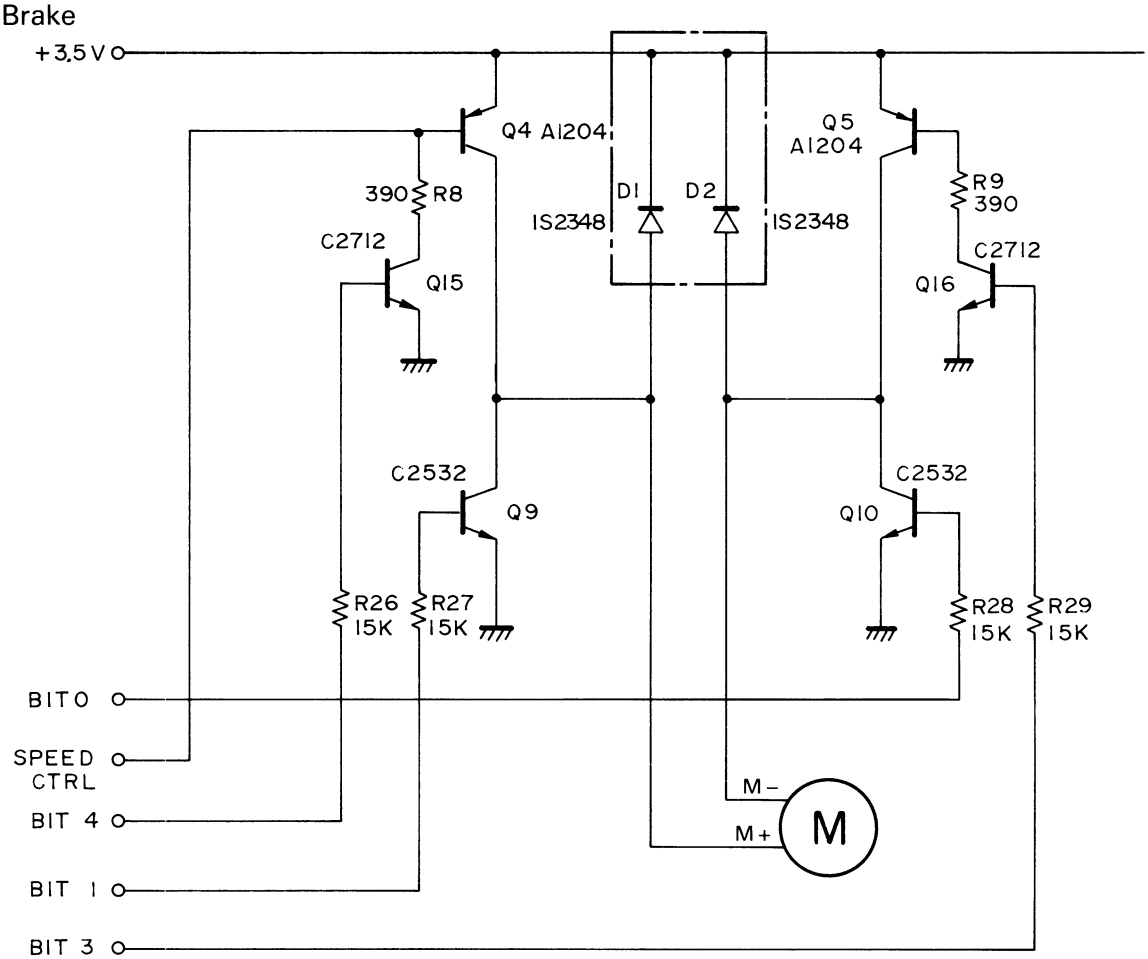


Fig. 4-6

(1) Stop (Command 00)

In this mode, no voltage is applied to the motor because voltage supply to the motor circuit is stopped (the PW SW signal goes low).

(2) Play (Read)/Rec (Write) (Play command 01, Rec command 81)

In the read or write mode, transistor Q10 is first turned on by command bit 0, and the motor M- (negative) goes to the ground level. At operation start, Pin 6 output from IC1 (TD6303F) is at low level so transistor Q4 is on and a voltage of about 3V is applied to the motor M+. Therefore, the motor starts running, and the timing generator that is attached to the motor generates a feedback pulse. This feedback pulse is checked for period by IC1, and is controlled to be 400 Hz by the Pin 6 output (motor bias control).

(3) REW (Rewind) (Command OA)

In the rewind mode, command bit 1 turns on transistor Q19 which is connected to the outside of Pin 9 of IC1. This puts IC1 into the standby mode (i.e., non-operating status), turns on transistor Q9 in the motor drive circuit, and sets the motor M+ to the ground level. Command bit 3 also turns on transistors Q16 and Q5 to apply a voltage of about 3V to the M– end of the motor. Thus, the voltage of about 3V drives the motor in the reverse direction at high speed to rewind the tape without speed control.

(4) FF (Fast Feed) (Command 11)

This mode is used for winding the tape to the desired position indicated by the tape counter (which counts with the microcassette photo-reflector). When an FF command is received, command bit 0 turns on transistor Q10 to set the motor M– to the ground level, and bit 4 turns on transistors Q15 and Q4 to apply a voltage of about +3V to the M+ end of the motor. In this case, IC1 for speed control operates, but since the base of transistor Q4 is at ground level, the speed control signal sent from Pin 6 of IC1 is ignored. Thus, the +3V drives the motor to wind the tape forward at high speed.

(5) Brake (Command 18)

The brake command is used for stopping REW, PLAY, FF or REC operation and braking the tape feed by the moment of inertia of the motor. Command bits 3 and 4 turn on transistors Q16 and Q5 and transistors Q15 and Q4 respectively, so a voltage of about +3V is simultaneously applied to both ends of the capstan motor to brake the motor.

Capstan Motor Bias

Command / Motor terminal	STOP	BRAKE	PLAY REC	REW	FF
M +	Floating	Counterelectro-motive force	SEE NOTE	GND	+ 3V
M –	Floating	Counterelectro-motive force	GND	+ 3V	GND

Note:

Not constant because controlled by IC1's speed control signal.
(Within the range of +3V to +1.5V)

Fig. 4-7

4.1.5 Head Pinch Motor Drive Circuit

The head pinch motor loads or unloads the read/write head on or from the tape. In read or write operation only, the head is loaded. In read or write operation only, the head is loaded. In all other cases, the head is unloaded.

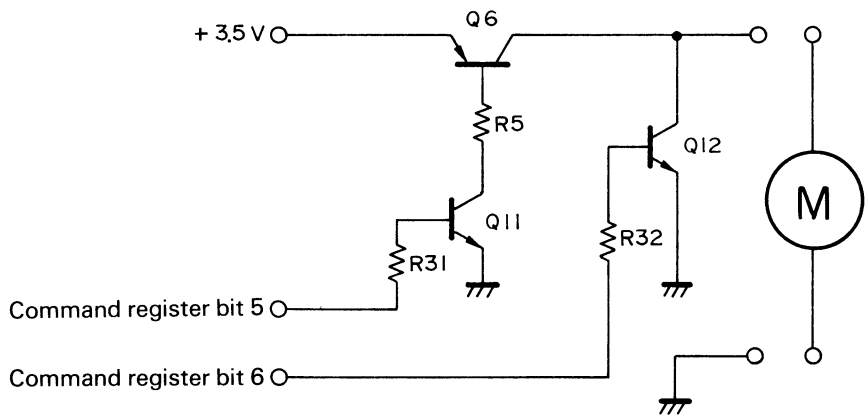


Fig. 4-8

4.1.6 Microcassette Commands

Command	Code (HEX)	Code Bit 7	6	5	4	3	2	1	0	Function
STOP	00									Operation stop
REW	0A					○		○		Rewind
PLAY	01								○	Data stop
FF	11				○				○	FF
REC	81	○							○	Data read
BRAKE	18				○	○				Capstan motor brake
HLD	20			○						Head motor (Head load/unload)
H BRAKE	40		○							Head motor brake

Fig. 4-9

Commands are sent as serial data from the slave CPU to the instruction register when no power is supplied to the motor circuit. The command bits input to the instruction register correspond to the transistors in the motor drive circuit so the command bits directly control the motor drive circuit.

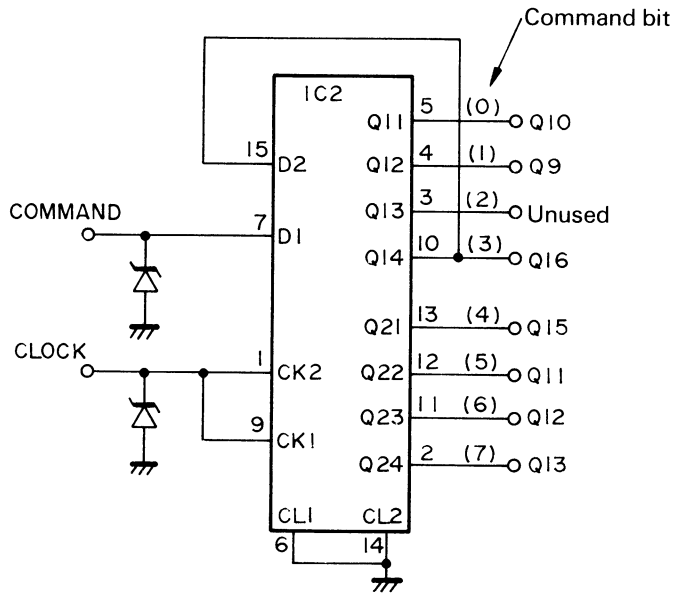


Fig. 4-10

4.1.7 Command Sequence

In switching one command over to another, be sure to stop power supply to the motor drive circuit, input the new command into the instruction register, and then supply power again to execute the required operation. Upon completion of a series of operations, send the stop command 00 to the instruction register at the end to clear the register. After fast feeding the tape with the aid of the counter, reading data from a specific file, and stopping operation is as described below.

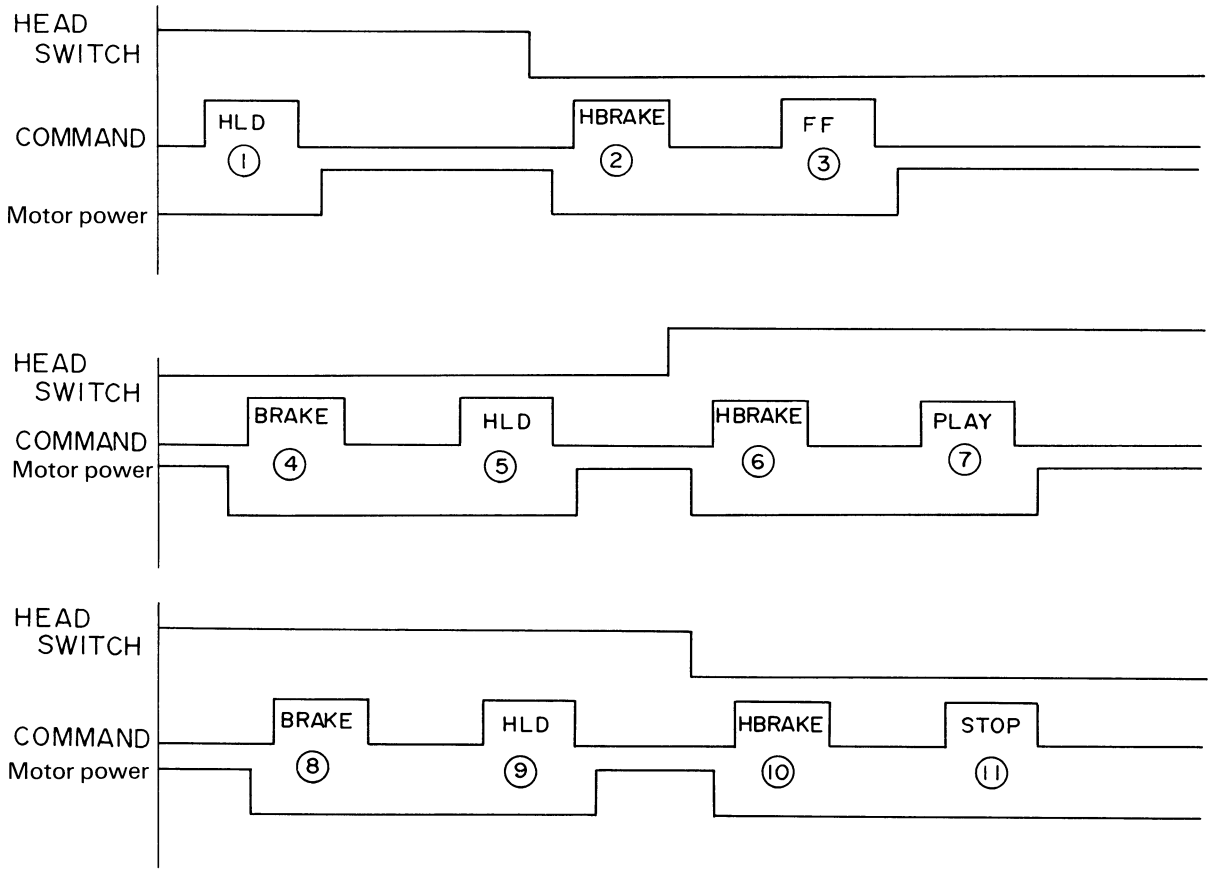


Fig. 4-11

(1) Check the R/W head switch, and confirm that the tape is unloaded. If it is loaded, operate the head motor to unload it.
(In the diagram below, the tape is unloaded if shaft C and the pinch roller are out of contact with each other; or loaded if otherwise.)

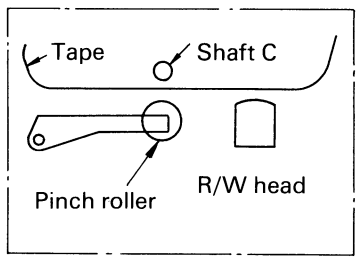


Fig. 4-12

(2) After turning power off, short both terminals of the motor to brake the rotation of the head mortor by its moment of inertia.
(3) Drive the capstan motor without speed control to wind the tape forward at high speed to the desired count (on the photo-reflector counter).
(4) After turning power off, short both terminals of the motor to brake the capstan motor.
(5) Set the R/W head into a loaded state.
(6) Brake the head motor which was driven by the above steps.
(7) Wind the tape at constant speed (under speed control at 2.4 cm/sec), and read data.
(8) Brake the capstan motor.
(9) Set the R/W head into an unloaded state.
(10) Brake the head motor.
(11) Send a stop command to clear the instruction register. (Clear it to 00 inside.)

4.1.8 Motor Speed Control

The rotating speed of the capstan motor is controlled only when it operates (read or write) by the PLAY or REC command. The capstan motor has a timing generator for checking its rpm, and speed is controlled by processing its timing period by IC1 (motor control IC).

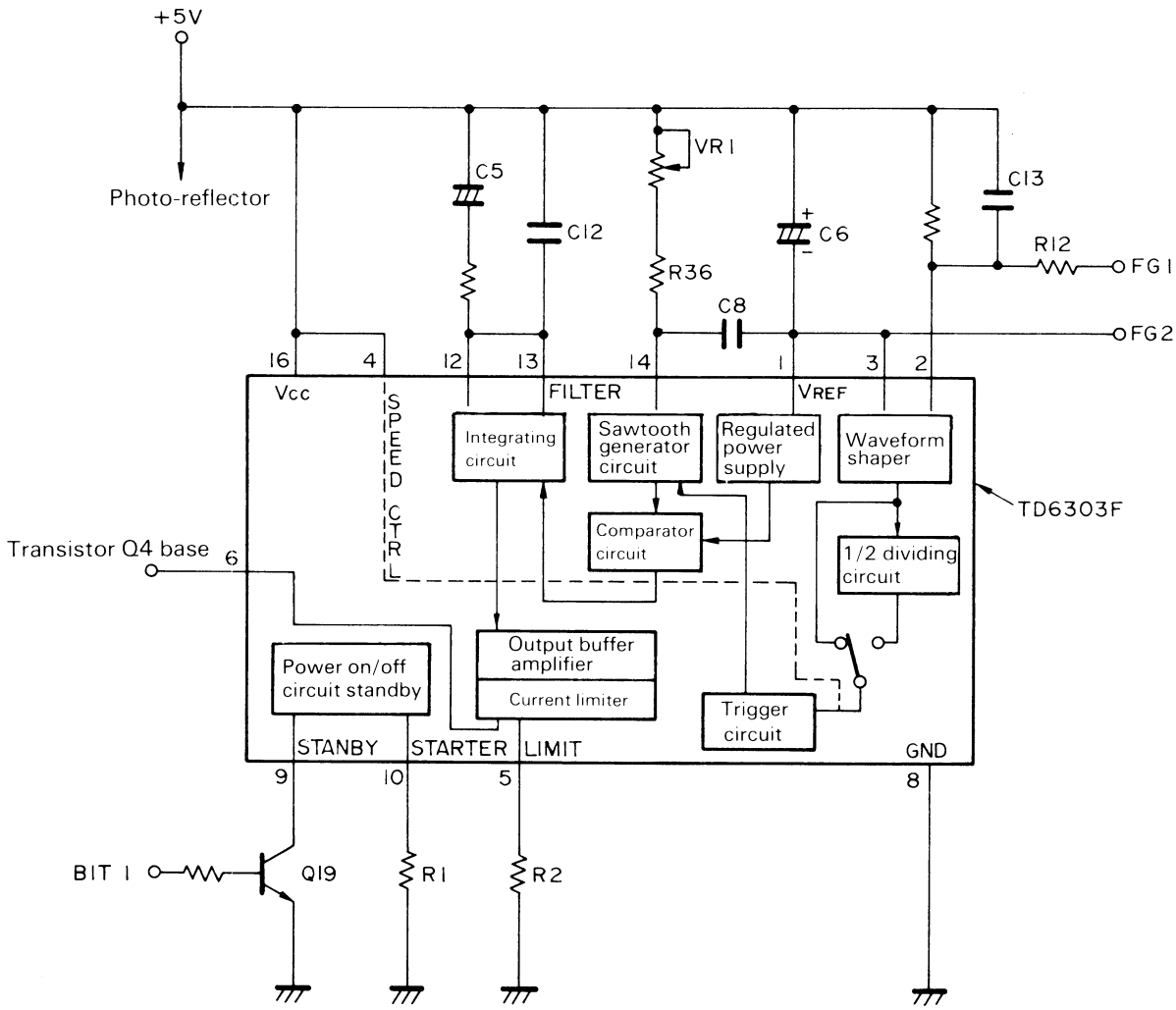


Fig. 4-13

(1) Operation

First, the signal FG2 from the timing generator enters Pin 3 of TD6303F, where the waveform is shaped. Here, the microcassette is running at 2.4 cm/sec, and the input to Pin 4 is at high level so that the signal is sent directly to the trigger circuit without going through the dividing circuit, and the output of the trigger circuit is supplied to the sawtooth generator circuit.

Since the basic clock of 400 Hz generated by an external oscillator circuit (composed of C8, R36 and VR1) is input to the sawtooth generator circuit, the periods of this basic clock and the feedback signal from the timing generator are compared, and the result is routed via the integrating circuit, output buffer amplifier, and current limiter to Pin 6, from which it is sent out. Pin 6 controls transistor Q4 in the motor circuit, and changes the voltage to be applied to the M+ terminal of the motor to change the motor rpm, thereby assuring that the tape is wound at constant speed.

Capstan motor

- Normally runs at 2400 rpm.

Timing generator

- Has 10 poles, and is coupled to the capstan motor shaft.

$$\frac{2400\ (\text{rpm}) \times 10\ (\text{poles})}{60\ (\text{seconds})} = 400\ \text{Hz (Basic clock frequency)}$$

- The speed control circuit also outputs a control signal from Pin 6 when processing the FF command. In this case, the FF command turns on transistor Q15 to hold the base of transistor Q4 at low level so that the control signal is ignored. When processing the REW command, the input to Pin 9 of TD6303F goes low due to bit 1 of the REW command so that the stanby mode is selected, and TD6303F will not operate.

4.1.9 Read/Write Circuit

The read/write circuit can be divided into the read/write bias supply circuit, read circuit, write circuit, and erase head circuit.

(1) Bias supply circuit

Read or write operation requires a steady bias for exciting the R/W head. First, transistor Q8 is turned on by a PW SW signal, causing transistor Q7 to turn on and the voltage V_L to be supplied to IC5. Here, the input voltage to Pin 3 of IC5 is controlled by zener diode ZD2 so an input voltage of about 2V is supplied. Then, the output of Pin 1 is fed back to Pin 2 for non-inverted DC amplification. In this case, the amplification ratio is 1 because Pin 1 and Pin 2 are directly connected to each other. Actually, therefore, Pin 2 is used not as a amplifier but as a regulator to stabilize the voltage.

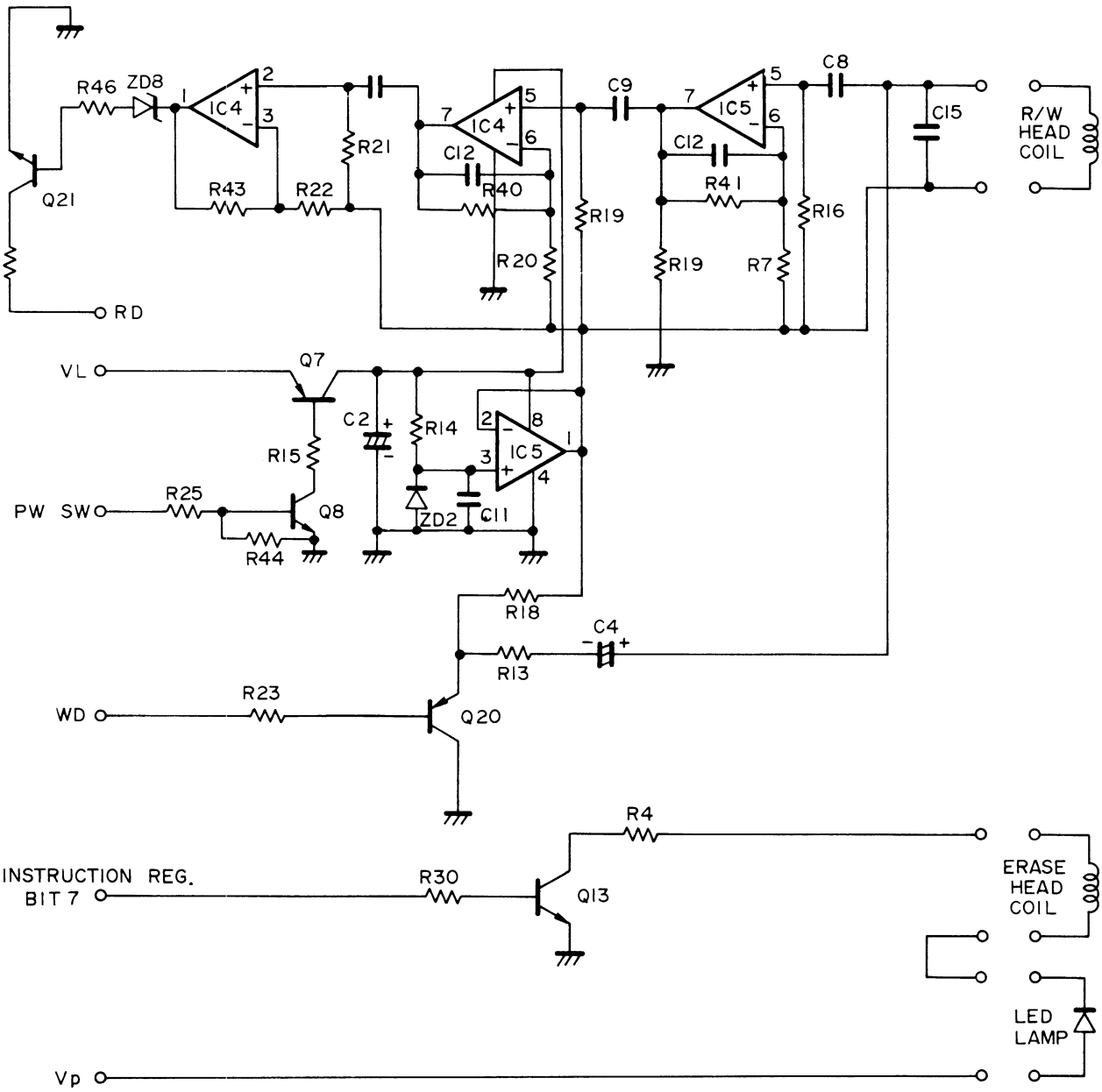


Fig. 4-14

(2) Read circuit

First, the input signal is amplified 34 dB(Av = 1 + $\frac{R40}{R20}$) by IC5 to generate a signal of about 0.8 Vp-p, which is output from Pin 7. Then, the signal is amplified twice by IC4, and finally transistor Q21 is switched on and off by using the zener yield effect of zener diode ZD8. After that, the read data is read out via IC3.

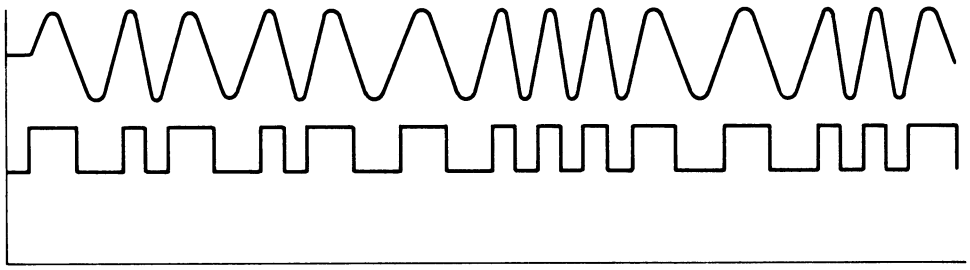


Fig. 4-15

(3) Write circuit

Transistor Q20 is turned on and off by a WD signal to control the current to the read/write head coil in writing data. When Q20 is turned on, capacitor C4 discharges so the current I1 flows to the head coil. When Q20 is turned off, the charging current I2 flows from the bias to capacitor C4 via the head coil. Data is written in this way by changing the magnetic polarity of the head by changing the direction of the current that flows to the head coil.

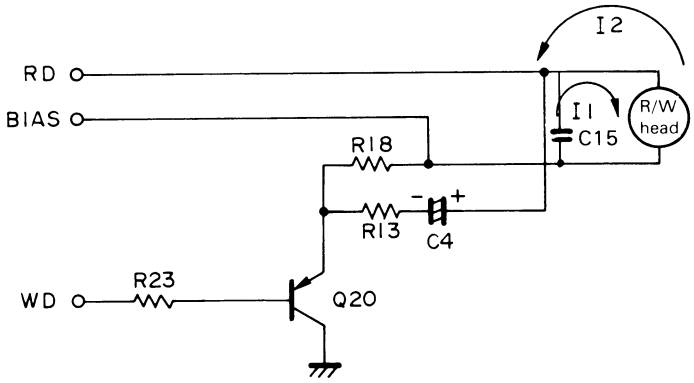


Fig. 4-16

(4) Erase head

Data can be erased only during write operation. First, the data on the tape is erased by the erase head, and data is written onto the tape by the R/W head. The erase head is connected in series to the LED lamp on the cartridge case so the LED lamp remains lit during write operation.

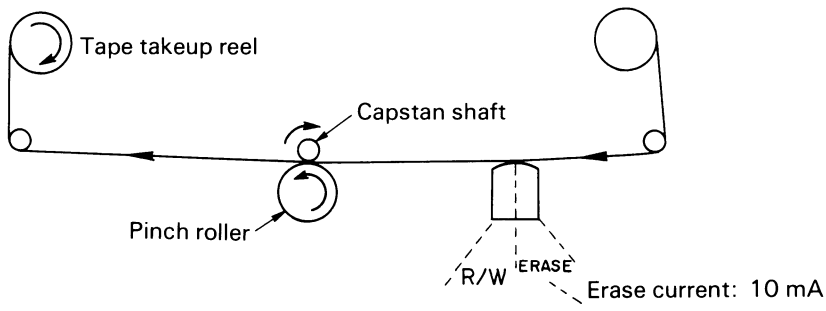


Fig. 4-17

4.1.10 Selector Circuit

The selector is controlled by a clock. When the clock is at high level, transistor Q17 is turned on, and its collector goes low so inputs to Pins 1 and 11 are output to Pins 2 and 10 respectively. If the clock is at low level, transistor Q17 is not turned on so Pins 5 and 6 go high. Thus, inputs to Pins 4 and 8 are output to Pins 3 and 9 respectively.

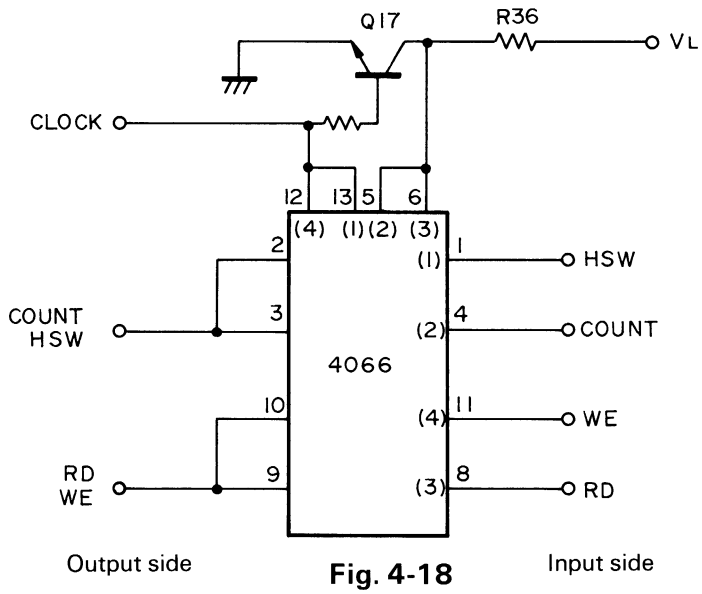


Fig. 4-18

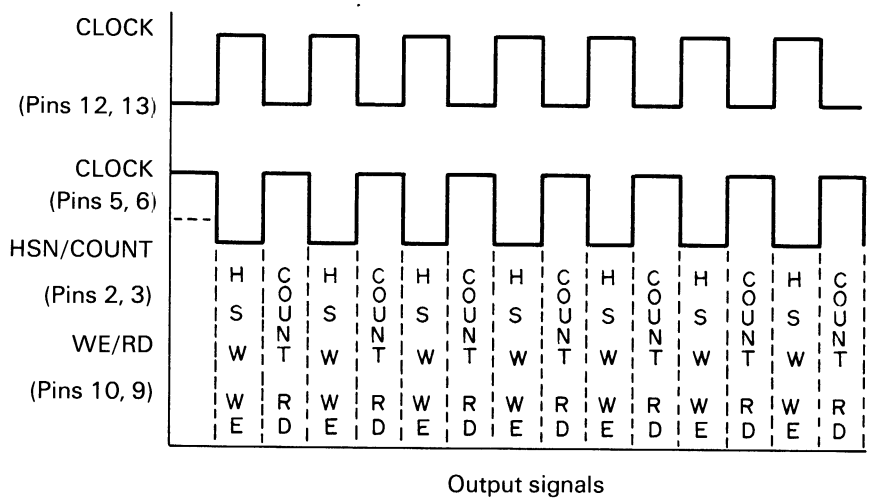


Fig. 4-19

4.2 ROM Cartridge

C MOS/N MOS ROM that has a pin arrangement compatible with the 2764 (8 KB), 27128 (16 KB), and 27256 (32 KB) as well as P-ROM can be placed in the ROM cartridge. The ROM cartridge offers various advantages, that is, the programs will not be damaged by an uncontrolled run because the programs and data are stored in the ROM; access time is far shorter than that of cassette tapes; and perfect read can be assured.

4.2.1 Theory of Operation

The ROM cartridge is connected to CN8 on the MOSU circuit board with the cable set No. 701. The ROM cartridge is controlled by the main CPU and slave CPU. The main CPU outputs addresses and reads data; and power is switched on or off, and the address counter and shift register are cleared by the slave CPU. Because programs or data are stored in files in the ROM cartridge, a file name must be designated in reading a program or data from the ROM cartridge.

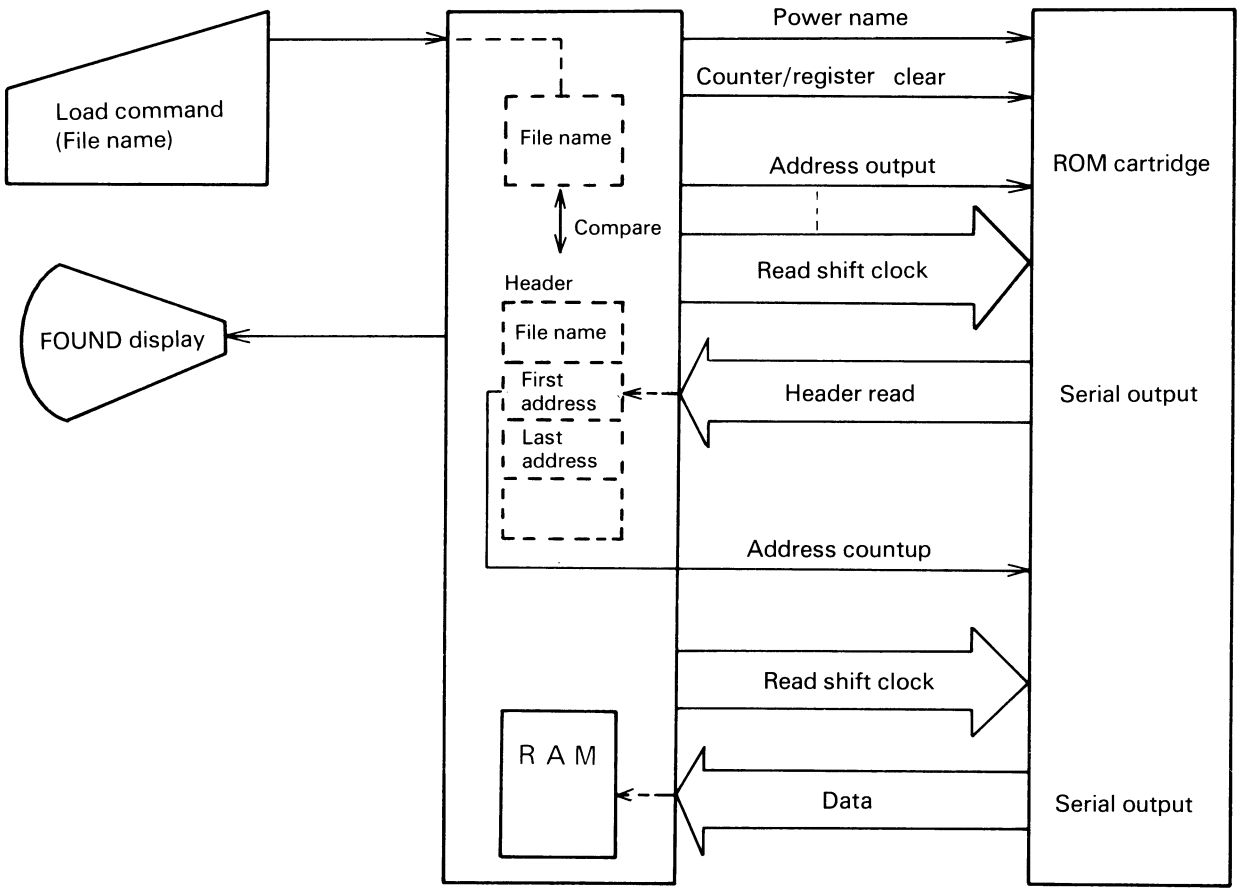


Fig. 4-20

First, when a load command (read) is excuted, the cartridge power is turned on, and the address counter and shift register are cleared. Then, the header data is read out of address 0000 in the form of serial data from the ROM cartridge by the address output and read shift clocks to the ROM cartridge. If the header has the file name that is designated by the load command, the data (with the first address) in the header is read into the system area of the RAM, and the word FOUND is displayed on the LCD screen. The operaton proceeds until the first address of the designated file is reached. When the first address of the designated file is reached, the read shift clocks are read, and the data is read into the main CPU in the form of serial data. (8 shift clocks are necessary for one byte of data.) This operation is continued until the last address, and the read data is converted into parallel data byte by byte, and then stored in the designated RAM address.

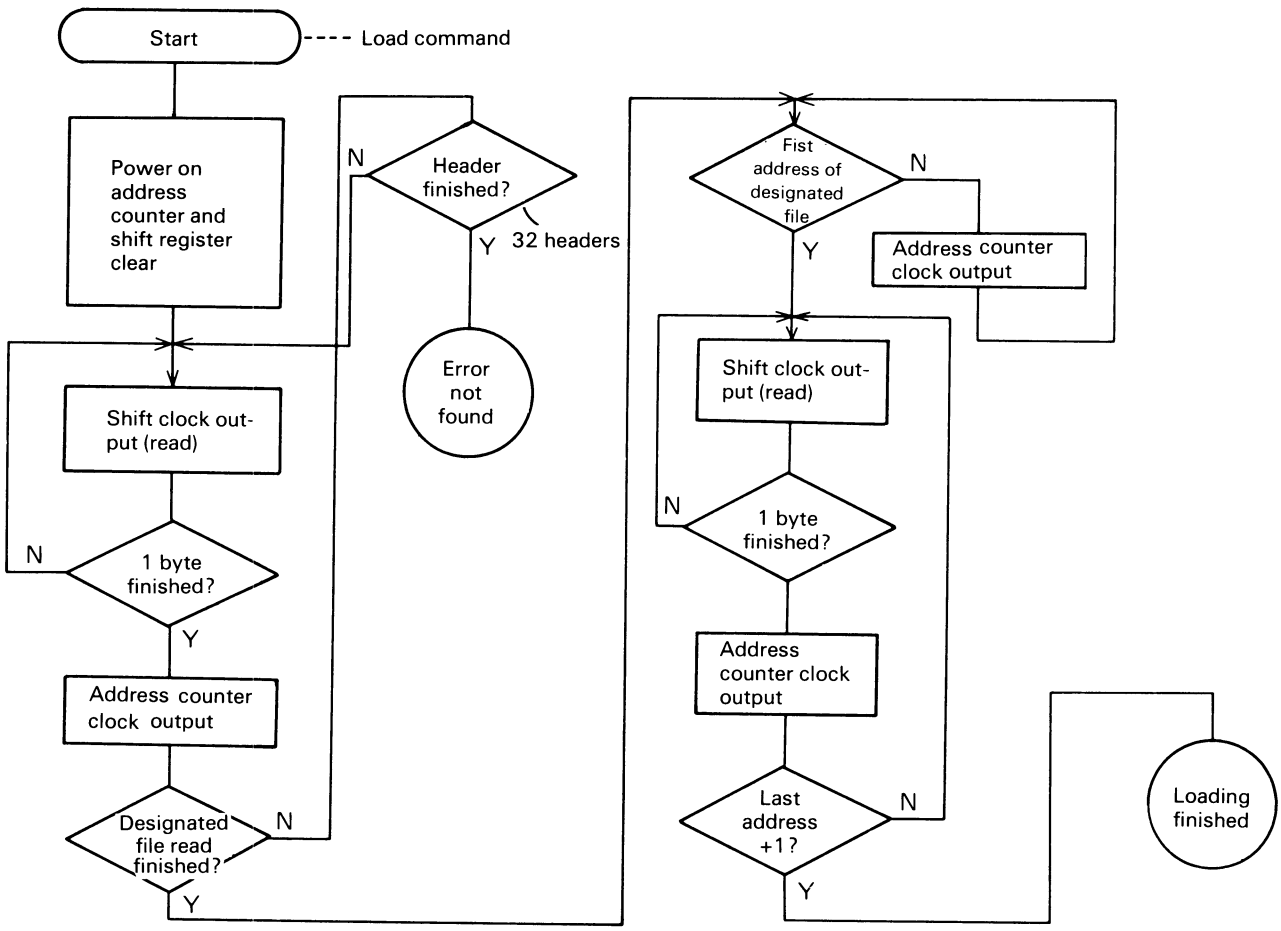


Fig. 4-21

4.2.2 ROM Format

The HX-20 uses the ROM cartridge as a sequential file so headers are employed in the first address part for the purpose of facilitating access to the files. Up to 31 headers can be used as desired.

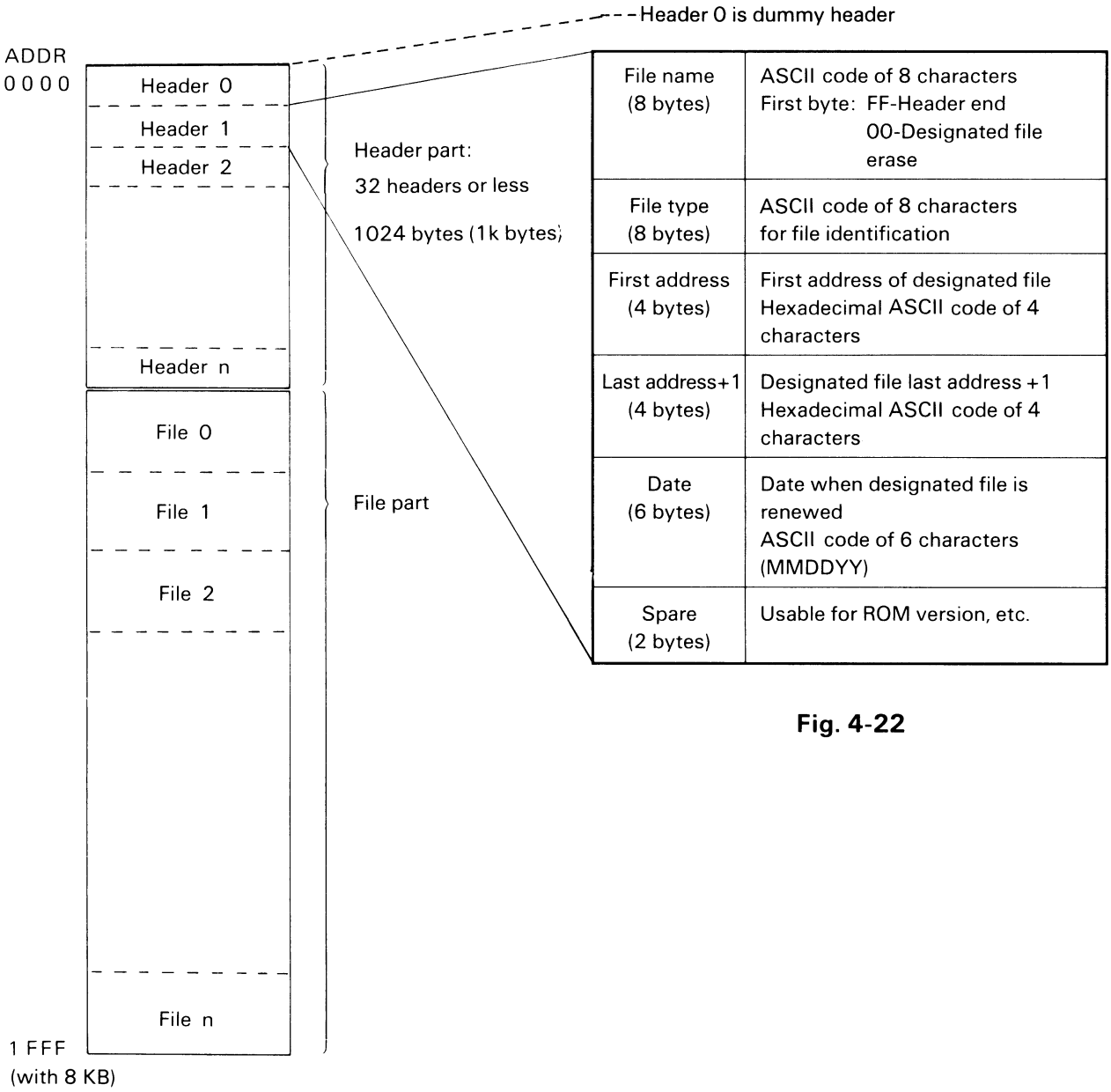


Fig. 4-22

4.2.3 Hardware Composition

The hardware consists of the power supply, address counter, shift register, and ROM.

Power supply:	After DC-DC conversion of voltage V_B, +5V is generated by a regulator.
Address couter:	Consists of two counter ICs, and can designate addresses up to 32 KB.
Shift register:	Converts the data read from ROM into serial data
ROM:	2764-pin compatible ROM

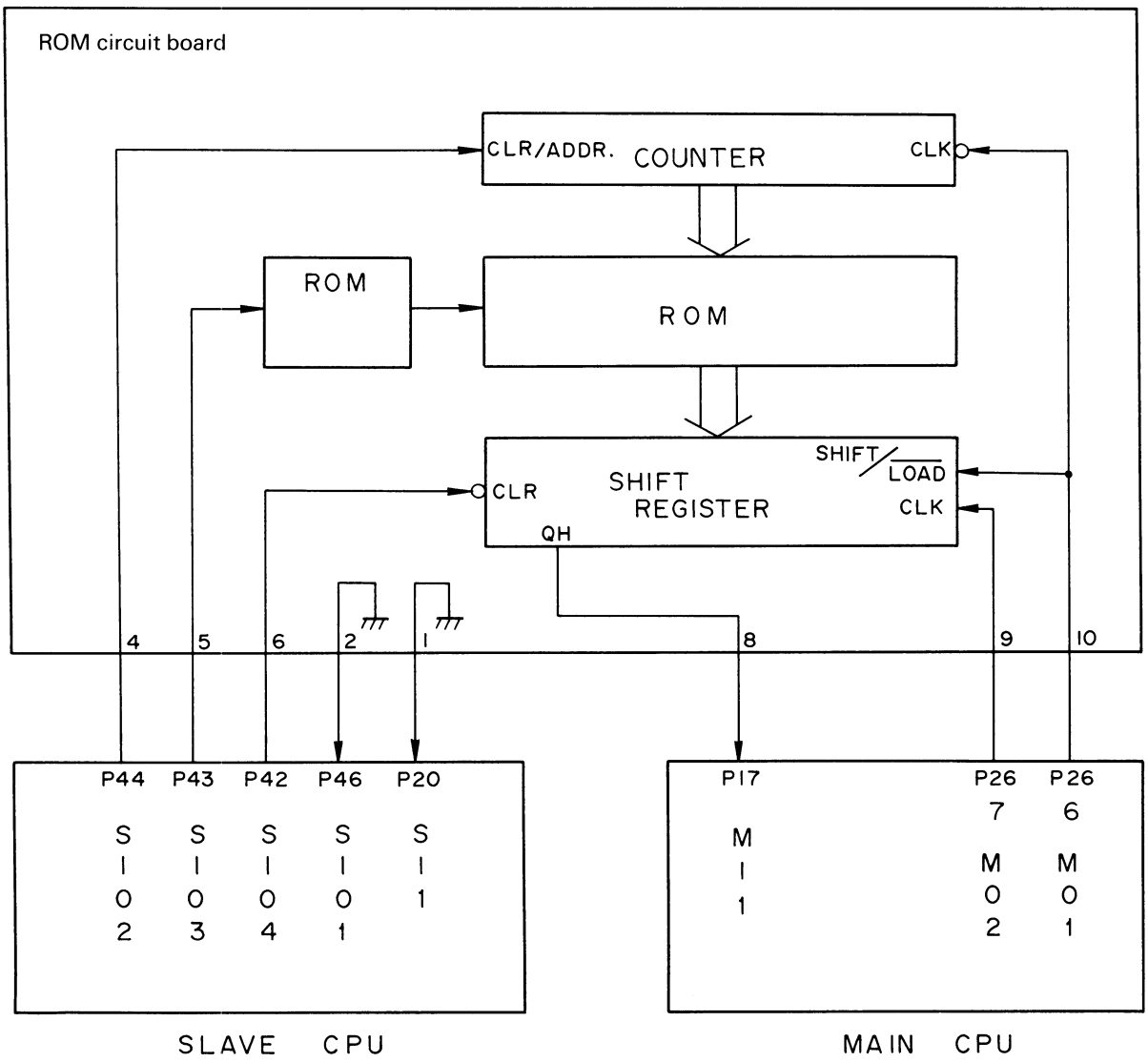


Fig. 4-23

4.2.4 Interface

The cable set No. 701 is used for connection to the MOSU circuit board.

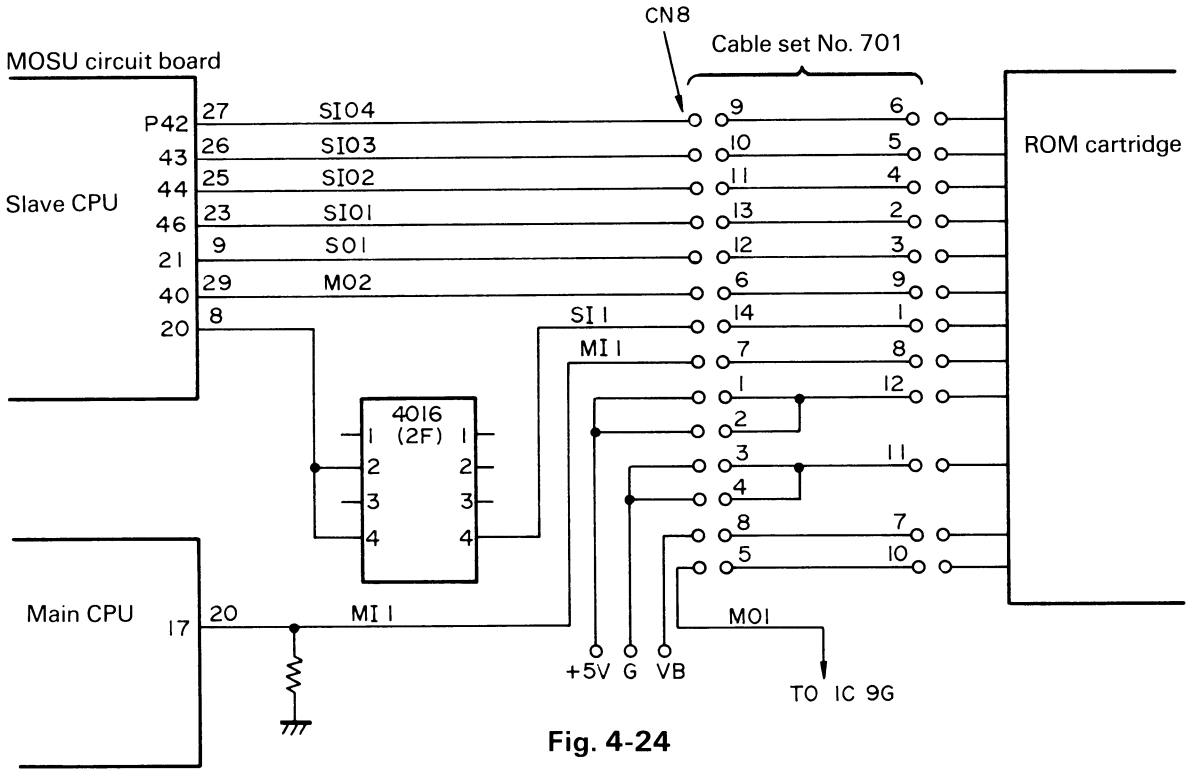


Fig. 4-24

Signal Pin No.	Signal	Signal Direction	Meaning of Signal
1 (14)	Si 1	In	ROM cassette judging input (always 0)
2 (13)	Sio 1	In	ROM cassette judging input (always 0)
3 (12)	So 1	–	Unused
4 (11)	Sio 2	Out	Address counter clear
5 (10)	Sio 3	Out	ROM power on
6 (9)	Sio 4	Out	Shift register clear (cleared by 0)
7 (8)	Mo 1	–	Battery power
8 (7)	Mi 1	In	Shift register output
9 (6)	Mo 1	Out	Shift register clock input
10 (5)	Mo 1	Out	Counter input (⌐↓_) Shift register shift/$\overline{\text{load}}$ switching
11 (4.3)	G	–	Ground
12 (2.1)	+5V	–	5V power (supplied by switching on)

Figures in parentheses indicate the pin numbers of CN8 on the MOSU circuit board.

Fig. 4-25

4.2.5 Power Supply

The power supply converts the battery voltage of VB (+5V) into a +8V, which is regulated into a stabilized voltage by a regulator and supplied to the circuits. This permits use of various types of ROMs compatible with the 2764 (ROMs with different loads can be used), and assures circuit voltage stability against load variation during operation

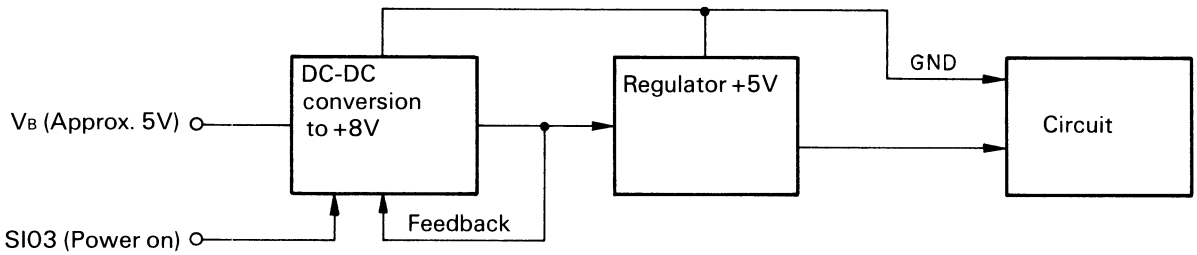


Fig. 4-26

(1) Power on

Power is turned on as the slave CPU on the MOSU circuit board sends an SI03 signal. This signal turns on transistor Q3, causing transistor Q2 to turn on. Transistor Q2 outputs the voltage VB from its collector to Pin 14 (Vcc) of the TL 497 to drive it, and a switching pulse is generated from it by an external capacitor C9. Transistor Q1 outputs the voltage VB (about 5V), which is supplied to capacitor C1 and regulator SR1 via R2, T1 and D1.

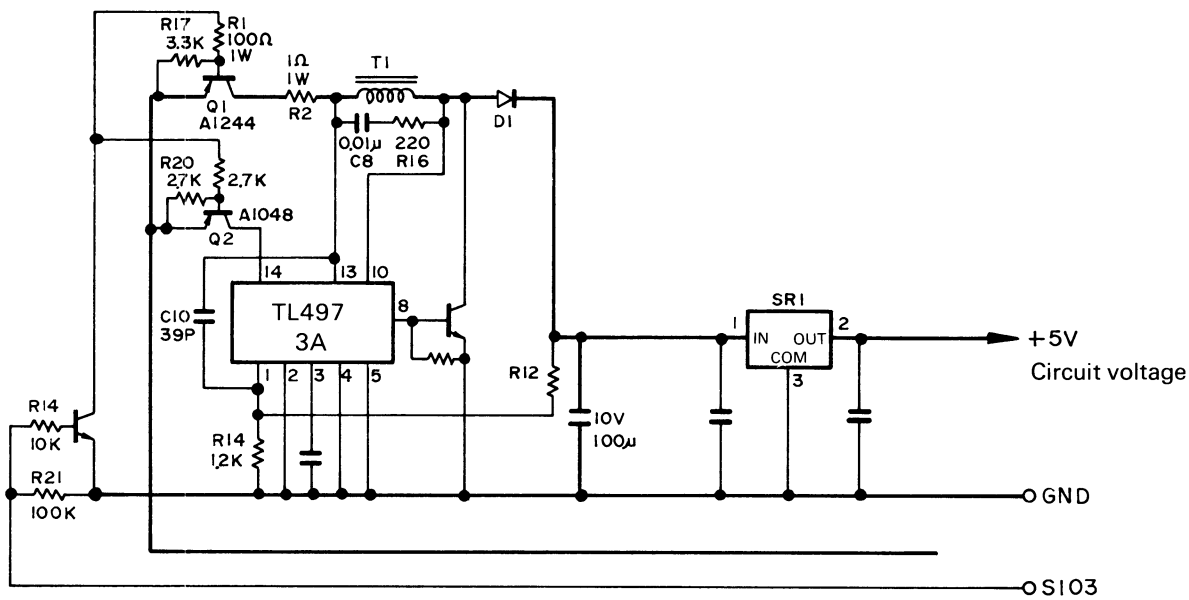


Fig. 4-27

(2) Voltage conversion (DC-DC conversion from +5V to +8V)

After power is turned on, the dividing circuit (R13: 6.8 kilohms; R14: 1.2 kilohms) on the cathode side of diode D1 divides the output voltage, and a feedback voltage is returned to the comparator input of the TL 497. The TL 497 generates a voltage of 1.2V as a compare voltage inside. This voltage is compared with the feedback voltage to the comparator input. If the feedback voltage is less than 1.2V, the oscillator circuit is put into operation to send a switching pulse to Pin 8 of the TL 497. If the feedback voltage is more than 1.2V, no switching pulse is sent out.

(+8V is the rated voltage on the cathode side of diode D1, and is divided by 6.8 kilohm and 1.2 kilohm resistors for detection of 1.2V level.)

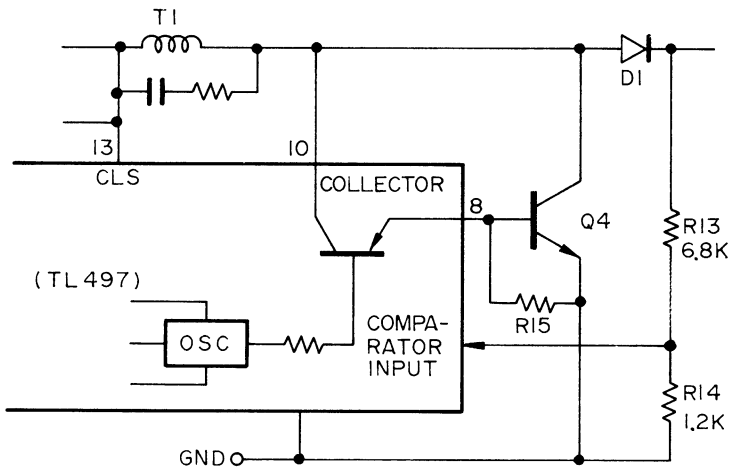


Fig. 4-28

When transistor Q4 receives a switching pulse from Pin 8 of the TL 497, the collector (V_B) is momentarily (for switching pulse on time) shorted with the emitter (GND) so that a large current momentarily runs to the ground via coil T1. As a result, electric energy is stored in coil T1. The stored energy is released during the switching pulse off time. Thus, a waveform such as shown in Fig. 4-29 is supplied from diode D1 to capacitor C1, where it is smoothed into a +8V.

C8 and R16 that are connected parallel to coil T1 are for preventing the generation of counterelectromotive force after coil energy release.

Regulator SR1 is a +5V regulator, which generates a +5V from the input voltage of +8V, and supplies it to the circuits.

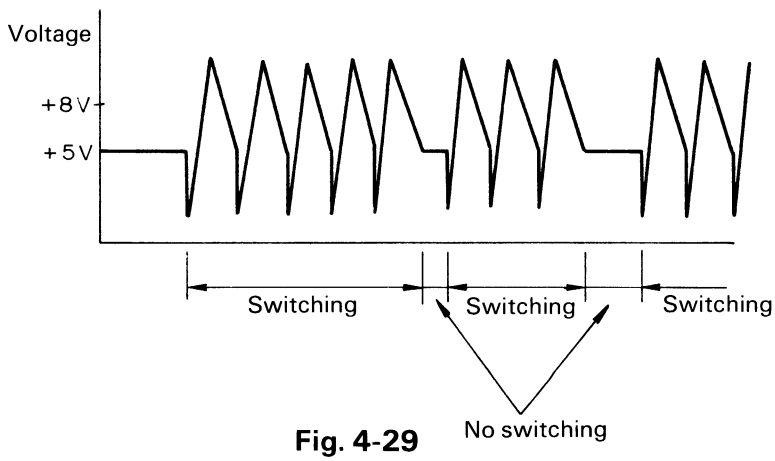


Fig. 4-29

4.2.6 Address Counter

The address counter uses two counter ICs, and designates addresses in sequence from the lowest, using MO1 signals. It is necessary, therefore, to continuously output address shift pulses (MO1 signals) until the first address of the designated file is reached even after header read. (This is because random address designation cannot be made.)

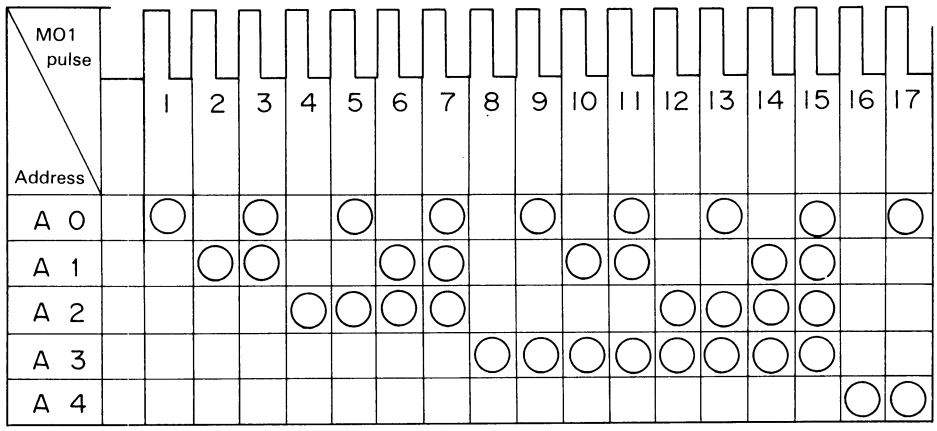


Fig. 4-30

4.2.7 Shift Register

The shift register reads 1 byte from the ROM, and reads it out to the serial data line MI1 bit by bit, using a shift clock signal MO2.

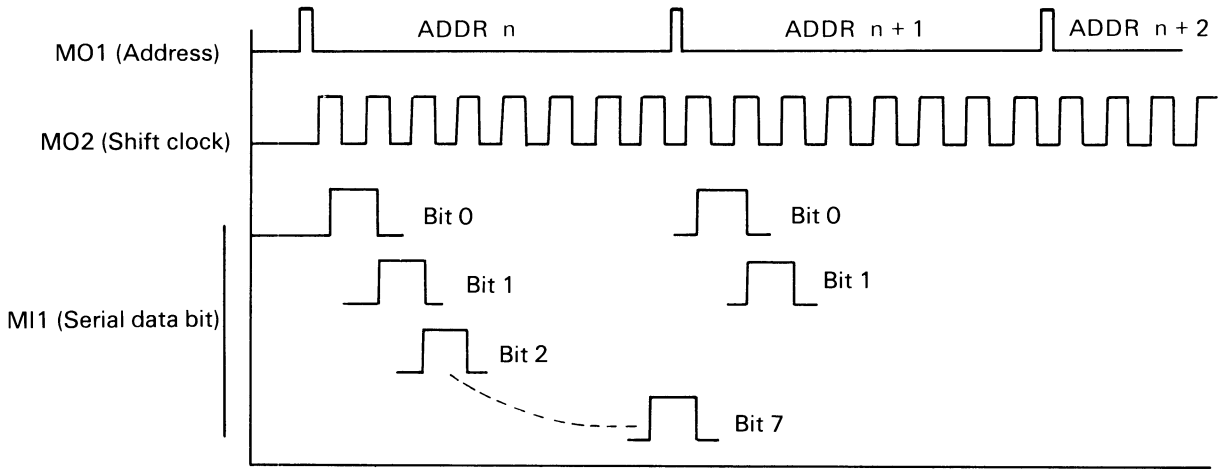


Fig. 4-31

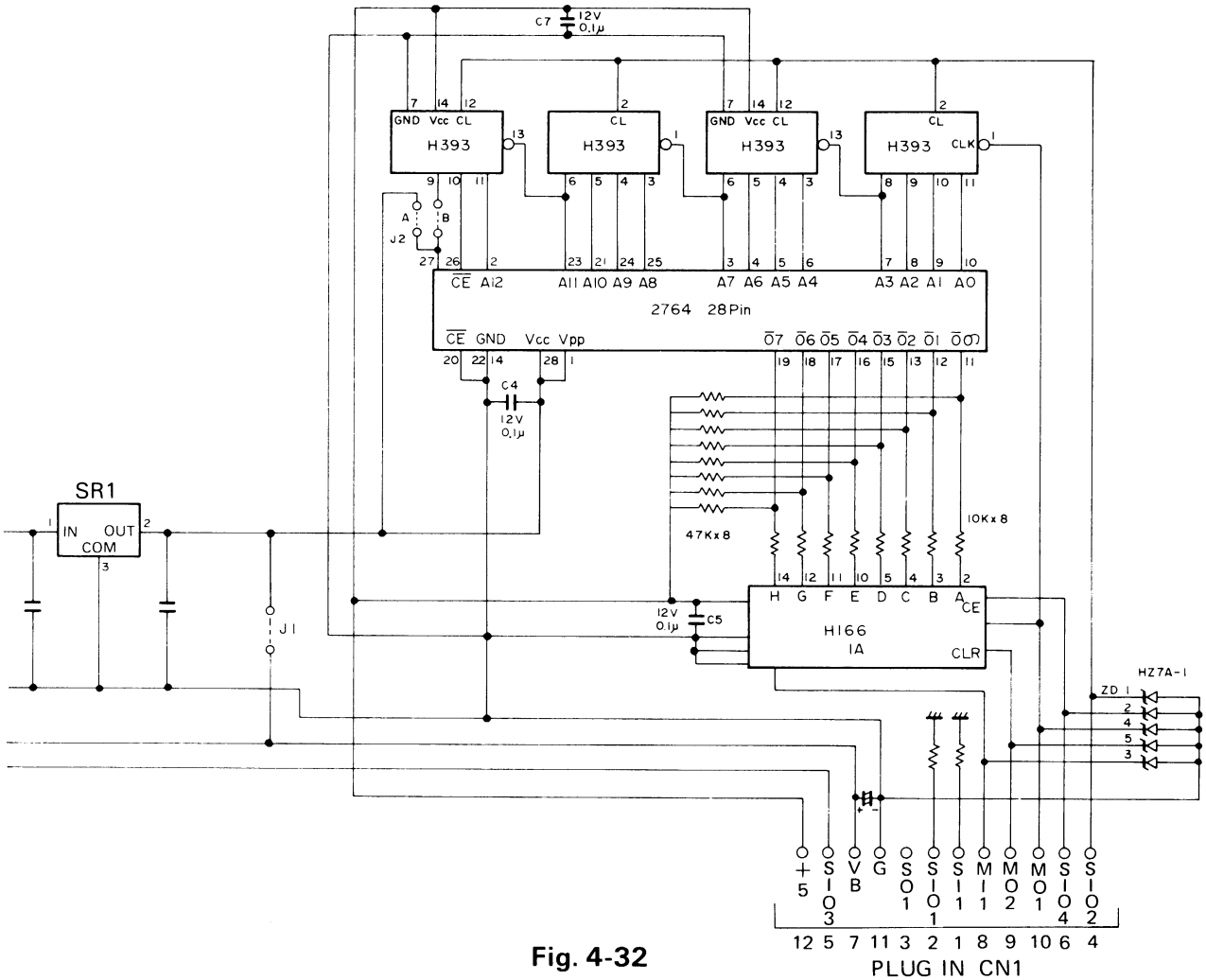


Fig. 4-32

4.2.8 ROM Jumpers

ROMs compatible with the 2764 (8 KB) can be used so that the jumpers on the circuit board must be reconnected as shown in the table below according to the kind of ROM (C-MOS, low power consumption; other than C-MOS, high power consumption) and capacity (8k, 16k, 32k).

Type / Capacity / Jumper	C-MOS		Non-C-MOS	
	8k or 16k bytes	32k bytes	8k or 16k bytes	32k bytes
J1	ON	ON	OFF	OFF
J2-A	ON	OFF	ON	OFF
J2-B	OFF	ON	OFF	ON

* If jumper J1 is on, voltage V_B is shortened with the output of regulator SR1 so power can be saved, but load variation will directly affect the battery voltage.

Fig. 4-33

4.2.9 Microcassette Identification

Identification is made by checking the levels of three signals as shown in the table below.

	MI 1 Main P17	SI 1 Slave P20	SI 01 Slave P46
ROM cartridge	LOW	LOW	LOW
Microcassette	HIGH	–	–
Spare	LOW	LOW	HIGH
Spare	LOW	HIGH	HIGH
NON OPTION CARTRIDGE	LOW	HIGH	LOW

Fig. 4-34

4.3 Expansion Unit

The expansion unit is used for additional installation of RAMs and ROMs in the HX-20, and can be attached to the expansion unit interface (CN7) for the HX-20. The expansion unit can mount RAMs and ROMs up to 32k bytes maximum, and is normally equipped with 16k bytes of RAMs. In mounting additional ROMs, part or all of the RAMs (16k bytes) that are the standard equipment of the expansion unit can be ignored by resetting the DIP switches and jumpers.

Thus, RAMs and ROMs can be added as suitable to a specific application.

Features of Expansion Unit

- The interface outputs address bus (16 lines), data bus (8 lines) and R/W signals in parallel so that the main CPU of the HX-20 can make direct access to the memories.
- No special power supply is required for the expansion unit because all the power that is necessary to drive it is supplied from the HX-20.
- The RAM area in the expansion unit can be backed up by the built-in batteries in the HX-20 so that, even if power is turned off, the programs (data) sotred in the RAMs of the expansion unit can be protected similar to the RAMs in the HX-20.
- Part of the RAM addresses and part or all of the ROM addresses in the expnasion unit overlap with the ROM addresses in the HX-20, so the addresses in the HX-20 and in the expansion unit are separately used through bank switching.

4.3.1 Hardware Composition

(1) The expansion unit consists of ROM and RAM select circuits and a bank control (bank switching) circuit. Fig. 4-27 shwos a block diagram of the expansion unit.

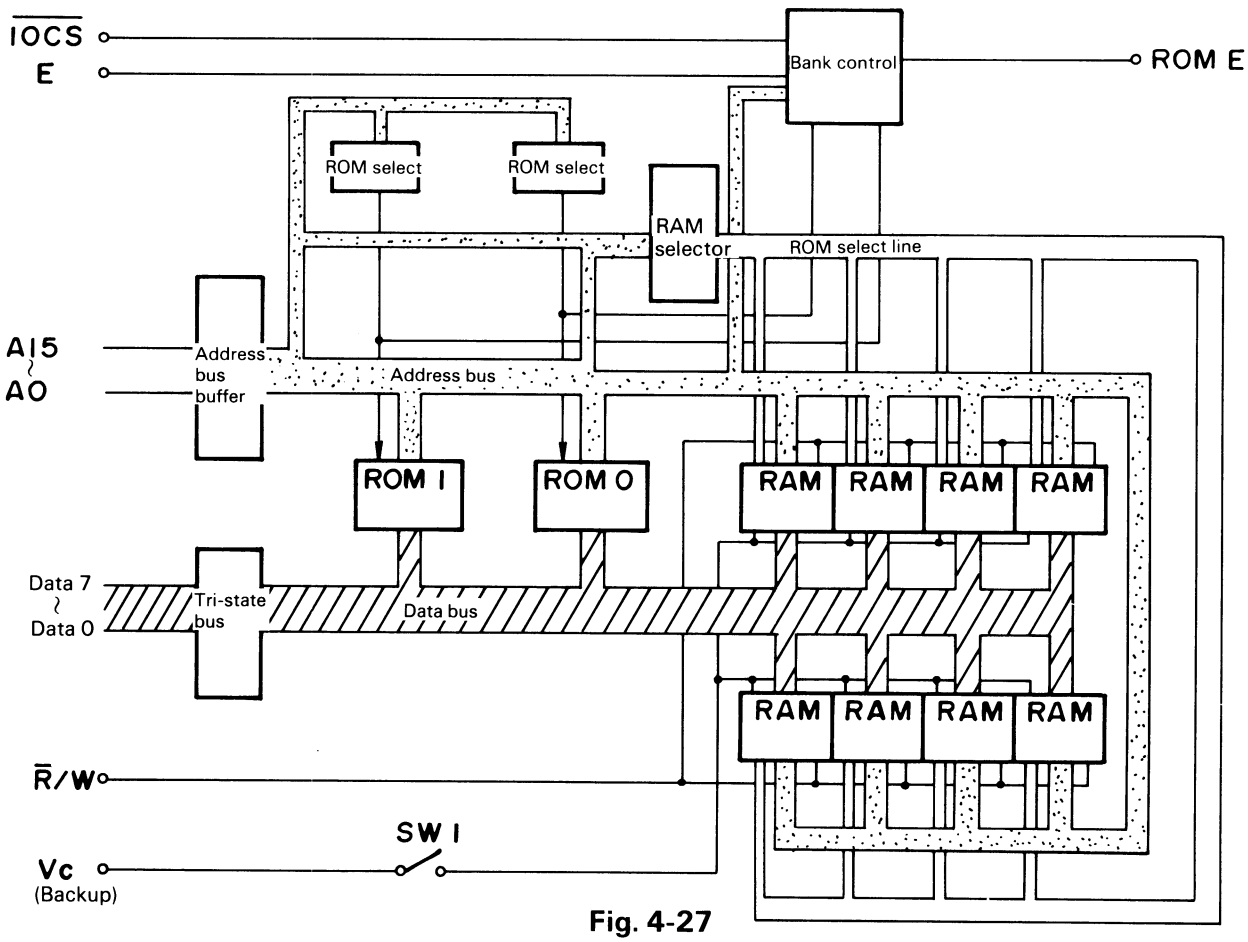
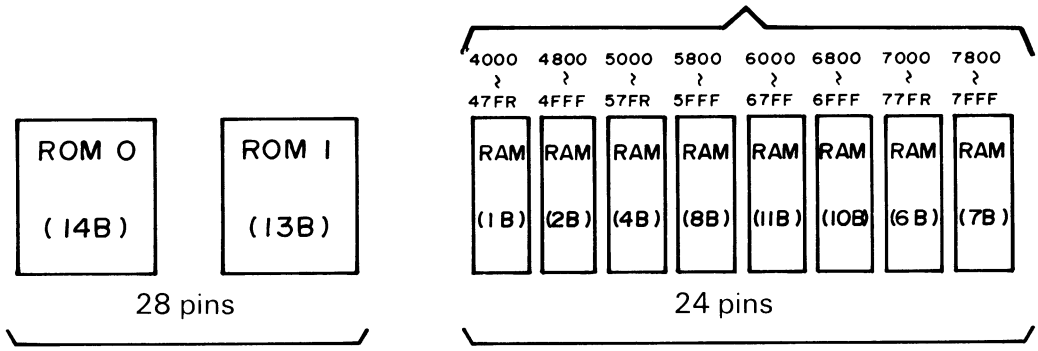


Fig. 4-27

(2) Expansion IC Socket

The expansion unit is normally equipped with 16k bytes of RAMs, and also has two 28-pin IC sockets for ROMs.



ROMs: 8k or 16k bytes each

RAMs: 2k bytes

(2) RAM and ROM Composition

A total of 32k bytes maximum of RAMs and ROMs can be installed. ROM/RAM areas and types of ROMs (8KB/16KB) can be selected by means of the jumpers (J1, J2) and DIP switch (SW2) shown below.

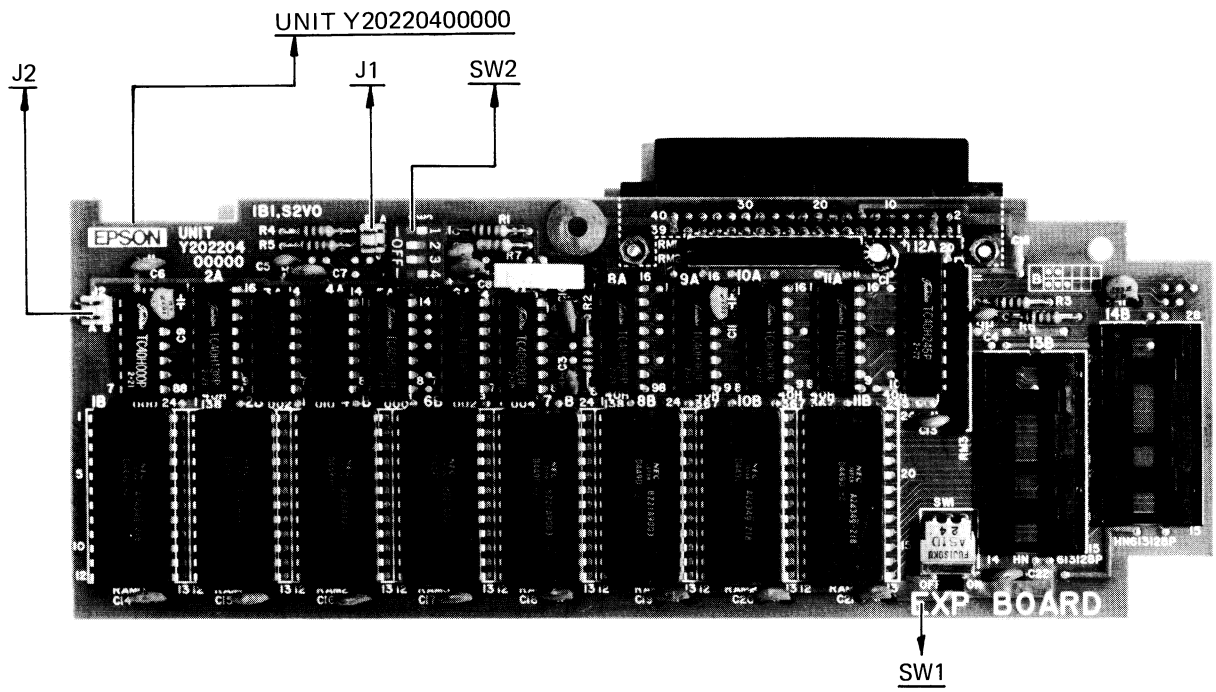


Fig. 4-28

4.3.2 ROM/RAM Select Circuits

● ROM select

Two expansion ROMs can be installed. ROM 0 (14B) is for the higher addresses, and ROM 1 (13B) for the lower addresses.

ROM addresses vary with ROM capacity (8k or 16k bytes) and quantity (1 ROM or 2 ROMs) so the circuit shown in Fig. 4-29 involving address A15 to A13, DIP switch (SW2) and jumper (J1/J2) is used for ROM selection.

For setting the DIP switch and reconnecting the jumper, refer to 4.3.3 Bank Switching and 4.3.5. Jumper (J1/J2) and DIP switch (SW1/2) Setting

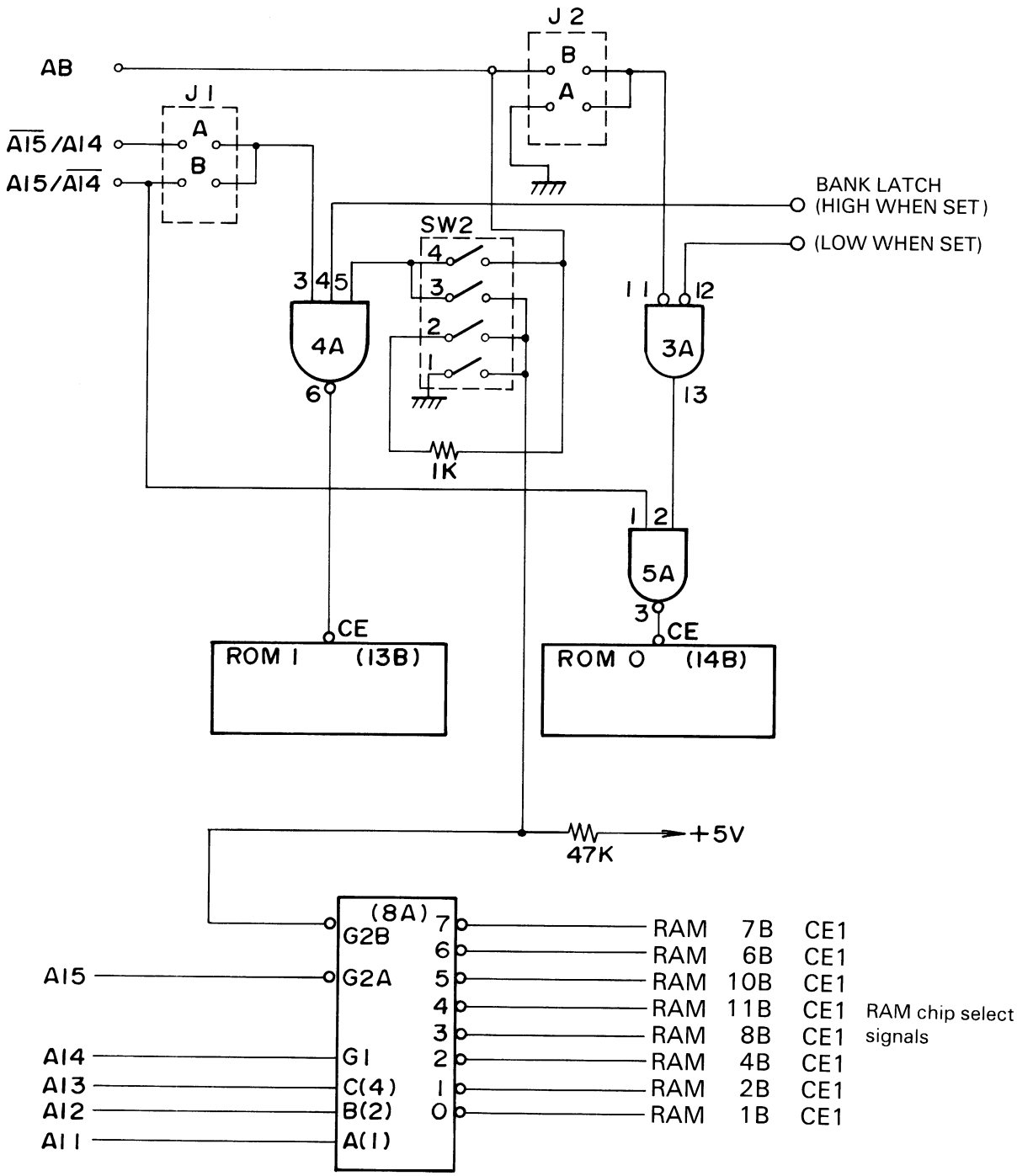


Fig. 4-29

● RAM selecting

RAM selection is basically performed by a decoder (IC 8A) using address lines A11 to A15. It is also controlled on the basis of DIP switch 2 setting because the range of addresses to be used must be changed depending on combination with ROMs.

Location	Address line					RAM address range
	15	14	13	12	11	
1B		○				4000 ~ 47FF
2B		○			○	4800 ~ 4FFF
4B		○		○		5000 ~ 57FF
8B		○		○	○	5800 ~ 5FFF
11B		○	○			6000 ~ 67FF
10B		○	○		○	6800 ~ 6FFF
6B		○	○	○		7000 ~ 77FF
7B		○	○	○	○	7800 ~ 7FFF

Note

○: HIGH

(Meanings of Jumpers and DIP Switch)

- SW2 bits 1 and 2 allocate ROM and RAM areas.
- SW2 bits 3 and 4 and jumpers J1 and J2 select a ROM capacity (8KB/16KB).

* Part or all of the 16k bytes of RAMs installed can be ignored by setting SW2 and the jumpers mentioned above.

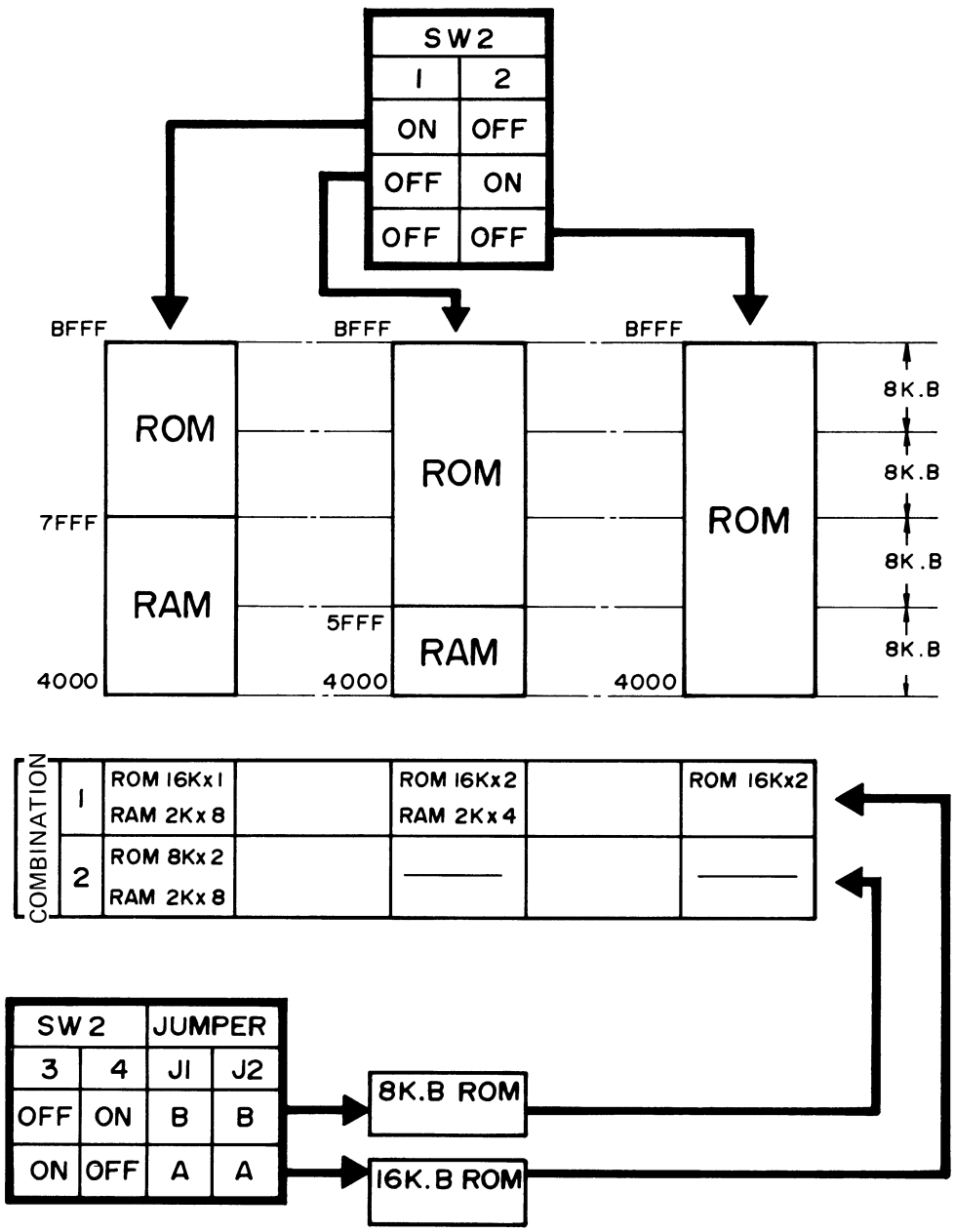


Fig. 4-30

4.3.3 Bank Switching

The HX-20 can directly select addresses up to 64k bytes (65,536 addresses). If the expansion unit is used, the total memory capacity of ROMs and RAMs may exceed 64k bytes. However, the HX-20 can make access to memories having the same logic address through bank switching.

Memory selection by bank switching is done by hardware and sorfware. Since the HX-20 operates in the multiplexed/RAM mode, it can use external memories for addresses 00FF to FFFF. Thus, the addresses 4000 to BFFF (32k bytes in total) in the external memory area can be used through bank switching. Memory selection can also be made by turning off the standard equipment ROMs (addresses 8000 to FFFF) in the HX-20 with the control signal ROM E.

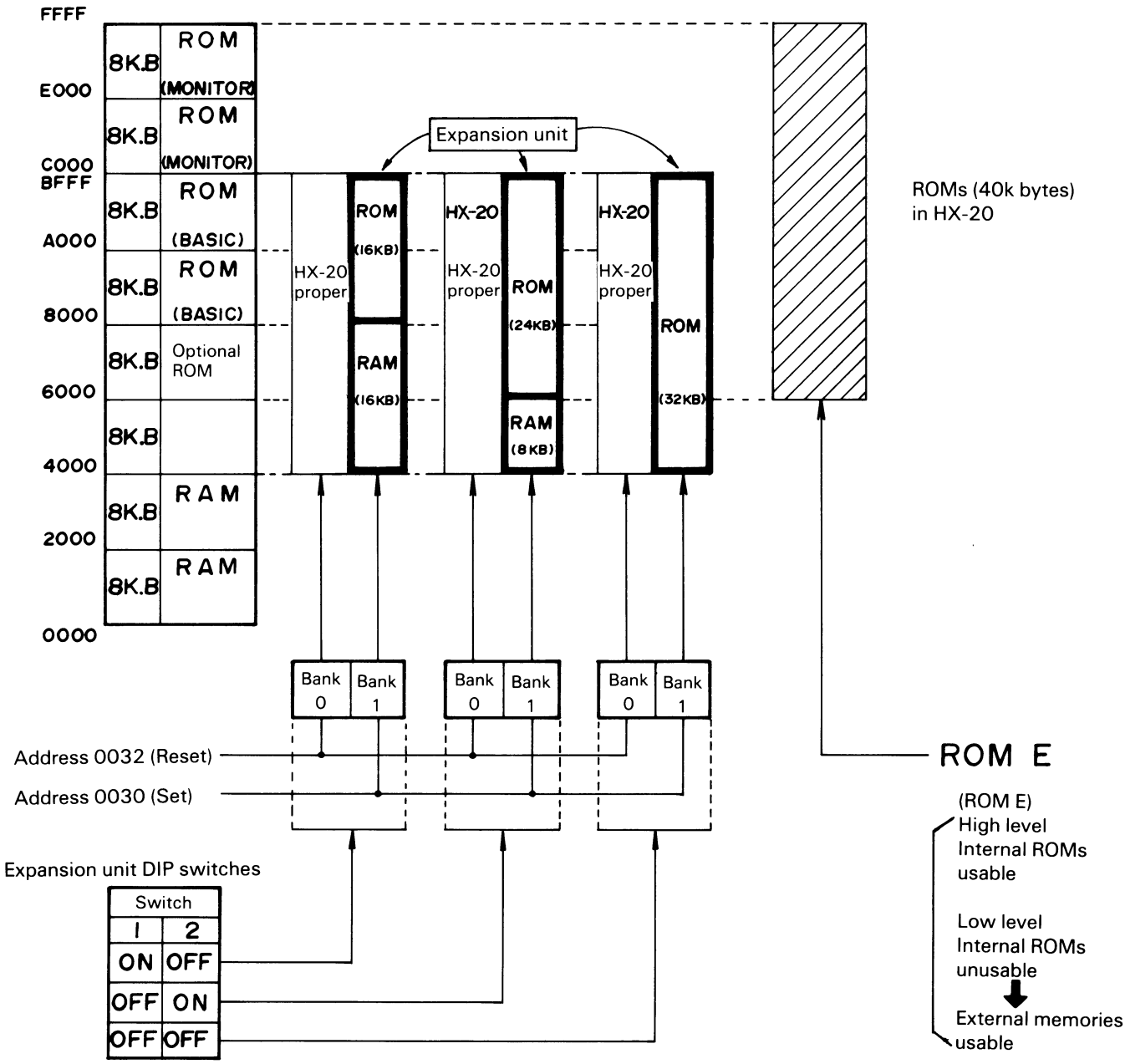


Fig. 4-31

● Bank switching is performed by a bank latch that uses address 0030 and 0032 and the ROM E signal based on control of address 14 and 15.

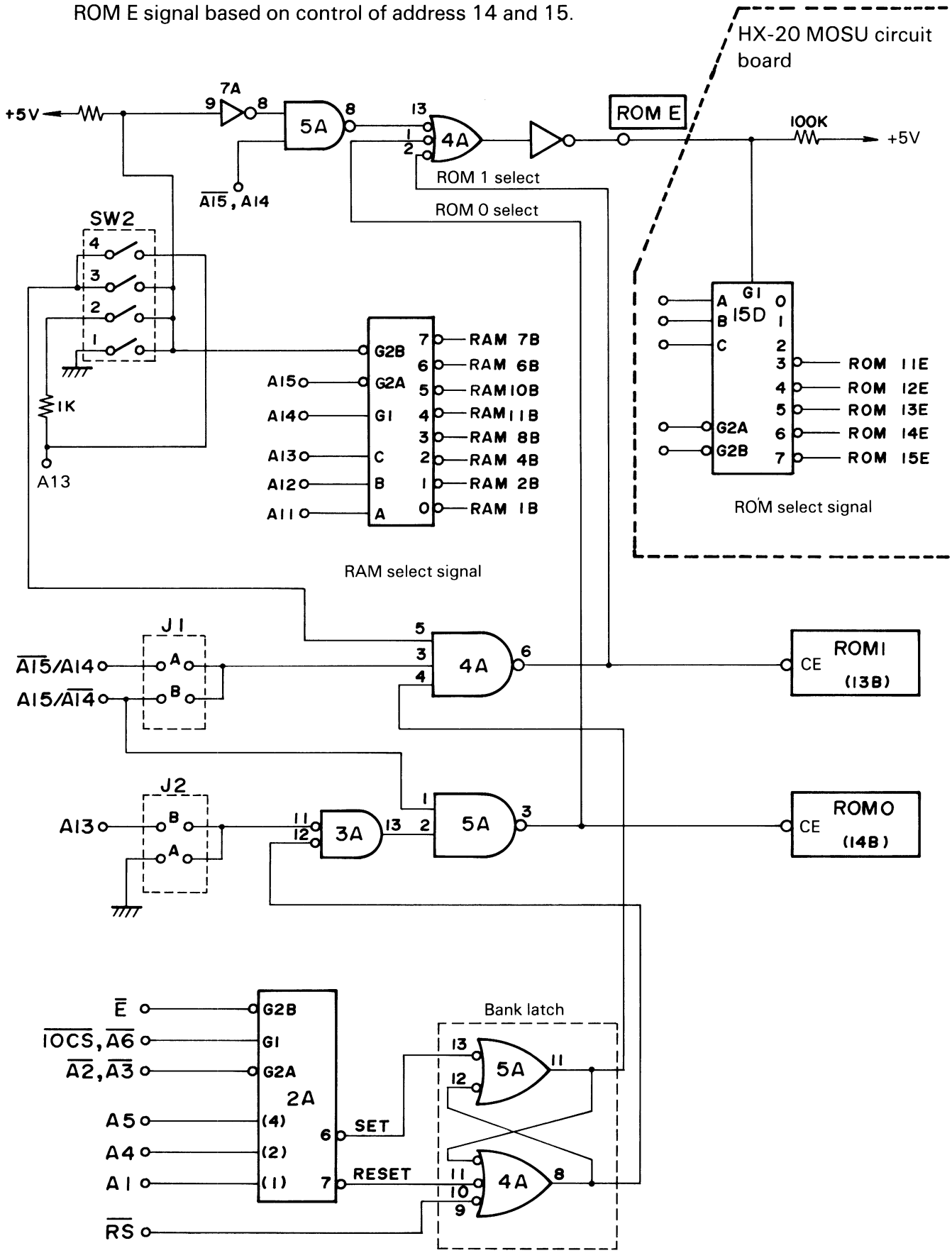


Fig. 4-32

(Bank Latch)

When the HX-20 is switched on, a reset signal ($\overline{RS}$) resets the latch. Thus, Pin 11 of IC 5A is low, and Pin 8 of IC 4A is high so that the expansion unit outputs none of its ROM 0/1 select and ROM E signals.

If address 0030 is output under this condition, the output from Pin 6 of IC2A goes low at the E (enable) timing to set the bank latch. That is, Pin 11 of IC5A goes high, and Pin 8 of IC4A goes low to permit outputting of ROM 0/1 select and ROM signals.

Bank switching from the expansion unit to the HX-20 proper can be made by outputting address 0032 to turn Pin 7 of IC2A low and reset the bank latch.

* The $\overline{IOCS}$ signal to be input to G1 of IC2A is output by $\overline{A7 \sim A15}$.

(ROM E Signal)

The ROM E signal is output from the expansion unit to the HX-20. It is connected to G1 of the ROM selector (IC15D on the MOSU circuit board) in the HX-20.

When no bank switching is under way, the ROM E signal is high so that the internal ROMs (addresses 6000 to FFFF) in the HX-20 are selected.

If address 0030 is output to select ROM 0 or ROM 1 in the expansion unit for bank switching, or if any RAM address over 6000 is selected, the ROM E signal goes low to inhibit access to the internal ROMs in the HX-20.

- Bank switching { Set by address 0030 / Reset by address 0032
- Bank switching signal: ROM E

ROM E Signal Output Conditions

		Case 1		Case 2				Case 3		
		1	2	1	2	3	4	1	2	3
Address	15	HIGH	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	LOW
	14	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH	HIGH	HIGH
	13	HIGH	–	–	HIGH	–	HGIH	LOW	–	LOW
J1	A	–	YES	–	–	YES	YES	–	–	–
	B	YES	–	YES	YES	–	–	–	–	–
J2	A	–	YES	–	–	YES	YES	–	–	–
	B	YES	–	YES	YES	–	–	–	–	–
SW2	1	–	–	–	–	–	–	–	ON	–
	2	–	–	–	–	–	–	ON	–	–
	3	–	–	ON	–	ON	–	–	–	ON
	4	–	–	–	ON	–	ON	–	–	ON
Address 0030		YES	YES	YES	YES	YES	YES	–	–	–

The ROM E signal can be output under nine conditions.

Case 1: When ROM 0 (14B) in the expansion unit is selected

(1) Addresses 15, $\overline{14}$

(2) Bank 1 select (address 0030)

(3) Address 13 (when J2 = B)/or J2 = A

Case 2: When ROM 1 (13B) in the expansion unit is selected

(1) Address 15, $\overline{14}$ (when J1 = B)/or addresses $\overline{15}$, 14 (when J1 = A)

(2) Bank 1 select (address 0030)

(3) Address 13 (SW2-4 on)/or SW2-3 on

Case 3: When an address over 6000 in the expnasion unit's RAM is selected

(1) Addresses $\overline{15}$, 14

(2) Address $\overline{13}$ (SW2-2 on)/or address $\overline{13}$ (SW2-3, SW2-4 on), or SW2-1 on

4.3.4 Interface

- The data buses have IC12A (tri-state output), which switches data bus direction with read and write signals.

  If the $\overline{\text{ROM E}}$ signal is high at the E (enable) signal timing, data bus direction is switched by R/W signal timing.

(IC12A H245)

Read	A	←	B
Write	A	→	B

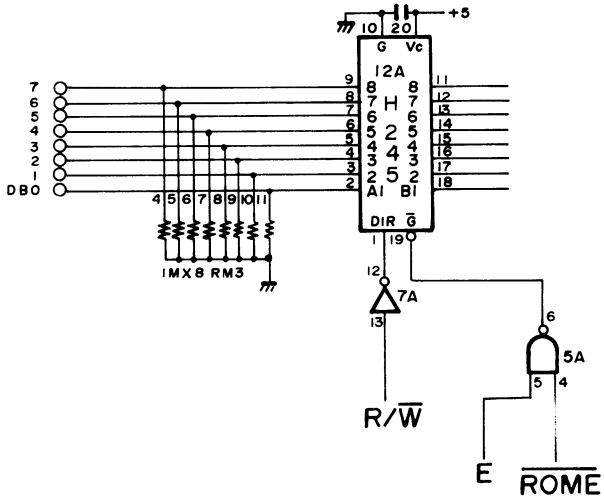
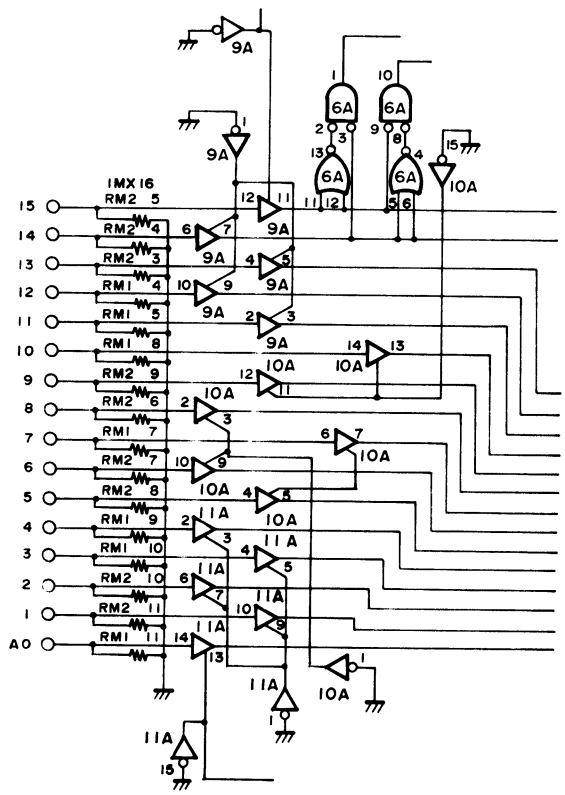


Fig. 4-33



4-34

- Address buses

  Address buses output addresses to each element via bus drivers IC9A, IC10A, and IC11A, which are connected so that each gate may be normally on. Thus, these ICs are immediately ready for operation when a +5V is supplied as power is turned on.

4.3.5 Jumper (J1/J2) and DIP Switch (SW1/2) Setting

- Part or all of the standard equipment of 16k bytes of RAMs can be ignored or replaced with ROMs by reconnecting the jumpers or setting DIP switches. Therefore, the expansion memory area can be used as shown in the table below without changing the standard equipment of 16k bytes of RAMs in the expansion unit.

				ROM/RAM combination in expansion unit					
Address			Standard	16KB ROM × 2	16KB ROM × 2 2KB RAM × 4	16KB ROM × 1 2KB RAM × 8	8KB ROM × 2 2KB RAM × 8	8KB ROM × 2	8KB ROM × 2 2KB RAM × 4
FFFF E000	8K (64)	ROM (MONITOR) 15E		–	–	–	–	–	–
DFFF C000	8K (56)	ROM (UTILITY) 14E		–	–	–	–	–	–
BFFF A000	8K (48)	ROM (BASIC) 13E		ROM 0 (14B)	ROM0 (14B)	ROM 0 (14B)	ROM 0 (14B)	ROM 0 (14B)	ROM0 (14B)
9FFF 8000	8K (40)	ROM (BASIC) 12E					ROM 1 (13B)	ROM 1 (13B)	ROM 1 (13)
7FFF 6000	8K (32)	(Optional ROM)		ROM 1 (13B)	ROM 1 (13B)	RAM (11B,10B,6B,7B)	RAM (11B,10B,6B,7B)		
5FFF 4000	8K (24)				RAM (1B,2B,4B,8B)	RAM (1B,2B,4B,8B)	RAM (1B,2B,4B,8B)		RAM (1B,2B,4B,8B)
3FFF 2000	8K (16)	RAM 16C,15C,14C,13C		–	–	–	–	–	–
1FFF 0000	8K	RAM 12G,13G,14G,15G		–	–	–	–	–	–
Setting inside expansion unit		1	–	OFF	OFF	ON	ON	OFF	OFF
	SW2	2	–	OFF	ON	OFF	OFF	OFF	ON
		3	–	ON	ON	ON	OFF	OFF	OFF
		4	–	OFF	OFF	OFF	ON	ON	ON
	Jum-	J1		A	A	A	B	B	B
	per	J2		A	A	A	B	B	B

* The expansion unit is originally set as follows before shipment form the factory.

Jumpers { J1 : B ; J2 : B }

DIP switch (SW2) { 1 : ON ; 2 : OFF ; 3 : OFF ; 4 : ON }

- SWTCH 1 (SW1) turns on and off the Vc voltage line through which Vc voltage is supplied from the HX-20. The Vc voltage line carries a voltage of approximately +5V when power is on, and drives the elements connected to the Vc line.
  The Vc voltage line also outputs a voltage of approximately +3V when power is off so that it may also be used for memory backup. The eight RAMs and IC1A in the expansion unit use this Vc voltage, which protects the data stored in the RAMs, and controls the RAM CE2 signal and reset signal.
  * Be sure to set this switch to the ON position before use.

4.4 Display Controller

The display controller is connected to the HX-20 with a serial interface. Displayed data and control commands are serially transferred. Transferred data are converted into parallel data, and the commands are stored in the RAM (stack area) of the CPU and the data in the V-RAM. Then, the data stored in the V-RAM are read out by VDG (video display generator), which controls the display and outputs the data to the RF modulator. As a result, the display controller outputs composite or RF display signals to show them on the screen.

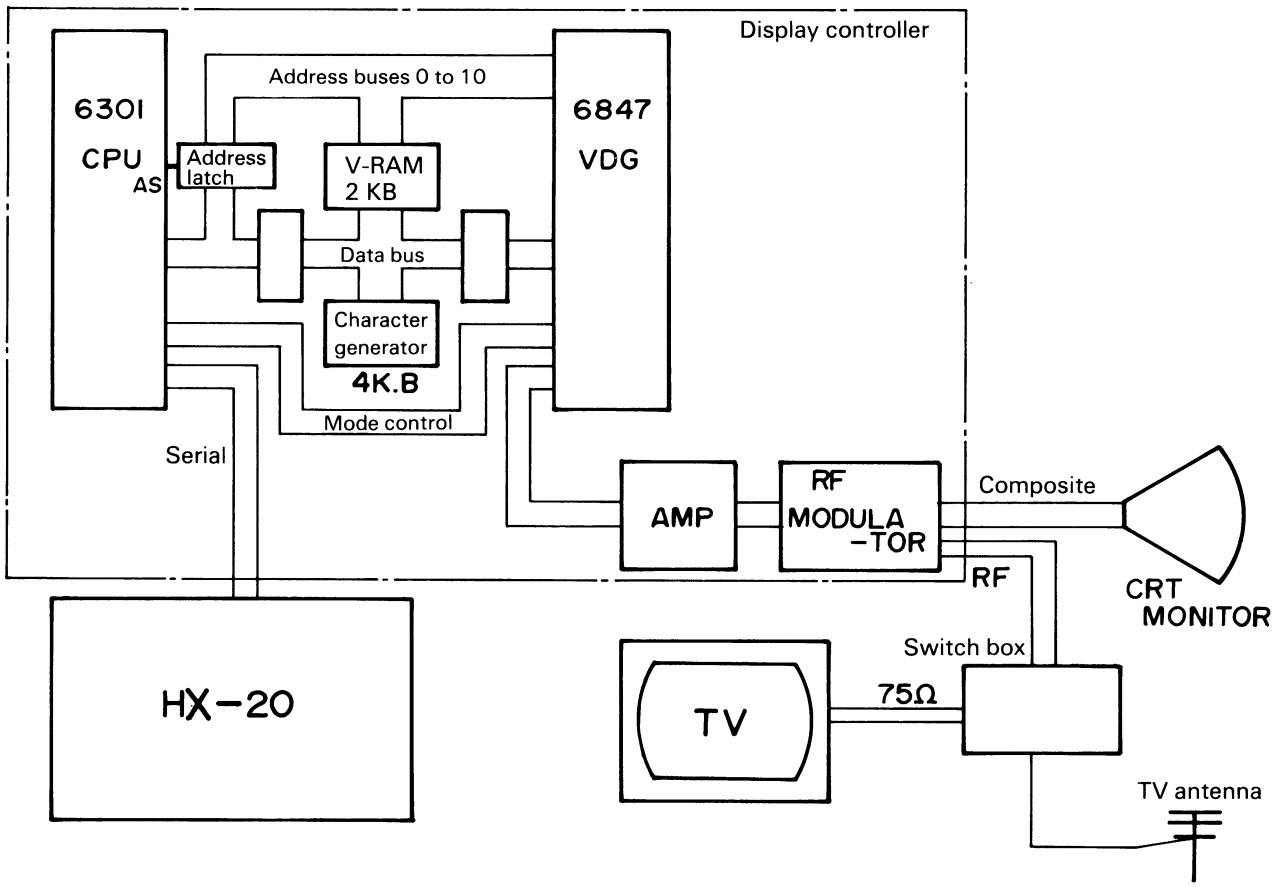


Fig. 4-35

Note: RF modulator output impedance is 75 ohms so that converter (75 ohms to 300 ohms) may be necessary when connecting with a monitor or a TV set.

4.4.1 Display Modes

- The main display modes are the text mode (alphanumeric mode) and the graphic mode. This equipement uses the three modes shown below.

Mode	Input terminal									Display		Color		
	$\overline{MS}$	$\overline{A}$/G	$\overline{A}$/S	$\overline{INT}$/EXT	GM2	GM1	GM0	CSS	INV	Mode	Description	Character	Background	Border
External alphanumeric mode	1	0	0	1	×	×	×	0	0	32 characters ×16 lines	8×12 dots/character	Green Black Orange Black	Black Green Black Orange	Black
									1					
								1	0					
									1					
128 × 96 graphic mode	1	1	×	×	0	1	1	0	×	128×96 picture elements	–	0: Black,1: Green 0: Black, 1 : White		Green White
								1						
128×64 color graphic mode	1	1	×	×	0	1	0	0	×	128×64 picture elements	–	* Refer to 4.4.3		Green White
								1						

- The screen display area is 256 dots maximum in the horizontal direction and 192 dots maximum in the vertical direction, but the usable area varies depending on the display modes.

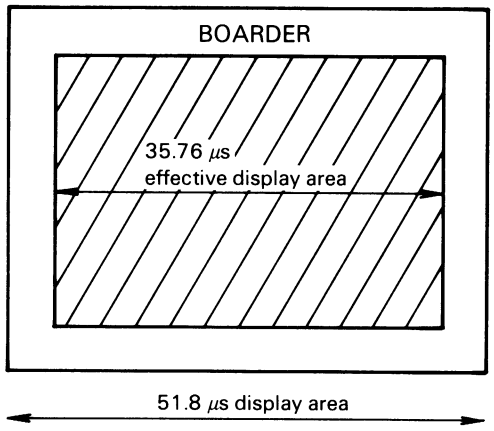


Fig. 4-36

- Display timing

  From a system clock of 3.5795 MHz, a dot clock twice in period (about 139.7 nsec) is generated in VDG6847 (2C), and the dots of this clock timing are displayed.

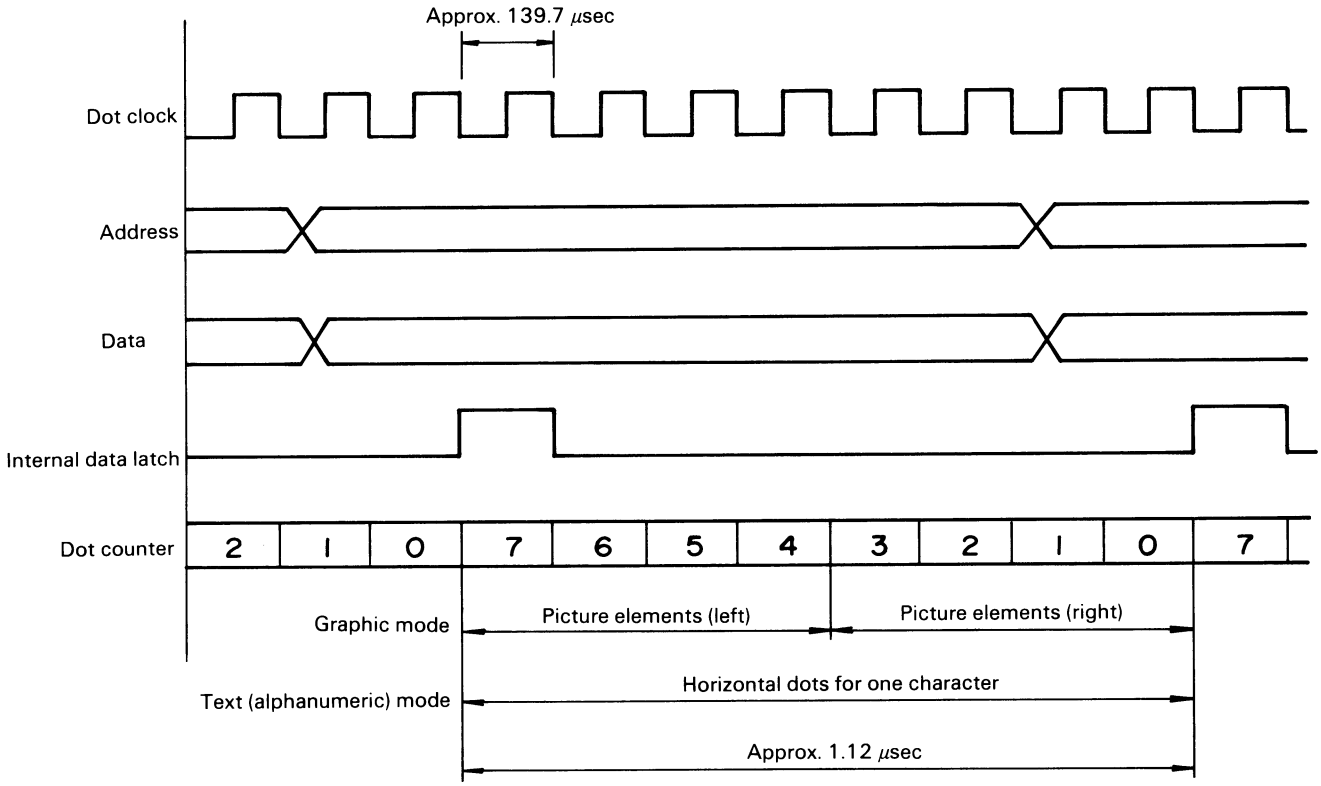


Fig. 4-37

1. Time required for displaying one dot line (256 dots)

139.7 nsec × 256 = 35.76 μsec

Boarder sweep time = approx. 16.06 μsec

} Approx. 51.8 μsec

4.4.2 Text Mode

In the text mode, 32 characters x 16 lines can be displayed, that is, a maximum of 512 characters can be shown on the screen.

Displayed data are stored in ASCII code in the V-RAM so, when displaying the data on the screen, display patterns are generated by the built-in character generator.

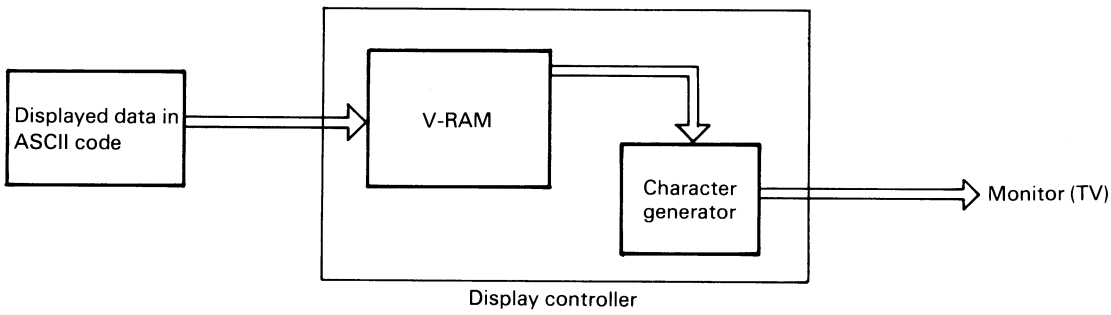


Fig. 4-38

One character is composed of a font of 8 (horizontal) x 12 (vertical) dots, but actually a font of 7 x 9 dots to for inter-character and inter-line spaces.

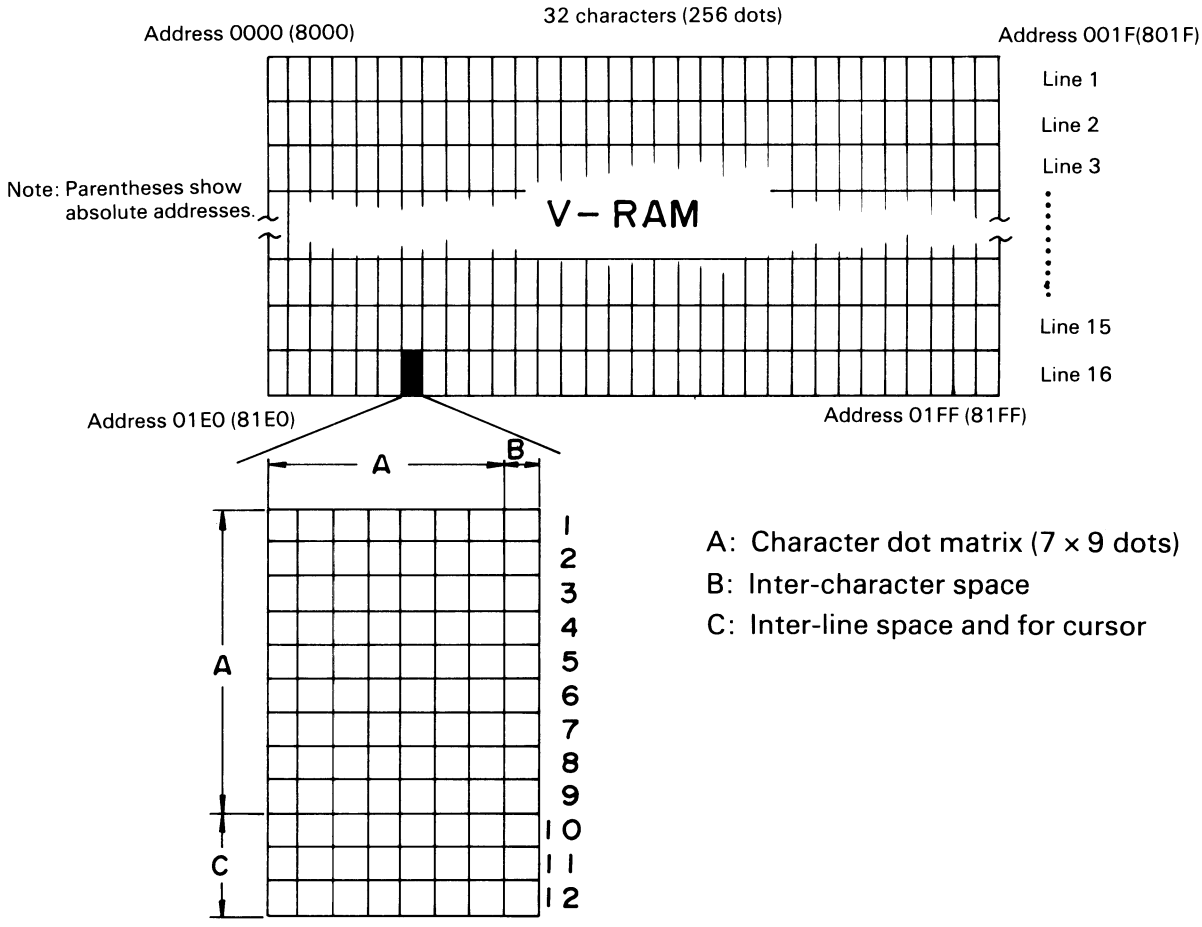


Fig. 4-39

4.4.3 Graphic Mode

There are two kinds of graphic mode, that is, color and monochrome, and display patterns are written on the V-RAM.

Therefore, the character generator is not used but the data sotred in the V-RAM are directly output to the screen in the graphic mode.

(Color Mode)

Eight colors can be displayed. These colors are divided into two groups of four each colors (color set 0 and color set 1). Select either of these color sets with a color command before dispalying data in color.

A color set can be selected by changing the VDG's (2C) CSS with port 20 of the CPU.

* Color selection

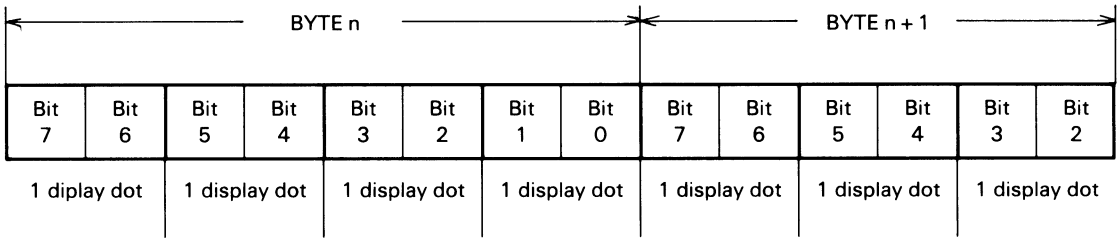
CSS: 0 Color set 0

Bit		Color
Higher	Lower	
0	0	Green
0	1	Yellow
1	0	Blue
1	1	Red

SCC: 1 Color set 1

Bit		Color
Higher	Lower	
0	0	White
0	1	Cyan
1	0	Magenta
1	1	Orange

Two bits are used to define one display dot in selecting a color in a color set.



In the color mode, the full area of 2k bytes in the V-RAM is used as shown below.

128 dots (horizontal) × 64 dots (vertical) × 2 (color) = 16,384 bits (2k bytes)

Monochrome Mode

In the monochrome mode, 128 dots (horizontal) × 96 dots (vertical) are displayed by showing bits on the V-RAM directly on the screen. Thus, 1.5k bytes of the V-RAM are used as expressed by the following formula.

128 dots (horizontal) × 96 dots (vertical) = 12,288 bits (1.5k bytes)

4.4.4 Operation Mode (Memory Map)

The main CPU's operation mode depends on hardware connection at ports 20, 21 and 22. The display controller hardware is as shown below. Here, an output from IC7A is input to port 22 at high level because the port state upon completion of resetting is latched to the mode control register. Thus, the main CPU operates in mode 6 (multiplexed partial decode).

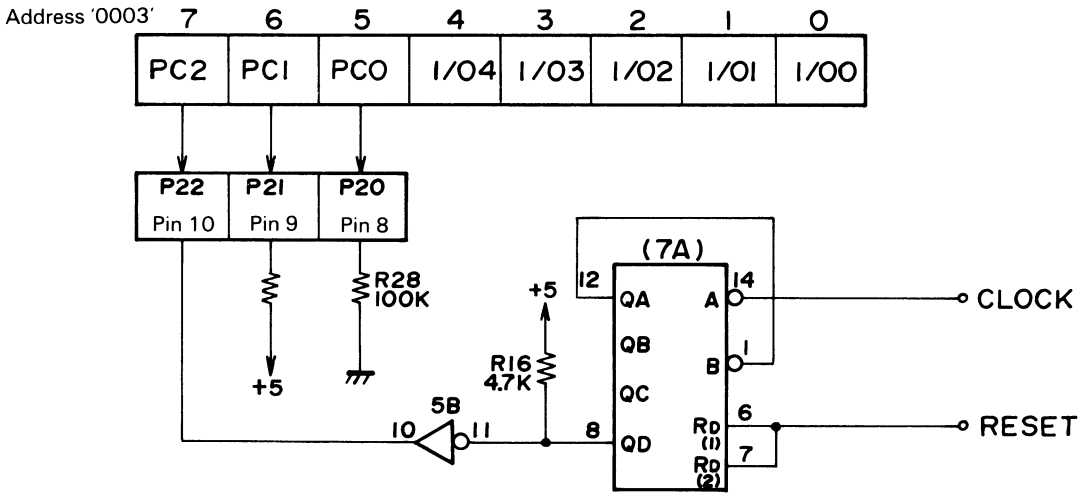
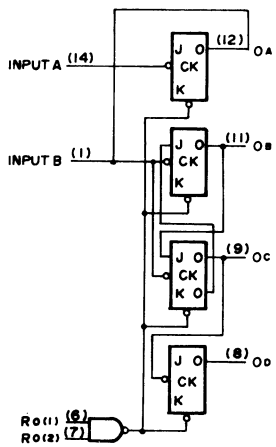


Fig. 4-40

After power is turned on, the P22 is used as an input terminal for external clocks. As shown below, an external clock is counted down to 1/12 by IC7A, and the resultant clock is supplied to the CPU. This clock is used for generating a serial interface bit rate.
The clock has a frequency of 3.6864 MHz, which is divided by 12 as an external clock to approximately 307 kHz. As in the case of the HX-20, data can be transferred at 38.4 kbps.



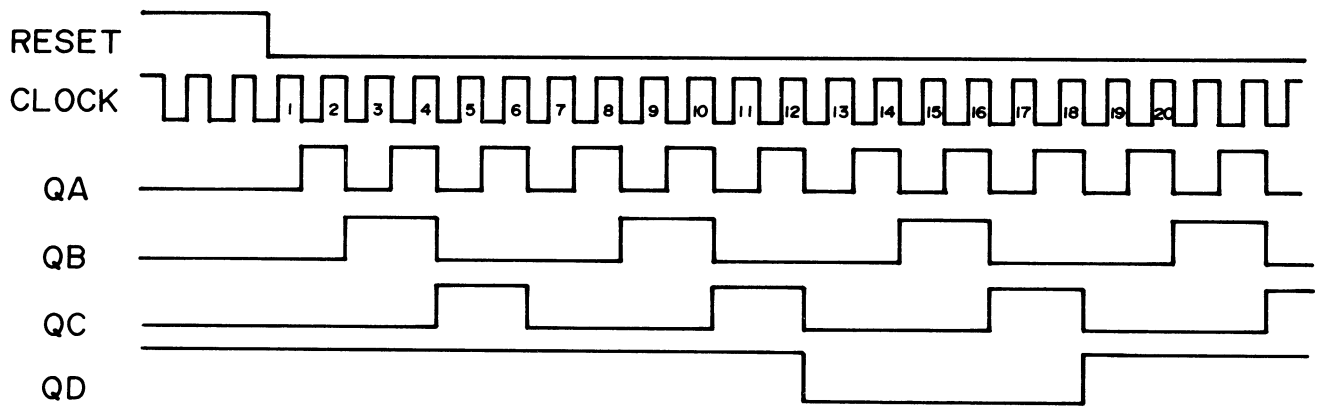


Fig. 4-41

(Memory Map)

In operation mode 6, the memories are allocated as shown below.

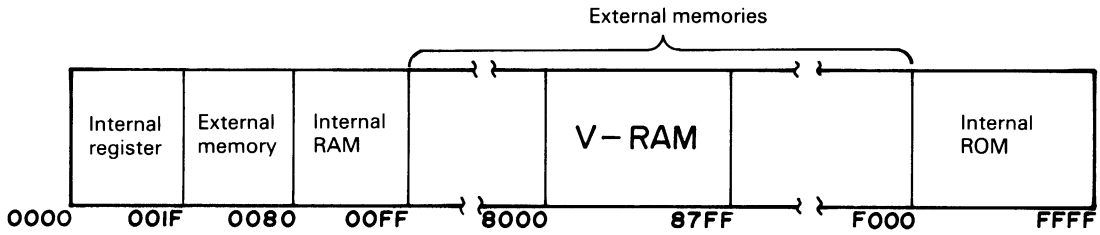


Fig. 4-42

In operation mode 6, addresses are allocated as shown before, but the area that is actually used is as follows:

- Addresses FFFF to F000: Internal mask ROM in CPU 6301 (7B)
- Addresses 8000 to 87FF (2k bytes): Addresses 0100 to EFFF are for external memories, but only 2k bytes of them are used for video RAM.

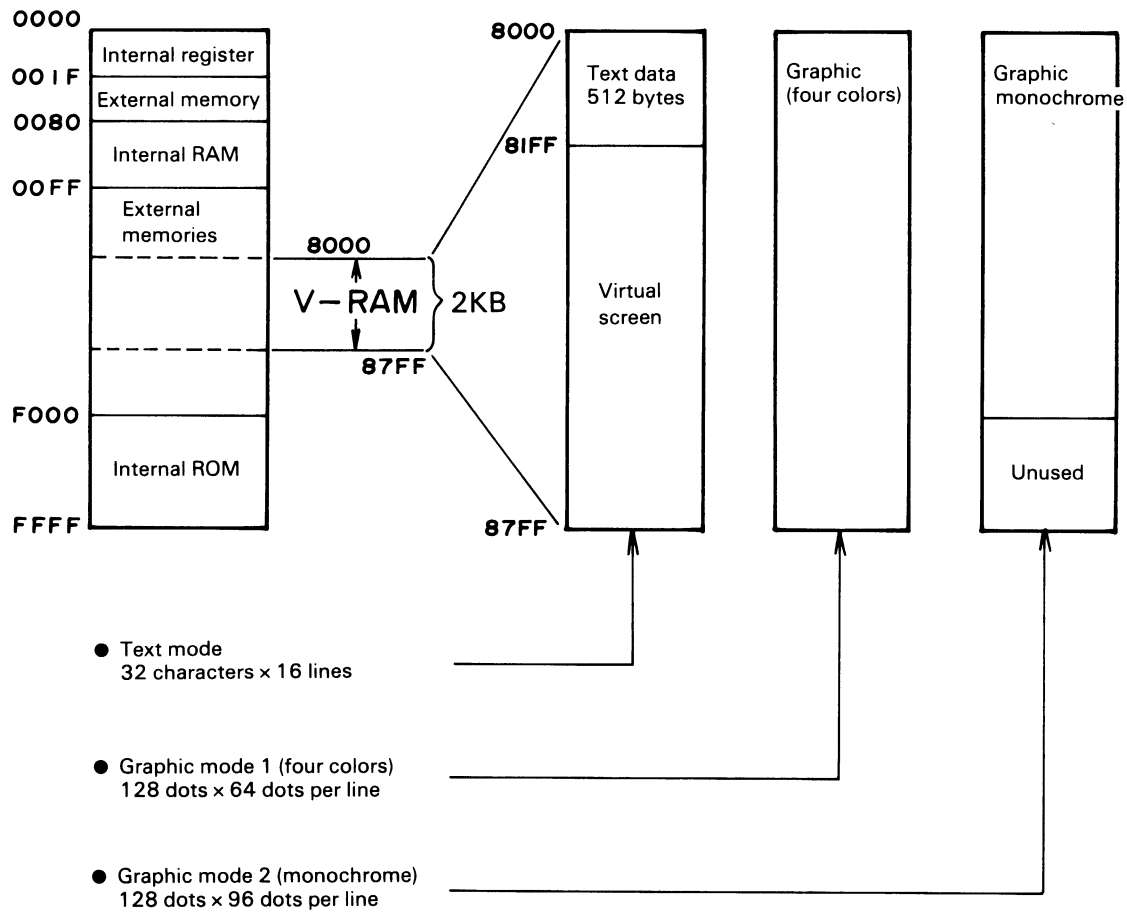


Fig. 4-43

4.4.5 Power Supply

The power supply consists of a filter circuit, transformer, and DC regulator as shown below, and generates four kinds of voltages.

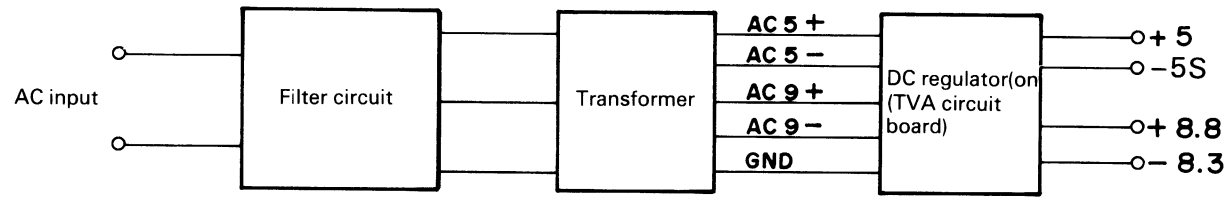


Fig. 4-44

(1) Filter circuit

The filter circuit has fuse F1 for protection from overcurrent (800 mA) and a circuit for eliminating AC line noise, and employs a π type filter as shown below.

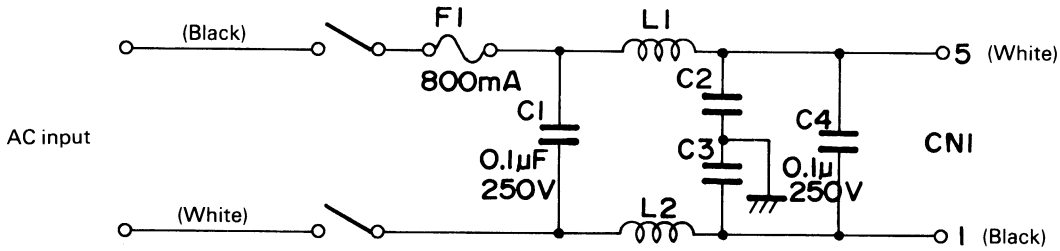


Fig. 4-45 Filter Circuit

(2) Transformer

The transformer genertes a +5V AC output and a +8V AC output from the AC input.

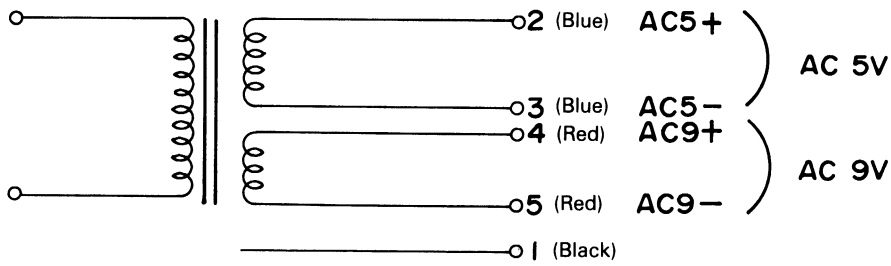


Fig. 4-46

(3) There are two kinds of DC regulator, that is, one is for +5V and the other for +8V, and generates the following voltage.

Voltage	Range	Use
+5V	4.8 to 5.2V	Circuit voltage
+5S	4.8 to 5.2V	Bias voltage for video display generator (2C)
+8.8V	8.0 to 10.0V	Voltage for serial (RS-232C level)
−8.3V	−8.0 to −10.0V	Voltage for serial (RS-232C level)
−5V	−4.8 to −5.2V	Chroma oscillation

(a) The input is full-wave rectified by diode bridge DB1 and smoothed by electrolytic capacitor C11. A +5V is generated from this smoothed DC voltage by3-terminal regulator (7805).

A smoothing capacitor C10 and a filter inductance L1 are provided on the output end to assure steady voltage supply. A diode D6 is provided against counterelectromotive force in switching power off.

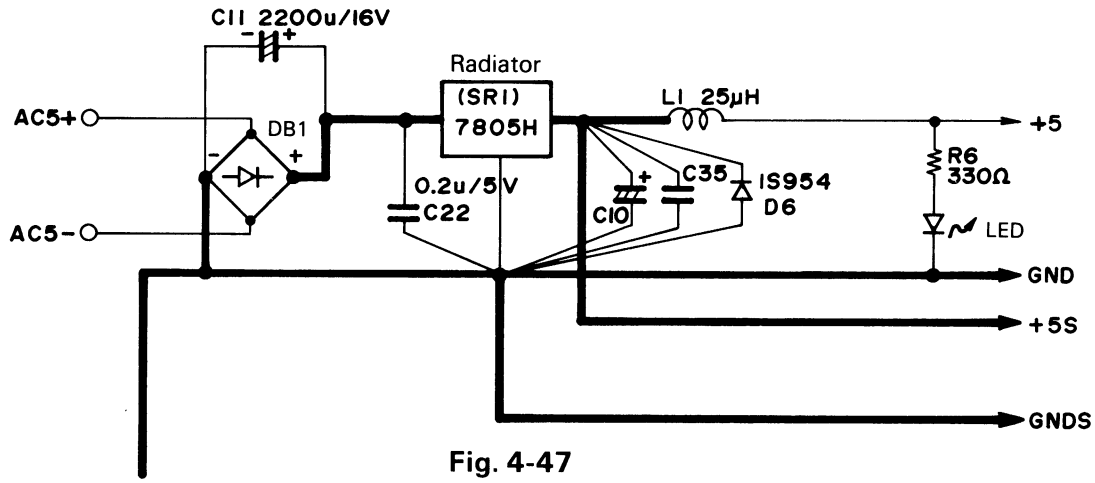


Fig. 4-47

(b) +8V

The input is full-wave rectified by diode bridge DB2, and the +8V is fed via resistor R3 to turn on transistor Q4. As a result, the voltage is output at the emitter. The output voltage is divided into resistor R21 (13.0 kohms) and resistor R14 (5.23 kohms), and fed back to Pin 8 of TL431.

The gate of TL431 operates at 1.5V so that, when the output voltage rises above about 5.2V, SCR turns on to cut off transistor Q4. A constant output voltage is maintained by repeating this process.

$$5.23k \times X = (5.23k + 10k) \times 1.5$$

$$X = \frac{27.345}{5.23}$$

$$\fallingdotseq 5.2$$

(c) −8V

When a negative voltage is output, it is routed via resistor 11 to turn the base of transistor Q1 low. As a result, Q1 turns on to output a −8.3V to the emitter.

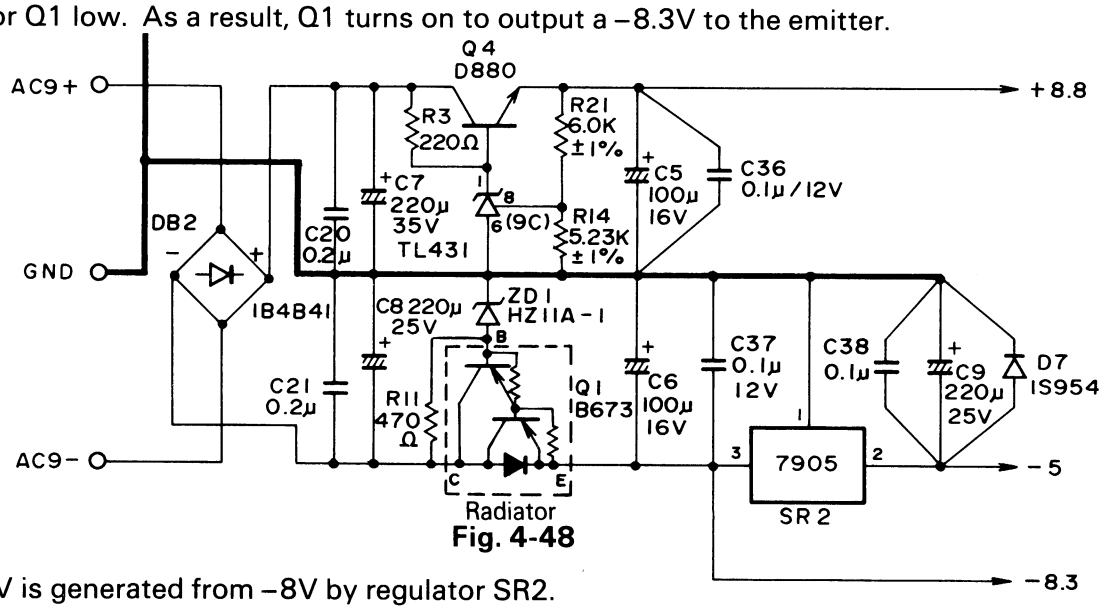


Fig. 4-48

−5V is generated from −8V by regulator SR2.

4.4.6 Oscillation Circuit

The 3.6864 MHz clock output by crystal oscillator CR1 is amplified by IC8A, and is routed via IC5A to the clock input terminal on the main CPU.

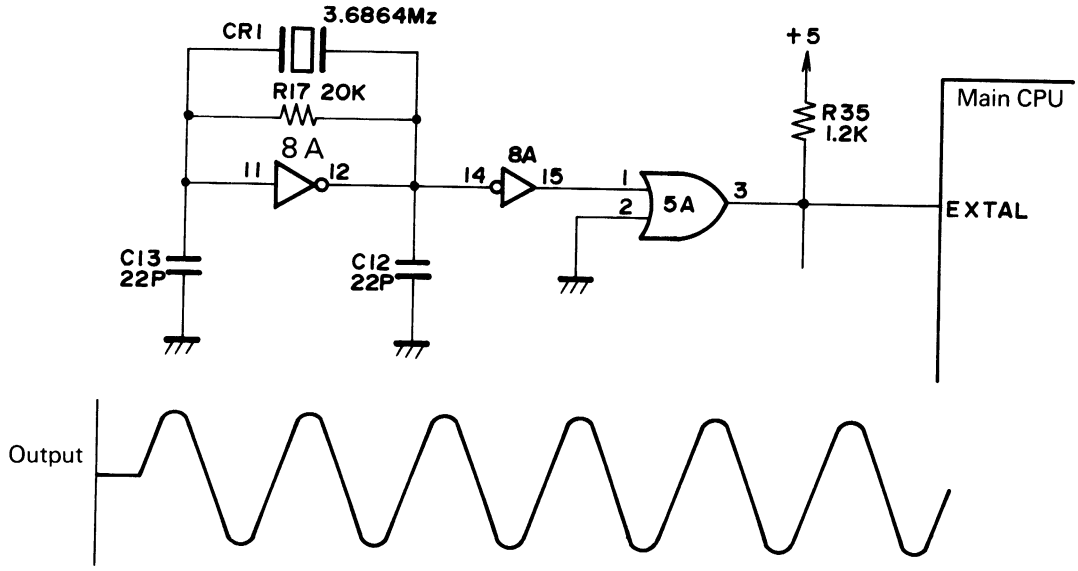


Fig. 4-49

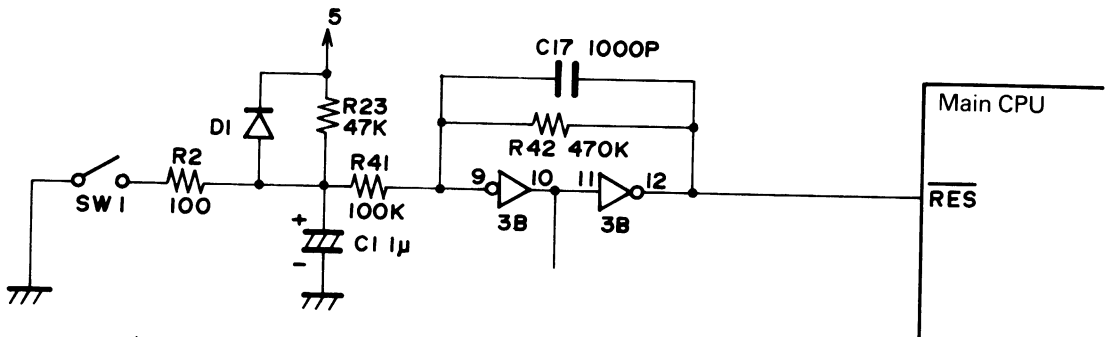
The main CPU has a 1/4 dividing circuit to divide the system clock to approximately 0.922 MHz (1.09 μsec period).

4.4.7 Reset Circuit

A reset signal is supplied to CPU 6301 (7B) only when power is turned on or when the reset switch is pushed.

Power-On Reset

When power is switched on, the circuit voltage +5V is supplied so that a charging current flows via resistor R23 to capacitor C1. Thus, Pin 9 of IC3B remains low for about 30 msec after power is switched on.



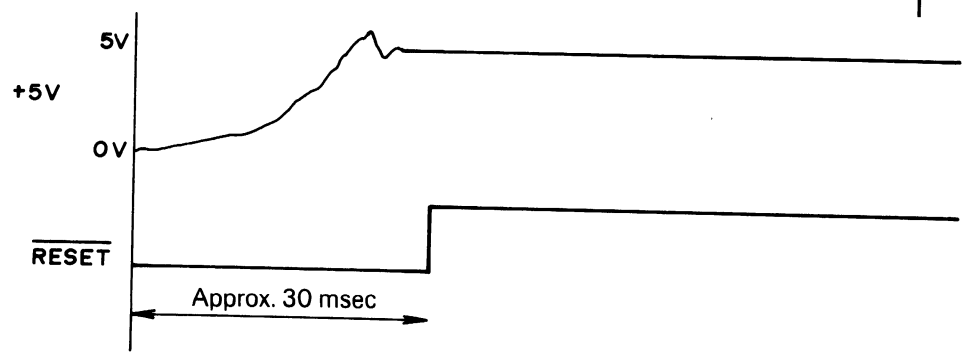


Fig. 4-50

The charging current flowing to capacitor C1 generates a delay time (of about 30 msec) for generating a reset signal.

When capacitor C1 has been charged, Pin 9 of IC3B goes high to stop reset operation.

Reset Switch

When the reset switch is pushed, the charge stored in that the positive end of C1 goes low to output a reset signal. When the reset swtich is released, the reset is released about 30 msec later as in power-on reset.

4.4.8 Interface

The interface is a high-speed serial interface for transferring data at 38.4 kbps. The interface operates at RS-232C level.

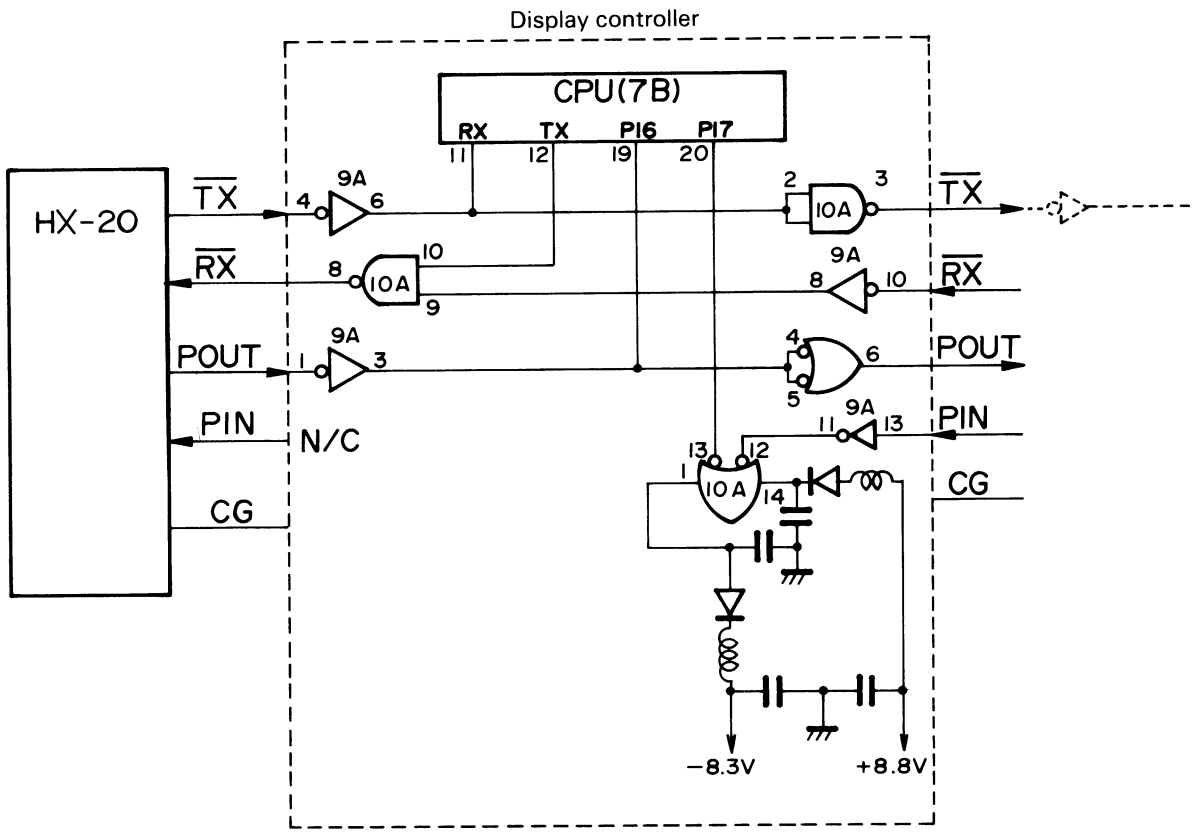


Fig. 4-51

The high-speed serial interface may connect not only the display controller but TF-20 to the smae line. (Daisy-chain connection) Thus, connections such as shown above are made inside the display controller.

(1) $\overline{TX}$ line:

IC9A Pin 6 output is taken into the CPU, and this signal is inverted by IC10A and output to TF-20.

(2) $\overline{RX}$ line:

- If only the display controller is connected to the HX-20, Pin 10 of IC9A is at floating level so USART IC (9A) is low. Thus, Pin 9 of IC10A is normally high, and the Pin 8 output is controlled by Pin 12 (TX) of CPU 7B in the display controller.
- If TF-20 is connected via the display controller, one of the transmitting units connected in a daisy-chain network (TF-20/display controller) is selected by an HX-20 protocol.

Thus, only one of the daisy-chain-connected units can transmit. The units not in the transmitting mode send a low level signal to the $\overline{RX}$ output line.

If the display controller is to send, Pin 10 of IC9A is low so that Pin 9 of IC10 goes high, and an input (TX) to Pin 10 of IC10A enables data to be transferred to the $\overline{RX}$ output line.

(3) P OUT line: IC9A Pin 3 output is taken into the CPU, and this signal is inverted by Pin 6 of IC10, and output to TF-20.

(4) P IN line: The output end of the line is open (N/C).
The input end of the line is connected via IC9A to IC10A, but the output of IC10A is open (N/C).

* P OUT and P IN signals are not actually used.

- Received serial data are converted into parallel data, of which the commands are stored in the CPU and the data in the V-RAM. When transferring data to the HX-20, the data stored in the V-RAM are read out, converted from parallel to serial data in the CPU, and output to the interface.

4.4.9 RAM Control

The video RAM (V-RAM) has 2k bytes of absolute addresses 8000 to 87FF. In RAM addressing, therefore, it is necessary to select not only relative addresses 000 to 7FF of the 2k-byte V-RAM by lines A0 to A10 but also address 8xxx by A15.

Write to V-RAM

First, by outputting RAM addresses (8000 to 87FF) to be stored at write timing, lower addresses are stored in the address latch at the rise timing of an AS signal, and the data bus gate (5C) is set in the output direction (CPU → RAM) by a $\overline{W}$ signal.

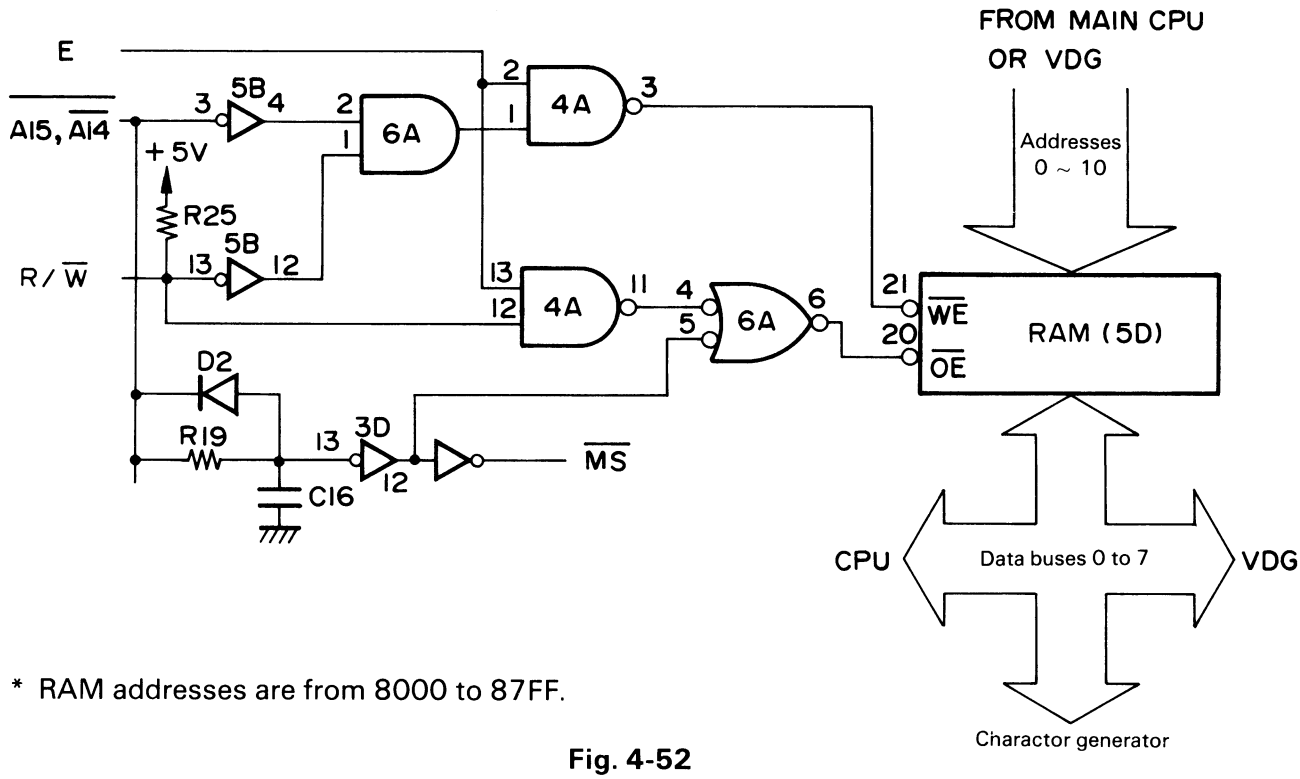
Then, the output of Pin 5 of IC4B goes low at the fall of the AS signal so that the lower addresses that have been stored are output from the address latch (6B) to an address bus. At the same time, the data bus gate (5C) turns on to keep the data bus in an output state (CPU → RAM) until the next E signal goes high. IC6C which controls so that selection of V-RAM addresses if accomplished perfectly.

Under this condition, the main CPU outputs one byte of data to a data bus so that the data can be stored in the selected RAM addresses.

Read from V-RAM

The $\overline{R}$/W signal goes low so that the data bus gate (IC5C) is set in the input direction (RAM → CPU). As RAM (5D) sets $\overline{OE}$ (output enable) if it is AND'ed with an E signal, the data stored in the selected RAM addresses can be read out. Address control is the same as in write operation.

RAM Control Circuit



* RAM addresses are from 8000 to 87FF.

Fig. 4-52

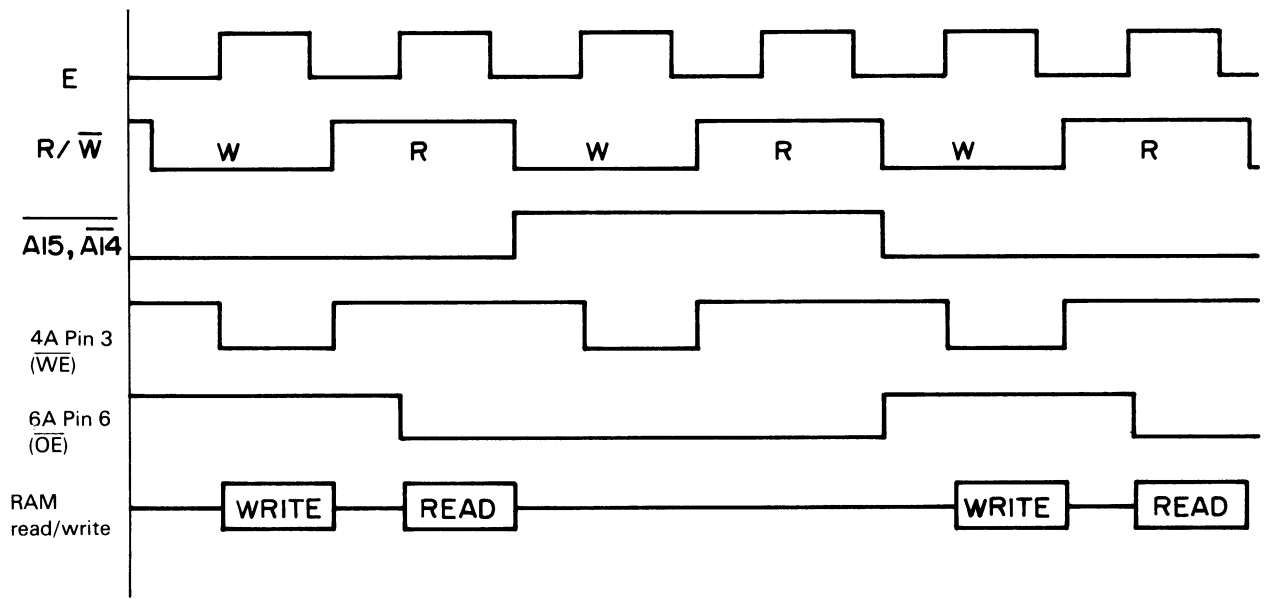


Fig. 4-53

4.4.10 Data Bus Control

IC5C and IC3C are located on the data buses to control the data lines. These ICs select a data direction for each operation. IC5C is a two-way gate, whose direction can be changed by an R/$\overline{W}$ signal. IC3C is a one-way gate, which is switched together with a character generator output by port 15 of the CPU.

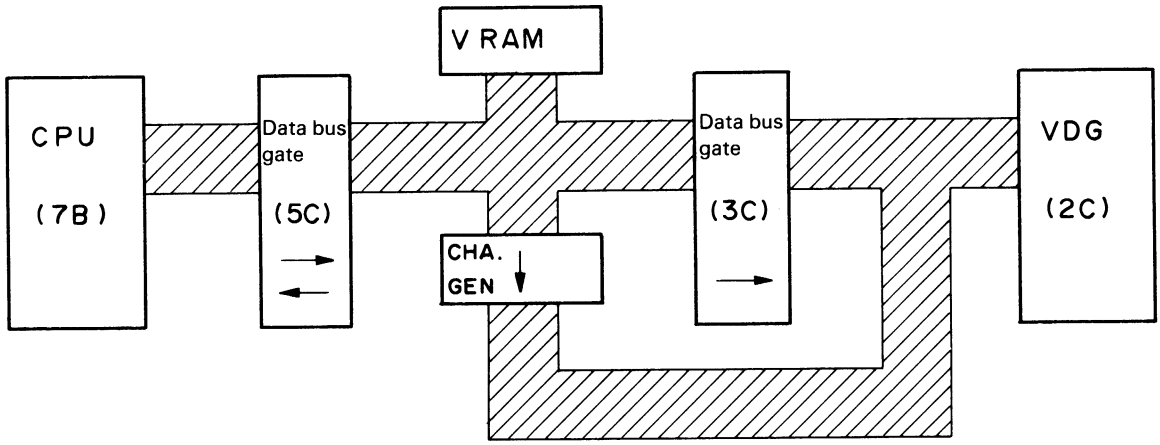


Fig. 4-53

There are four operations using data buses as mentioned below.

(1) V-RAM → CPU : Read from V-RAM
(2) CPU → V-RAM : Write to V-RAM
(3) V-RAM → VDG : Graphic display
(4) CHA. GEN → VDG : Text display

(V-RAM → CPU, CPU → V-RAM)

The data buses are controlled by an AND with addresses A15, A14, and E (enable) signal, and a data direction is selected by and R/$\overline{W}$ signal.

Addresses A15, $\overline{A14}$ mean that V-RAM will be selected, and signal A15, $\overline{A14}$ is hold at the rise of the AS signal. If signal A15, $\overline{A14}$ is output, that is, if absolute addresses 8000 to 87FF in V-RAM are selected, the Pin 5 output of IC4B goes low at the timing of the input (fall of the AS signal) to Pin 3 of IC4B.

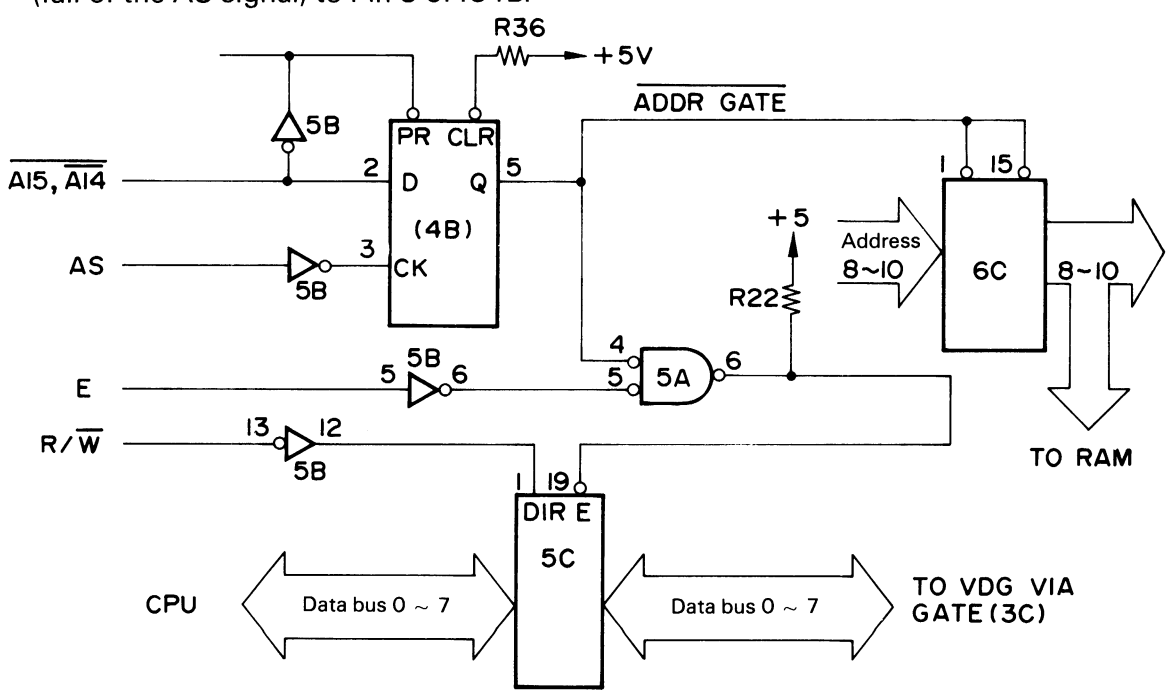
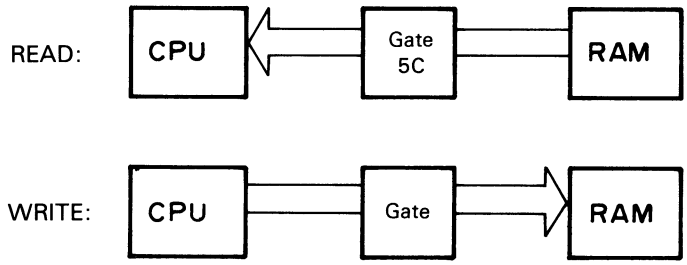


Fig. 4-54

When the IC4B Pin 5 output is set low, the gate of IC6C turns on to output A10 to A8 to an address bus, and supply to Pin 4 of IC5A. Thus, data bus gate IC5C is put into operating condition by an AND with an $\overline{E}$ singnal.

Under this condtion, the data bus gate's signal direction is switched by the R/$\overline{W}$ signal as shown below.



(V-RAM → VDG, CHA GEN → VDG)

Data input to IC2C (VDG) varies depending on the graphic mode and text mode. In the text mode, data output from the character generator (4C) are directly input so that the data bus gate of IC3C turns off. In this case, the data buses are disconnected from the CPU.

In the graphic mode, however, the character generator is not used, but data output from the V-RAM are directly displayed. Accordingly, port 15 of the CPU is used to stop character generatoir output, turn the gate of IC3C on, and take the data output from the V-RAM into IC2C (VDG).

As described above, the character generator and data bus gate are conrolled by port 15 of the CPU according to the display commands.

Port 15 High: Graphic mode
Low: Text mode

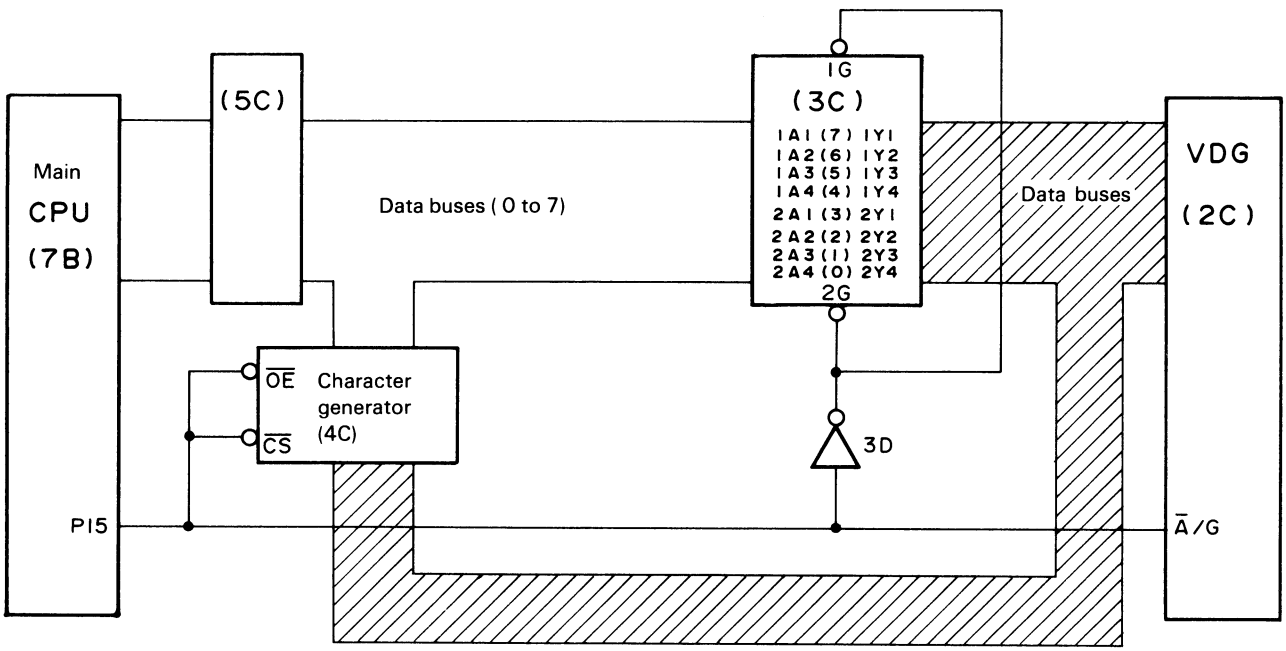
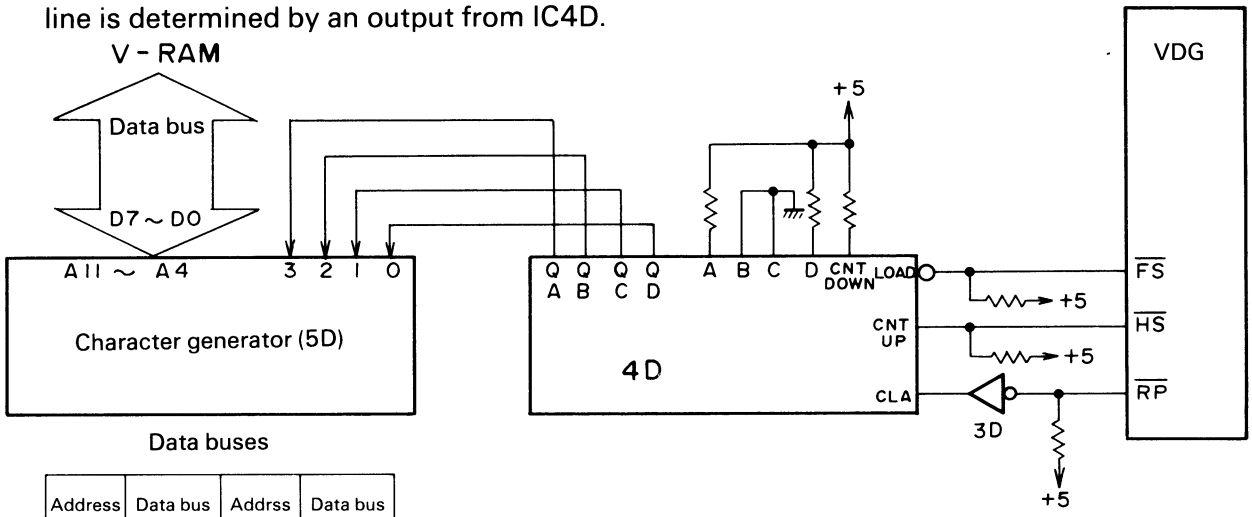


Fig. 4-54

4.4.11 Character Generators

Character generators are used in the text (alphanumeric) mode. The start address of a character generator corresponding to an ASCII code is selected by data buses D7 to D0 (which correspond to A11 to A4), and a character generator pattern corresponding to a display dot line is determined by an output from IC4D.



Data buses

Address	Data bus	Addrss	Data bus
11	DA7	7	DA3
10	DA6	6	DA2
9	DA5	5	DA1
8	DA4	4	DA0

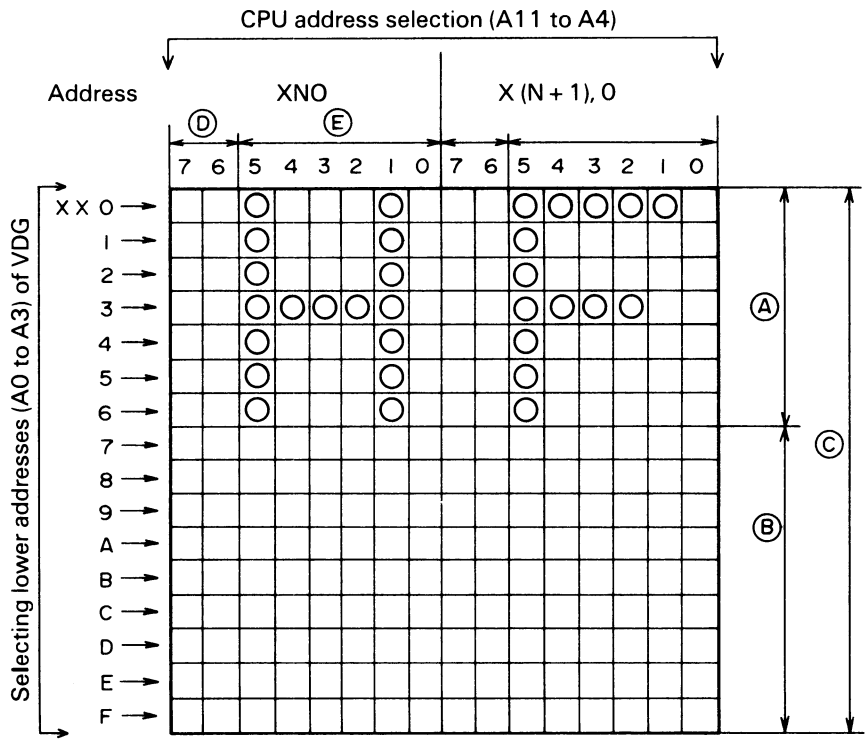
* $\overline{FS}$ (field sync output): End of effective display area
$\overline{HS}$ (horizontal sync output): Horizontal sync signal
$\overline{RP}$ (Rope reset): Output when using external character generator ROM (5D)

Fig. 4-55

A signle-character generator consists of 16 bytes, but the number of bytes actually used for display is 12, including inter-line space.

This is due to character generator address selection, that is, to the fact that a system by which the start address of a character generator corresponding to ASCII code is selected by the CPU using addresses A11 to A4 is employed.

The data which have been read out are taken into the VDG, byte by byte, and displayed.



Note: Address XN is a character of ASCII code.

(A): Column dots acually displayed
(B): Space between lines
(C): Character generator addresses shared by characters
(D): Ignored. No function
(E): Row dots displaying 5 bits

* Bit 0 at the bottom is used for inter-line space.

Fig. 4-56

4.4.12 Address Latch

The address latch is used to hold lower addresses A0 to A7.

The lower addresses on address data buses are latched to IC6B at the rise of an AS (address strobe) signal (L → H) and are kept latched until the next AS signal is output.

If addresses A15 and $\overline{A14}$ are simultaneously output, the rising edge of the AS signal turns Pin 5 of IC4B low to output an $\overline{ADDR\ GATE}$ signal, and A8, A9, and A10 are output from IC6C. At the same time, the address latch output control ($\overline{OC}$) turns on to output addresses A0 to A7 to address bus lines. As a result, V-RAM addresses are selected by A0 to A10.

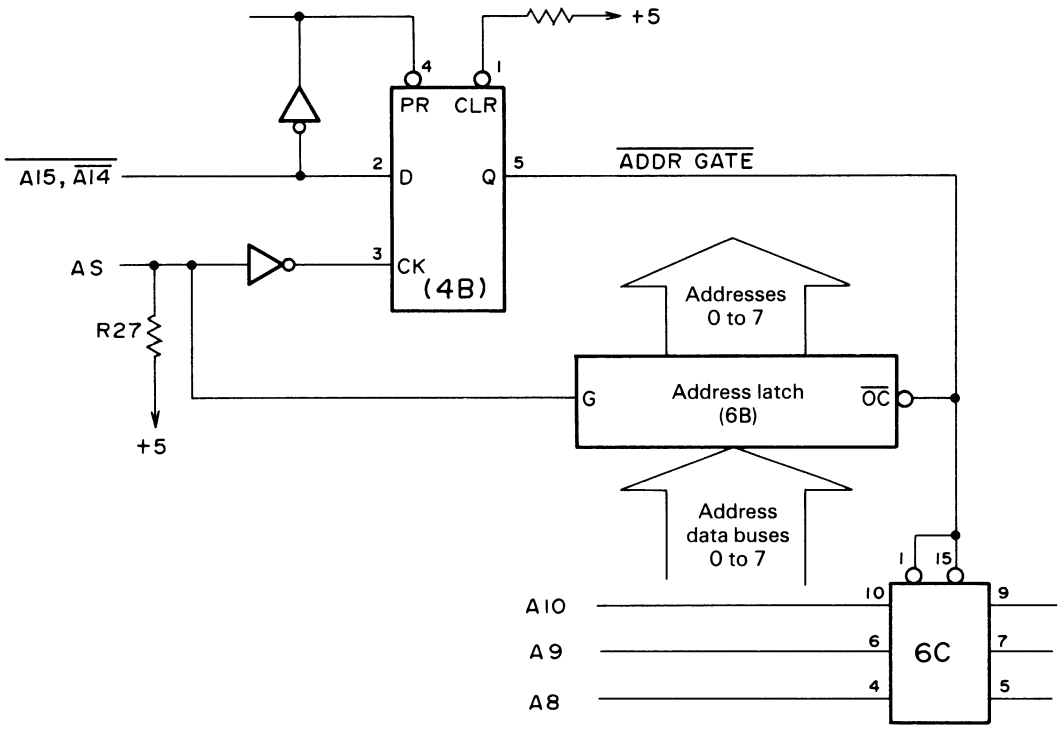
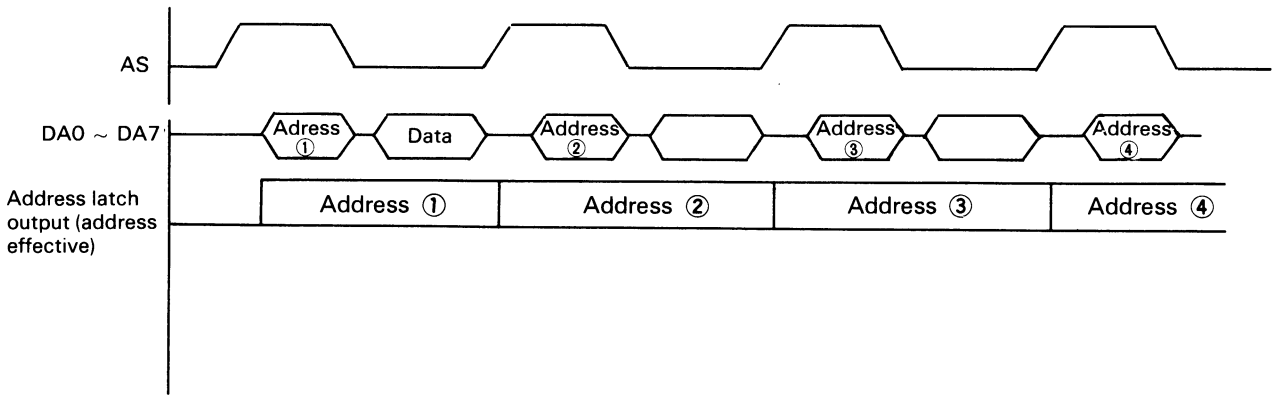


Fig. 4-57



4.4.13 Modulator Circuit

IC1C is used for modulating purposes. The modulator circuit receives chroma bias, B-Y and R-Y signals from the VDG, and modulates them for color display. The relationship between colors and signals is shown in Fig. 4-62. CV1 is an oscillation frequency control for generating clocks of 3.57956 to 3.57952 MHz, but normally, it must not be turned.

IC1C has a video bias control volume VR1/2 on its output end, which may be used for output adjustment.

VR1 is used for bias adjustment, and VR2 for wave peak adjustment. Normally, these VRs must not be turned either. If it is absolutely necessary to adjust these VRs, observe the following instructions.

Step 1: Adjust burst signal to 3.0V with VR1.

Step 2: Adjust wave peak to 1.0V with VR2.

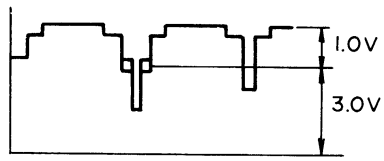


Fig. 4-59

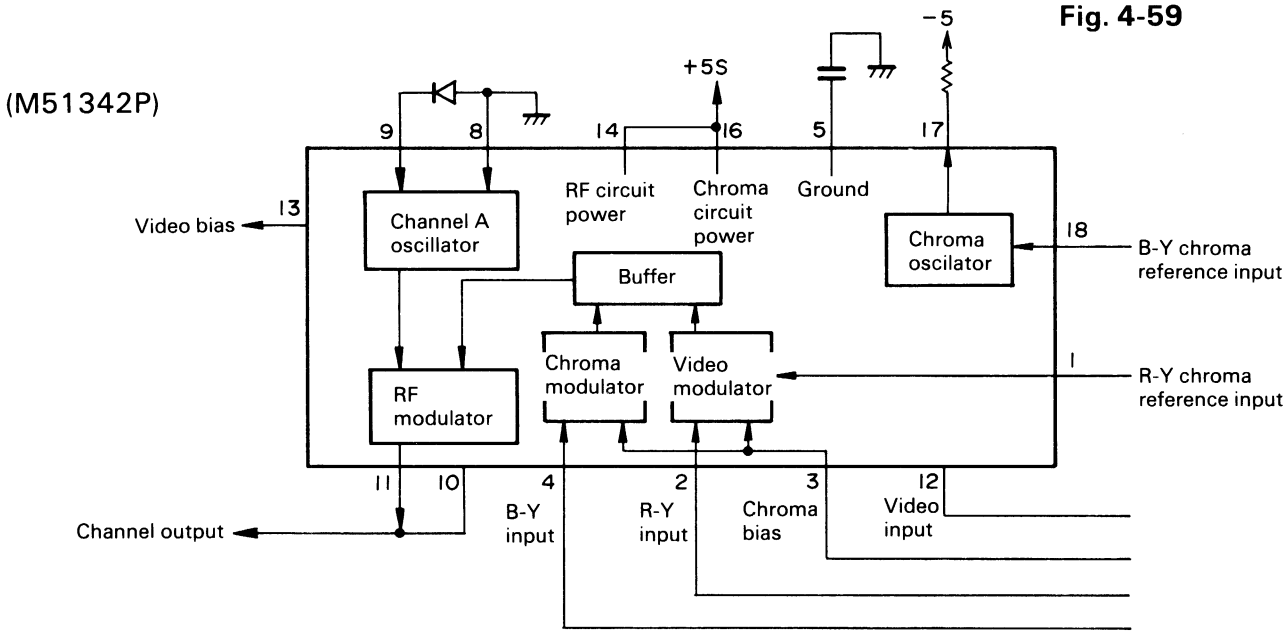


Fig. 4-60

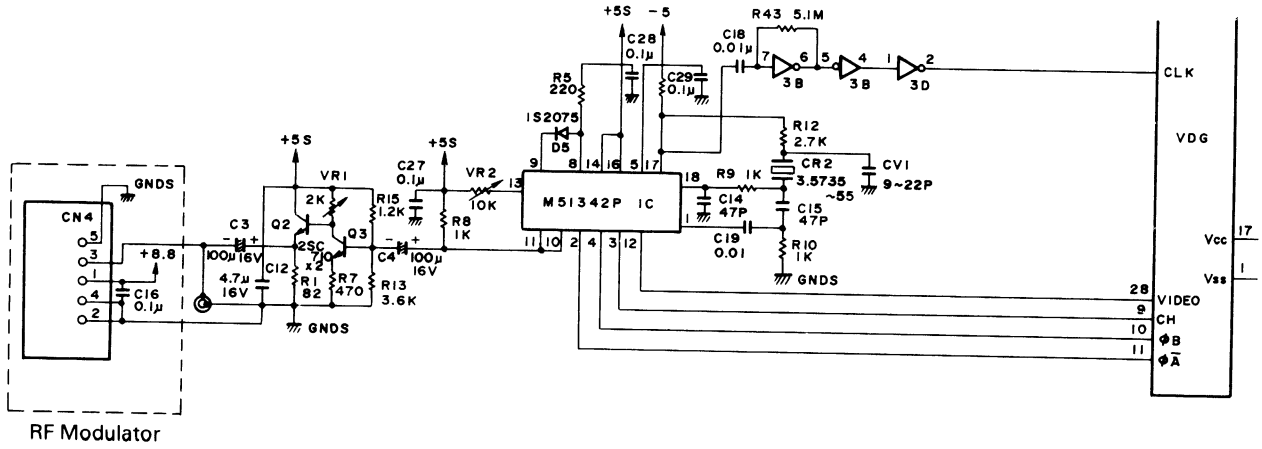
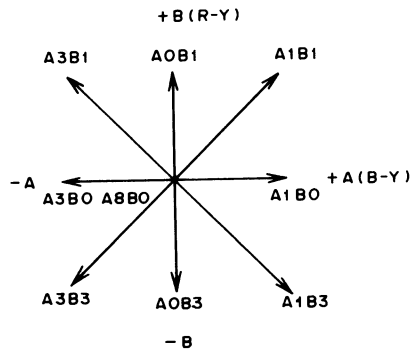


Fig. 4-61



Color modulation signal level (Standard 7.5V)		Approximate color
Chroma A (B-Y)	Chroma B (R-Y)	
A0 = 0V	B0 = 0V	Light grey
A0 = 0V	B1 = −0.8V	Red
A0 = 0V	B3 = −0.8V	Cyan
A1 = −0.8V	B0 = 0V	Blue
A1 = −0.8V	B1 = −0.8V	Magenta
A1 = −0.8V	B3 = −0.8V	Blue cyan
A3 = −0.8V	B0 = 0V	Yellow
A3 = −0.8V	B1 = −0.8V	Orange
A3 = −0.8V	B3 = −0.8V	Green
A3 (BURST) = −0.4V	B0 = 0V	Burst

Chroma bias versus chroma modulation signals and versus approximate colors.

Fig. 4-62

— MEMO —

— MEMO —