STANDARD MICROSYSTEMS CORPORATION

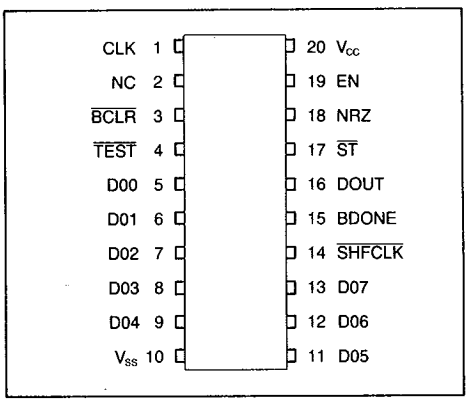
HDC 1100-01
PRELIMINARY

Hard Disk Serial to Parallel Converter

FEATURES

- ☐ Single +5 Volt Power Supply
- ☐ Double Buffered
- ☐ Byte Strobe Outputs
- ☐ 5 MBit Shift Rate
- ☐ Serial Input/Parallel Out
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

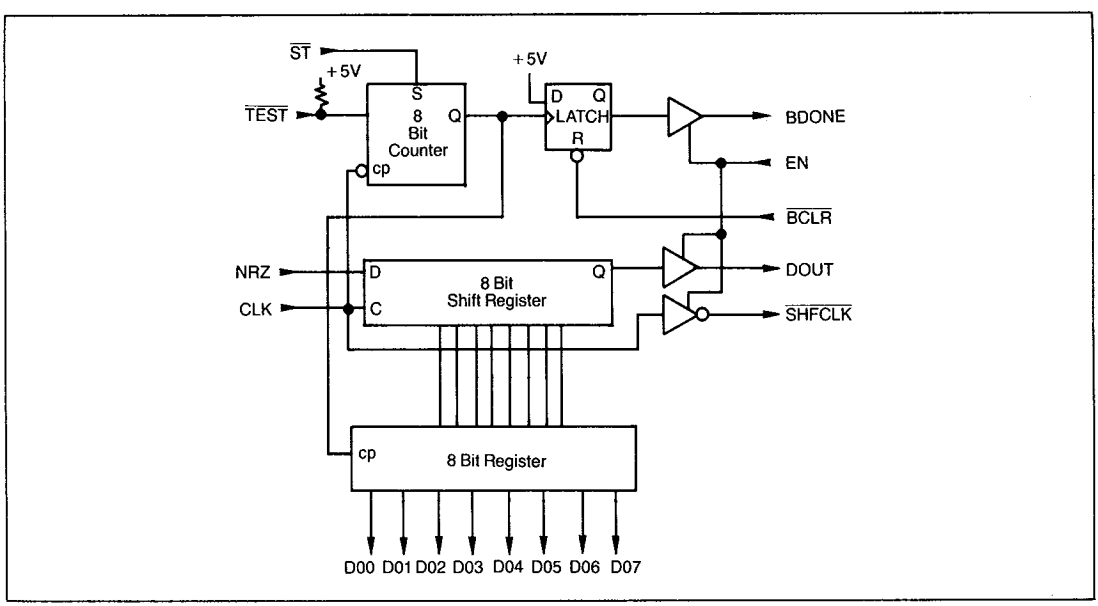
PIN CONFIGURATION



GENERAL DESCRIPTION

The HDC 1100-01 converts NRZ data from a Winchester disk drive into eight bit parallel form. Additional inputs are provided to initiate the conversion process, as well as output strobes to indicate the completion.

The HDC 1100-01 contains two sets of 8 bit registers. This allows one register to be read (in parallel) while serial data is being shifted into the other.



SECTION VI

DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	CLK	CLOCK	NRZ data is entered into the 8-bit shift register on the low-to-high transition of clock.
2	NC	NO CONNECTION	No connection. This pin is to be left open by the user.
3	$\overline{BCLR}$	$\overline{BYTE\ CLEAR}$	When this line is at a logic 0, the BDONE (pin 15) line is held reset.
4	$\overline{TEST}$	$\overline{TEST\ INPUT}$	This pin must be left open by the user.
5-9, 11-13	D00-D07	DATA0-DATA7	8 bit parallel data outputs.
10	V_{SS}	GROUND	Ground.
14	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	Inverted copy of CLOCK (pin 1) which is active when EN (pin 19) is at a logic 1.
15	BDONE	BYTE DONE	This signal is forced to a logic 1 signifying 8 bits of data have been assembled. BDONE remains in a logic 1 state until reset by a logic 0 on the BCLR (pin 3) line.
16	DOUT	DATA OUT	Serial Data Output from the 8th stage of the internal shift register. DOUT is in a high impedance state whenever EN (pin 19) is at a logic 0.
17	$\overline{ST}$	$\overline{START}$	This line enables the byte counter and is used for synchronization. It must be held to a logic 1 prior to first data bit on the NRZ (Pin 18) line.
18	NRZ	NRZ DATA	NRZ serial data is entered on this pin and clocked by the low to high transition of CLK (pin 1).
19	EN	ENABLE	When this signal is at a logic 0, DOUT, $\overline{SHFCLK}$, and BDONE outputs are in a high impedance state.
20	V_{CC}	V_{CC}	+5V power supply input.

OPERATION

Prior to shifting data through the device, the HDC 1100-01 must be synchronized to the data stream. The ST line (Pin 17 high) is used to hold the internal bit counter in a cleared state until valid data (NRZ) and clocks (CLK) are entered. The $\overline{ST}$ line is a synchronous input and therefore requires one full cycle of the CLK line (Pin 1) to occur in order to accept a $\overline{ST}$ condition. After this happens, the device is ready to perform serial to parallel conversions.

Data is entered on the NRZ line and clocked into the 8-bit shift register on the low-to-high transition of CLK. The $\overline{ST}$ line must be set low during the low time of CLK. Data is accepted on low-to-high transition of the clock while the high-to-low transition of CLK increments the bit counter. After 8 data bits have been entered the final high-to-low transition of CLK sets an internal latch tied to the BDONE line (Pin 15). At the same time, the contents of the shift register are parallel loaded into an 8 bit register making the parallel data available on the D00-D07 outputs. BDONE will remain in a latched state until the $\overline{BCLR}$ is set to a logic 0, clearing off the BDONE signal. $\overline{BCLR}$ is a level triggered input and must be set back to a logic 1 before the next 8 bits are shifted through the register. $\overline{BCLR}$ has no effect on the serial shifting process. When the next 8 bits are received, BDONE will again be set and the operation continues.

When interfacing to a microprocessor, BDONE is used to indicate a parallel byte is ready to be read. As the processor reads the data out of the D00-D07 lines, the $\overline{BCLR}$ line should be strobed to clear off BDONE in anticipation of the next assembled byte. An address decode signal generated at the host may be used for this purpose. During a power-up condition, the state of BDONE is indeterminant. It is recommended that BCLR be strobed low after power-up to insure that BDONE is cleared.

The serial output line from the last stage of the shift register is available on the DOUT pin. An inverted copy of CLK is available on the $\overline{SHFCLK}$ pin. Both DOUT (Pin 16) and $\overline{SHFCLK}$ (Pin 14) can be used to drive another shift register external to the device.

The three signals BDONE, DOUT, and $\overline{SHFCLK}$ can be placed in a high impedance state by setting EN (Pin 19) to a logic 0. Likewise, EN must be at a logic 1 in order for these signals to be active.

The TEST pin is internally OR'ed with the $\overline{ST}$ line to inhibit the bit counter. It is recommended that $\overline{TEST}$ be left open by the user. An internal pull-up resistor is tied to this pin to satisfy the appropriate logic level required internally for proper device operation.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +50°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +7.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.2V
Power Dissipation ..... 1.0 watt

*Stresses above those listed may cause permanent damage to the device. This is a stress ... ion of the device at these or at any other condition above those indicated in the operational sections of this ...

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

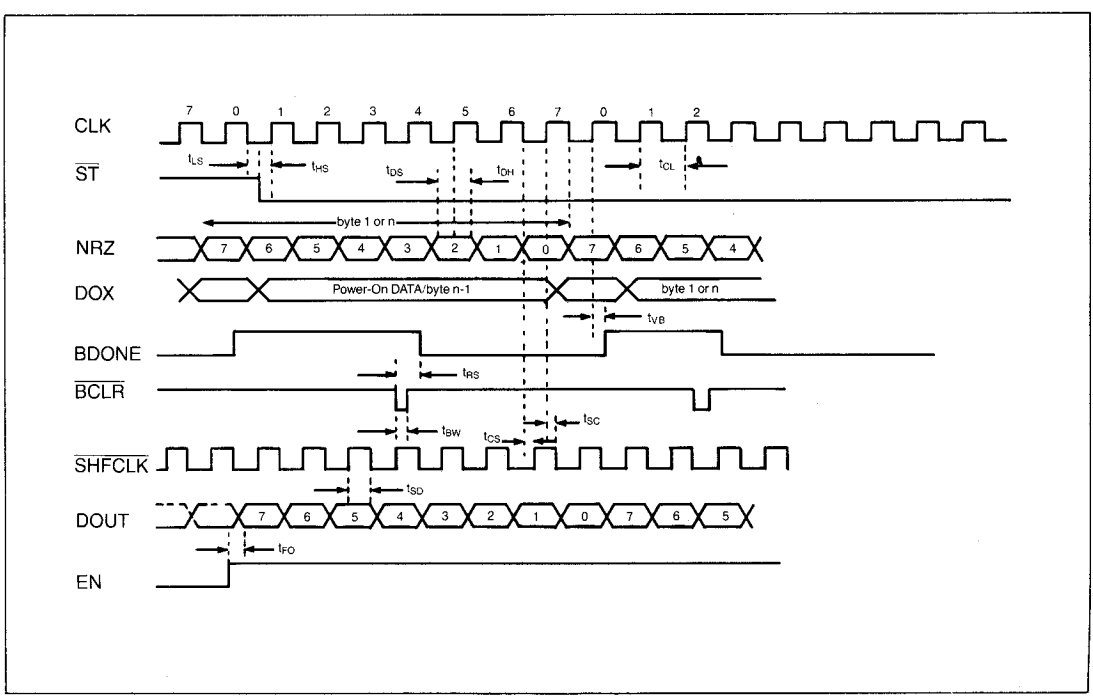
DC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_O	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{CL}	CLK FREQUENCY	0		5.25	MHZ	
t_{LS}	↓ CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{HS}	↑ CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{DS}	Data set-up to ↑ CLK	15			nsec	
t_{VB}	BDONE valid from ↑ CLK	65		110	nsec	EN = 1
t_{RS}	BDONE reset from $\overline{BCLR}$			110	nsec	EN = 1
t_{BW}	$\overline{BCLR}$ Pulse Width	50			nsec	EN = 1
t_{SC}	↑ CLK to ↓ $\overline{SHFCLK}$			90	nsec	EN = 1
t_{CS}	↓ CLK to ↑ $\overline{SHFCLK}$			100	nsec	EN = 1
t_{SD}	Data delay from ↑ $\overline{SHFCLK}$			55	nsec	EN = 1
t_{FO}	Enable to DOUT ACTIVE			90	nsec	
t_{DH}	Data Hold w.r.t. ↑ CLK	25			nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V



SECTION VI

STANDARD MICROSYSTEMS CORPORATION

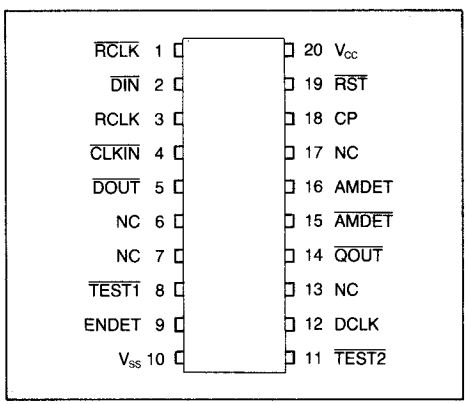
HDC 1100-03
PRELIMINARY

Hard Disk Address Mark Detector

FEATURES

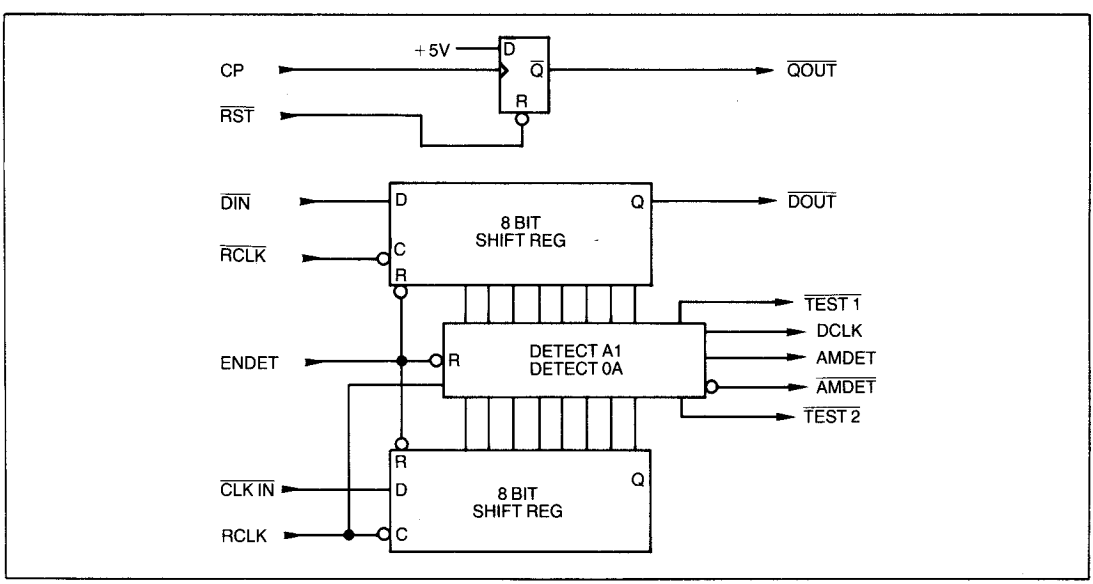
- ☐ Single +5 Volt Power Supply
- ☐ Decodes A1-0A
- ☐ Synchronous Clock/Data Outputs
- ☐ 5 MBit Data Rate
- ☐ Address Mark Detection
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

PIN CONFIGURATION



GENERAL DESCRIPTION

The HDC 1100-03 Address Mark Detector Provides an efficient means of detecting Address Mark Fields in an MFM (NRZ) data stream. MFM clocks and data are fed to the device along with a window clock generated by an external data separator. The HDC 1100-03 searches the data stream for a DATA = A1, CLK = 0A pattern and produces and AM DET signal when the pattern has been found. NRZ data is output from the device for driving a serial/parallel converter. An uncommitted latch is also provided for use by the data separator circuitry if required.



SECTION VI

DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{\text{RCLK}}$	$\overline{\text{READ CLOCK}}$	Complimentary clock inputs used to clock DIN and $\overline{\text{CLK IN}}$ into the AM detector.
3	RCLK	READ CLOCK	
2	$\overline{\text{DIN}}$	$\overline{\text{DATA INPUT}}$	MFM data pulses from the external Data Separator are connected on this line.
4	$\overline{\text{CLK IN}}$	$\overline{\text{CLOCK INPUT}}$	MFM clock pulses from the external Data Separator are connected on this line.
5	$\overline{\text{DOUT}}$	$\overline{\text{DATA OUTPUT}}$	Data Output from the internal Data Shift register, synchronized with DCLK.
6, 7, 13, 17	NC	No Connection	To be left open by the user.
8 11	$\overline{\text{TEST 1}}$ $\overline{\text{TEST 2}}$	$\overline{\text{TEST 1}}$ $\overline{\text{TEST 2}}$	To be left open by the user.
9	ENDET	ENABLE DETECTION	A logic 1 on this line enables the detection logic to search for a data $A1_{16}$ and clock.
10	V_{SS}	V_{SS}	GROUND.
12	DCLK	DATA CLOCK	Clock output that is synchronized with $\overline{\text{DATA OUT}}$ (Pin 5).
14	$\overline{\text{QOUT}}$	$\overline{\text{LATCH OUTPUT}}$	Signal output from the uncommitted latch.
15	$\overline{\text{AMDET}}$	$\overline{\text{ADDRESS MARK DETECT}}$	Complimentary Address Mark Detector output. These signals will go active when a Data = $A1_{16}$ Clock = $0A_{16}$ pattern is detected in the data stream.
16	AMDET	ADDRESS MARK DETECT	
18	CP	CLOCK PULSE	A low-to-high transition on this line will cause the $\overline{\text{QOUT}}$ (Pin 14) to be latched at a logic 0.
19	$\overline{\text{RST}}$	$\overline{\text{RESET}}$	A logic 0 on this line will cause the QOUT (Pin 14) signal to be set at a logic 1.
20	V_{CC}	V_{CC}	+5V power supply input.

OPERATION

Prior to shifting data through the device, the internal logic must be initialized. While the ENDET (Pin 9) line is at a logic 0, shifting of data will be inhibited and AMDET, $\overline{\text{AMDET}}$, DCLK, and $\overline{\text{DATA OUT}}$ will remain inactive.

When ENDET is at a logic 1, shifting is enabled. NRZ data is entered on the $\overline{\text{DIN}}$ line (Pin 2) and shifted on the high-to-low transition of $\overline{\text{RCLK}}$ (Pin 1). NRZ clocks are entered on the $\overline{\text{CLK IN}}$ line, and shifted on the high-to-low transition of RCLK (Pin 3). The $\overline{\text{DOUT}}$ line (Pin 5) is tied to the last stage of the Internal Data Shift register and will reflect information clocked into the $\overline{\text{DIN}}$ line delayed by 8 bits.

While each bit is being shifted, a 16 bit comparator is continuously checking the parallel contents of the shift registers for the DATA = $A1_{16}$ CLK = $0A_{16}$ pattern. When this pattern is detected, $\overline{\text{AMDET}}$ will be set to a logic 0 and AMDET will be set to a logic 1. $\overline{\text{AMDET}}$ and AMDET will remain latched until the device is re-initialized by forcing ENDET to a logic 0.

When an AM is detected, DCLK will begin to toggle. Data present on the $\overline{\text{DOUT}}$ line may then be clocked into an external serial/parallel converter. DCLK will remain inactive when ENDET is held at a logic 0.

An uncommitted edge-triggered flip/flop has been provided to facilitate the detection of high-frequency by the data separator, but may be used for any purpose. The low-to-high transition of CP (Pin 18) will set the $\overline{\text{QOUT}}$ (Pin 14) to a logic 0. $\overline{\text{QOUT}}$ may be reset back to a logic 1 by a low level on the RST line (Pin 19).

$\overline{\text{TEST1}}$ and $\overline{\text{TEST2}}$ are output lines. $\overline{\text{TEST1}}$ is an active low pulse when an $A1_{16}$ is detected, and $\overline{\text{TEST2}}$ is an active low pulse when a $0A_{16}$ is detected. These signals are used for test points and therefore should be left open by the user if not required.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +50°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +7.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.2V
Power Dissipation 0.75W

*Stresses above those listed may cause permanent damage to the device. This is a stress rat... operation of the device at these or at any other condition above those indicated in the operational sections of t...

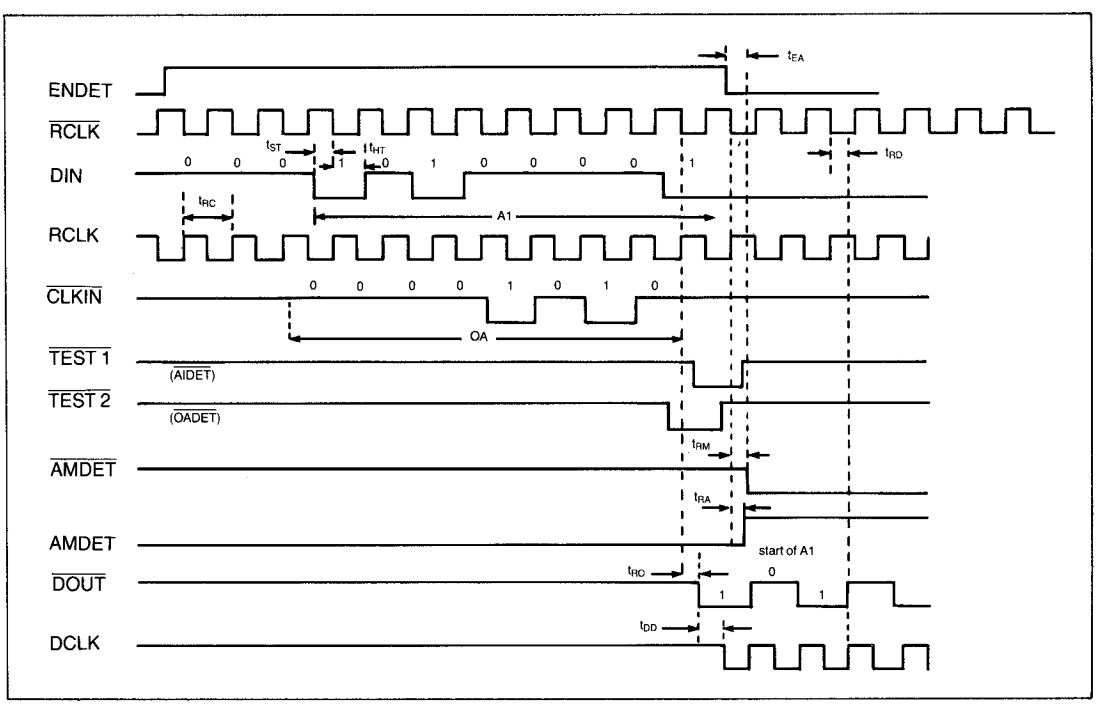
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.7	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{RC}	RCLK Frequency			5.25	MHZ	
t_{ST}	Data Setup time	40			nsec	
t_{HT}	Data Hold time	10			nsec	
t_{DD}	$\overline{DOUT}$ to DCLK DELAY			110	nsec	
t_{RD}	↓ $\overline{RCLK}$ to ↑ DCLK			120	nsec	
t_{RA}	↓ $\overline{RCLK}$ to ↑$\overline{AMDET}$			115	nsec	
t_{RM}	↓ $\overline{RCLK}$ to ↓ $\overline{AMDET}$			125	nsec	
t_{RO}	↓ $\overline{RCLK}$ to $\overline{DOUT}$			135	nsec	
t_{EA}	↓ $\overline{ENDET}$ to ↓ $\overline{AMDET}$			130	nsec	
t_{RQ}	↓ $\overline{RST}$ to ↑ $\overline{QOUT}$			110	nsec	
t_{RW}	Pulse width of $\overline{RST}$	50			nsec	
t_{CW}	CP Pulse width	90			nsec	
t_{CQ}	↑ CP to ↓ $\overline{QOUT}$			106	nsec	



SECTION VI

STANDARD MICROSYSTEMS CORPORATION

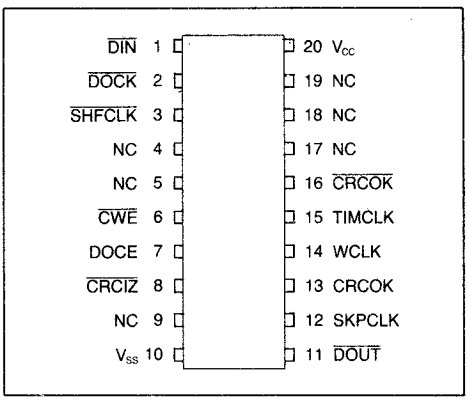
HDC 1100-04
PRELIMINARY

Hard Disk CRC Checker/Generator

FEATURES

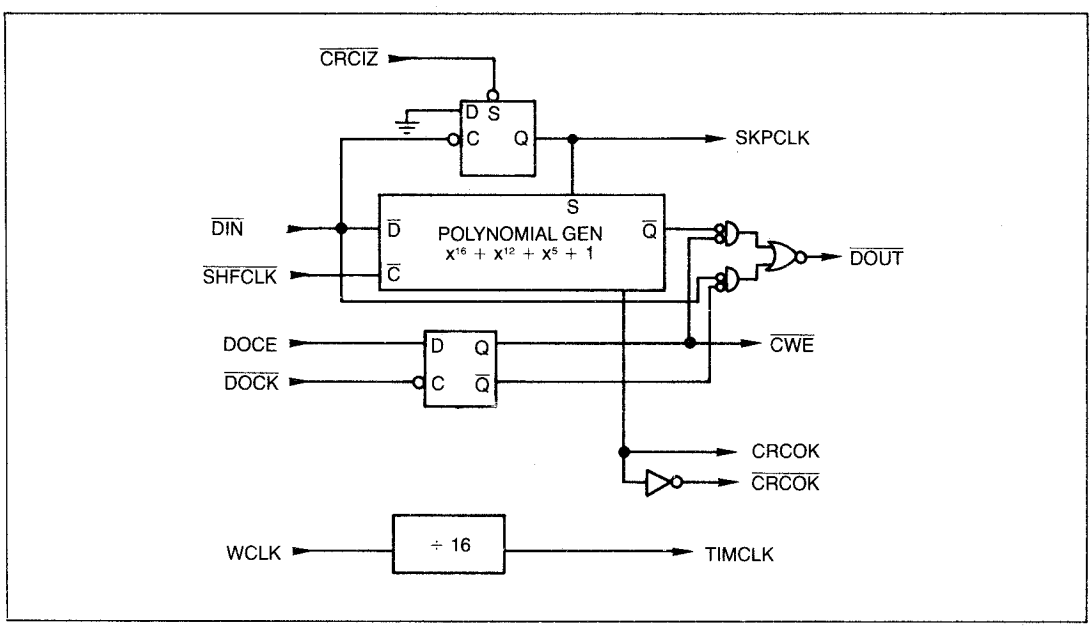
- ☐ Single +5 Volt Power Supply
- ☐ Generates/Checks CRC
- ☐ Latched Error Outputs
- ☐ CCITT-16 CRC
- ☐ Automatic Preset
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

PIN CONFIGURATION



GENERAL DESCRIPTION

The HDC 1100-04 CRC Checker/Generator generates a Cyclic Redundancy Checkword from a serial data stream, and checks for the proper CRC in a received serial data stream. In addition to the transmitted CRC output, complimentary latched "CRCOK" outputs are provided to indicate CRC errors in the check mode.



SECTION VI

DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{DIN}$	$\overline{DATA\ INPUT}$	Active low serial input data stream is used to generate/check the 2 byte CRC word.
2	$\overline{DOCK}$	$\overline{DATA\ OR\ CRC\ WORD\ CLOCK}$	After a byte of data has been transferred, in, this input signal is used to latch the state of DOCE in an internal D flop with a high to low transition.
3	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	The falling edge shifts data bits into the CRC generator/checker. It also transfers the CRC check word to $\overline{DOUT}$ in the write mode (DOCE = LOW). The rising edge also activates the CRCOK lines in the read mode when no error is found.
4, 5	N.C.	NO CONNECTION	
6	$\overline{CWE}$	$\overline{CHECK\ WORD\ ENABLE}$	This active low output indicates that the CRC checkword is being output on the $\overline{DOUT}$ line. When $\overline{CWE}$ is high, data is being output on $\overline{DOUT}$.
7	DOCE	DATA OR CRC ENABLE	Initially, this input line is held high to direct input data (pin 1) to the output data (pin 11). After the next to the last BYTE is transmitted but before the last BYTE occurs DOCE must be low to direct the 2 CRC check bytes to DOUT (pin 11). DOCE must be maintained low for a minimum of 2 byte times. DOCE is used only in the write mode.
8	$\overline{CRCIZ}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ INITIALIZE}$	When this line is at a logic 0, the SKPCLK output line is held high and the CRC generator is held preset to hex "FFFF."
9	N.C.	NO CONNECTION	NO CONNECTION
10	V_{SS}	GROUND	GROUND.
11	$\overline{DOUT}$	$\overline{DATA\ OUTPUT}$	In the write mode, this line outputs the unmodified data stream along with the 2 byte CRC word appended to the end of the stream.
12	SKPCLK	SKIP CLOCK	The first high-to-low transition on $\overline{DIN}$ (pin 1) resets SKPCLK low and enables the CRC to either generate or check the CRC word.
13	CRCOK	CYCLIC REDUNDANCY CHECK OKAY	In the read mode, after the 2 byte CRC word is entered on $\overline{DIN}$ and no error has been detected, this line is set high to indicate no errors have occurred. This line will then remain high as long as $\overline{DIN}$ is maintained high.
14	WCLK	WRITE CLOCK	This input clock is divided by 16 to produce TIMCLK (pin 15) and has no effect on the rest of the internal circuitry.
15	TIMCLK	TIMING CLOCK	See above.
16	$\overline{CRCOK}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ OKAY}$	Complementary output version of CRCOK (pin 13).
17-19	N.C.	NO CONNECTION	
20	V_{CC}	V_{CC}	+5V power supply input.

OPERATION

Prior to shifting data thru the device (either in the read or write modes) the CRC generator/checker is initialized by strobing the $\overline{CRCIZ}$ (pin 8) low. This forces the SKPCLK (pin 12) line to the high state. The first low going transition on $\overline{DIN}$ (pin 1), namely the most significant bit of an address mark, resets the SKPCLK line. The HDC 110-04 has now been properly initialized and is ready to generate/check the CRC bytes. The CRCOK and $\overline{CRCOK}$ lines should be set to their inactive states.

In the write mode, initially the DOCE (pin 7) is held high and a pseudo DOCK is produced by supplying a string of zeros before the address mark. This ensures the proper state of the internal D flip flip to gate input data to the output line $\overline{DOUT}$ (pin 11). As shown in the block diagram the $\overline{CWE}$ (pin 6) will be set high. Sometime between the next to the last and the last $\overline{DOCK}$ that indicates the end of the data stream, DOCE (pin 7) is lowered to ensure the smooth transition of the 2 byte CRC checkword to the output line DOUT (pin 11).

DOCE must be maintained low for a minimum of 2 byte times. After the CRC word is generated, $\overline{DOUT}$ will produce a string of zeros (i.e., held high). This portion of the circuitry is dormant in the read mode.

After proper initialization, input data is entered on DIN (pin 1) along with the 2 byte CRC word for the read mode of operation. At the end of the data stream, if no errors were detected the CRCOK (pin 13) is set high. Accordingly the

complementary output (pin 16) is set low. These output states will be maintained as long as DIN is held high and CRCIZ (pin 8) is not strobed. If the CRCOK lines do not become active, an error has been detected and a re-try is in order. If successive re-tries fail, an error flag may be set to determine a further course of action as desired by the user.

WCLK is divided by 16 to produce TIMCLK which may be used as a buffered step clock for SA1000 compatible drives.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +50°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +7.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.2V
Power Dissipation ..... 1 watt

*Stresses above those listed may cause permanent damage to the device. This is a stress rati... of the device at these or at any other condition above those indicated in the operational sections of this sp...

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

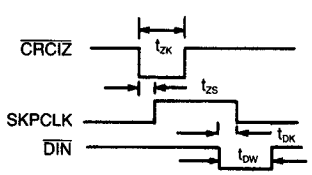
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200µA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{WT}	↑ WCLK to ↓ TIMCLK			95	nsec	
t_{WR}	↑ WCLK to ↑TIMCLK			85	nsec	
t_{ZS}	↓ $\overline{\text{CRCIZ}}$ to ↑ SKPCLK			120	nsec	
t_{ZK}	$\overline{\text{CRCIZ}}$ pulse width	90			nsec	
t_{BS}	$\overline{\text{DOCE}}$ set up time w.r.t. ↓ $\overline{\text{DOCK}}$	20			nsec	
t_{BH}	$\overline{\text{DOCE}}$ hold time w.r.t. ↓ $\overline{\text{DOCK}}$	40			nsec	
t_{DD}	$\overline{\text{DIN}}$ to $\overline{\text{DOUT}}$ delay			105	nsec	CWE set high

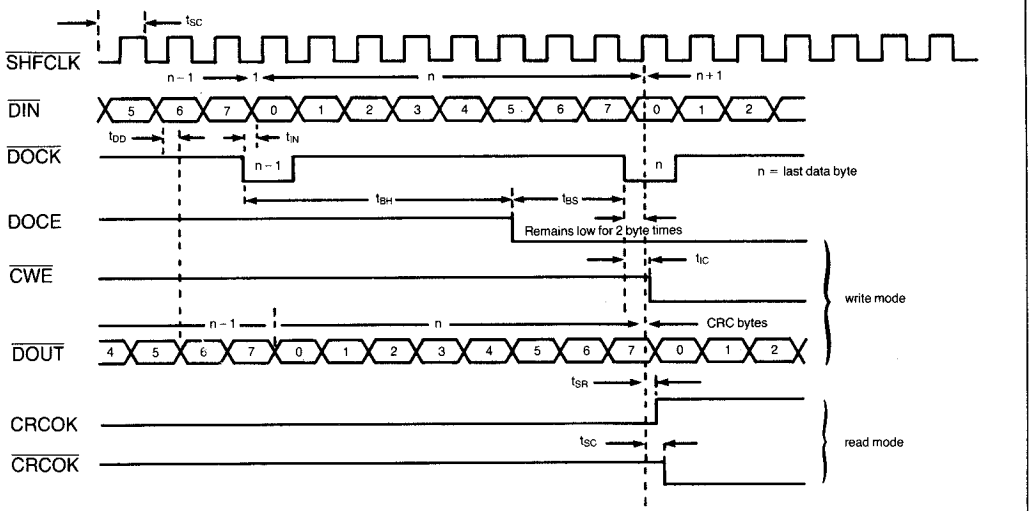
SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{DK}	↓$\overline{\text{DIN}}$ to ↓ SKPCLK			120	nsec	
t_{DW}	$\overline{\text{DIN}}$ P.W. to reset SKPCLK	50			nsec	
t_{IC}	↓ $\overline{\text{DOCK}}$ to ↓ $\overline{\text{CWE}}$			120	nsec	
t_{BC}	↓ $\overline{\text{DOCK}}$ to ↑ $\overline{\text{CWE}}$			120	nsec	
t_{SC}	$\overline{\text{SHFCLK}}$ frequency			5.25	MHZ	
t_{SR}	↑ $\overline{\text{SHFCLK}}$ to ↑ CRCOK			85	nsec	
t_{SC}	↑ $\overline{\text{SHFCLK}}$ to ↓ $\overline{\text{CRCOK}}$			90	nsec	
t_{IN}	↓ $\overline{\text{DOCK}}$ to ↓ $\overline{\text{DIN}}$			90	nsec	

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = +5.0V



Initialize

SECTION VI



Write Mode

STANDARD MICROSYSTEMS CORPORATION

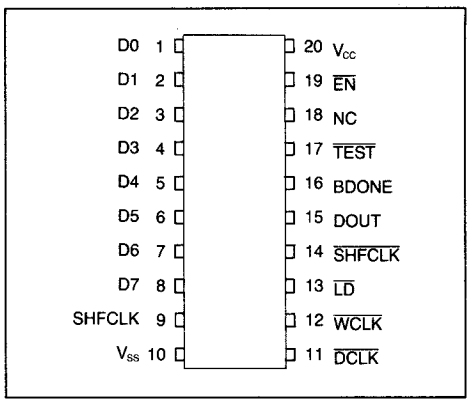
HDC 1100-05
PRELIMINARY

Hard Disk Parallel to Serial Converter

FEATURES

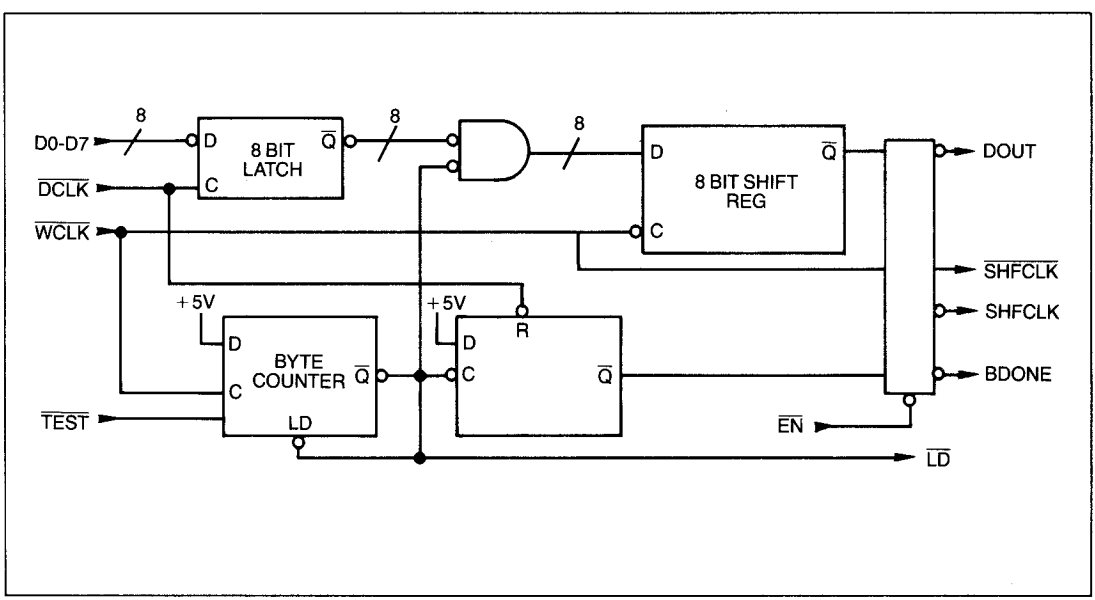
- ☐ Single +5 Volt Power Supply
- ☐ Double Buffered
- ☐ Byte Strobe Outputs
- ☐ 5 Mbit Data Rate
- ☐ Parallel In/Serial Out
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

PIN CONFIGURATION



GENERAL DESCRIPTION

The HDC 1100-05 converts bytes of parallel data to a serial data stream for writing to disk memories or other serial devices. Parallel data is entered via the D0-D7 lines. A synchronous byte counter is used to signify that 8 bits of data have been shifted out and that the 8 bit latch is ready to be reloaded. The double buffering of the data permits another byte to be loaded while the previous byte is in the process of being shifted.



SECTION VI

DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	SYMBOL	NAME	FUNCTION
1-8	D0-D7	DATA 0-DATA 7	8 bit parallel data inputs (bit 7 = MSB).
9	SHFCLK	SHIFT CLOCK	Inverted copy of $\overline{\text{WCLK}}$ (pin 12) which is active when ENABLE (pin 19) is at a logic 0.
10	V_{SS}	GROUND	GROUND.
11	$\overline{\text{DCLK}}$	$\overline{\text{DATA CLOCK}}$	Active low input signal resets the BDONE (pin 16) latch. The low-to-high (trailing edge) clocks the input data into the internal 8 bit latch.
12	$\overline{\text{WCLK}}$	$\overline{\text{WRITE CLOCK}}$	The high-to-low (↓) edge of this clock signal is used to shift the data out serially. The low-to-high (↑) edge is used to update the internal byte counter (modulo 8).
13	$\overline{\text{LD}}$	$\overline{\text{LOAD}}$	This active low signal indicates that the Byte Counter is being preset to 1. Normally left open by the user.
14	$\overline{\text{SHFCLK}}$	$\overline{\text{SHIFT CLOCK}}$	Delayed copy of $\overline{\text{WCLK}}$ (pin 12) which is active when EN (pin 19) is at a logic 0.
15	DOUT	DATA OUT	Serial data output enabled by EN (pin 19).
16	BDONE	BYTE DONE	This output signal is forced to a logic 1 whenever 8 bits of data have been shifted out. BDONE remains in this state unless reset by the loading of another byte of data.
17	$\overline{\text{TEST}}$	$\overline{\text{TEST INPUT}}$	This pin must be left open by the user.
18	NC	No Connection	NO CONNECTION
19	$\overline{\text{EN}}$	$\overline{\text{ENABLE}}$	This active low signal enables DOUT, $\overline{\text{SHFCLK}}$, SHFCLK, and BDONE outputs. When high, these output signals are in a high impedance state.
20	V_{CC}	V_{CC}	+5 power supply input.

OPERATION

Prior to loading the HDC 1100-05, it is recommended that 00H (or FF) be loaded into the input buffers to ensure that DOUT is at a fixed level. $\overline{\text{EN}}$ (pin 19) is set to a logic 0 to enable the device outputs.

Data is entered on the D0-D7 input lines and is strobed into the data latches on the rising edge of $\overline{\text{DCLK}}$ (pin 11). $\overline{\text{DCLK}}$ also resets BCONE (pin 16). The first BDONE that comes up simply means that the HDC 1100-05 is ready to accept another byte of data and that the previous byte entered is in the process of being shifted out. If the BDONE is serviced prior to every 8th $\overline{\text{WRITE CLOCK}}$ pulse the output data will represent a contiguous block of the bytes entered. Due to the asynchronous nature of the HDC 1100-05, the input data will be available in serial form at the output anywhere from 8 to 16 write clock cycles later.

Data is shifted out on the high-to-low transition of the $\overline{\text{WCLK}}$ (pin 12). The low-to-high transition of $\overline{\text{WCLK}}$ increments a byte counter which in turn sets the BDONE signal high after 8 bits of data have been shifted out. The low-to-high transition of BDONE also causes the loading of the data buffer into the shift register. The data buffer is now ready to be reloaded with the next byte.

The loading of the next byte automatically clears the BDONE signal. The entire process as outlined above is repeated. BDONE always needs to be serviced within 8 WCLK cycles unless the next byte to be transmitted is the same as the previous byte.

Four signals, BDONE, DOUT, SHFCLK, and $\overline{\text{SHFCLK}}$, can be placed in a high impedance state of setting $\overline{\text{EN}}$ (pin 19) to a logic 1. Likewise, $\overline{\text{EN}}$ must be at a logic 0 in order for these signals to drive any external device.

The $\overline{\text{TEST}}$ pin is internally OR'd with the counter output to produce the $\overline{\text{LD}}$ (pin 13) signal. This is used to inhibit the bit counter by external means for test purposes. It is recommended that $\overline{\text{TEST}}$ be left open by the user. An internal pullup register is tied to this pin to satisfy the appropriate logic level required for proper device operation.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +50°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +7.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.2V
Power Dissipation ..... 1.0 watt

*Stresses above those listed may cause permanent damage to the device. This is a stress rati... ...tion of the device at these or at any other condition above those indicated in the operational sections of this sp...

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

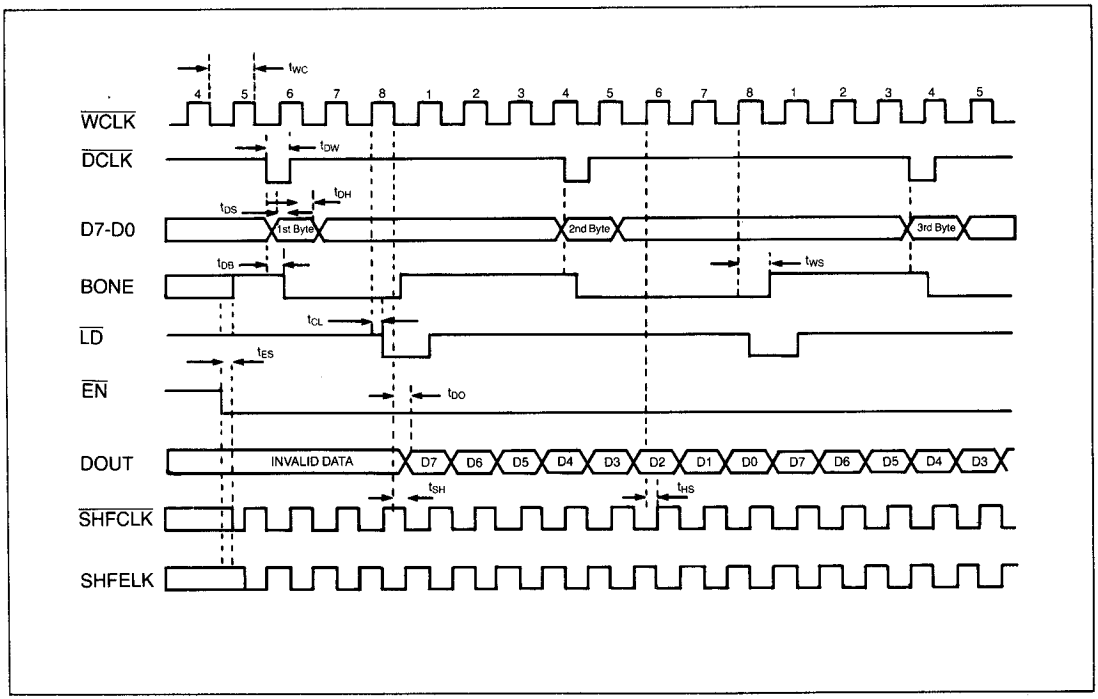
DC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{OH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200µA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{WC}	WCLK frequency			5.25	MHZ	
t_{DW}	DCLK pulse width	50			nsec	
t_{DS}	Data set-up w.r.t. ↑ DCLK	30			nsec	
t_{DH}	Data hold time w.r.t. ↑ DCLK	30			nsec	
t_{DB}	↓ DCLK to ↓ BDONE			130	nsec	EN = 0
t_{DO}	↓ WCLK to DOUT			130	nsec	EN = 0
t_{SH}	↓ WCLK to ↓ SHFCLK			75	nsec	EN = 0
t_{HS}	↓ WCLK to ↑ SHFCLK			70	nsec	EN = 0
t_{WB}	↑ WCLK to ↑BDONE	75		180	nsec	
t_{ES}	↓ $\overline{EN}$ to BDONE, DOUT SHFCLK ACTIVE			25	nsec	
t_{CL}	↑ WCLK to ↓ $\overline{LD}$			50	nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V



SECTION VI

STANDARD MICROSYSTEMS CORPORATION

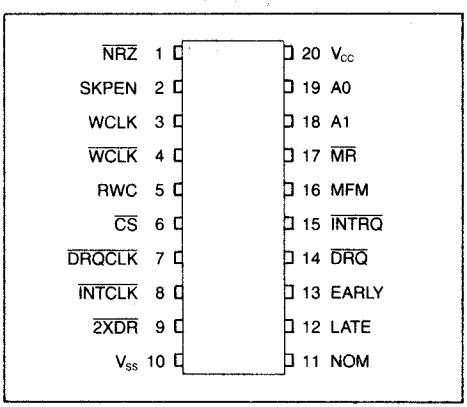
HDC 1100-12
PRELIMINARY

Hard Disk Improved MFM Generator

FEATURES

- ☐ Single +5 Volt Power Supply
- ☐ Write Precompensation
- ☐ Address Mark Generation
- ☐ 5 Mbit Data Rate
- ☐ Converts NRZ to MFM
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

PIN CONFIGURATION

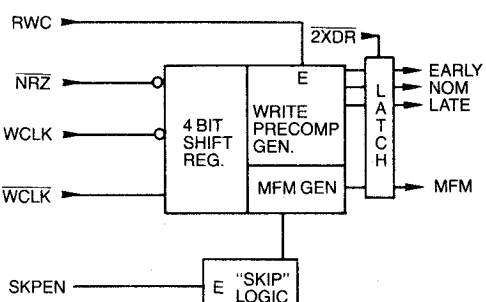


GENERAL DESCRIPTION

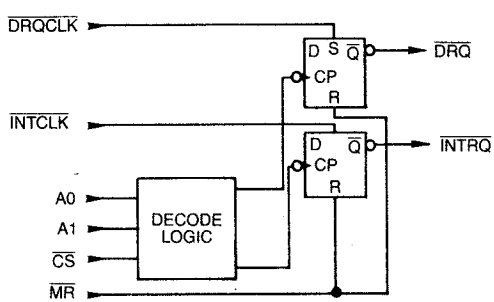
The HDC 1100-12 "improved" MFM Generator converts serial NRZ data into an MFM (Modified Frequency Modulated) data stream. The MFM signal may be used to record information on a Winchester Disk.

In addition, the HDC 1100-12 generates Write Precompensation signals required to compensate for bit shift effects on the recording medium.

The HDC 1100-12 has the ability to delete clock pulses in the outgoing data stream in order to record Address Marks.



MFM GENERATOR



INTERRUPT CONTROLLER

SECTION VI

DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{NRZ}$	NON-RETURN-TO ZERO	NRZ data input that is strobed into the MFM generator by WCLK (↓).
2	SKPEN	SKIP ENABLE	This input arms the SKIP logic for recording Address Marks when set to a logic 1.
3	WCLK	WRITE CLOCK	Complimentary clock inputs. $\overline{NRZ}$ data is clocked into the MFM Generator on the high-to-low transition of WCLK (pin 3).
4	$\overline{WCLK}$	WRITE CLOCK	
5	RWC	REDUCED WRITE CURRENT	This signal when high, enables EARLY, LATE and NOM outputs.
9	$\overline{2 \times DR}$	2 TIMES DATA RATE	This input is used to latch EARLY, LATE, NOM and MFM outputs.
10	V_{SS}	V_{SS}	Ground.
11	NOM	NOMINAL	Output signal from the Write Precompensation Logic used to signify that data is to be written nominal.
12	LATE	LATE	Output signal from the Write Precompensation Logic used to signify that data is to be shifted LATE before writing.
13	EARLY	EARLY	Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing.
16	MFM	MFM DATA	This output contains the MFM encoded data derived from the $\overline{NRZ}$ (pin 1) line.
6	$\overline{CS}$	CHIP SELECT	Low input signal used to enable the Address decode logic.
8	$\overline{INTCLK}$	INTERRUPT REQUEST CLOCK	A high-to-low transition on this line will latch the INTRQ (pin 15) at a logic 0.
7	$\overline{DRQCLK}$	DATA REQUEST CLOCK	A high-to-low transition on this line will latch the DRQ (pin 14) at a logic 0.
15	$\overline{INTRQ}$	INTERRUPT REQUEST	This output is latched at a logic 0 when INTCLK (pin 8) makes a high-to-low transition while the decode logic is disabled.
14	$\overline{DRQ}$	DATA REQUEST	This output is latched at a logic 0 when DRQCLK (pin 7) makes a high-to-low transition while the decode logic is disabled.
17	$\overline{MR}$	MASTER RESET	A low level on this line causes DRQ and INTRQ to set at a logic 1.
18, 19	A_0, A_1	ADDRESS 1, 0	When CS is low and the address lines are high, INTRQ is cleared; if the address lines are low then DRQ gets cleared. (i.e. set at a logic 1).
20	V_{CC}	V_{CC}	+5V power supply input.

OPERATION

The HDC 1100-12 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic may be used to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the NRZ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1.

The SKPEN signal is used to record a unique data/clock pattern as an Address Mark, using A1 data with 0A clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the NRZ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the A1 16) the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of OE_{16}. Although other data patterns may be used,

$\overline{MR}$	A_1	A_0	$\overline{CS}$	$\overline{DRQ}$	$\overline{INTRQ}$
0	X	X	X	H	H
1	X	X	1	Q_N	Q_N
1	0	0	0	H	Q_N
1	1	1	0	Q_N	H
1	1	0	0	Q_N	Q_N
1	0	1	0	Q_N	Q_N

X = Don't care Q_N = remains at previous state

INTERRUPT REQUEST LOGIC TABLE

the MSB of the pattern must be a 1 (80_{16} or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests (INTRQ) by selecting $\overline{CS}$ (pin 6) in combination with A0 and A1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INTRQ}$ simultaneously. $\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only by a low level or $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A1 and A0.

LAST DATA SENT	SENDING	TO BE SENT NEXT	EARLY	LATE	NOM
X 1	1	0	H	L	L
X 0	1	1	L	H	L
0 0	0	1	H	L	L
1 0	0	0	L	H	L
ANY OTHER PATTERN			L	L	H

WRITE PRECOMPENSATION LOGIC TABLE

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +50°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +7.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.2V
Power Dissipation ..... 1.0 watt

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and fu... device at these or at any other condition above those indicated in the operational sections of this specification is ...

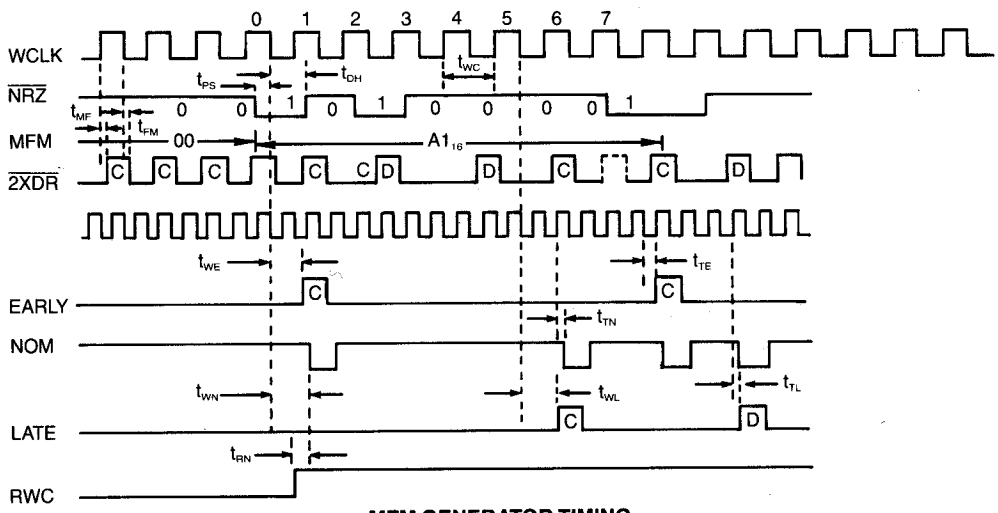
DC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200µA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{FR}	WCLK FREQUENCY			5.25	MHZ	
t_{DS}	Data Setup w.r.t. ↓ WCLK	10			nsec	
t_{DH}	Data hold w.r.t. ↓ WCLK	25			nsec	
t_{MF}	↑ WCLK to ↑MFM delay			210	nsec	Pin 1 LOW
t_{FM}	↓ WCLK to ↓ MFM delay			230	nsec	Pin 1 LOW
t_{WN}	Data delay to NOM from ↓ WCLK			240	nsec	
t_{WE}	Data delay to EARLY from ↓ WCLK			230	nsec	
t_{WL}	Data delay to LATE from ↓ WCLK			230	nsec	
t_{MR}	Master reset pulse width	50			nsec	
t_{MD}	↓ $\overline{MR}$ to ↑ $\overline{DRQ}$			150	nsec	
t_{MI}	↓MR to ↑ $\overline{INTRQ}$			150	nsec	
t_{DQ}	$\overline{DRQCLK}$ pulse width	50			nsec	
t_{IQ}	$\overline{INTCLK}$ pulse width	50			nsec	
t_{DD}	↓ $\overline{DRQCLK}$ to $\overline{DRQ}$			120	nsec	
t_{II}	↓ $\overline{INTCLK}$ to $\overline{INTRQ}$			120	nsec	
t_{AD}	↓ AX to ↑ $\overline{DRQ}$			145	nsec	
t_{AI}	↑ AX to ↑ $\overline{INTRQ}$			160	nsec	
t_{CD}	↓ $\overline{CS}$ to ↑ $\overline{DRQ}$			145	nsec	
t_{CI}	↓ $\overline{CS}$ to ↑ $\overline{INTRQ}$			180	nsec	
t_{RN}	↑ RWC to ↓ NOM			145	nsec	
t_{TE}	↓ $\overline{2XDR}$ to ↑ EARLY			75	nsec	
t_{TN}	↓ $\overline{2XDR}$ to ↑ NOM			75	nsec	
t_{TL}	↓ $\overline{2XDR}$ to ↑ LATE			75	nsec	

Notes: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V.



MFM GENERATOR TIMING