# TMS 5501 MULTIFUNCTION INPUT/OUTPUT CONTROLLER

## 1. INTRODUCTION

### 1.1 DESCRIPTION

The TMS 5501 is a multifunction input/output circuit for use with TI's TMS 8080 CPU. It is fabricated with the same N-channel silicon-gate process as the TMS 8080 and has compatible timing, signal levels, and power supply requirements. The TMS 5501 provides a TMS 8080 microprocessor system with an asynchronous communications interface, data I/O buffers, interrupt control logic, and interval timers.

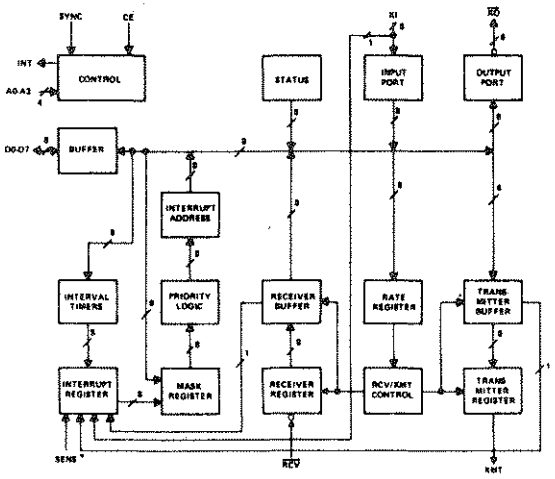



FIGURE 1–TMS 5501 BLOCK DIAGRAM

The I/O section of the TMS 5501 contains an eight-bit parallel input port and a separate eight-bit parallel output port with storage register. Five programmable interval timers provide time intervals from 64 μs to 16.32 ms.

The interrupt system allows the processor to effectively communicate with the interval timers, external signals, and the communications interface by providing TMS 8080-compatible interrupt logic with masking capability.

Data transfers between the TMS 5501 and the CPU are carried by the data bus and controlled by the interrupt, chip enable, sync, and address lines. The TMS 8080 uses four of its memory-address lines to select one of 14 commands to which the TMS 5501 will respond. These commands allow the CPU to:

- read the receiver buffer
- read the input port
- read the interrupt address
- read TMS 5501 status
- issue discrete commands
- load baud rate register
- load the transmitter buffer
- load the output port
- load the mask register
- load an interval timer

The commands are generated by executing memory referencing instructions such as MOV (register to memory) with the memory address being the TMS 5501 command. This provides a high degree of flexibility for I/O operations by letting the systems programmer use a variety of instructions.

### 1.2 SUMMARY OF OPERATION

**Addressing the TMS 5501**

A convenient method for addressing the TMS 5501 is to tie the chip enable input to the highest order address line of the CPU's 16-bit address bus and the four TMS 5501 address inputs to the four lowest order bits of the bus. This, of course, limits the system to 32,768 words of memory but in many applications the full 65,536 word memory addressing capability of the TMS 8080 is not required.

**Communications Functions**

The communications section of the TMS 5501 is an asynchronous transmitter and receiver for serial communications and provides the following functions:

Programmable baud rate – A CPU command selects a baud rate of 110, 150, 300, 1200, 2400, 4800, or 9600 baud.

Incoming character detection – The receiver detects the start and stop bits of an incoming character and places the character in the receive buffer.

Character transmission – The transmitter generates start and stop bits for a character received from the CPU and shifts it out.

Status and command signals – Via the data bus, the TMS 5501 signals the status of: framing error and overrun error flags; data in the receiver and transmitter buffers; start and data bit detectors; and end-of-transmission (break) signals from external equipment. It also issues break signals to external equipment.

**Data Interface**

The TMS 5501 moves data between the CPU and external devices through its internal data bus, input port, and output port. When data is present on the bus that is to be sent to an external device, a Load Output Port (LOP) command from the CPU puts the data on the $\overline{XO}$ pins of the TMS 5501 by latching it in the output port. The data remains in the port until another LOP command is received. When the CPU requires data that is present on the External Input (XI) lines, it issues a command that gates the data onto the internal data bus of the TMS 5501 and consequently onto the CPU's data bus at the correct time during the CPU cycles.

**Interval Timers**

To start a countdown by any of the five interval timers, the program selects the particular timer by an address to the TMS 5501 and loads the required interval into the timer via the data bus. Loading the timer activates it and it counts down in increments of 64 microseconds. The 8-bit counters provide intervals that vary in duration from 64 to 16,320 microseconds. Much longer intervals can be generated by cascading the timers through software. When a timer reaches zero, it generates an interrupt that typically will be used to point to a subroutine that performs a servicing function such as polling a peripheral or scanning a keyboard. Loading an interval value of zero causes an immediate interrupt. A new value loaded while the interval timer is counting overrides the previous value and the interval timer starts counting down the new interval. When an interval timer reaches zero it remains inactive until a new interval is loaded.

### Servicing Interrupts

The TMS 5501 provides a TMS 8080 system with several interrupt control functions by receiving external interrupt signals, generating interrupt signals, masking out undersired interrupts, establishing the priority of interrupts, and generating RST instructions for the TMS 8080. An external interrupt is received on pin 22, SENS. An additional external interrupt can be received on pin 32, XI7, if selected by a discrete command from the TMS 8080 (See Figure 4). The TMS 5501 generates an interrupt when any of the five interval timers count to zero. Interrupts are also generated when the receiver buffer is loaded and when the transmitter buffer is empty.

When an interrupt signal is received by the interrupt register from a particular source, a corresponding bit is set and gated to the mask register. A pattern will have previously been set in the mask register by a load-mask-register command from the TMS 8080. This pattern determines which interrupts will pass through to the priority logic. The priority logic allows an interrupt to generate an RST instruction to the TMS 8080 only if there is no higher priority interrupt that has not been accepted by the TMS 8080. The TMS 5501 prioritizes interrupts in the order shown below:

1st – Interval Timer #1
2nd – Interval Timer #2
3rd – External Sensor
4th – Interval Timer #3
5th – Receiver Buffer Loaded
6th – Transmitter Buffer Emptied
7th – Interval Timer #4
8th – Interval Timer #5 or an External Input (XI 7)

The highest priority interrupt passes through to the interrupt address logic, which generates the RST instruction to be read by the TMS 8080. See Table 3 for relationship of interrupt sources to RST instructions and Figures 6 and 8 for timing relationships.

The TMS 5501 provides two methods of servicing interrupts; an interrupt-driven system or a polled-interrupt system. In an interrupt-driven system, the INT signal of the TMS 5501 is tied to the INT input of the TMS 8080. The sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt signal and readies the appropriate RST instruction. (2) The TMS 5501 INT output, tied to the TMS 8080 INT input, goes high signaling the TMS 8080 that an interrupt has occured. (3) If the TMS 8080 is enabled to accept interrupts, it sets the INTA (interrupt acknowledge) status bit high at SYNC time of the next machine cycle. (4) If the TMS 5501 has previously received an interrupt-acknowledge-enable command from the CPU (see Bit 3, Paragraph 2.2.5), the RST instruction is transferred to the data bus.

In a polled-interrupt system, INT is not used and the sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt and readies the RST instruction. (2) The TMS 5501 interrupt-pending status bit (see Bit 5, Paragraph 2.2.4) is set high (the interrupt-pending status bit and the INT output go high simultaneously). (3) At the prescribed time, the TMS 8080 polls the TMS 5501 to see if an interrupt has occurred by issuing a read-TMS 5501-status command and reading the interrupt-pending bit. (4) If the bit is high, the TMS 8080 will then issue a read-interrupt-address command, which causes the TMS 5501 to transfer the RST instruction to the data bus as data for the instruction being executed by the TMS 8080.

## 1.3 APPLICATIONS

### Communications Terminals

The functions of the TMS 5501 make it particularly useful in TMS 8080-based communications terminals and generally applicable in systems requiring periodic or random servicing of interrupts, generation of control signals to external devices, buffering of data, and transmission and reception of asynchronous serial data. As an example, a system configuration such as shown in Figure 2 can function as the controller for a terminal that governs employee entrance into a plant or security areas within a plant. Each terminal is identified by a central computer through ID switches. The central system supplies each terminal's RAM with up to 16 employee access categories applicable to that terminal. These categories are compared with an employee's badge character when he inserts his badge into the badge sensor. If a

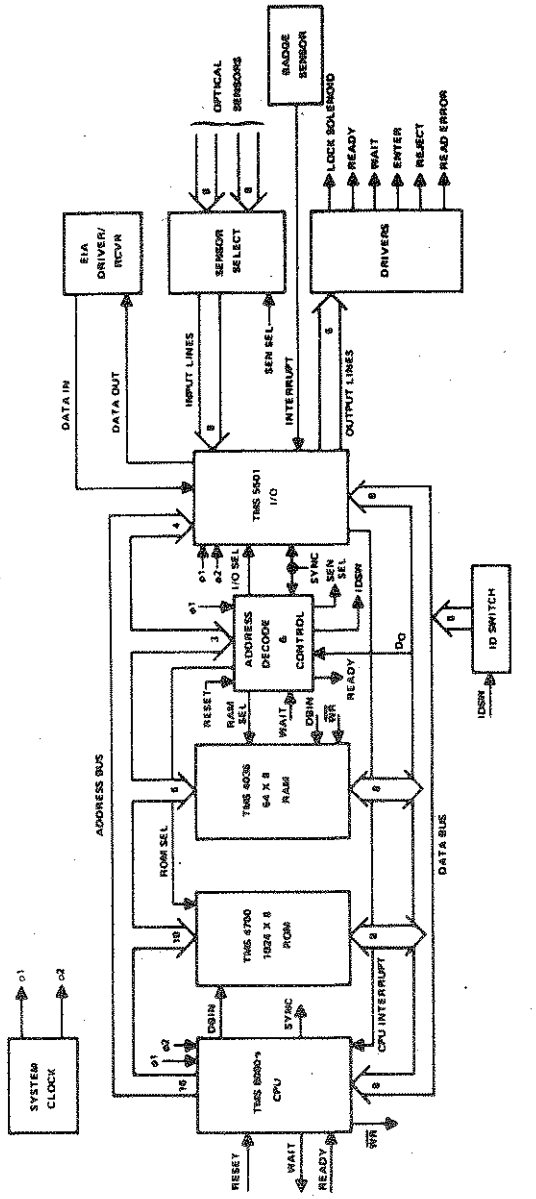



FIGURE 2–ACCESS CONTROL SYSTEM BLOCK DIAGRAM

match is not found, a reject light will be activated. If a match is found, the terminal will transmit the employee's badge number and access category to the central system, and a door unlock solenoid will be activated for 4 seconds. The central computer then may take the transmitted information and record it along with time and date of access.

The TMS 4700 is a 1024 x 8 ROM that contains the system program, and the TMS 4036 is a 64 x 8 RAM that serves as the stack for the TMS 8080 and storage for the access category information. TTL circuits control chip-enable information carried by the address bus. Signals from the CPU gate the address bits from the ROM, the RAM, or the TMS 5501 onto the data bus at the correct time in the CPU cycle. The clock generator consists of four TTL circuits along with a crystal, needed to maintain accurate serial data assembly and disassembly with the central computer.

The TMS 5501 handles the asynchronous serial communication between the TMS 8080 and the central system and gates data from the badge reader onto the data bus. It also gates control and status data from the TMS 8080 to the door lock and badge reader and controls the time that the door lock remains open. The TMS 5501 signals the TMS 8080 when the badge reader or the communication lines need service. The functions that the TMS 5501 is to perform are selected by an address from the TMS 8080 with the highest order address line tied to the TMS 5501 chip enable input and the four lowest order lines tied to the address inputs.

## 2. OPERATIONAL AND FUNCTIONAL DESCRIPTION

This detailed description of the TMS 5501 consists of:

INTERFACE SIGNALS – a definition of each of the circuit's external connections

COMMANDS – the address required to select each of the TMS 5501 commands and a description of the response to the command.

### 2.1 INTERFACE SIGNALS

The TMS 5501 communicates with the TMS 8080 via four address lines: a chip enable line, an eight-bit bidirectional data bus, an interrupt line, and a sync line. It communicates with system components other than the CPU via eight external inputs, eight external outputs, a serial receiver input, a serial transmitter output, and an external sensor input. Table 1 defines the TMS 5501 pin assignments and describes the function of each pin.

**TABLE 1**
**TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS**

| SIGNATURE | PIN | DESCRIPTION |
|---|---|---|
| | | **INPUTS** |
| CE | 18 | Chip enable—When CE is low, the TMS 5501 address decoding is inhibited, which prevents execution of any of the TMS 5501 commands. |
| A3 | 17 | Address bus—A3 through A0 are the lines that are addressed by the TMS 8080 to select a particular |
| A2 | 16 | TMS 5501 function. |
| A1 | 15 | |
| A0 | 14 | |
| SYNC | 19 | Synchronizing signal—The SYNC signal is issued by the TMS 8080 and indicates the beginning of a machine cycle and availability of machine status. When the SYNC signal is active (high), the TMS 5501 will monitor the data bus bits D0 (interrupt acknowledge) and D1 ($\overline{WO}$, data output function). |
| $\overline{RCV}$ | 5 | Receiver serial data input line—$\overline{RCV}$ must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receive circuitry. |

**TABLE 1 (continued)**
**TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS**

| SIGNATURE | PIN | DESCRIPTION |
|---|---|---|
| | | **INPUTS** |
| XI 0 | 39 | External inputs—These eight external inputs are gated to the data bus when the read-external-inputs |
| XI 1 | 38 | function is addressed. External input n is gated to data bus bit n without conversion. |
| XI 2 | 37 | |
| XI 3 | 36 | |
| XI 4 | 35 | |
| XI 5 | 34 | |
| XI 6 | 33 | |
| XI 7 | 32 | |
| SENS | 22 | External interrupt sensing – A transition from low to high at SENS sets a bit in the interrupt register, which, if enabled, generates an interrupt to the TMS 8080. |
| | | **OUTPUTS** |
| $\overline{XO}$ 0 | 24 | External outputs—These eight external outputs are driven by the complement of the output |
| $\overline{XO}$ 1 | 25 | register; i.e., if output register bit n is loaded with a high (low) from data bus bit n by a load- |
| $\overline{XO}$ 2 | 26 | output register command, the external output n will be a low (high). The external outputs change |
| $\overline{XO}$ 3 | 27 | only when a load-output-register function is addressed. |
| $\overline{XO}$ 4 | 28 | |
| $\overline{XO}$ 5 | 29 | |
| $\overline{XO}$ 6 | 30 | |
| $\overline{XO}$ 7 | 31 | |
| XMT | 40 | Transmitter serial data output line—This line remains high when the TMS 5501 is not transmitting. |
| | | **DATA BUS INPUT/OUTPUT** |
| D0 | 13 | Data bus – Data transfers between the TMS 5501 and the TMS 8080 are made via the 8-bit |
| D1 | 12 | bidirectional data bus. D0 is the LSB. D7 is the MSB. |
| D2 | 11 | |
| D3 | 10 | |
| D4 | 9 | |
| D5 | 8 | |
| D6 | 7 | |
| D7 | 6 | |
| INT | 23 | Interrupt—When active (high), the INT output indicates that at least one of the interrupt conditions has occurred and that its corresponding mask-register bit is set. |
| | | **POWER AND CLOCKS** |
| $V_{SS}$ | 4 | Ground reference |
| $V_{BB}$ | 1 | Supply voltage (–5 V nominal) |
| $V_{CC}$ | 2 | Supply voltage (5 V nominal) |
| $V_{DD}$ | 3 | Supply voltage (12 V nominal) |
| $\phi 1$ | 20 | Phase 1 clock |
| $\phi 2$ | 21 | Phase 2 clock |

## 2.2 TMS 5501 COMMANDS

The TMS 5501 operates as memory device for the TMS 8080. Functions are initiated via the TMS 8080 address bus and the TMS 5501 address inputs. Address decoding to determine the command function being issued is defined in Table 2.

**TABLE 2**
**COMMAND ADDRESS DECODING**
**When Chip Enable Is High**

| A3 | A2 | A1 | A0 | COMMAND | FUNCTION | PARAGRAPH |
|---|---|---|---|---|---|---|
| L | L | L | L | Read receiver buffer | RBn → Dn | 2.2.1 |
| L | L | L | H | Read external inputs | XIn → Dn | 2.2.2 |
| L | L | H | L | Read interrupt address | RST → Dn | 2.2.3 |
| L | L | H | H | Read TMS 5501 status | (Status) → Dn | 2.2.4 |
| L | H | L | L | Issue discrete commands | See Figure 4 | 2.2.5 |
| L | H | L | H | Load rate register | See Figure 4 | 2.2.6 |
| L | H | H | L | Load transmitter buffer | Dn → TBn | 2.2.7 |
| L | H | H | H | Load output port | Dn → $\overline{XO}$n | 2.2.8 |
| H | L | L | L | Load mask register | Dn → MRn | 2.2.9 |
| H | L | L | H | Load interval timer 1 | Dn → Timer 1 | 2.2.10 |
| H | L | H | L | Load interval timer 2 | Dn → Timer 2 | 2.2.10 |
| H | L | H | H | Load interval timer 3 | Dn → Timer 3 | 2.2.10 |
| H | H | L | L | Load interval timer 4 | Dn → Timer 4 | 2.2.10 |
| H | H | L | H | Load interval timer 5 | Dn → Timer 5 | 2.2.10 |
| H | H | H | L | No function | | |
| H | H | H | H | No function | | |

RBn = Receiver buffer bit n
Dn = Data bus I/O terminal n
XIn = External input terminal n
RST = 11 ($IA_2$) ($IA_1$) ($IA_0$) 1 1 1 (see Table 3)
TBn = Transmit buffer bit n
$\overline{XO}$n = Output register bit n
MRn = Mask register bit n

**TABLE 3**
**RST INSTRUCTIONS**

| DATA BUS BIT 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | INTERRUPT CAUSED BY |
|---|---|---|---|---|---|---|---|---|
| H | H | H | L | L | L | H | H | Interval Timer 1 |
| H | H | H | H | L | L | H | H | Interval Timer 2 |
| H | H | H | L | H | L | H | H | External Sensor |
| H | H | H | H | H | L | H | H | Interval Timer 3 |
| H | H | H | L | L | H | H | H | Receiver Buffer |
| H | H | H | H | L | H | H | H | Transmitter Buffer |
| H | H | H | L | H | H | H | H | Interval Timer 4 |
| H | H | H | H | H | H | H | H | Interval Timer 5 or X17 |

The following paragraphs define the functions of the TMS 5501 commands.

**2.2.1 Read receiver buffer**

Addressing the read-receiver-buffer function causes the receiver buffer contents to be transferred to the TMS 8080 and clears the receiver-buffer-loaded flag.

**2.2.2 Read external input lines**

Addressing the read-external-inputs function transfers the states of the eight external input lines to the TMS 8080.

**2.2.3 Read interrupt address**

Addressing the read interrupt address function transfers the current highest priority interrupt address onto the data bus as read data. After the read operation is completed, the corresponding bit in the interrupt register is reset.

If the read-interrupt-address function is addressed when there is no interrupt pending, a false interrupt address will be read. TMS 5501 status function should be addressed in order to determine whether or not an interrupt condition is pending.

**2.2.4 Read TMS 5501 status**

Addressing the read-TMS 5501-status function gates the various status conditions of the TMS 5501 onto the data bus. The status conditions, available as indicated in Figure 3, are described in the following paragraphs.

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | START BIT DETECT | FULL BIT DETECT | INTRPT PENDING | XMIT BUFFER EMPTY | RCV BUFFER LOADED | SERIAL RCVD | OVERRUN ERROR | FRAME ERROR |

**FIGURE 3--DATA BUS ASSIGNMENTS FOR TMS 5501 STATUS**

**Bit 0, framing error**

A high in bit 0 indicates that a framing error was detected on the last character received (either one or both stop bits were in error). The framing error flag is updated at the end of each character. Bit 0 of the TMS 5501 status will remain high until the next valid character is received.

**Bit 1, overrun error**

A high in bit 1 indicates that a new character was loaded into the receiver buffer before a previous character was read out. The overrun error flag is cleared each time the read-I/O-status function is addressed or a reset command is issued.

**Bit 2, serial received data**

Bit 2 monitors the receiver serial data input line. This line is provided as a status input for use in detecting a break and for test purposes. Bit 2 is normally high when no data is being received.

**Bit 3, receiver buffer loaded**

A high in bit 3 indicates that the receiver buffer is loaded with a new character. The receiver-buffer-loaded flag remains high until the read-receiver-buffer function is addressed (at which time the flag is cleared). The reset function also clears this flag.

**Bit 4, transmitter buffer empty**
A high in bit 4 indicates that the transmitter buffer register is empty and ready to accept a character. Note, however, that the serial transmitter register may be in the process of shifting out a character. The reset function sets the transmitter-buffer-empty flag high.

**Bit 5, interrupt pending**
A high in bit 5 indicates that one or more of the interrupt conditions has occured and the corresponding interrupt is enabled. This bit is the status of the interrupt signal INT.

**Bit 6, full bit detected**
A high in bit 6 indicates that the first data bit of a receive-data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

**Bit 7, start bit detected**
A high in bit 7 indicates that the start bit of an incoming data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

### 2.2.5 Issue discrete commands

Addressing the discrete command function causes the TMS 5501 to interpret the data bus information according to the following descriptions. See Figure 4 for the discrete command format. Bits 1 through 5 are latched until a different discrete command is received.

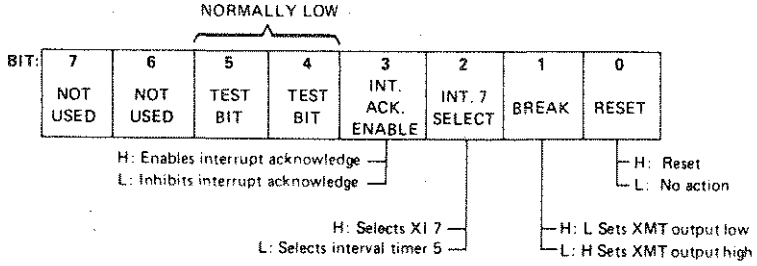



**FIGURE 4—DISCRETE COMMAND FORMAT**

**Bit 0, reset**
A high in bit 0 will cause the following:

1) The receiver buffer and register are cleared to the search mode including the receiver-buffer-loaded flag, the start-bit-detected flag, the full-bit-detected flag, and the overrun-error flag. The receiver buffer is not cleared and will contain the last character received.
2) The transmitter data output is set high (marking). The transmitter-buffer-empty flag is set high indicating that the transmitter buffer is ready to accept a character from the TMS 8080.
3) The interrupt register is cleared except for the bit corresponding to the transmitter buffer interrupt, which is set high.
4) The interval timers are inhibited.

A low in bit 0 causes no action. The reset function has no affect on the output port, the external inputs, interrupt acknowledge enable, the mask register, the rate register, the transmitter register, or the transmitter buffer.

**Bit 1, break**
A low in bit 1 causes the transmitter data output to be reset low (spacing).

If bit 0 and bit 1 are both high, the reset function will override.

**Bit 2, interrupt 7 select**
Interrupt 7 may be generated either by a low to high transition of external input 7 or by interval timer 5.

A high in bit 2 selects the interrupt 7 source to be the transition of external input 7. A low in bit 2 selects t interrupt 7 source to be interval timer 5.

**Bit 3, interrupt acknowledge enable**
The TMS 5501 decodes data bus (CPU status) bit 0 at SYNC of each machine cycle to determine if an interru acknowledge is being issued.

A high in bit 3 enables the TMS 5501 to accept the interrupt acknowledge decode. A low in bit 3 causes the TMS 55( to ignore the interrupt acknowledge decode.

Bit 4 and bit 5 are used only during testing of the TMS 5501. For correct system operation both bits must be kept lo

Bit 6 and bit 7 are not used and can assume any value.

### 2.2.6 Load rate register

Addressing the load-rate-register function causes the TMS 5501 to load the rate register from the data bus and interpr the data bits (See Figure 5) as follows.

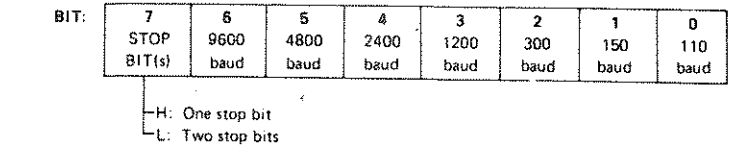



**FIGURE 5—DATA BUS ASSIGNMENTS FOR RATE COMMANDS**

**Bits 0 through 6, rate select**

The rate select bits (bits 0 through 6) are mutually exclusive, i.e., only one bit may be high. A high in bits 0 through will select the baud rate for both the transmitter and receiver circuitry as defined below and in Figure 5:

Bit 0 110 baud
Bit 1 150 baud
Bit 2 300 baud
Bit 3 1200 baud
Bit 4 2400 baud
Bit 5 4800 baud
Bit 6 9600 baud

If more than one bit is high, the highest rate indicated will result. If bits 0 through 6 are all low, both the receiver an the transmitter circuitry will be inhibited.

**Bit 7, stop bits**

Bit 7 determines whether one or two stop bits are to be used by both the transmitter and receiver circuitry. A high in bit 7 selects one stop bit. A low in bit 7 selects two stop bits.

### 2.2.7 Load transmitter buffer

Addressing the load-transmitter-buffer function transfers the state of the data bus into the transmitter buffer.

### 2.2.8 Load output port

Addressing the load-output-port function transfers the state of the data bus into the output port. The data is latched and remains on $\overline{XO}\ 0$ through $\overline{XO}\ 7$ as the complement of the data bus until new data is loaded.

### 2.2.9 Load mask register

Addressing the load-mask-register function loads the contents of the data bus into the mask register. A high in data bus bit n enables interrupt n. A low inhibits the corresponding interrupt.

### 2.2.10 Load timer n

Addressing the load-timer-n function loads the contents of the data bus into the appropriate interval timer. Time intervals of from 64 $\mu$s (data bus = LLLLLLLH) to 16,320 $\mu$s (data bus HHHHHHHH) are counted in 64-$\mu$s steps. When the count of interval timer n reaches 0, the bit in the interrupt register that corresponds to timer n is set and an interrupt is generated. Loading all lows causes an interrupt immediately.

## 3. TMS 5501 ELECTRICAL AND MECHANICAL SPECIFICATIONS

### 3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

| | |
|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | −0.3 V to 20 V |
| Supply voltage, $V_{DD}$ (see Note 1 | −0.3 V to 20 V |
| Supply voltage, $V_{SS}$ (see Note 1) | −0.3 V to 20 V |
| All input and output voltages (see Note 1) | −0.3 V to 20 V |
| Continuous power dissipation | 1.1 W |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may effect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, $V_{BB}$ (substrate). Throughout the remainder of this data sheet, voltage values are with respect to $V_{SS}$ unless otherwise noted.

### 3.2 RECOMMENDED OPERATING CONDITIONS

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{BB}$ | −4.75 | −5 | −5.25 | V |
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Supply voltage, $V_{DD}$ | 11.4 | 12 | 12.6 | V |
| Supply voltage, $V_{SS}$ | | 0 | | V |
| High-level input voltage, $V_{IH}$ (all inputs except clocks) | 3.3 | | $V_{CC}+1$ | V |
| High-level clock input voltage, $V_{IH(\phi)}$ | $V_{DD}-1$ | | $V_{DD}+1$ | V |
| Low-level input voltage, $V_{IL}$ (all inputs except clocks) (see Note 2) | −1 | | 0.8 | V |
| Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 2) | −1 | | 0.6 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only.

### 3.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $I_I$ | Input current (any input except clocks and data bus) | $V_I$ = 0 V to $V_{CC}$ | | ±10 | µA |
| $I_{I(\phi)}$ | Clock input current | $V_{I(\phi)}$ = 0 V to $V_{DD}$ | | ±10 | µA |
| $I_{I(DB)}$ | Input current, data bus | $V_{I(DB)}$ = 0 V to $V_{CC}$, CE at 0 V | | −100 | µA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 400 µA | 3.7 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1.7 mA, | | 0.45 | V |
| $I_{BB(av)}$ | Average supply current from $V_{BB}$ | Operating at $t_{c(\phi)}$ = 480 ns, $T_A$ = 25°C | | −1 | mA |
| $I_{CC(av)}$ | Average supply current from $V_{CC}$ | | | 100 | |
| $I_{DD(av)}$ | Average supply current from $V_{DD}$ | | | 40 | |
| $C_i$ | Capacitance, any input except clock | $V_{CC}$ = $V_{DD}$ = $V_{SS}$ = 0 V, $V_{BB}$ = −4.75 to −5.25 V, f = 1 MHz, All other pins at 0 V | | 10 | pF |
| $C_{i(\phi)}$ | Clock input capacitance | | | 75 | |
| $C_o$ | Output capacitance | | | 20 | |

### 3.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 5 AND 6)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{c(\phi)}$ | Clock cycle time | 480 | 2000 | ns |
| $t_{r(\phi)}$ | Clock rise time | 5 | 50 | ns |
| $t_{f(\phi)}$ | Clock fall time | 5 | 50 | ns |
| $t_{w(\phi1)}$ | Pulse width, clock 1 high | 60 | | ns |
| $t_{w(\phi2)}$ | Pulse width, clock 2 high | 200 | 300 | ns |
| $t_{d(\phi1L-\phi2)}$ | Delay time, clock 1 low to clock 2 | 0 | | ns |
| $t_{d(\phi2-\phi1)}$ | Delay time, clock 2 to clock 1 | 70 | | ns |
| $t_{d(\phi1H-\phi2)}$ | Delay time, clock 1 high to clock 2 (time between leading edges) | 130 | | ns |
| $t_{su(ad)}$ | Address setup time | 50 | | ns |
| $t_{su(CE)}$ | Chip-enable setup time | 50 | | ns |
| $t_{su(da)}$ | Data setup time | 50 | | ns |
| $t_{su(sync)}$ | Sync setup time | 50 | | ns |
| $t_{su(XI)}$ | External input setup time | 50 | | ns |
| $t_{h(ad)}$ | Address hold time | 0 | | ns |
| $t_{h(CE)}$ | Chip-enable hold time | 10 | | ns |
| $t_{h(da)}$ | Data hold time | 10 | | ns |
| $t_{h(sync)}$ | Sync hold time | 10 | | ns |
| $t_{h(XI)}$ | External input hold time | 40 | | ns |
| $t_{w(sens\ H)}$ | Pulse width, sensor input high | 500 | | ns |
| $t_{w(sens\ L)}$ | Pulse width, sensor input low | 500 | | ns |
| $t_{d(sens-int)}$ | Delay time, sensor to interrupt (time between leading edges) | | 2000 | ns |
| $t_{d(rst-int)}$ | Delay time, RST instruction to interrupt (time between trailing edges) | | 500 | ns |

**Bit 7, stop bits**

Bit 7 determines whether one or two stop bits are to be used by both the transmitter and receiver circuitry. A high in bit 7 selects one stop bit. A low in bit 7 selects two stop bits.

### 2.2.7 Load transmitter buffer

Addressing the load-transmitter-buffer function transfers the state of the data bus into the transmitter buffer.

### 2.2.8 Load output port

Addressing the load-output-port function transfers the state of the data bus into the output port. The data is latched and remains on $\overline{XO}$ 0 through $\overline{XO}$ 7 as the complement of the data bus until new data is loaded.

### 2.2.9 Load mask register

Addressing the load-mask-register function loads the contents of the data bus into the mask register. A high in data bus bit n enables interrupt n. A low inhibits the corresponding interrupt.

### 2.2.10 Load timer n

Addressing the load-timer-n function loads the contents of the data bus into the appropriate interval timer. Time intervals of from 64 μs (data bus = LLLLLLLH) to 16,320 μs (data bus HHHHHHHH) are counted in 64-μs, steps. When the count of interval timer n reaches 0, the bit in the interrupt register that corresponds to timer n is set and an interrupt is generated. Loading all lows causes an interrupt immediately.

## 3. TMS 5501 ELECTRICAL AND MECHANICAL SPECIFICATIONS

### 3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

| | |
|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | −0.3 V to 20 V |
| Supply voltage, $V_{DD}$ (see Note 1 | −0.3 V to 20 V |
| Supply voltage, $V_{SS}$ (see Note 1) | −0.3 V to 20 V |
| All input and output voltages (see Note 1) | −0.3 V to 20 V |
| Continuous power dissipation | 1.1 W |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may effect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, $V_{BB}$ (substrate). Throughout the remainder of this data sheet, voltage values are with respect to $V_{SS}$ unless otherwise noted.

### 3.2 RECOMMENDED OPERATING CONDITIONS

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{BB}$ | −4.75 | −5 | −5.25 | V |
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Supply voltage, $V_{DD}$ | 11.4 | 12 | 12.6 | V |
| Supply voltage, $V_{SS}$ | | 0 | | V |
| High-level input voltage, $V_{IH}$ (all inputs except clocks) | 3.3 | | $V_{CC}$+1 | V |
| High-level clock input voltage, $V_{IH(\phi)}$ | $V_{DD}$−1 | | $V_{DD}$+1 | V |
| Low-level input voltage, $V_{IL}$ (all inputs except clocks) (see Note 2) | −1 | | 0.8 | V |
| Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 2) | −1 | | 0.6 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only.

### 3.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

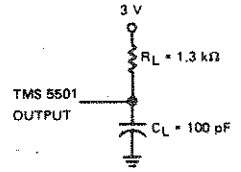
| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $I_I$ | Input current (any input except clocks and data bus) | $V_I$ = 0 V to $V_{CC}$ | | ±10 | μA |
| $I_{I(\phi)}$ | Clock input current | $V_{I(\phi)}$ = 0 V to $V_{DD}$ | | ±10 | μA |
| $I_{I(DB)}$ | Input current, data bus | $V_{I(DB)}$ = 0 V to $V_{CC}$, CE at 0 V | | −100 | μA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 400 μA | 3.7 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1.7 mA, | | 0.45 | V |
| $I_{BB(av)}$ | Average supply current from $V_{BB}$ | Operating at $t_{c(\phi)}$ = 480 ns, $T_A$ = 25°C | | −1 | mA |
| $I_{CC(av)}$ | Average supply current from $V_{CC}$ | | | 100 | |
| $I_{DD(av)}$ | Average supply current from $V_{DD}$ | | | 40 | |
| $C_i$ | Capacitance, any input except clock | $V_{CC}$ = $V_{DD}$ = $V_{SS}$ = 0 V, $V_{BB}$ = −4.75 to −5.25 V, f = 1 MHz, All other pins at 0 V | | 10 | pF |
| $C_{i(\phi)}$ | Clock input capacitance | | | 75 | |
| $C_o$ | Output capacitance | | | 20 | |

### 3.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 5 AND 6)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{c(\phi)}$ | Clock cycle time | 480 | 2000 | ns |
| $t_{r(\phi)}$ | Clock rise time | 5 | 50 | ns |
| $t_{f(\phi)}$ | Clock fall time | 5 | 50 | ns |
| $t_{w(\phi1)}$ | Pulse width, clock 1 high | 60 | | ns |
| $t_{w(\phi2)}$ | Pulse width, clock 2 high | 200 | 300 | ns |
| $t_{d(\phi1L-\phi2)}$ | Delay time, clock 1 low to clock 2 | 0 | | ns |
| $t_{d(\phi2-\phi1)}$ | Delay time, clock 2 to clock 1 | 70 | | ns |
| $t_{d(\phi1H-\phi2)}$ | Delay time, clock 1 high to clock 2 (time between leading edges) | 130 | | ns |
| $t_{su(ad)}$ | Address setup time | 50 | | ns |
| $t_{su(CE)}$ | Chip-enable setup time | 50 | | ns |
| $t_{su(da)}$ | Data setup time | 50 | | ns |
| $t_{su(sync)}$ | Sync setup time | 50 | | ns |
| $t_{su(XI)}$ | External input setup time | 50 | | ns |
| $t_{h(ad)}$ | Address hold time | 0 | | ns |
| $t_{h(CE)}$ | Chip-enable hold time | 10 | | ns |
| $t_{h(da)}$ | Data hold time | 10 | | ns |
| $t_{h(sync)}$ | Sync hold time | 10 | | ns |
| $t_{h(XI)}$ | External input hold time | 40 | | ns |
| $t_{w(sens\ H)}$ | Pulse width, sensor input high | 500 | | ns |
| $t_{w(sens\ L)}$ | Pulse width, sensor input low | 500 | | ns |
| $t_{d(sens-int)}$ | Delay time, sensor to interrupt (time between leading edges) | | 2000 | ns |
| $t_{d(rst-int)}$ | Delay time, RST instruction to interrupt (time between trailing edges) | | 500 | ns |

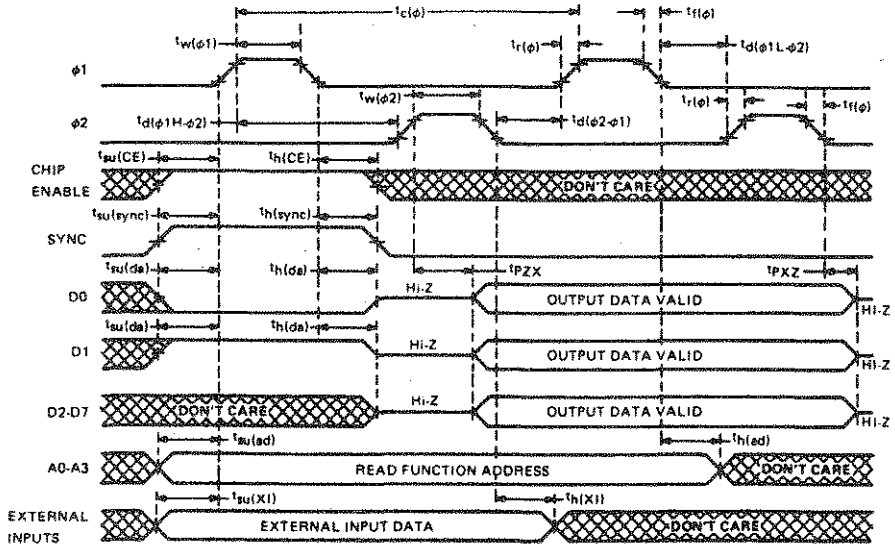
### 3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 6 AND 7)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{PZX}$ | Data bus output enable time | $C_L$ = 100 pF, $R_L$ = 1.3 kΩ | | 200 | ns |
| $t_{PXZ}$ | Data bus output disable time to high-impedance state | | | 180 | ns |
| $t_{PD}$ | External data output propagation delay time from ϕ2 | | | 200 | ns |



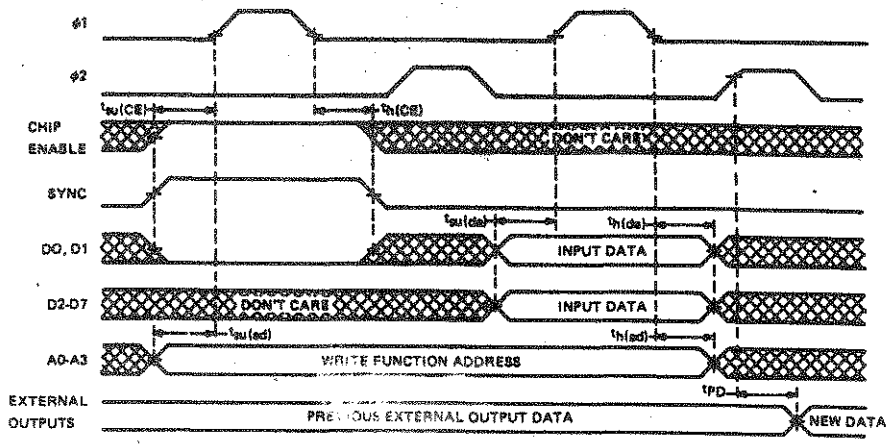

$C_L$ includes probe and jig capacitance

LOAD CIRCUIT



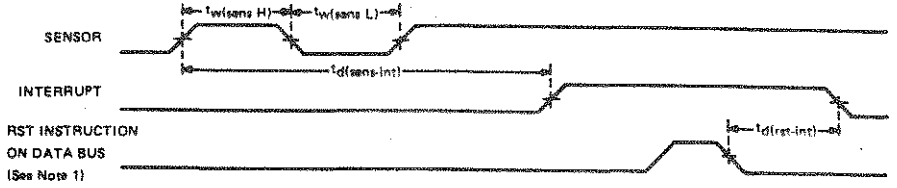

NOTE: For ϕ1 or ϕ2 inputs, high and low timing points are 90% and 10% of $V_{IH(\phi)}$. All other timing points are the 50% level.

FIGURE 6–READ CYCLE TIMING




NOTE: For ϕ1 and ϕ2 inputs, high and low timing points are 90% and 10% of $V_{IH(\phi)}$. All other timing points are the 50% level.

FIGURE 7–WRITE CYCLE TIMING

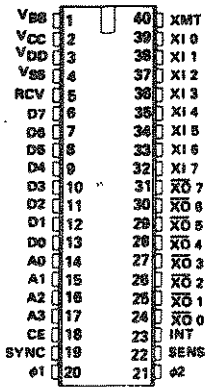



NOTES: 1. The RST instruction occurs during the output data valid time of the read cycle.
2. All timing points are 50% of $V_{IH}$.

FIGURE 8–SENSOR/INTERRUPT TIMING

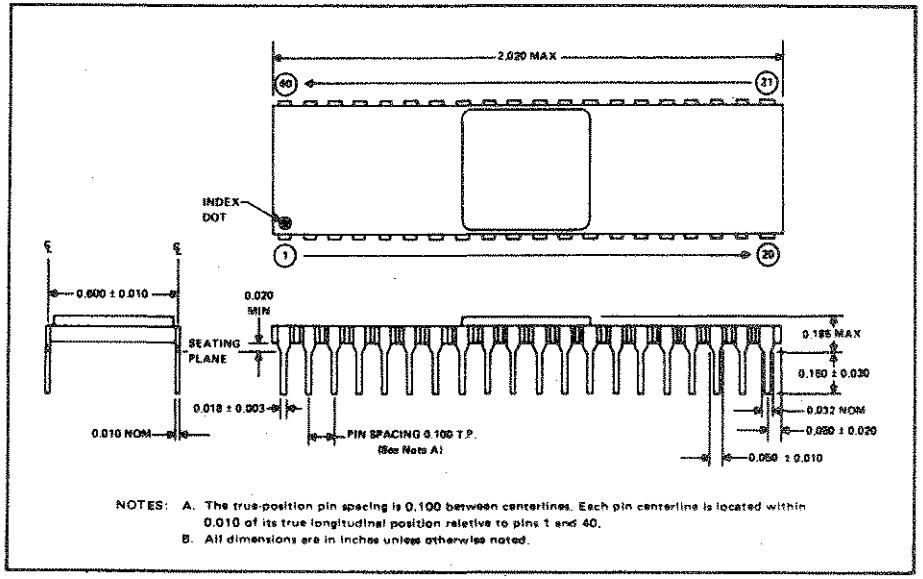
### 3.6 TERMINAL ASSIGNMENTS

TMS 5501




### 3.7 MECHANICAL DATA

40-PIN CERAMIC PACKAGE




NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 40.
B. All dimensions are in inches unless otherwise noted.